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# ORCA® ORSPI4 Evaluation Board

## User's Guide

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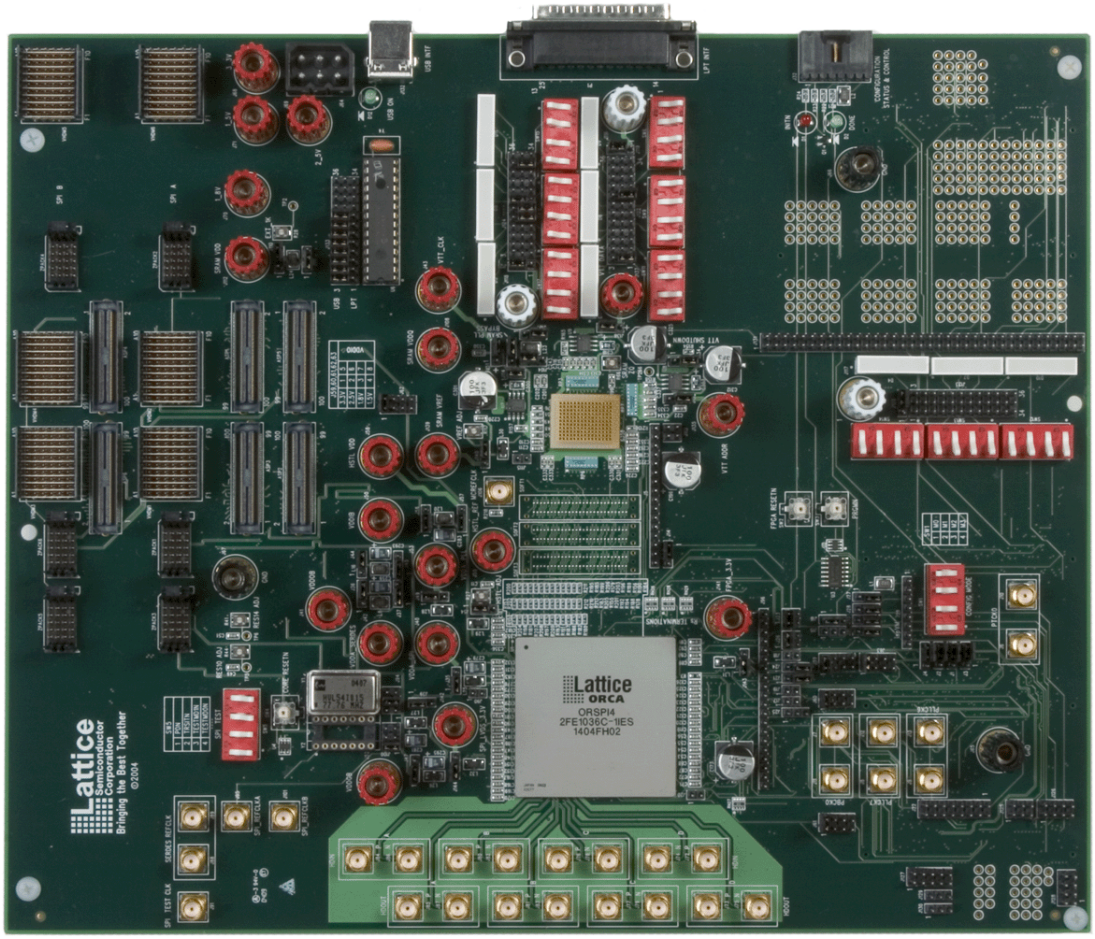
# Introduction

This user's guide describes the Lattice evaluation board for the ORSPI4 device, a stand-alone evaluation PCB that provides a functional platform for device feature demonstrations. The board includes the following features:

- Power connections
- ispVM® programming support
- On-board and external reference clock sources
- High-speed interconnections to both SPI4.2 compliant interfaces
- SPI4.2 interface logic analyzer connections
- Quad Data Rate memory controller interface to SRAM device
- Discrete high-speed interface SMA test points and clock connections
- ORCAstra Demonstration Software interface
- SERDES high-speed layout structures

The contents of this user's guide include top-level functional descriptions of the various portions of the evaluation board, descriptions of the connectors, diodes and switches and a complete set of schematics for version 1.2 of the board. Figure 1 shows the functional partitioning of the board.

***Figure 1. ORSPI4 Evaluation Board***



## J29

An 8-pin connector that provides the interface to the ispDOWNLOAD® cable.

| Pin Number | Signal |
|---|---|
| Pin 1 | VDD |
| Pin 2 | TDO |
| Pin 3 | TDI |
| Pin 4 | NC |
| Pin 5 | NC |
| Pin 6 | TMS |
| Pin 7 | GND |
| Pin 8 | TCK |

## J32

A 7-pin serial connector used for serial configuration.

| Pin Number | Signal |
|---|---|
| Pin 1 | GND |
| Pin 2 | NC |
| Pin 3 | PROGRMN |
| Pin 4 | DONE |
| Pin 5 | D0 |
| Pin 6 | CCLK |
| Pin 7 | VDD |

### Header Connections

Standard 0.100 headers are provided for interconnecting points on the board. This can be accomplished with 0.100 IDC connectors and ribbon cable for bus connections or 0.025 pin socket patch cords (such as Pomona Electronics #5948 (www.pomonelectronics.com). 0.100 jumpers shunts are also used for board selections such as Sullins Electronics P/N SPC02SYAN (www.sullinselectronics.com).

## D1, D2

These LEDs indicate the status of configuration to the FPGA DONE/INITN status pins. When D2 is illuminated, this indicates the successful completion of configuration. Illumination of D1 indicates that the programming was aborted or reinitialized.

## J21, 24

These standard 3x1 headers provide connections of the PROGRAMN and RESETN control pins. For standard evaluation board use, a 2-pin shunt should be placed across pins 1 and 2. This will connect the pins to on-board push-button switches.

| | Pin Number | Signal |
|---|---|---|
| J21 | Pin 1 | Local |
| | Pin 2 | RESETN |
| | Pin 3 | Global |
| J24 | Pin 1 | Local |
| | Pin 2 | PROGRMN |
| | Pin 3 | Global |

## J23, 26

These standard 2x2 headers provide connection of the DONE and INITN status pins. For standard evaluation board use, a 2-pin shunt should be placed across pins 1 and 2. This will connect the pins to on-board LED indicators.

| Pin Number | | Signal |
|---|---|---|
| J23 | Pin 1 | Local |
| | Pin 2 | DONE |
| | Pin 3 | Global |
| | Pin 4 | DONE |
| J26 | Pin 1 | Local |
| | Pin 2 | INITN |
| | Pin 3 | Global |
| | Pin 4 | INITN |

## J27, J28, J30, J31

These standard 1x3 header provide connection of the JTAG pins to the ispVM down connection. For standard evaluation board use, a 2-pin shunt should be placed across pins 2 and 3. This will connect the pins to J30.

| | Pin Number | Signal |
|---|---|---|
| J27 | Pin 1 | Global |
| | Pin 2 | TDO |
| | Pin 3 | Local |
| J28 | Pin 1 | Global |
| | Pin 2 | TDI |
| | Pin 3 | Local |
| J30 | Pin 1 | Global |
| | Pin 2 | TMS |
| | Pin 3 | Local |
| J31 | Pin 1 | Global |
| | Pin 2 | TCK |
| | Pin 3 | Local |

## J1, J2, J3, J4

These standard 1x3 header provide connection of the configuration MODE pins to the on board DIP switches. For standard evaluation board use, a 2-pin shunt should be placed across pins 2 and 3.

| | Pin Number | Signal |
|---|---|---|
| J1 | Pin 1 | Global |
| | Pin 2 | Mode1 |
| | Pin 3 | Local |
| J2 | Pin 1 | Global |
| | Pin 2 | Mode2 |
| | Pin 3 | Local |
| J3 | Pin 1 | Global |
| | Pin 2 | Mode3 |
| | Pin 3 | Local |
| J4 | Pin 1 | Global |
| | Pin 2 | Mode0 |
| | Pin 3 | Local |

## J14, J15, J16, J25

These standard 1x3 headers connect CCLK, DIN, RDCFGN, PTEMP pins.

| | Pin Number | Signal |
|---|---|---|
| J14 | Pin 1 | DATA0 |
| | Pin 2 | DIN |
| | Pin 3 | CABLE |
| J15 | Pin 1 | PROM |
| | Pin 2 | CCLK |
| | Pin 3 | CABLE |
| J16 | Pin 1 | 3.3V |
| | Pin 2 | RDCFGN |
| | Pin 3 | CABLE |
| J25 | Pin 1 | 3.3V |
| | Pin 2 | PTEMP |
| | Pin 3 | GND |

## Control Switches

The following switches provide the user control of the various control pins.

| Switch | Use | Notes |
|---|---|---|
| SW1 | Configuration Mode Pins[3:0] | A=M0,B=M1,C=M2,D=M3 |
| SW2 | | Pushbutton for RESETN |
| SW3 | | Pushbutton for PROGMN |
| SW4 | | Pushbutton for PASB_RESETN(SERDES RESET) |
| SW5 | Test pins | A=PDN, B=TRISTN, C=TESTMD1N, D=TESTMD0N |

## J17, J18, J19

These 2x1 standard headers allows connection of the Chip Selects to various sources. For standard evaluation board use, place shunt across J17, J18=OPEN, J19, pins 1 and 2.

| | Pin Number | Signal |
|---|---|---|
| J17-CS0N | Pin 1 | 3.3V |
| | Pin 2 | CS1 |
| J18-CS1 | Pin 1 | CS0N |
| | Pin 2 | GND |
| J19-CS0N | Pin 1 | Source |
| | Pin 2 | CS1 |

## J20

These 2x1 standard headers allows connection of the LVDS_R pin to a 100Ω resistor to GND. For standard evaluation board use, leave header open.

| Pin Number | Signal |
|---|---|
| Pin 1 | 100Ω |
| Pin 2 | LDVS_R |

## General Purpose FPGA I/O Selection

These 12x3 standard headers allow connection of the DIP switch packs or LEDS to general purpose I/O pins.

| Pin Number | Signal |
|---|---|
| J122 | GEN_FPGA[0:11] |
| J123 | GEN_FPGA[24:35] |
| J124 | GEN_FPGA[12:23] |

## General Purpose Switch Selection

These 3x1 standard headers allows connection of the DIP switch packs to either an externally supplied voltage or the on-board 2.5V source.

| Switch | Selections |
|---|---|
| J119 | GEN_FPGA_SWITCH_SEL[0:11] |
| J120 | GEN_FPGA_SWITCH_SEL[24:35] |
| J121 | GEN_FPGA_SWITCH_SEL[12:23] |

## General Purpose LED Selection

These 3x1 standard headers allows connection of the LED packs to the designated FPGA pin.

| LED Bank | Selections |
|---|---|
| D3 | LED array connected to J94-General IO[0:3] |
| D4 | LED array connected to J95-General IO[24:27] |
| D5 | LED array connected to J100-General IO[12:15] |
| D6 | LED array connected to J94-General IO[4:7] |
| D7 | LED array connected to J95-General IO[28:31] |
| D8 | LED array connected to J100-General IO[16:19] |
| D9 | LED array connected to J94-General IO[8:11] |
| D10 | LED array connected to J95-General IO[32:35] |
| D11 | LED array connected to J100-General IO[20:23] |

## General Purpose I/O Connections

The 12x3 headers are jumper programmable to connect a particular FPGA pin to either a switch or a LED. The table below provides the connectivity to the device pins.

| Net | Pad | BGA | Header | Switch | Device | LED |
|---|---|---|---|---|---|---|
| GEN_FPGA_PIN0 | PB34C | BA22 | J122 | 1 | 2 | 3 |
| GEN_FPGA_PIN1 | PB34D | BB22 | J122 | 4 | 5 | 6 |
| GEN_FPGA_PIN2 | PB35A | AW22 | J122 | 7 | 8 | 9 |
| GEN_FPGA_PIN3 | PB35B | AY22 | J122 | 10 | 11 | 12 |
| GEN_FPGA_PIN4 | PB35C | BD21 | J122 | 13 | 14 | 15 |
| GEN_FPGA_PIN5 | PB35D | BC21 | J122 | 16 | 17 | 18 |
| GEN_FPGA_PIN6 | PB36C | BD20 | J122 | 19 | 20 | 21 |
| GEN_FPGA_PIN7 | PB36D | BC20 | J122 | 22 | 23 | 24 |
| GEN_FPGA_PIN8 | PB37A | AY21 | J122 | 25 | 26 | 27 |
| GEN_FPGA_PIN9 | PB37B | AW21 | J122 | 28 | 29 | 30 |
| GEN_FPGA_PIN10 | PB37C | BB20 | J122 | 31 | 32 | 33 |
| GEN_FPGA_PIN11 | PB37D | BA20 | J122 | 34 | 35 | 36 |
| GEN_FPGA_PIN12 | PB38A | BA21 | J124 | 1 | 2 | 3 |
| GEN_FPGA_PIN13 | PB38B | BB21 | J124 | 4 | 5 | 6 |
| GEN_FPGA_PIN14 | PB38C | BD19 | J124 | 7 | 8 | 9 |
| GEN_FPGA_PIN15 | PB38D | BC19 | J124 | 10 | 11 | 12 |
| GEN_FPGA_PIN16 | PB39A | AY20 | J124 | 13 | 14 | 15 |
| GEN_FPGA_PIN17 | PB39B | AW20 | J124 | 16 | 17 | 18 |
| GEN_FPGA_PIN18 | PB39C | BB19 | J124 | 19 | 20 | 21 |
| GEN_FPGA_PIN19 | PB39D | BA19 | J124 | 22 | 23 | 24 |
| GEN_FPGA_PIN20 | PB40A | AY19 | J124 | 25 | 26 | 27 |
| GEN_FPGA_PIN21 | PB40B | AW19 | J124 | 28 | 29 | 30 |
| GEN_FPGA_PIN22 | PB40C | BD18 | J124 | 31 | 32 | 33 |
| GEN_FPGA_PIN23 | PB40D | BC18 | J124 | 34 | 35 | 36 |
| GEN_FPGA_PIN24 | PB41A | AY18 | J123 | 1 | 2 | 3 |
| GEN_FPGA_PIN25 | PB41B | AW18 | J123 | 4 | 5 | 6 |
| GEN_FPGA_PIN26 | PB41C | BB18 | J123 | 7 | 8 | 9 |

| Net | Pad | BGA | Header | Switch | Device | LED |
|---|---|---|---|---|---|---|
| GEN_FPGA_PIN27 | PB41D | BA18 | J123 | 10 | 11 | 12 |
| GEN_FPGA_PIN28 | PB42A | AY17 | J123 | 13 | 14 | 15 |
| GEN_FPGA_PIN29 | PB42B | AW17 | J123 | 16 | 17 | 18 |
| GEN_FPGA_PIN30 | PB42C | BD17 | J123 | 19 | 20 | 21 |
| GEN_FPGA_PIN31 | PB42D | BC17 | J123 | 22 | 26 | 24 |
| GEN_FPGA_PIN32 | PB43A | AY16 | J123 | 25 | 23 | 27 |
| GEN_FPGA_PIN33 | PB43B | AW16 | J123 | 28 | 29 | 30 |
| GEN_FPGA_PIN34 | PB43C | BB17 | J123 | 31 | 32 | 33 |
| GEN_FPGA_PIN35 | PB43D | BA17 | J123 | 34 | 35 | 36 |

## Non-Applicable Headers

Standard headers are used for lab purpose only and are left unused for standard evaluation board use.

| Location | Description |
|---|---|
| J125 | HEADER 16X1 |
| J126 | HEADER 8X2 |
| J102 | HEADER 3x2 |
| J103 | HEADER 2x4 |
| J104 | HEADER 5X2 |
| J105 | HEADER 2x4 |
| J106 | HEADER 3x1 |
| J107 | HEADER 3x1 |

## SERDES/SPI4 and QDR Memory Controller Voltage Supply Selections

These 3x1 standard headers are used for selecting voltage sources for the following power supplies.

| Header | Pin1 | Pin2 | Pin3 | Default Shunt |
|---|---|---|---|---|
| J39 | 1.5V | VDDA | Banana | 1-2 |
| J47 | VDDA | VDDGB | Banana | 1-2 |
| J44 | 1.8V | VDDIB | 1.5V | 2-3 |
| J45 | On-Board | VDDIB | Banana | 1-2 |
| J36 | 1.8V | VDDOB | 1.5V | 2-3 |
| J37 | On-Board | VDDOBA | Banana | 1-2 |
| J35 | On-Board | VDDA_SPI | Banana | 1-2 |
| J49 | On-Board | VDDA_PLL | Banana | 1-2 |
| J56 | 1.5V | VDDH | 1.8V | 1-2 |
| J57 | On-Board | VDDH | Banana | 1-2 |
| J54 | On-Board | REF_I | Banana | 1-2 |

## VDDIO

These standard 2x4 headers select the input for the VDDIO voltage. Placing shunts connects the specified voltage level to the associated VDDIO bank and are as follows.

| Header | VDDIO Bank |
|---|---|
| J59 | VDDIO7 |
| J60 | VDDIO6 |
| J61 | VDDIO5 |
| J62 | VDDIO1 |
| J63 | VDDIO0 |

| | | |
|---|---|---|
| 5 | 1 | 3.3V |
| 6 | 2 | 2.5V |
| 7 | 3 | 1.8V |
| 8 | 4 | 1.5V |

VDDIO Selection

## ORCAstra PC Interface

### J133

The standard 12x3 headers select the input for the ORCAstra demo interface. Placing shunts connects the specified source, either LPT or USB communications of a PC. Placing shunts across 2-3, 5-6, 8-9, 11-12, 14-15, 17-18, 20-21, 23-24 will connect the USB to the interface.

The following designators are used to interface with the ORCAstra GUI:

| Jack # | Size | Function |
|---|---|---|
| D12 | LED | Green LED indicates USB connected for ORCAstra |
| J132 | 4-pin | Universal Serial Bus (USB) ORCAstra Interface |
| P1 | 24-pin | Parallel Port (LPT) ORCAstra Interface |

### External SERDES REFCLK

These SMA connectors connect to the reference clock pins of the SERDES. These pins receive a direct differential reference clock.

| SMA Connector | SERDES Clock |
|---|---|
| J88 | REFCLKA_N |
| J89 | REFCLKA_P |

## On-Board SPI REFCLK

These DIP sockets connect an oscillator for the SPI reference clocks.

| Socket | SERDES Clock | Type | Description |
|---|---|---|---|
| Y1 | REFCLKA | 4-pin DIP | Oscillator for REFCLKA |
| Y2 | REFCLKB | 4-pin DIP | Oscillator for REFCLKB |

## SERDES Channels

These SMA connectors connect to the SERDES Tx and Rx channels of the SERDES.

| SMA Connector | SERDES Channel |
|---|---|
| J72 | HDIN_D_P |
| J73 | HDOUT_D_P |
| J74 | HDIN_D_N |
| J75 | HDOUT_D_N |
| J76 | HDIN_C_P |
| J77 | HDOUT_C_P |
| J78 | HDIN_C_N |
| J79 | HDOUT_C_N |
| J80 | HDIN_B_P |
| J81 | HDOUT_B_P |
| J82 | HDIN_B_N |
| J83 | HDOUT_B_N |
| J84 | HDIN_A_P |
| J85 | HDOUT_A_P |
| J86 | HDIN_A_N |
| J87 | HDOUT_A_N |

## Additional Connections

SMA connectors are available to connect to several FPGA clock pins.

| SMA | Signal | BGA Pin |
|---|---|---|
| J6 | PTCK0T | C30 |
| J7 | PTCK0T | BC28 |
| J8 | PLL_CK7C | AT40 |
| J9 | PLL_CK6C | BD42 |
| J10 | PTCK0C | D30 |
| J11 | PTCK0C | BD28 |
| J12 | PLL_CK7T | AT39 |
| J13 | PLL_CK6T | BC42 |

SMA connection for SPI4.2 Test clock.

| SMA | Signal | BGA Pin |
|---|---|---|
| J91 | TESTCLK | BD4 |

Additional FPGA pins

| BGA | Signal | J96 Pin |
|---|---|---|
| D20 | PT44C | 1 |
| C20 | PT44D | 2 |
| E23 | PT44B | 3 |
| F23 | PT44A | 4 |
| E20 | PT43D | 5 |
| BD13 | PB44A | 6 |
| BC13 | PB44B | 7 |
| BD16 | PB44C | 8 |
| BC16 | PB44D | 9 |
| BB16 | PB45C | 10 |
| BA16 | PB45D | 11 |
| BD12 | PB46A | 12 |
| BC12 | PB46B | 13 |
| BD14 | PB46C | 14 |
| BD15 | PB46D | 15 |
| AR40 | PL45C | 16 |
| AR41 | PL45D | 17 |
| AT41 | PL46C | 18 |
| AU41 | PL46D | 19 |

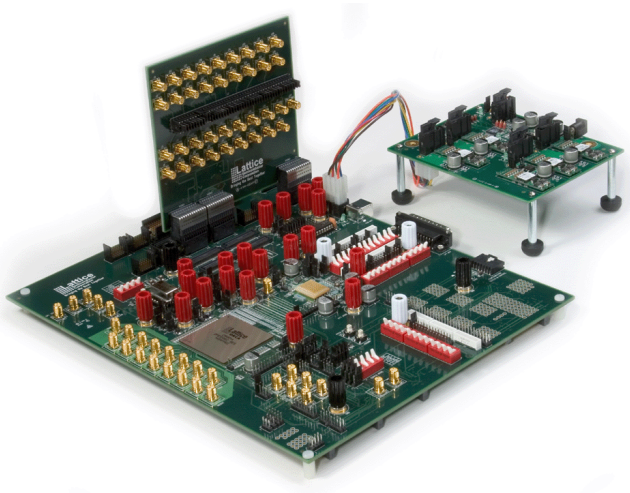
## External Power Supply Connections

The following banana jack connectors are available for supplying power to the evaluation board from an external source:

| Connector | Type | External | Typical Voltage |
|---|---|---|---|
| J42 | Red Binding Post | VDDA | +1.5V |
| J52 | Red Binding Post | VDDGB | +1.5V |
| J50 | Red Binding Post | VDDIB | +1.5V/1.8V |
| J41 | Red Binding Post | VDDOB | +1.5V/1.8V |
| J58 | Red Binding Post | HSTL_VDD | +1.5V/1.8V |
| J53 | Red Binding Post | VDDA_PLL | +3.3V |
| J55 | Red Binding Post | HSTL_VREF | +0.75/0.9V |
| J141 | Red Binding Post | FPGA_VDD33 | +3.3V |
| J142 | Red Binding Post | SPI_LVDS_3.3V | +3.3V |
| J68 | Red Binding Post | VDD33 | +3.3V |
| J69 | Red Binding Post | VDD25 | +2.5V |
| J70 | Red Binding Post | VDD18 | +1.8V |
| J71 | Red Binding Post | VDD15 | +1.5V |
| J116 | White Binding Post | GEN_FPGA[0:11] | Input Pad Dependent |
| J118 | White Binding Post | GEN_FPGA[12:23] | Input Pad Dependent |
| J117 | White Binding Post | GEN_FPGA[34:35] | Input Pad Dependent |
| J65 | Black Binding Post | GND | Negative supply |
| J66 | Black Binding Post | GND | Negative supply |
| J67 | Black Binding Post | GND | Negative supply |
| J112 | Red Binding Post | QDR SRAM VDD | Positive supply(+1.5V-1.8V) |
| J108 | Red Binding Post | SRAM VDDQ | Positive supply(+1.5V-1.8V) |
| J139 | Red Binding Post | SRAM VREF | Positive supply(+0.75-09.V |

A Molex 6-pin power connector (J64) is provided for interconnection of a power module (GL009).This module integrates the ispPAC®-POWR1208 device and specified power regulator devices to provide adequate +1.5V, +1.8V, +2.5V, and +3.3V rails to supply this board via a standard wall-transformer module. Figure 2 highlights the connection between the evaluation and the PWR1208 power module board.

***Figure 2. ORSPI4 Evaluation Board with Power Module (ICM) Board***



# SPI4.2

## SPI Reference Clocks

### J95 and J217

These 2x3 standard headers connect the reference clock pins of the SPI to an on-board oscillator or a direct differential reference clock sourced from SMA.

| | Pin | |
|---|---|---|
| J94 | Pin 1, 3, 5 | REFCLKA |
| | Pin 2 | OSC |
| | Pin 4 | External SMA |
| J100 | Pin 1, 3, 5 | REFCLKB |
| | Pin 2 | OSC |
| | Pin 4 | External SMA |

## SPI4.2 Interoperability Connections

### VHDM 1 -6

These high-speed connectors provide an interface of the SPI4.2 signals. They can provide capabilities to interconnect the evaluation board to other vendor boards. The Molex VHDM 6-row connector provides both daughter card and cable interconnections.

### ASP 1 -6

High-speed logic analyzer connectors are provided to observe the SPI4.2 interface. The Samtec connectors are provided to connect to an Agilent Logic Analyzer. Because the SPI4.2 bus uses LVDS, the POS-PHY L4 Toolset provided for the Agilent 16760A logic analyzer and the E5379A probes provides capabilities to capture data synchronously on the transmit and receive paths which includes a clock, a 16-bit data bus and control signals.

## QDR Memory Controller Interface

A dedicated interface is included to a 165-BGA QDR memory device. This interface includes proper termination for data, address, and control of a Quad-data rate SRAM device. It also includes the ability to observe transactions through a logic analyzer interconnection.

| SMA | Signal | BGA Pin |
|---|---|---|
| J106 | Memory Controller Ref. Clock | E13 |

# Technical Support Assistance

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