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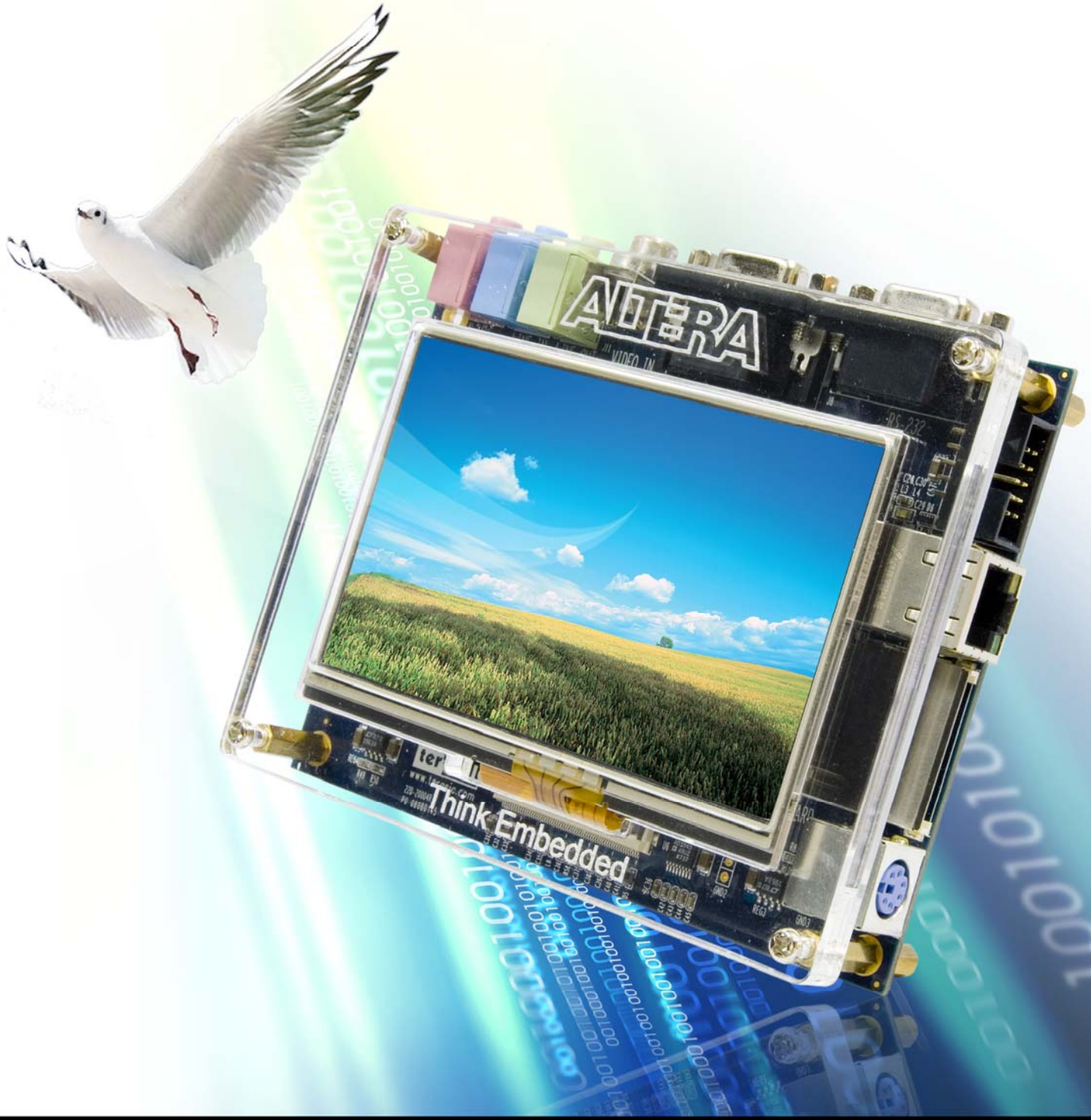
Terasic Multimedia Touch Panel Daughter Board (MTDB) V2.0

User Manual



CONTENTS

Chapter 1
The Package

The Multimedia Touch Panel Daughter board **(MTDB)** package contains all components needed for MTDB in conjunction with an Altera FPGA board with HSMC connector.

1.1 Package Contents

The MTDB package includes:

- The Terasic Multimedia Touch Panel daughter board
- [Optional] Components to assemble the MTDB with a Cyclone III Starter Board into a BRICK format as shown in Figure 1.1. The detailed instructions on how to assemble MTDB with a Cyclone III Starter board into a BRICK format can be found in the *CycloneIII_Starter_Board/BRICK* folder of the **MTDB System CD-ROM**

Figure 1.1. The BRICK form of combining the MTDB to an Altera Cyclone III Starter Board.

1.2 Getting Help

Here are the addresses where you can get help if you encounter problems:

- Terasic Technologies
  No. 356, Sec. 1, Fusing E. Rd.
  Jhubei City, HsinChu County, Taiwan, 302
  Email: support@terasic.com
  Web: www.terasic.com

Chapter 2
MTDB Hardware Specification

This chapter presents the features and design characteristics of the MTDB hardware.

2.1 Layout and Components

A photograph of the MTDB is shown in Figure 2.1, Figure 2.2, Figure 2.3, Figure 2.4, and Figure 2.5. These pictures depict the layout of the board and indicate the location of the connectors and key components.

Figure 2.1. The MTDB (Top View)

Figure 2.2. The MTDB (Connector view 1)

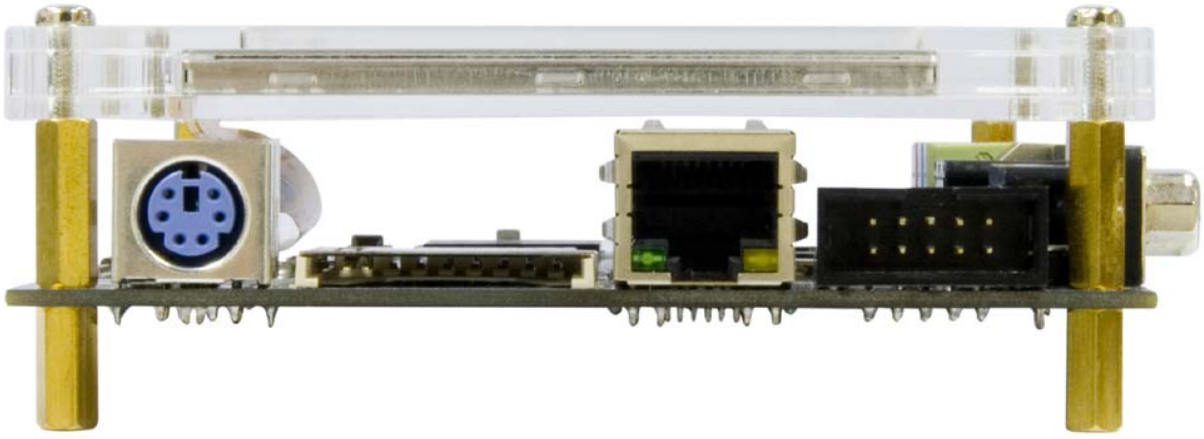


Figure 2.3. The MTDB (Connector view 2)

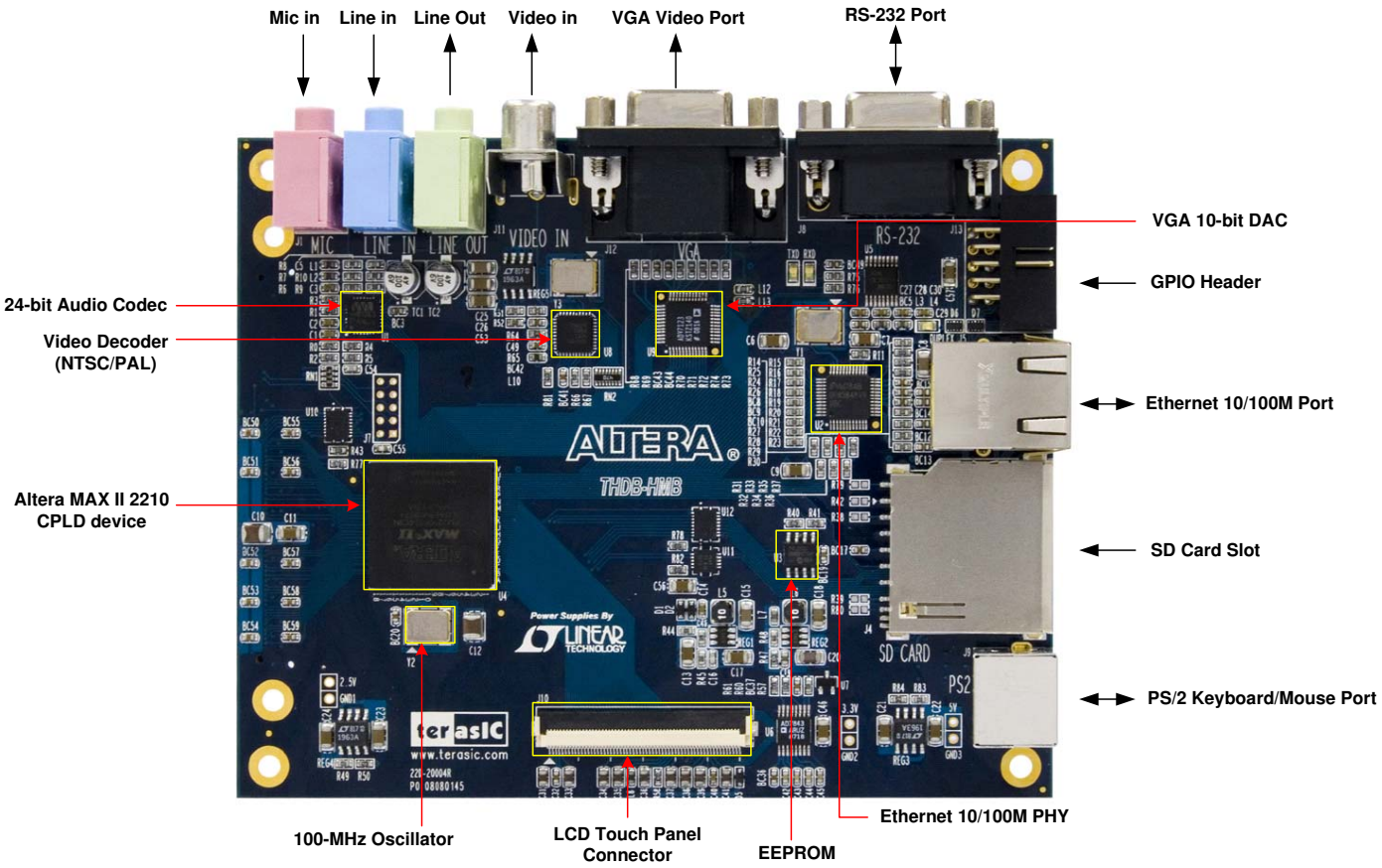


Figure 2.4 The MTDB PCB and Component diagram

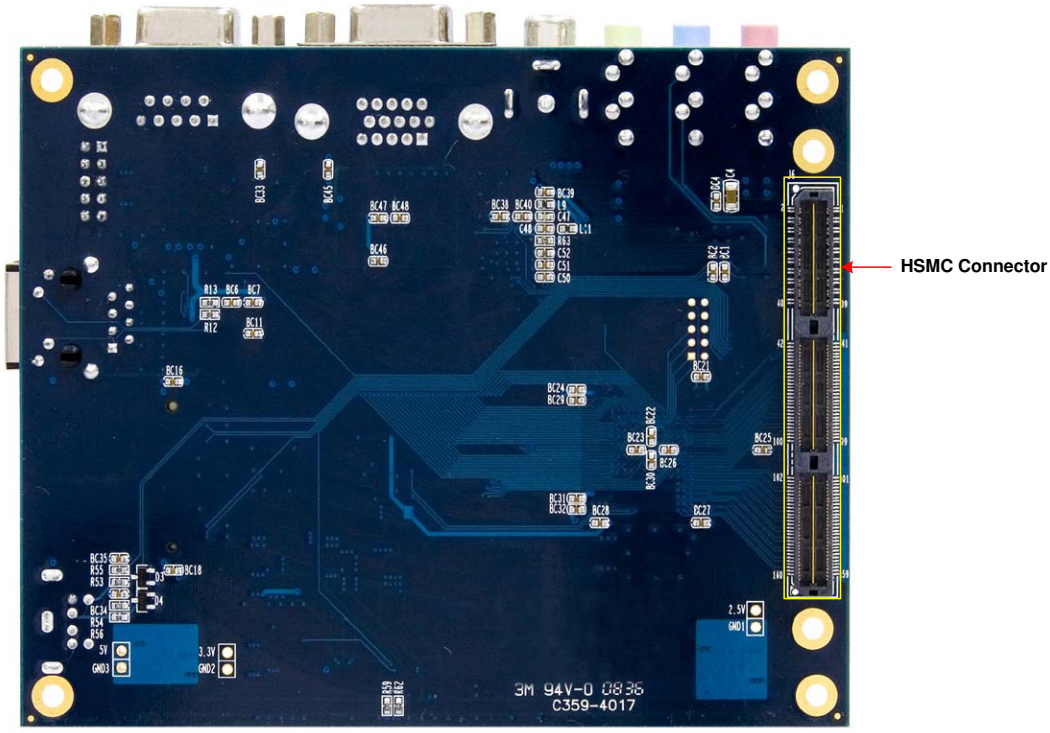


Figure 2.5. The MTDB Back side – HSMC connector view

The MTDB board has many features that allow users to implement a wide range of designed circuits, from simple circuits to various multimedia projects with touch panel applications.

The following hardware is provided on the MTDB board:

- Altera MAX II 2210 CPLD device
- SD Card socket
- 100-MHz oscillator for clock sources
- 24-bit CD-quality audio CODEC with line-in, line-out, and microphone-in jacks
- VGA DAC (10-bit high-speed triple DACs) with VGA-out connector
- Video decoder (NTSC/PAL/SECAM) and TV-in connector
- 10/100M Ethernet Physical Layer Transceiver
- RS-232 transceiver and 9-pin connector
- PS/2 mouse/keyboard connector
- 800x480 Active matrix color TFT LCD Touch Panel module
- I2C Serial EEPROM
- General Purpose I/O

To use the MTDB, the user has to be familiar with the Quartus II software.

2.2 Block Diagram of the MTDB

Figure 2.6 gives the block diagram of the MTDB. To provide maximum flexibility for the user, all connections are made through the HSMC connector device. Thus, the user can configure the FPGA on the mother board to implement any system design.

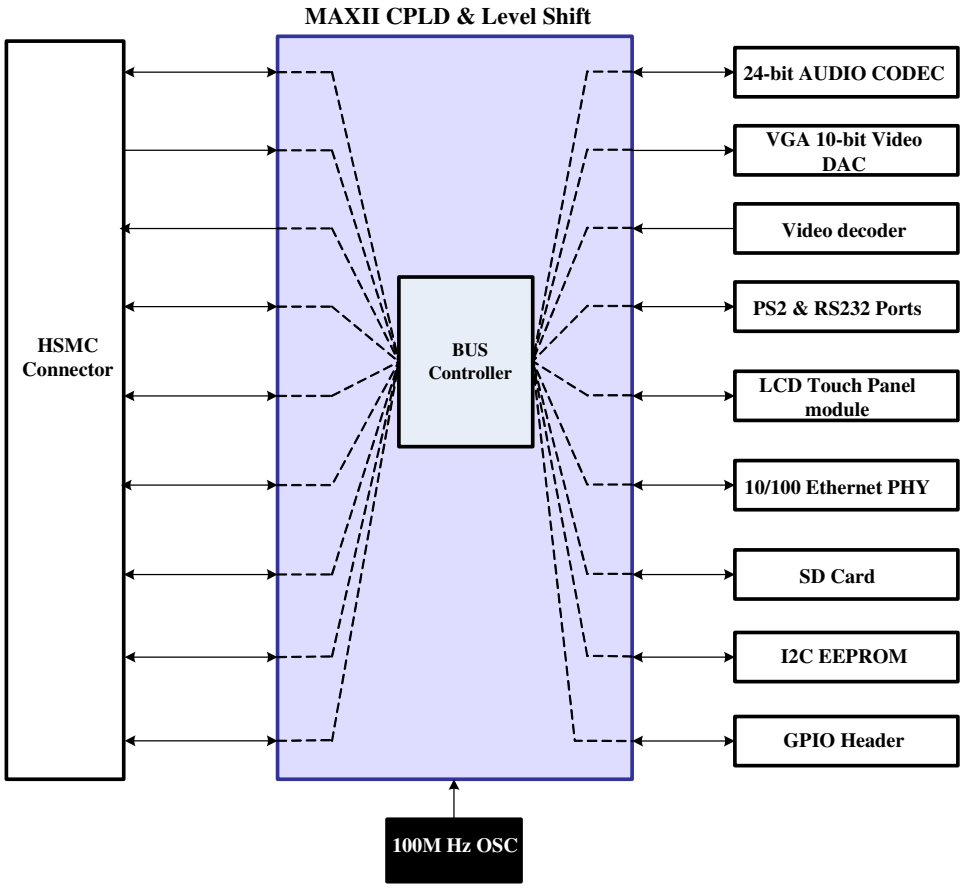


Figure 2.6. Block diagram of the MTDB board.

Following is more detailed information about the blocks in Figure 2.6:

MAX II 2210 CPLD

- 2210 LEs
- 272 user IO pins
- FineLine BGA 324-pin package

4.3” 800x480 LCD Touch panel Module and Touch Screen Digitizer

- Equipped with Toppoly TD043MTEA1 active matrix color TFT LCD module.
- Uses the Analog Devices AD7843 touch screen digitizer
- Support 24-bit parallel RGB interface.
- 3-wire register control for display and function selection.
- Built-in contrast, brightness and gamma modulation.

SD card socket

- Accessible as memory in both SPI and 4-bit SD modes.

Clock inputs

- 100-MHz oscillator.

Audio CODEC

- Wolfson WM8731 24-bit sigma-delta audio CODEC.
- Line-level input, line-level output, and microphone input jacks.
- Sampling frequency: 8 to 96 KHz.
- Applications for MP3 players and recorders, PDAs, smart phones, voice recorders, etc.

VGA output

- Uses the ADV7123 140-MHz triple 10-bit high-speed video DAC.
- With 15-pin high-density D-sub connector.

NTSC/PAL Video decoder circuit

- Uses the ADV7180 Multi-format SDTV Video Decoder.
- Supports worldwide NTSC/PAL/SECAM color demodulation.
- One 10-bit ADC, 4X over-sampling for CVBS.
- Supports Composite Video (CVBS) RCA jack input.
- Supports digital output formats : 8-bit ITU-R BT.656 YCrCb 4:2:2 output + HS, VS, and FIELD
- Applications: DVD recorders, LCD TV, Set-top boxes, Digital TV, and Portable video devices

Ethernet Physical Layer Transceiver

- Uses the DP83848C Single Port 10/100M Ethernet Physical Layer Transceiver
- Supports both 100Base-T and 10Base-T Ethernet protocols
- Supports Auto-MDIX for 10/100M

Serial ports

- One RS-232 port
- One PS/2 port
- DB-9 serial connector for the RS-232 port
- PS/2 connector for connecting a PS2 mouse or keyboard to the MTDB board.

I2C serial EEPROM

- Use one 128-bit EEPROM.
- Supports 2-wire serial interface, I2C compatible.

General Purpose I/O

- 8 general purpose I/O pins, as well as 3.3 volt power and ground line.

Chapter 3
MTDB Bus Controller

The MTDB comes with a bus controller that allows user to access all components on the board through the HSMC connector, without being limited by the number of user I/Os of the HSMC connector. This chapter describes its structure in block diagram form, and finally describes its capabilities.

3.1 MTDB Bus Controller Introduction

The two major functions of the MTDB Bus Controller are listed

1. Provide time-division multiplexing functions to the LCD and VGA color data bus.
2. Provide level shifting feature for the 2.5V (Cyclone III FPGA) and 3.3V (the MTDB side) domains.

3.2 Block Design of the MTDB Bus Controller

Figure 3.1 shows the block diagram of MTDB Bus Controller. Both the LCD and VGA TDM blocks are simple 8-bit to 24-bit and 10-bit to 30-bit data de-multiplexing functions respectively, which are final logic driving the LCD panel and VGA DAC. In the LCD TDM block, the 8-bit input data (successive BGR color data) comes in at 3 times the rate of the 24-bit output data bus (8-bit B + 8bit G + 8bit R) we drive to the LCD panel. This function can reduce the pin-count of the HSMC connector. The I2C_Bir_bus block provides bidirectional control for I2C Serial EEPROM data bus.

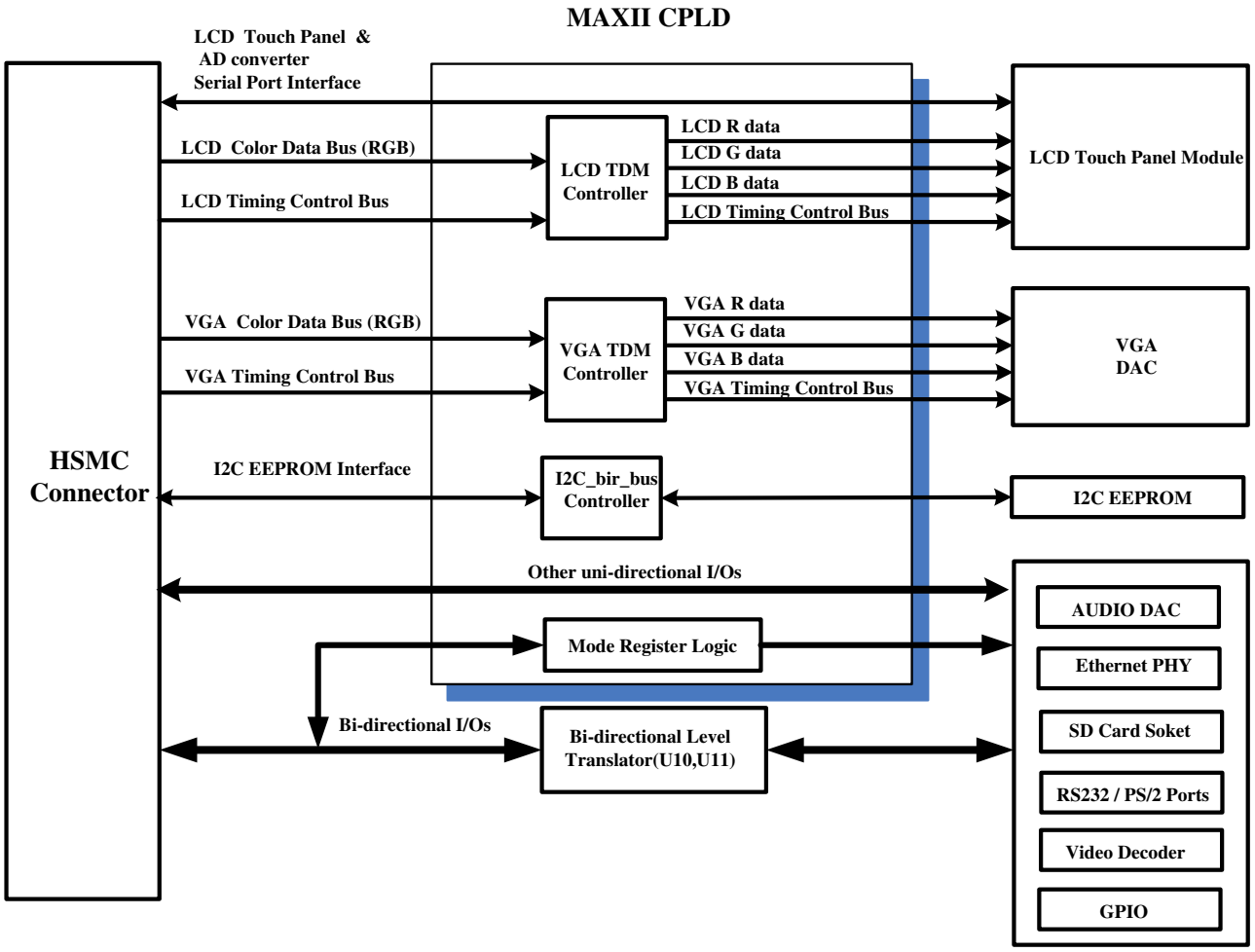


Figure 3.1. The Block Diagram of MTDB Bus Controller

3.3 Timing Protocol of the LCD TDM Controller

Figure 3.2 describes the input timing waveform information of the LCD TDM Controller. The 8-bit wide HC_LCD_DATA signal is presumed to contain a stream of color pixel data, with each pixel represented by three successive clock-cycles of the stream. The data is presented as "BGR". The LCD TDM Controller uses the HC_HD pulse to determine the position of the BLUE color sample, and thus the start of each three-clock pixel-period. State transitions on HC_HD (0-->1 or 1-->0) coincide with the presentation of BLUE color on the HC_LCD_DATA input. The GREEN and RED values for that same pixel are presented on the next two clock-cycles. Figure 3.3 shows the timing information from the output side. The LCD TDM block will generate a NCLK clock and 24-bit RGB data to the LCD panel. The NCLK signal runs at 1/3 frequency of the incoming clock HC_NCLK. In addition, the timing protocol of the VGA TDM controller is very similar to the LCD TDM controller. The input color data bus HC_VGA_DATA changes from 8-bit to 10-bit, and the VGA TDM controller uses the HC_VGA_HS to determine the position of the BLUE color sample.

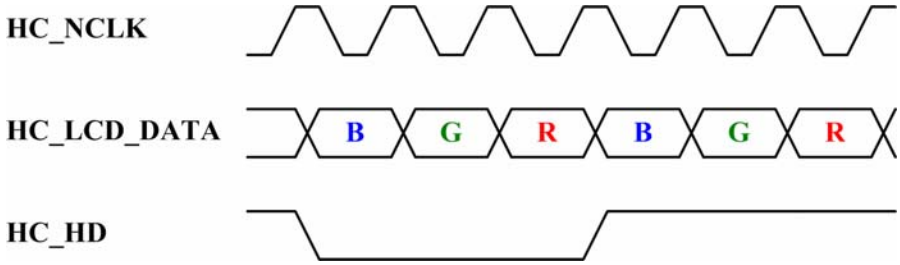


Figure 3.2. The timing diagram shows the input side of the VGA TDM Controller

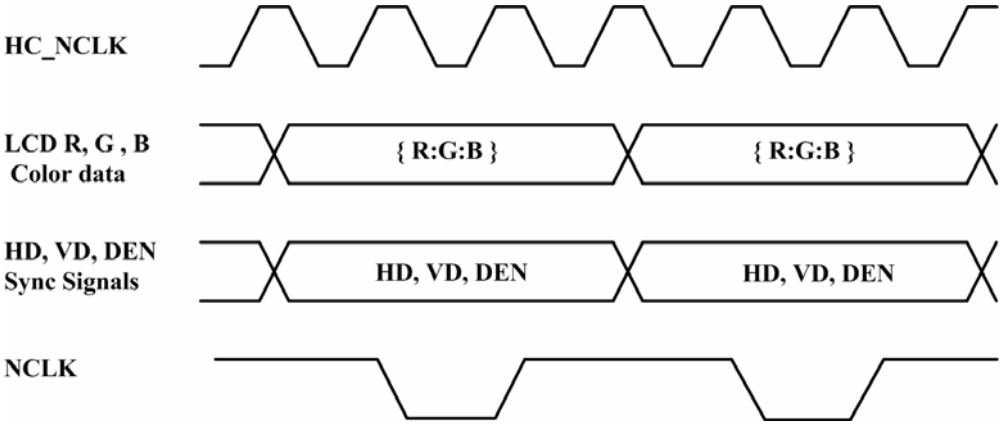


Figure 3.3. The timing diagram shows the output side of the LCD TDM Controller

3.4 Level Translators and MAX II Mode Control Register

Bidirectional level shift interface (U10, U11, U12)

There are 3 bidirectional level shifters on the board (U10, U11, and U12). These chips are all Texas Instruments TXB0108 or TXB0104 devices. U10 is used completely as bi-directional level-shifters from 2.5V input (Cyclone III FPGA) to 3.3V required by many of the interface chips. U11 and U12, however, are also used to multiplex signals based on the setting of the mode-select logic register.

Figure 3.4 shows the block diagram and signals for the combination of the HSMC connector, the MAX II device and the level-shifters. Figure 3.5 shows the Level Shift Interface schematic. Table 3.1 shows the pinouts of level shift interface with HSMC connector for U11 (straight level shifting).

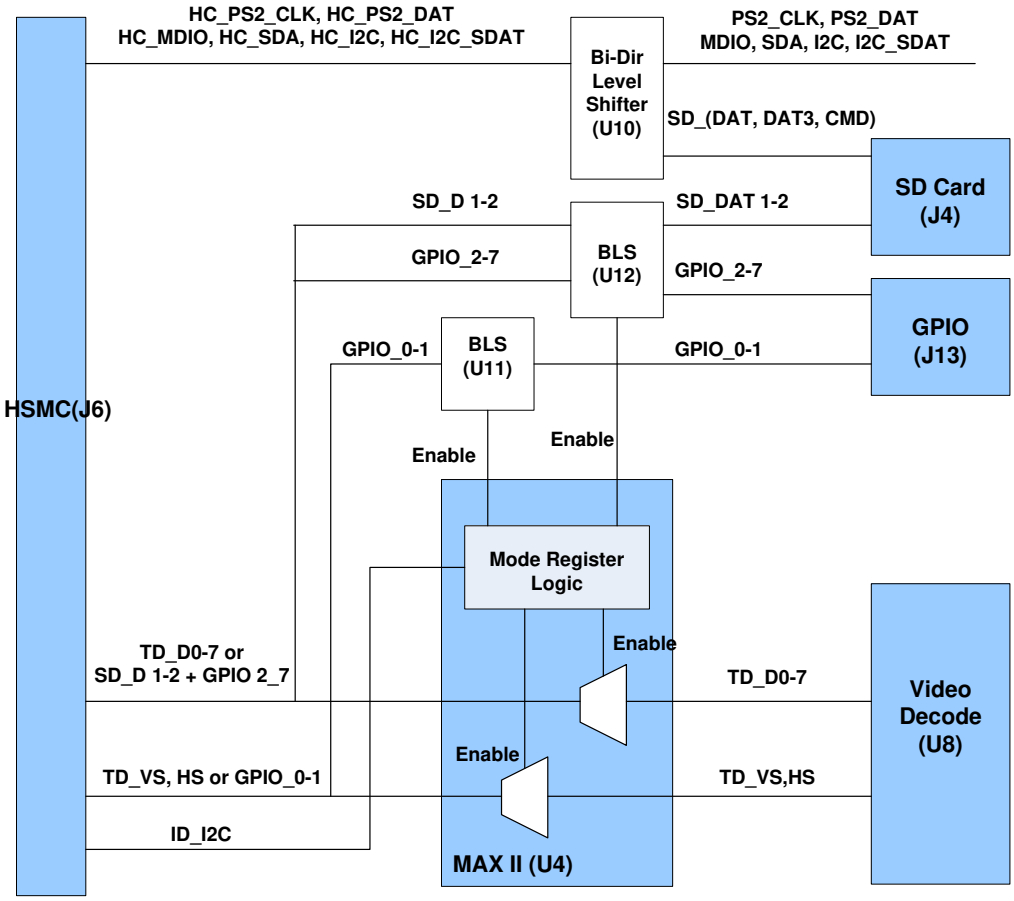


Figure 3.4. Block Diagram of Bidirectional Level Shift Interface and MAX II Control

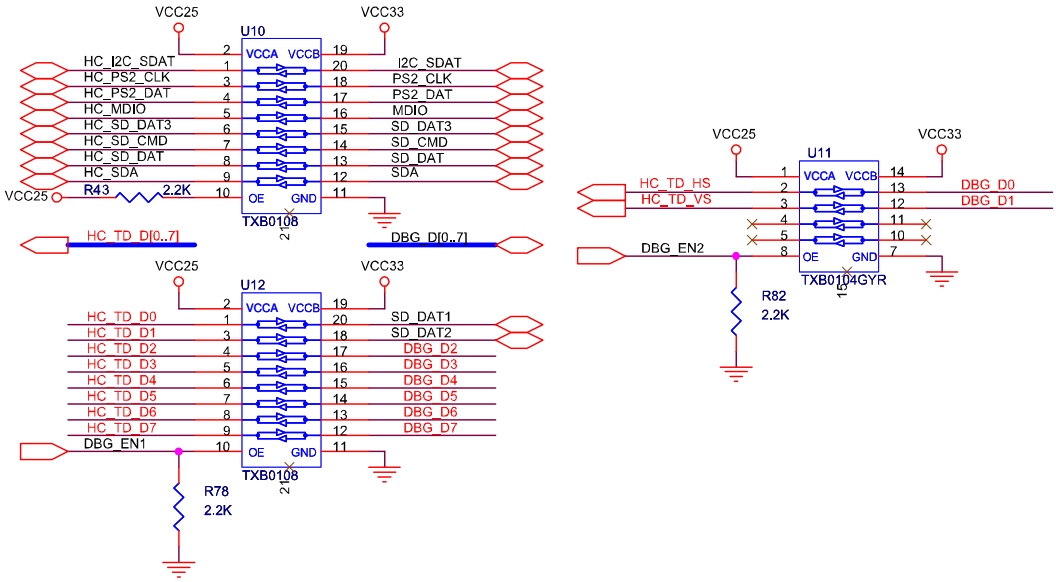


Figure 3.5. Level Shift Interface Schematic.

Table 3.1 Device U11 Level Shift Interface Pinouts with HSMC Connector

HSMC PIN#	Signal Name		Interface Device	
	HSMC Side	Device Side	Pin #	Signal Description
33	HC_I2C_SDAT	I2C_SDAT	U1.27,U8.33	I2C data to audio codec and video decoder.
43	HC_PS2_CLK	PS2_CLK	J9.6	PS/2 Clock
47	HC_PS2_DAT	PS2_DAT	J9.1	PS/2 Data
49	HC_MDIO	MDIO	U2.30	Ethernet PHY Management Data I/O
53	HC_SD_DAT3	SD_DAT3	J4.1	SD 1-bit Mode: Card Detect SD 4-bit Mode: Data3 SPI Mode: Chip Select (Active Low)
44	HC_SD_CMD	SD_CMD	J4.2	SD 1-bit Mode: Command Line SD 4-bit Mode: Command Line SPI Mode: Data In
48	HC_SD_DAT	SD_DAT	J4.7	SD 1-bit Mode: Data Line SD 4-bit Mode: Data0 SPI Mode: Data Out
50	HC_SDA	SDA	J10.44	LCD 3-Wire Serial Interface Data

Bidirectional level shift interfaces and the Mode Control Registers

In order to provide additional peripheral flexibility, the MTDB provides the user with 3 separate pinout modes. These modes as described in Table 3.2, affect the usage of the Video Decoder (U8), the SD-Card Connector (J4), and the 10-pin GPIO connector (J13). This section describes the mode configuration details and signals that are affected for each mode. Chapter Appendix describes the EEPROM and Mode-Settings tool used to change the mode register value.

Table 3.2 Device U11 Level Shift Interface Pinouts with HSMC Connector

Mode Register	Action	Video Decoder	GPIO	SD Card
0	Video decoder in standard x8 operating mode. SD Card in 1-bit mode. No GPIO.	Enabled	0	1-bit
1	Video decoder disabled. 8 GPIO available. SD-Card in 4-bit mode.	Disabled	8	4-bit
2	Video decoder enabled, but Vertical Sync (VS) and Horizontal Sync (HS) pins disabled. 2 GPIO pins available - others are disabled. SD-Card in 1-bit mode.	Enabled but no VS or HS signals	2	1-bit

- **Bidirectional level shift interfaces for Mode 0**

Mode 0 is the compatibility mode for the original version of the MTDB. In this mode, The bidirectional voltage level shifters U11 and U12 are disabled, and the SD-Card (J4) has a 1-bit interface, there no GPIO pins available on J13, and the video decoder (U8) is enabled. Figure 3.6 shows the block diagram for this mode which is a subset of the block diagram shown in Figure 3.4. Table 3.3 shows the signals enabled to the HSMC connector.

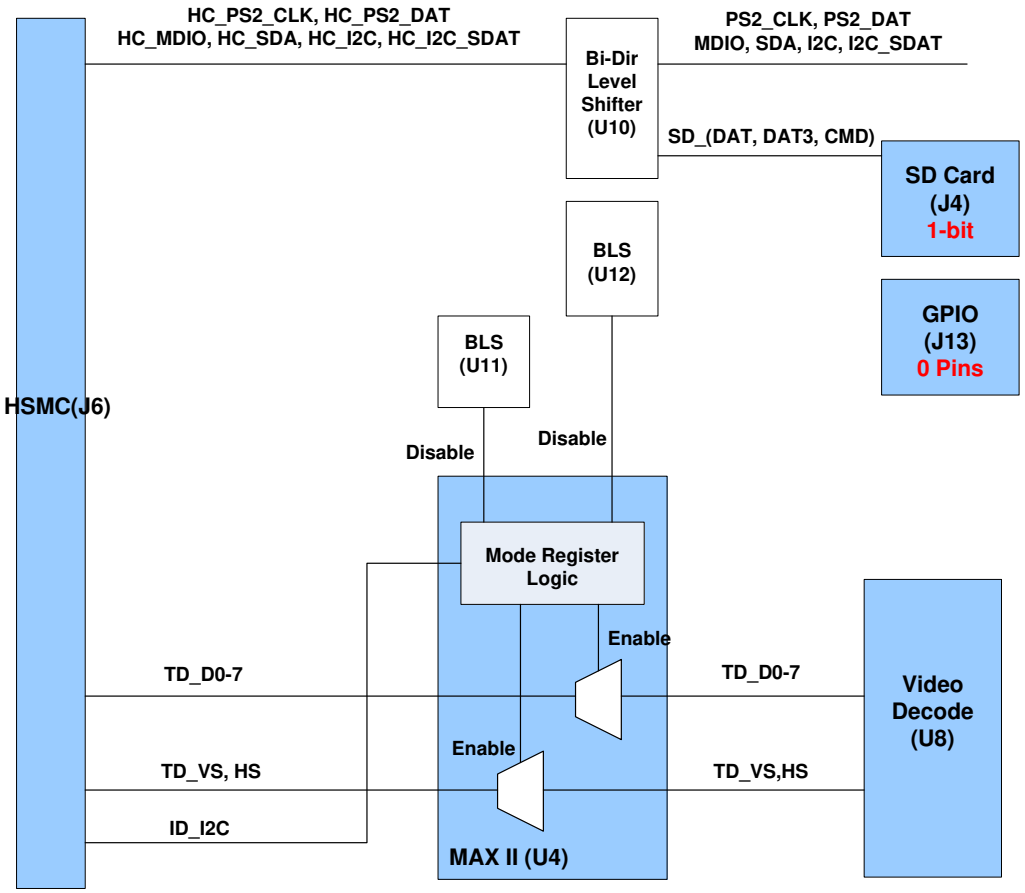


Figure 3.6. Block Diagram of Bidirectional Level Shift Interface for Mode 0

Table 3.3 MAXII Pinouts with HSMC Connector in Mode 0

HSMC PIN#	Signal Name		Interface Device	
	HSMC Side	Device Side	Pin #	Signal Description
56	HC_TD_D0	TD_D0	U4.V8	Video decoder data0
60	HC_TD_D1	TD_D1	U4.T8	Video decoder data1
62	HC_TD_D2	TD_D2	U4.T9	Video decoder data2
66	HC_TD_D3	TD_D3	U4.V9	Video decoder data3
68	HC_TD_D4	TD_D4	U4.U9	Video decoder data4
72	HC_TD_D5	TD_D5	U4.U10	Video decoder data5
74	HC_TD_D6	TD_D6	U4.V10	Video decoder data6
78	HC_TD_D7	TD_D7	U4.T10	Video decoder data7
84	HC_TD_VS	TD_D8	U4.V11	Video decoder vertical sync signal
86	HC_TD_HS	TD_D9	U4.T11	Video decoder horizontal sync signal

- **Bidirectional level shift interfaces for Mode 1**

In mode 1, the bidirectional voltage level shifters U11 and U12 are enabled and the multiplexing in the MAXII device is disabled. This mode disables the signals from the video decoder (U8) and provides the signals to all the SD-Card (J4) to run in 4-bit mode. Also there are now 8 GPIO pins available on J13. Figure 3.7 shows the block diagram for this mode which is a subset of the block diagram shown in Figure 3.4. Table 3.4 shows the signals enabled to the HSMC connector.

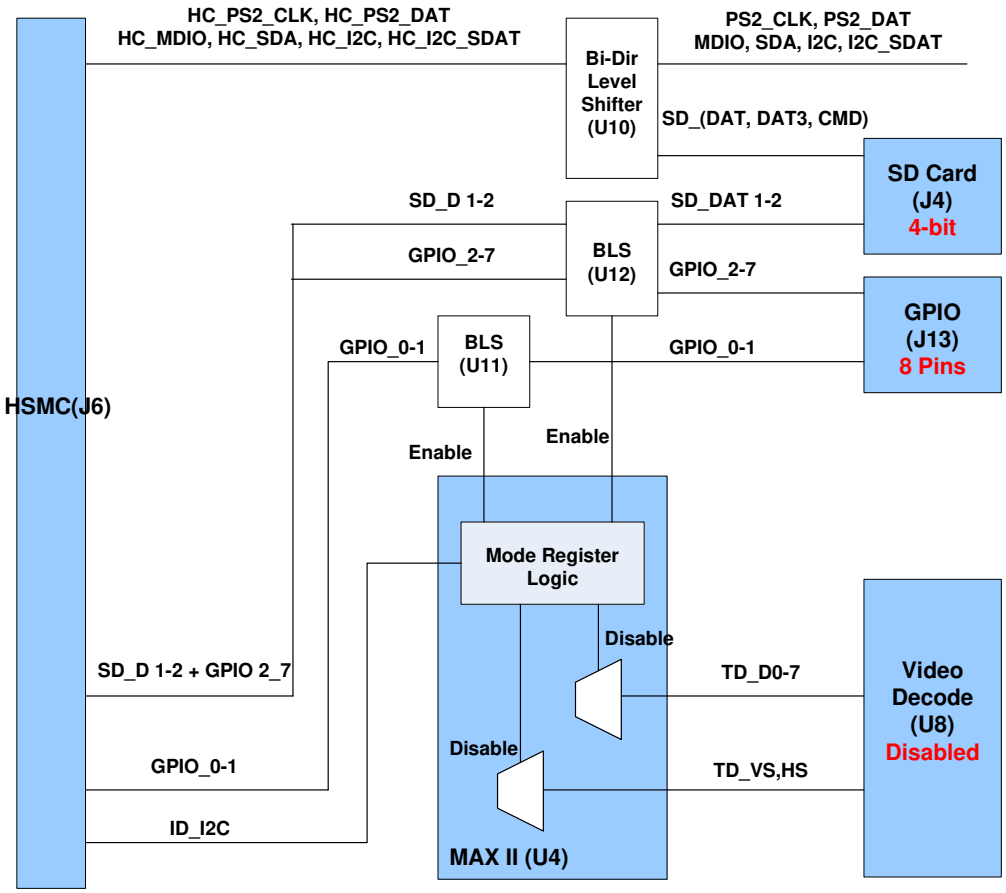


Figure 3.7. Block Diagram of Bidirectional Level Shift Interface for Mode 1

Table 3.4 Device U11 and U12 Level Shift Interface Pinouts with HSMC Connector in Mode 1

HSMC PIN#	Signal Name		Interface Device	
	HSMC Side	Device Side	Pin #	Signal Description
56	HC_TD_D0	SD_DAT1	U12.20	SD-Card data bus signal 1 for 4-bit mode
60	HC_TD_D1	SD_DAT2	U12.18	SD-Card data bus signal 2 for 4-bit mode
62	HC_TD_D2	DBG_D2	U12.17	GPIO data pin 2
66	HC_TD_D3	DBG_D3	U12.16	GPIO data pin 3
68	HC_TD_D4	DBG_D4	U12.15	GPIO data pin 4
72	HC_TD_D5	DBG_D5	U12.14	GPIO data pin 5
74	HC_TD_D6	DBG_D6	U12.13	GPIO data pin 6
78	HC_TD_D7	DBG_D7	U12.12	GPIO data pin 7
84	HC_TD_VS	DBG_D1	U11.12	GPIO data pin 1
86	HC_TD_HS	DBG_D0	U11.13	GPIO data pin 0

- **Bidirectional level shift interfaces for Mode 2**

In mode 2, the bidirectional voltage level shifter U11 is enabled, allowing GPIO signals 0 and 1 to propagate to the GPIO Header (J13). The complementary multiplexer in the MAX II device disables the vertical sync and horizontal sync signals from the video decoder chip (U8) from propagating. Also in this mode U12 is disabled thus GPIO signals 2 – 7 are not available on the GPIO header (J13), but the complementary multiplexer in the MAX II device enables the propagation of the data bus signals 0 – 7 from the video decoder (U8) to the HSMC connector (J6). Figure 3.8 shows the block diagram for this mode which is a subset of the block diagram shown in Figure 3.4. Table 3.5 shows the signals enabled to the HSMC connector.

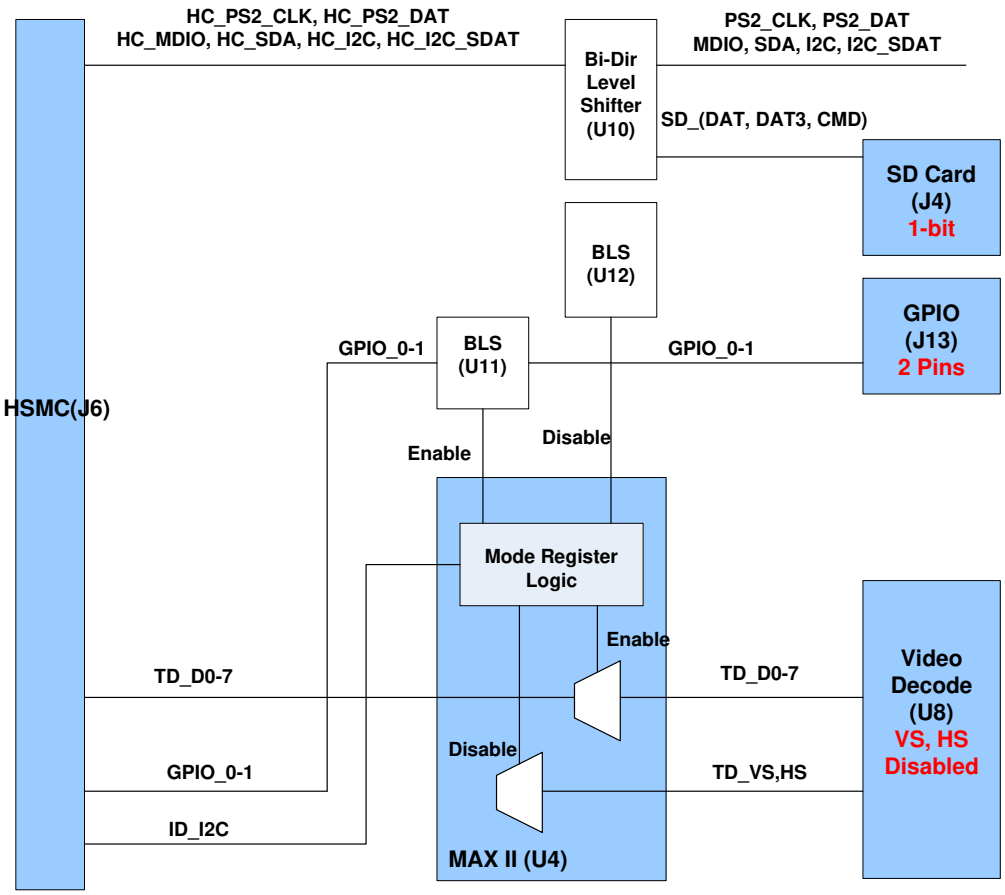


Figure 3.8. Block Diagram of Bidirectional Level Shift Interface for Mode 2

Table 3.5 MAX II and U11 Device Pinouts with HSMC Connector in Mode 2

HSMC PIN#	Signal Name		Interface Device	
	HSMC Side	Device Side	Pin #	Signal Description
56	HC_TD_D0	TD_D0	U4.V8	Video decoder data0
60	HC_TD_D1	TD_D1	U4.T8	Video decoder data1
62	HC_TD_D2	TD_D2	U4.T9	Video decoder data2
66	HC_TD_D3	TD_D3	U4.V9	Video decoder data3
68	HC_TD_D4	TD_D4	U4.U9	Video decoder data4
72	HC_TD_D5	TD_D5	U4.U10	Video decoder data5
74	HC_TD_D6	TD_D6	U4.V10	Video decoder data6
78	HC_TD_D7	TD_D7	U4.T10	Video decoder data7
84	HC_TD_VS	DBG_D1	U11.12	GPIO data pin 1
86	HC_TD_HS	DBG_D0	U11.13	GPIO data pin 0

Chapter 4
Using the MTDB

This chapter gives instructions for using MTDB and describes each of its IO devices. The MTDB is designed for an Altera FPGA board with a HSMC connector. The demonstration projects illustrated here are using MTDB with the latest Cyclone III Starter Board.

4.1 Configuring the Cyclone III Starter Board

The procedure for downloading a circuit from a host computer to the Cyclone III Starter board is described in the Cyclone III Starter Kit User Manual. This tutorial is found in the *CycloneIII_Starter_Kit* folder on the **MTDB System CD-ROM,** and it is also available on the Altera Cyclone III Starter Kit web pages. User is encouraged to read the tutorial first, and to treat the information below as a short reference.

Figure 4.1 illustrates how to connect your MTDB to a Cyclone III Starter board. To download a configuration bit stream into the Cyclone III FPGA, perform the following steps:

- Ensure that power is applied to the Cyclone III Starter board
- Connect the supplied USB cable to the USB Blaster port on the Cyclone III Starter board
- The FPGA can now be programmed by using the Quartus II Programmer module to select a configuration bit stream file with the *.sof* filename extension

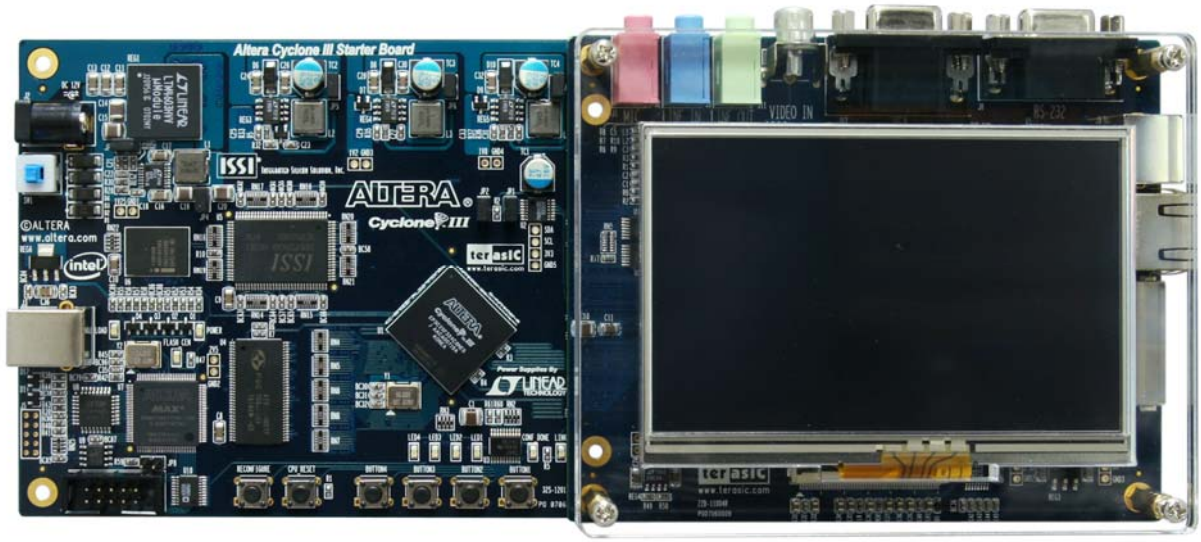


Figure 4.1. Connection of a MTDB Board and a Cyclone III Starter Board.

Users can find the default demonstration project under the *Demonstrations/default* folder in the **MTDB System CD-ROM. Users are also encouraged to examine the top-level RTL code when reading the following sections.**

4.2 Connecting MTDB Board with the Altera DE3 Board

To connect the MTDB board with the Altera DE3 board, please refer to the How_to_connect_MTDB_to_DE3.pdf which can be available from the directory "Using_MTDB_on_DE3" in the **MTDB SYSTEM CD**.

4.3 Using the 4.3" LCD Touch Panel Module

The MTDB provides a 4.3" Toppoly TD043MTEA1 active matrix color TFT LCD panel. The LCD Touch Panel module has the highest resolution (800x480) to provide users the best display quality for developing applications. The LCD panel supports 24-bit parallel RGB data interface and provides 3-wire serial port interface to control the display function registers.

The MTDB Board is also equipped with an Analog Devices AD7843 touch screen digitizer chip. The AD7843 is a 12-bit analog to digital converter (ADC) for digitizing x and y coordinates of touch points applied to the touch screen. Also, the coordinates of the touch point can be read through the serial port interface on the AD7843. However, because of limited IOs of the HSMC connector, the clock signal of the serial port interface for the LCD panel and AD7843 share the same HSMC connector IO called HC_ADC_DCLK, **users must not control both LCD panel and AD7843 at the same time.**

To display images on the LCD panel correctly, the first thing users need to do is that the RGB color data and synchronization signals need to follow the timing specification of the LCD Touch panel as shown in Figure 4.2, Figure 4.3, Table 4.1, and Table 4.2. Further more, because the number of user IOs of the HSMC connector are limited, the LCD RGB data and synchronization signals outputted to the MTDB board need to be multiplex to fit the input timing specification of the LCD TDM Controller on the MTDB board as mention in the Section 3.3.

Finally, the associated schematic of the LCD touch panel module is given in Figure 4.4, and the pin assignments are listed in Table 4.3. Detailed information for using the LCD panel and AD7843 are available in their datasheets, which can be found in the *Datasheet* folder of the **MTDB System CD-ROM** or from the manufacturers' web site.

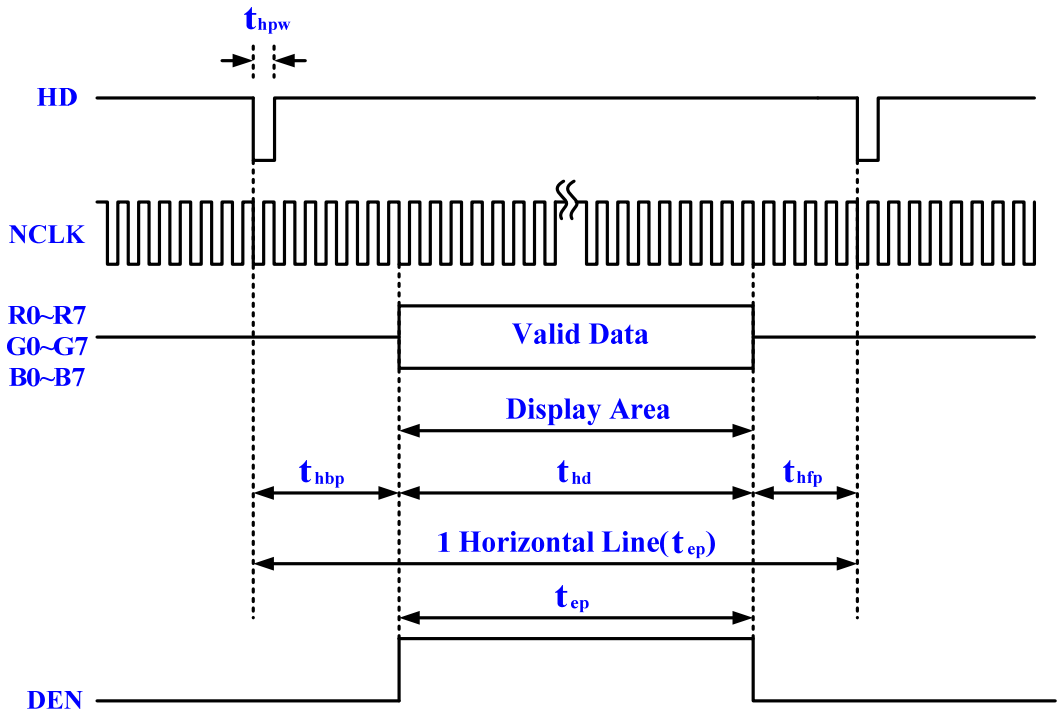


Figure 4.2 LCD horizontal timing specification

Table 4.1 LCD horizontal timing parameters

Parameter		Symbol	Panel Resolution			Unit
			800xRGBx480	480xRGBx272	400xRGBx240	
NCLK Frequency		FNCLK	33.2	9	8.3	MHz
Horizontal valid data		t_{hd}	800	480	400	NCLK
1 Horizontal Line		t_h	1056	525	528	NCLK
HSYNC Pulse Width	Min.	t_{hpw}	1			NCLK
	Typ.		-			
	Max.		-			
Hsync back porch		t_{hbp}	216	43	108	NCLK
Hsync front porch		t_{hfp}	40	2	20	NCLK
DEN Enable Time		t_{ep}	800	480	400	NCLK

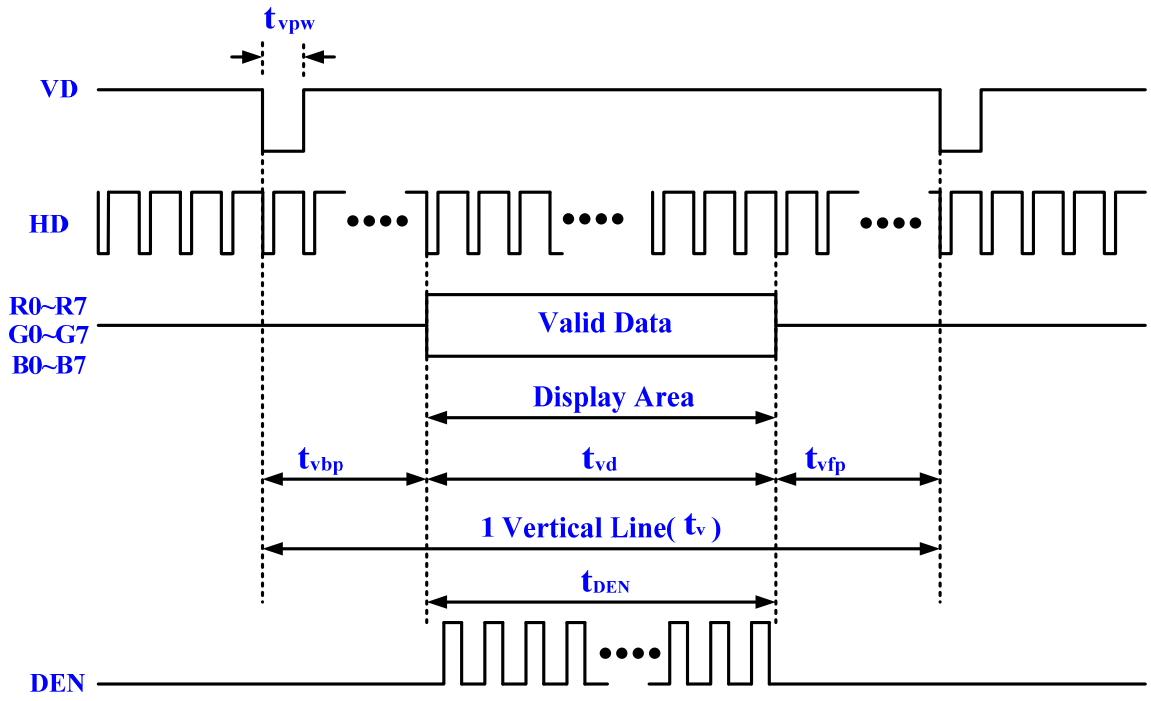


Figure 4.3 LCD vertical timing specification

Table 4.2 LCD vertical timing parameters

Parameter		Symbol	Panel Resolution			Unit
			800xRGBx480	480xRGBx272	400xRGBx240	
Vertical valid data		t_{vd}	480	272	240	H
Vertical period		t_{v}	525	286	262	H
VSYNC Pulse Width	Min.	t_{vpw}	1			H
	Typ.		-			
	Max.		-			
Vertical back porch		t_{vbo}	35	12	20	H
Vertical front porch		t_{vfpo}	10	2	2	H
Vertical blanking		t_{vb}	45	14	22	H