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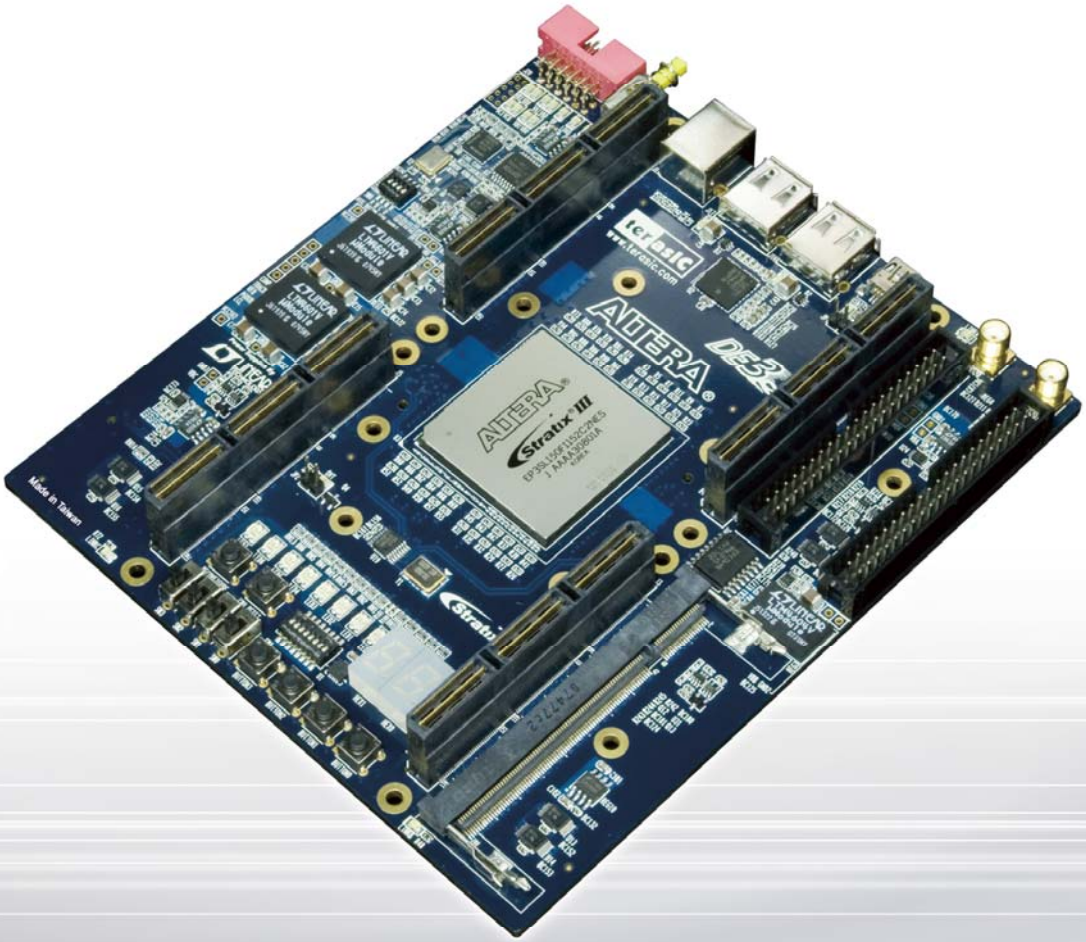


ALTERA®

DE3

Development and Education Board

User Manual

Stratix™III

NiosII

USB
UNIVERSAL SERIAL BUS

CONTENTS

Chapter 1
Overview

This chapter presents the features and design characteristics of the DE3 board.

1.1 Introduction

The DE3 board has plenty of features that allow users to implement a wide range of designed circuits. The Stratix® III device is capable of dealing with resource-consuming projects and complex algorithm verification; the HSTC interface is equipped for high-speed inter-connection and configurable I/O standards. The DDR2 SO-DIMM socket puts the experience of faster memory access into practice, while the SD card socket provides the realization of data storage extension.

In addition, the DE3 board has an innovative stackable mechanism which allows users to assemble DE3 boards into a powerful system as shown in Figure 1.1. The DE3 can also connect with multiple daughter boards designed by Terasic in stock.

Figure 1.1 The stackable mechanism of the DE3 board

1.2 Layout and Components

Figure 1.2 and Figure 1.3 is the top and bottom view of the DE3 board. It depicts the layout of the board and indicates the location of the connectors and key components. Users can refer to this figure for relative location when the connectors and key components are introduced in the following chapters.

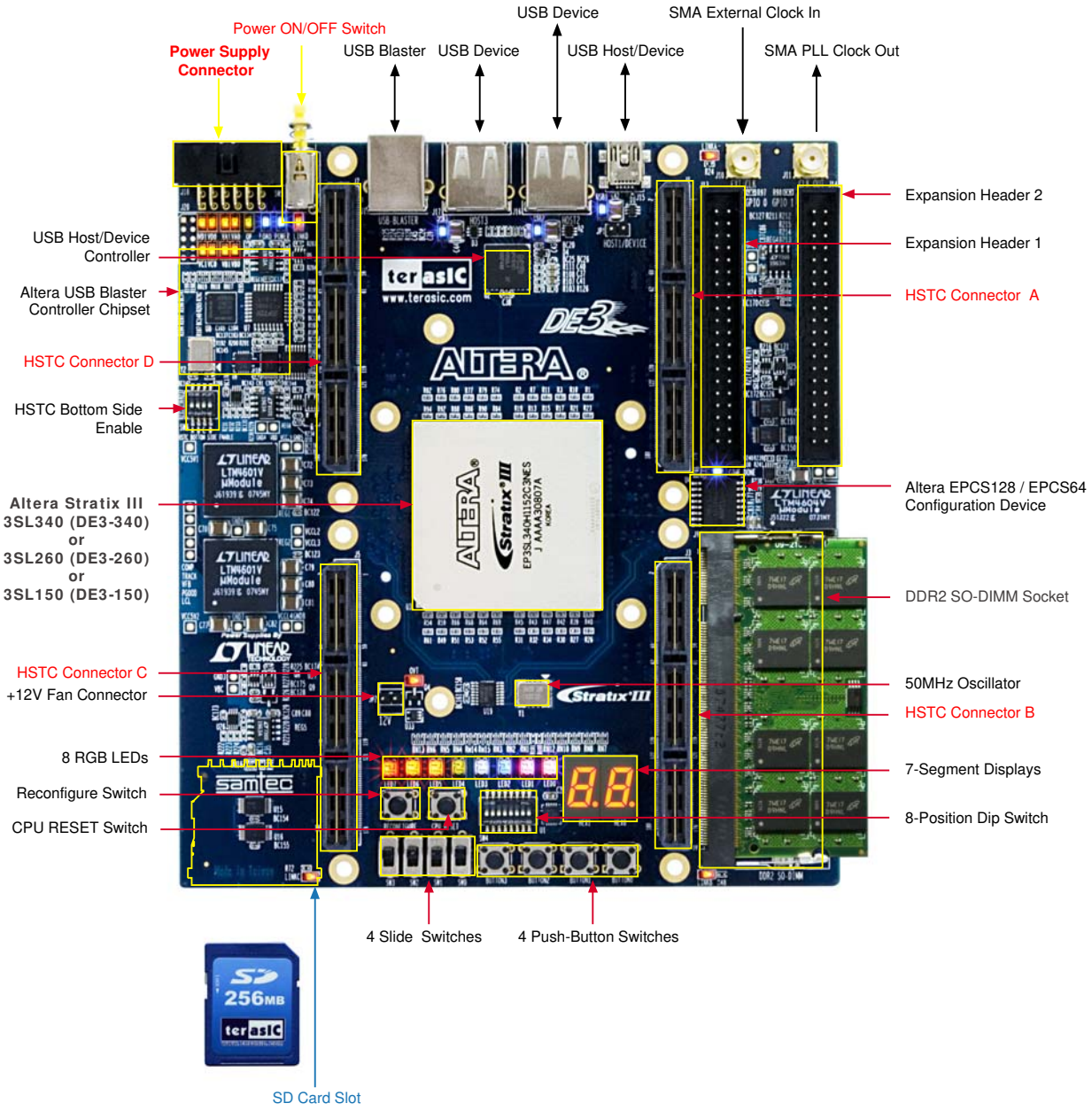


Figure 1.2 The DE3 board (Top view)

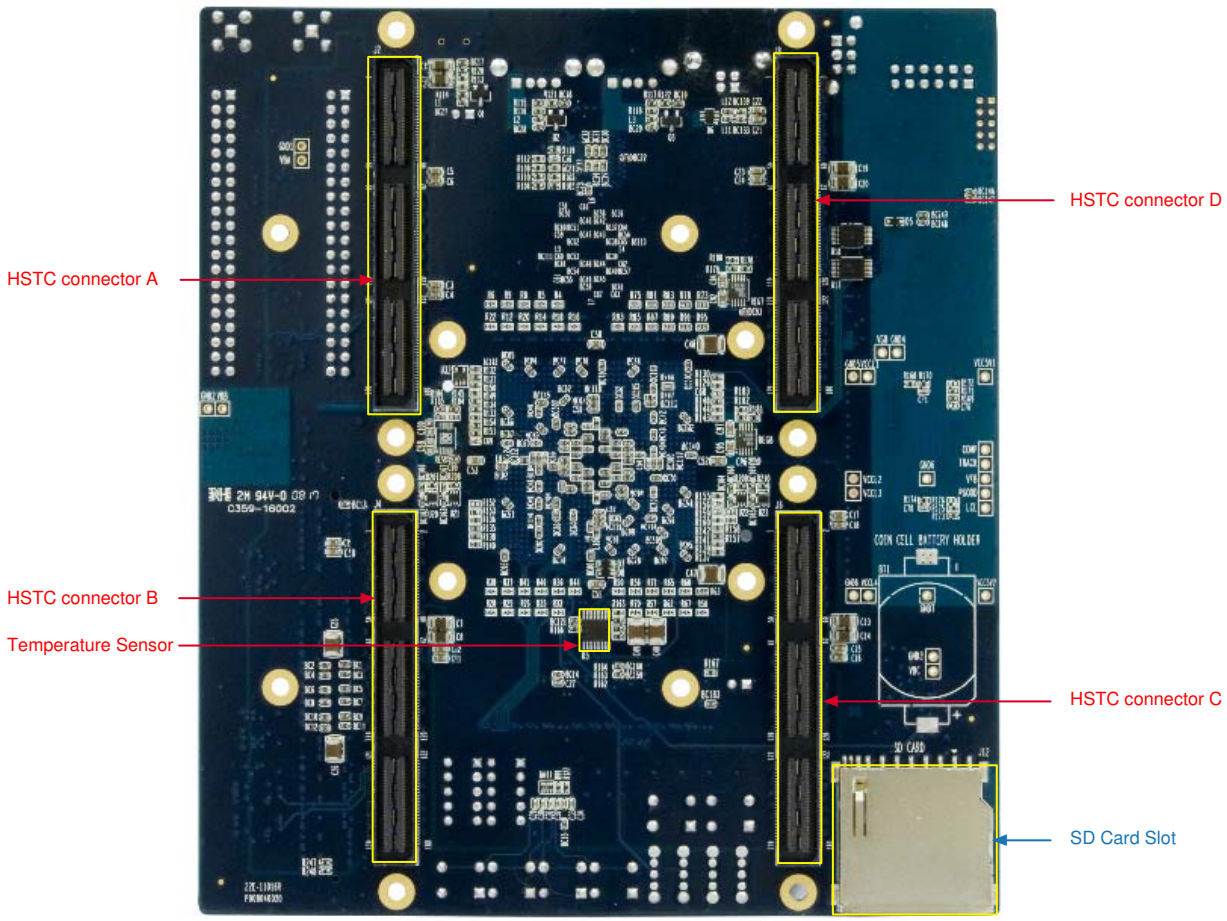


Figure 1.3. The DE3 board (Bottom view)

The following hardware is implemented on the DE3 board:

- Altera Stratix® III FPGA device (3SL340/3SE260/3SL150)
- FPGA configuration interface:
  - Built-in USB Blaster circuit for programming and user API control
  - Altera Serial Configuration device – EPCS128/EPCS64
- Expansion Interface:
  - 8 HSTC connectors
  - Two 40-pin Expansion Headers
- Memory Interface:
  - DDR2 SO-DIMM socket
  - SD Card socket

- User I/O Interface:
  - 4 push-button switches
  - 4 slide switches
  - 1 eight position DIP switch
  - 2 seven-segment displays
  - 8 RGB LEDs
- Clock system
  - One 50MHz oscillator
  - 2 SMA connectors for external clock input and PLL clock output
- Other interface
  - 1 USB Host/Slave controller(1 three-ports USB Host/Device controller)
  - 1 temperature sensor chip for FPGA temperature measurement

1.3 Block Diagram of the DE3 Board

Figure 1.4 shows the block diagram of the DE3 board. To provide maximum flexibility for the users, all key components are connected with the Stratix III FPGA device. Thus, users can configure the FPGA to implement any system design.

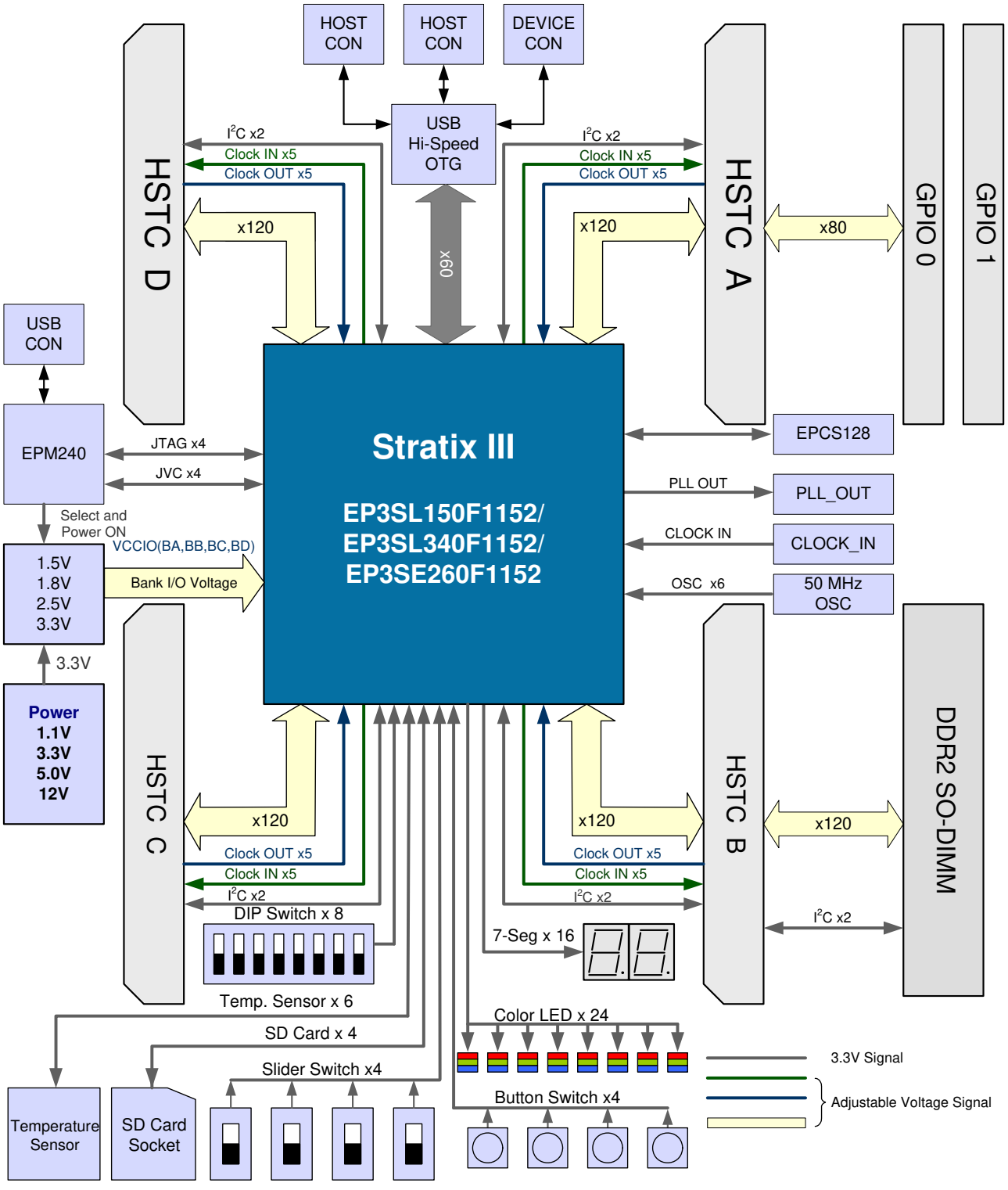


Figure 1.4 Block diagram of the DE3 board

Below is more detailed information regarding the blocks in Figure 1.4:

Stratix III FPGA

- **EP3SL340**
  - 338,000 logic elements (LEs)
  - 18,381K Total Memory Kbits
  - 526 18x18-bit Multipliers blocks
  - 12 phase-locked-loops (PLLs)
  -
- **EP3SE260**
  - 254,400 logic elements (LEs)
  - 16,282K Total Memory Kbits
  - 768 18x18-bit Multipliers blocks
  - 12 phase-locked-loops (PLLs)

- **EP3SL150**
  - 142,000 logic elements (LEs)
  - 6,390K Total Memory Kbits
  - 384 18x18-bit Multipliers blocks
  - 8 phase-locked-loops (PLLs)

Serial Configuration device and USB Blaster circuit

- Altera's EPCS128/EPCS64 Serial Configuration device
- On-board USB Blaster for programming and user API control
- Support JTAG mode

DDR2 SO-DIMM socket

- Up to 4GB capacity
- Share the same I/O bus with HSTC connector B

SD card socket

- Provides SPI and 1-bit SD mode for SD Card access

Push-button switches

- 6 push-button switches
  - 1 CPU Reset
  - 1 FPGA Reconfigure
  - 4 user-defined inputs
- Debounced by a Schmitt trigger circuit
- Normally high; generates one active-low pulse when the switch is pressed

Slide switches

- 4 slide switches for user-defined inputs
- When a switch is set to the DOWN or UP position (i.e., close to or away from the edge of the DE3 board), it causes logic 0 or 1, respectively.

Clock inputs

- 50MHz oscillator
- 1 SMA connector for PLL clock output
- 1 SMA connector for external clock input

USB Host/Slave controller

- Complies fully with Universal Serial Bus Specification Rev. 2.0
- Support data transfer at high-speed, full-speed, and low-speed
- Support both USB host and device
- Three USB ports (one type mini-AB for host/device and two type A for host)
- Support Nios II with the Terasic driver
- Support Programmed I/O (PIO) and Direct Memory Access (DMA)

Eight 180-pin High Speed Terasic Connectors (HSTC) expansion headers

- 4 male and 4 female connectors are on the top and the bottom of DE3 board, respectively.
- 240 LVDS pairs of user-defined IO pins
- Configurable I/O voltage for 3.3V, 2.5V, 1.8V, and 1.5V

Two 40-pin expansion headers

- 72 FPGA I/O pins, as well as 8 power and ground lines, are brought out to two 40-pin expansion connectors
- 40-pin header is designed to accept a standard 40-pin ribbon cable used for IDE hard drives
- Share the same I/O pins with HSTC connector A

1.4 Before You Begin

At all times, read the manual for the application instruction and keep precaution on the equipment during operation to ensure nothing goes wrong. If so, stop operation immediately and revise the procedures again or contact us if there is anything unclear in the instruction manual. Never try to revise equipment I/O direction, including wires and cables, or plug the DB(s) onto the MB in the way which it is not designed for. By doing so, it can cause problems that beyond warranty.

The information in this document is subject to change without notice and does not represent a commitment on the part of the vendor, who assumes no liability or responsibility for any errors that may appear in this manual.

If you do not properly set the device setting, causing the device to malfunction or fail, we cannot guarantee any responsibility. About

Chapter 2
Using the DE3 Board

This chapter gives instructions for using the DE3 board and its components.

It is strongly recommended that users should read the *Getting Started with the Altera DE3 board.pdf* before using the DE3 board. The document is located in the *DE3_usermanual* folder on the **DE3 System CD**. The contents of the document includes following:

1. Purpose of the DE3 Board
2. Scope of the DE3 Board and Supporting Material
3. Installing the Altera Design Software
4. Obtain a License File from Altera's website
5. Setup the License File for Terasic Power Controller IP.
6. Install the USB Blaster Driver
7. Power up the DE3 Board
8. Programming the FPGA Device on the DE3 Board

2.1 Configuring the FPGA and Serial Configuration Device

■ **Programming the FPGA device:**
The DE3 board has a built-in USB Blaster circuit, which allows users to program the FPGA device using USB cable and Quartus II programmer in JTAG mode. Current configuration will be lost when the power is turned off.

To download a configuration bit stream into the Stratix III FPGA, perform the following steps:

- Make sure that power is provided to the DE3 board
- Connect the USB cable supplied to the USB Blaster port of the DE3 board (see Figure 2.1)
- The FPGA can now be programmed in the Quartus II Programmer by selecting a configuration bit stream file with the *.sof* filename extension.

Please refer to *Getting Started with the Altera DE3 board.pdf* for more detailed procedure of FPGA programming.

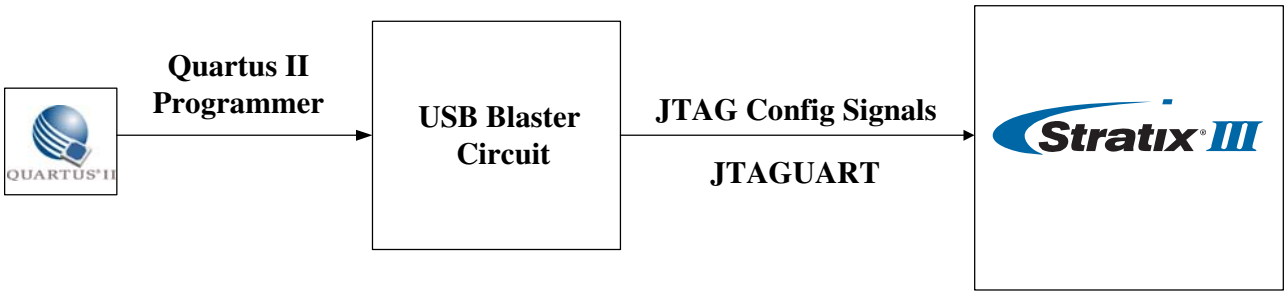


Figure 2.1 The JTAG configuration scheme

■ **Programming the serial configuration device :**

The DE3 board contains a serial configuration device (U4) that stores configuration data for the Stratix III FPGA. This configuration data is automatically loaded from the serial configuration device chip into the FPGA when the board is powered up.

Since the *Active Serial* programming interface is not supported on the DE3 board, users will need to use a Serial Flash Loader (SFL) function to program the serial configuration device via the JTAG interface. The FPGA-based SFL is a soft intellectual property (IP) core within the FPGA that bridges the JTAG and flash interfaces. The SFL mega-function is available from Quartus II software. Figure 2.2 shows the programming method when adopting a SFL solution.

Please refer to *Appendix C Programming the Serial Configuration device* for the basic programming instruction on the serial configuration device. More detailed information on the SFL mega-function can be found in *Altera Application Note 370: Using the Serial Flash Loader With the Quartus II Software.*

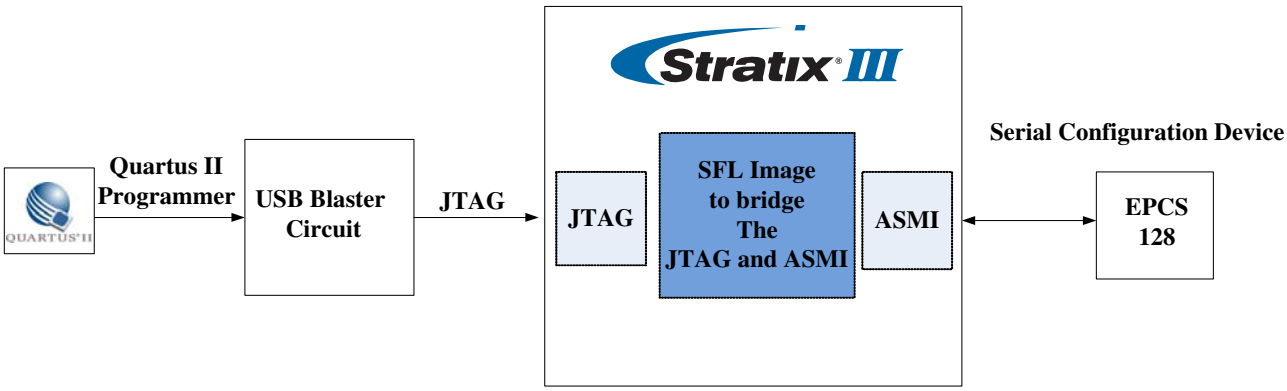


Figure 2.2. Programming a serial configuration device with the SFL solution

2.2 JTAG Chain

This section describes how to setup the JTAG chain on DE3 board.

If the DE3 board is used without any board connected and all the positions in SW6 are switched to OFF (i.e., down position), the JTAG-interface signals of all HSTC connectors are bypassed, as shown in Figure 2.3.

When the top HSTC connector is not connected with any daughter board, the JTGA interface is bypassed. If a daughter board is connected to the top HSTC connector, the JTAG interface will be enabled automatically. Figure 2.4 shows the JTAG chain with a daughter board connected to the DE3 board via top HSTC connector A. Note that if the daughter board does not use the JTAG interface, the TDI and TOD pins on the daughter board must be shorted for the JTAG signals to pass through.

A four position DIP switch (SW6) on DE3 board is used to control the JTAG interface signals of bottom HSTC connectors. Table 2-1 indicates the detailed configurations of SW6. When the bottom connector is connected with other DE3 board or an daughter board, users need to configure the SW6 to connect the JTAG chain to other board accordingly. Figure 2.5 shows there are two DE3 boards stacked, and the JTAG chain is established through HSTA connector A, as shown in Figure 2.6.

Table 2-1. DIP switch (SW6) setting for JTAG interface on bottom HSTC connectors

Position	Switch Setting	
	Turn OFF (lower position)	Turn ON (upper position)
1	Bypass the JTAG interface on the Bottom HSTC connector A(J2)	Enable the JTAG interface for Bottom HSTC connector A(J2)
2	Bypass the JTAG interface on the Bottom HSTC connector B(J4)	Enable the JTAG interface for Bottom HSTC connector B(J4)
3	Bypass the JTAG interface on the Bottom HSTC connector C(J6)	Enable the JTAG interface for Bottom HSTC connector C(J6)
4	Bypass the JTAG interface on the Bottom HSTC connector D(J8)	Enable the JTAG interface for Bottom HSTC connector D(J8)

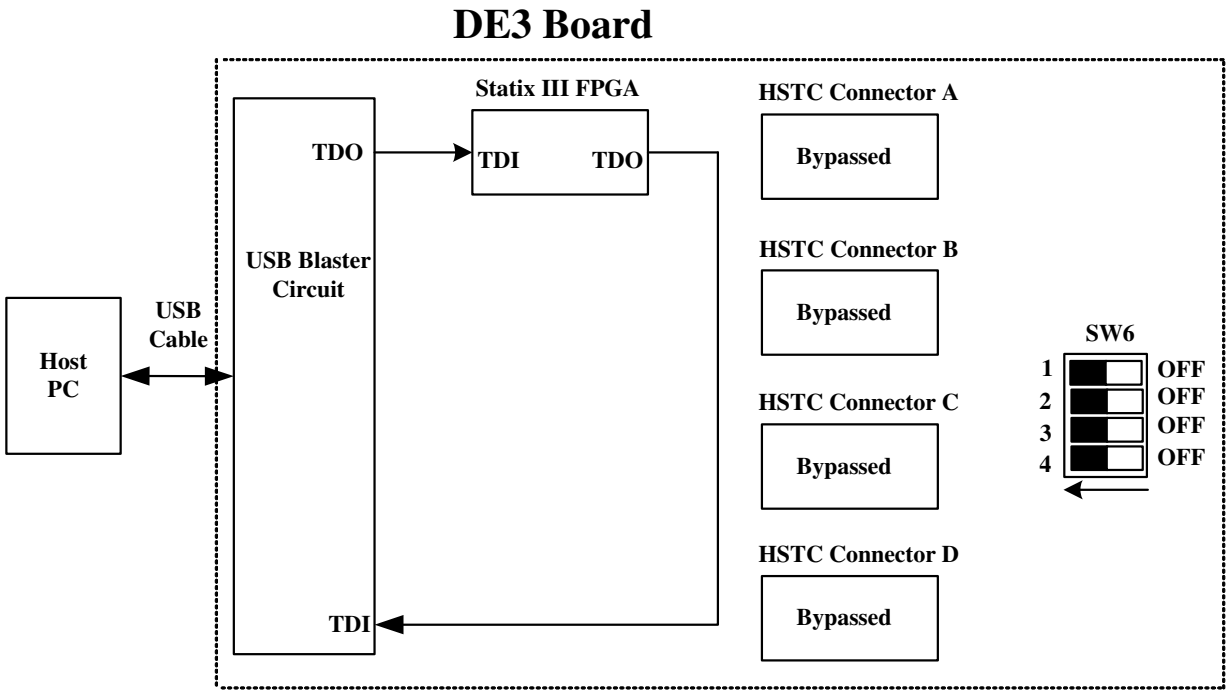


Figure 2.3. JTAG chain for a standalone DE3 board

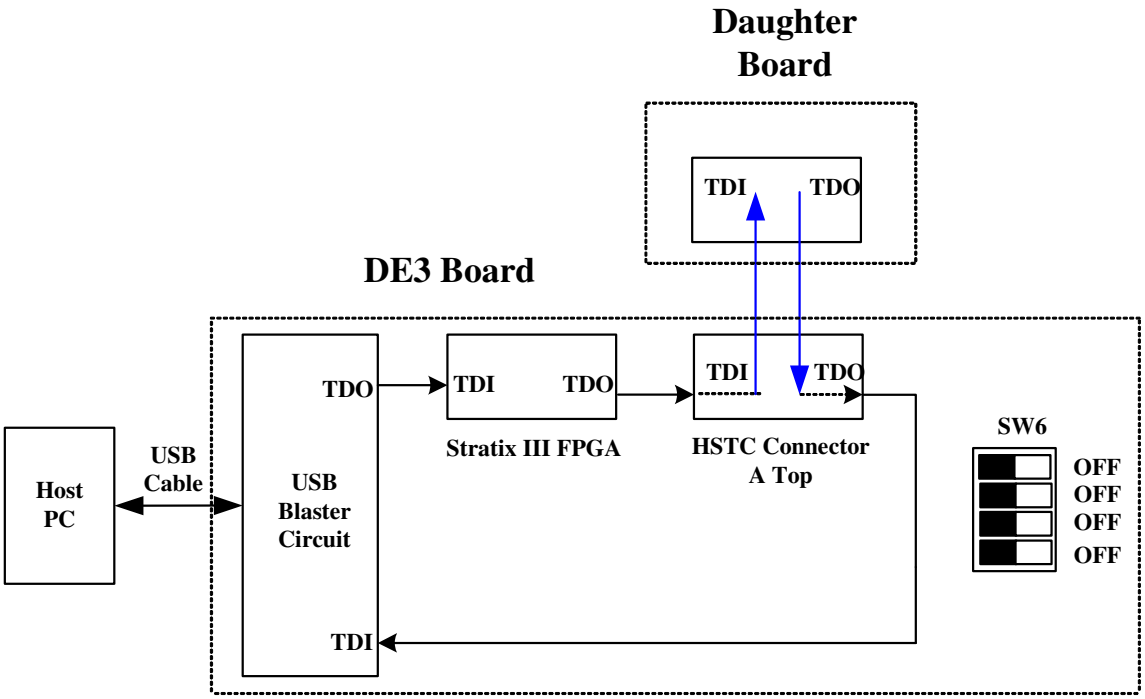


Figure 2.4. JTAG chain for a daughter board connected with DE3 board via top HSTC connector A

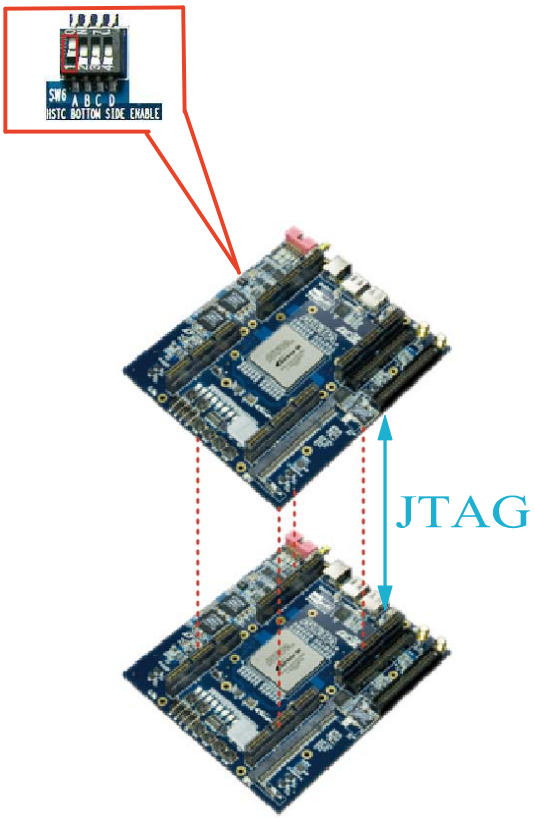


Figure 2.5. The two DE3 boards stacked and the JTAG path is established through HSTC connector A.

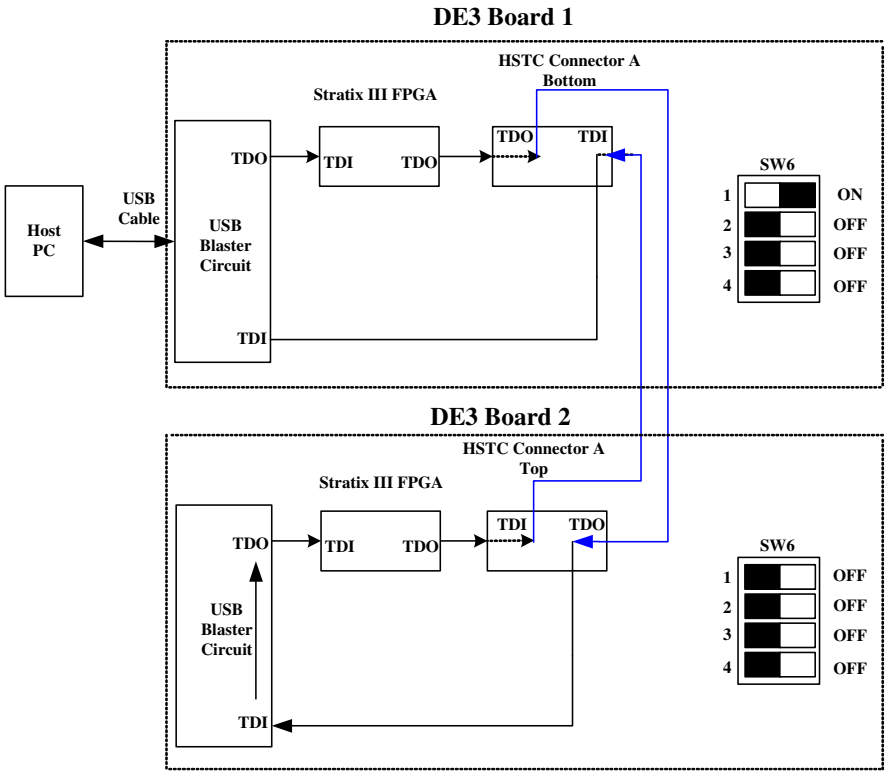


Figure 2.6. JTAG chain for two stacked DE3 boards

2.3 Using the User I/O Interface

- **Push-Button Switches:**

The DE3 board provides four user-defined, one CPU reset, and one Reconfigure push-button switches. The Reconfigure push-button is used to force a re-boot of the FPGA from the serial configuration device.

The CPU reset push-button is an input to the Stratix III device. It is intended to be the master reset signal for the FPGA designs loaded into the Stratix III device. The CPU reset push -button is connected to the DEV_CLRn pin on the FPGA. The DEV_CLRn setting is a pin option in the Quartus II software that users must enable to function the CPU reset as DEV_CLRn instead of a standard I/O.

Each of these switches is de-bounced using a Schmitt Trigger circuit, as indicated in Figure 2.7. Each push-button provides a high logic level (3.3 volts) or a low logic level (0 volts) when it is not pressed or pressed, respectively. Table A-1 shows the connections between the push-buttons and the FPGA.

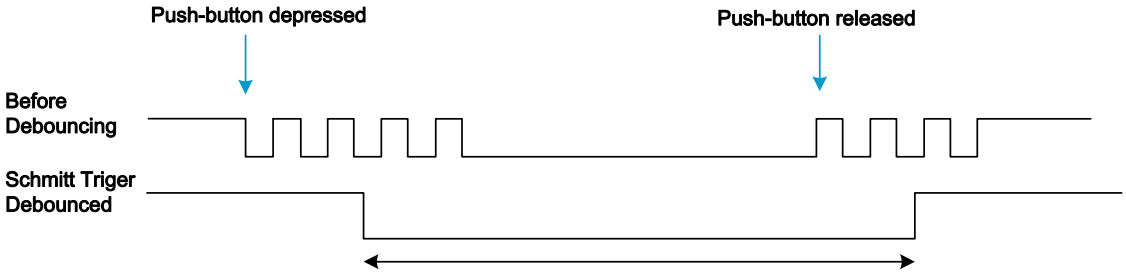


Figure 2.7. Switch debouncing

- **Slide Switches and DIP Switch**

There are also four slide switches and one 8-position DIP switch on the DE3 board. Each switch is connected directly to a pin of the Stratix III FPGA. When a slide switch is in the DOWN position (i.e., closest to the edge of the board) or the UP position, it provides a low logic level (0 volts) or a high logic level (3.3 volts) to the FPGA, respectively. For 8-position DIP switch, when a switch is in the DOWN position (closest to the edge of the board) or the UP position, it provides a high logic level (3.3 volts) or a low logic level (0 volts) to the FPGA. The connections between the slide switches and the FPGA are shown in Table A-2, whereas Table A-3 shows the connections between the 8-position DIP switch and the FPGA.

- **RGB LEDs**

There are 8 RGB user-controllable LEDs on the DE3 board. Each LED has red, green, and

blue color, driven directly by the Stratix III FPGA; The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin names on the FPGA that are connected to the RGB LEDs is given in Table A-4.

■ **7-Segment Displays**

The DE3 board has two 7-segment displays. As indicated in the schematic in Figure 2.8, the seven segments are connected to pins of the Stratix III FPGA. Applying a low or high logic level to a segment to light it up or turns it off.

Each segment in a display is identified by an index listed from 0 to 6 with the positions given in Figure 2.9. In addition, the decimal point is identified as DP. Table A-5 shows the mapping of the FPGA pin assignments to the 7-segment displays.

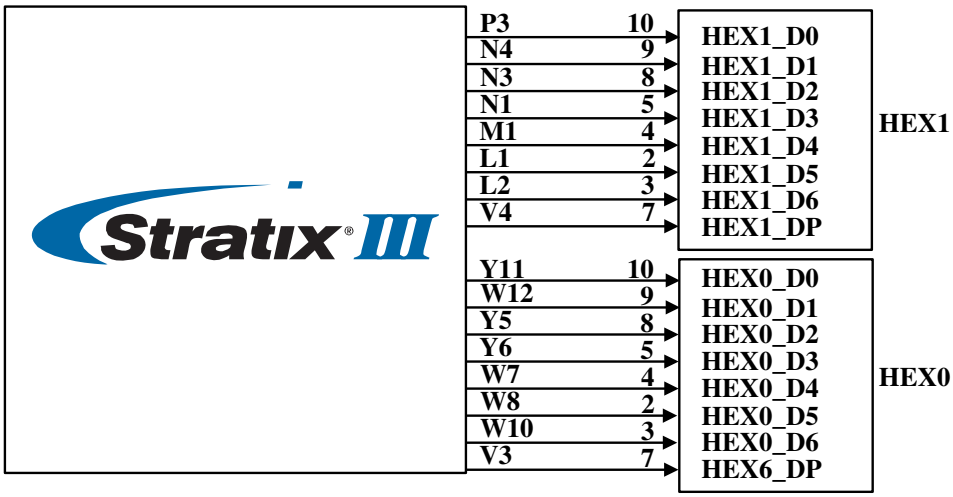


Figure 2.8. Connection between 7-segment displays and Stratix III FPGA

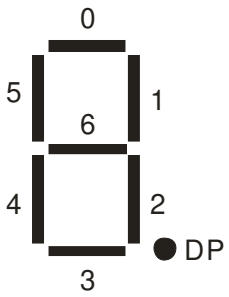


Figure 2.9. Position and index of each segment in a 7-segment display

2.4 I/O Groups and V_{CCIO} Control Circuit

Most of the user-defined I/O pins on Stratix III device are used for connectors. They are divided

into four I/O groups, named A, B, C and D. Table 2-2 shows the relation between I/O groups and connectors.

Table 2-2 The relation between I/O groups and connectors

I/O Group	Connectors
A	HSTC connector A, GPIO expansion headers *(1)*
B	HSTC connector B, DDR2 SO-DIMM socket *(2)*
C	HSTC connector C
D	HSTC connector D

Note:

(1): HSTC connector A and GPIO expansion headers share the same I/O pins.

(2): HSTC connector B and DDR2 SO-DIMM socket share the same I/O pins.

Besides, the V_{CCIO} level for these I/O groups of the FPGA can be configured, and many I/O standards are supported. The I/O standard of each I/O group on DE3 board has to be set through a software utility named "**DE3 System Builder**". Such tool is intended to generate a top level Quartus II project, which includes the power controller IP.

After the FPGA is programmed, the power controller IP will control the V_{CCIO} control circuit to provide desired V_{CCIO} and V_{CCPD} level to the FPGA, according to I/O standard selected by users as indicated in Figure 2.10.With this feature, users can not only confirm if the V_{CCIO} level meets the design requirement, but also reduce the chance of the DE3 board and its daughter cards being damaged.

Please refer to *Stratix III handbook chapter 7. Stratix III Device I/O Features* for more information about the I/O standard and voltage levels of the Stratix III device. There will be more instructions for **DE3 System Builder** in Chapter 4.

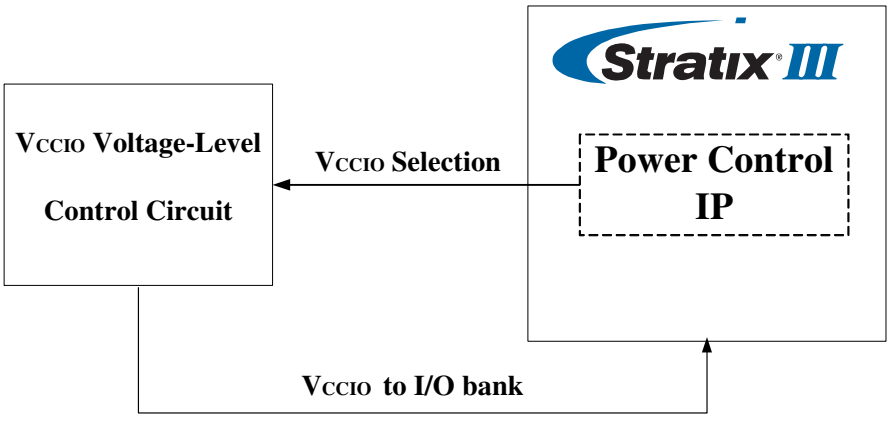


Figure 2.10. The architecture of Power Control IP and V_{CCIO} control circuit

Finally, there are LEDs located at the left-top corner of the DE3 board to indicate the VCCIO voltage level of each I/O group, as shown in Figure 2.11. For example, the LED VA1 and VA2 will be turned on and off, respectively, when the VCCIO of I/O Group A is set to 2.5V. Please refer to Table 2-3 for the status of the LED indicator.

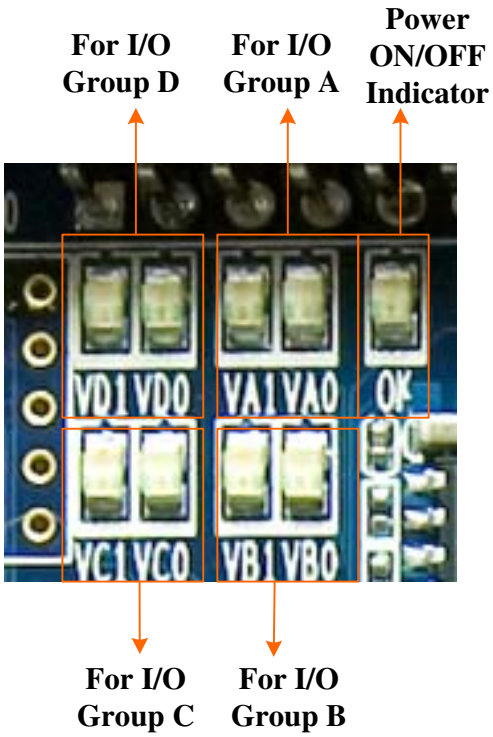


Figure 2.11. The Voltage-Level Indicator for the I/O Groups

Table 2-3 The LEDs indicates the VCCIO voltage level of each IO Group.

LED / VCCIO	Vx1*(1)*	Vx0*(1)*	OK
3.3V	Light ON	Light ON	Light ON
2.5V	Light ON	Light OFF	Light ON
1.8V	Light OFF	Light ON	Light ON
1.5V	Light OFF	Light OFF	Light ON
0V	Light OFF	Light OFF	Light OFF

Note:

(1): Vx1 can be VA1, VB2, VC3, and VD1; Vx0 can be VA0, VB0, VC0, and VD0

2.5 Using the HSTC Connectors

The High Speed Terasic Connector (HSTC) is a high speed expansion interface defined by Terasic Technologies. The DE3 board is equipped with 8 HSTC connectors (J1 ~ J8), which can be used to connect the Stratix III FPGA with daughter boards or the other DE3 boards. The detailed specifications of the HSTC connector are described below:

- **4 HSTC Connector Groups:**
  The eight HSTC connectors on the DE3 board are divided into 4 groups: HSTC A, HSTC B, HSTC C, and HSTC D. Each group has a male and female HSTC connector on the top and bottom side of the DE3 board, respectively. In addition, both the male and female HSTC connector shares the same I/O pins except JTAG and I2C interface.

- **I/O Distribution:**
  Each HSTC connector has 120 single-ended I/O (60 pair differential channels), 10 single-ended IO with 5 each for clock input and output (2 differential clock input and output channel), JTAG and I2C bus. In addition, there are three banks on a HSTC connector. The I/O pins used in differential transceiver channels on bank 1 support true LVDS inout. On bank 2 and 3, the I/O pins used in differential transmitter channels support emulated LVDS via a termination resistor, and the differential receiver channels support true LVDS, as shown in. Figure 2.12. In addition, there is a software utility named "**DE3_HSTC**" which can perform the connection test between the I/O pins of the HSTC connector and Stratix III FPGA. The detailed information about this utility can be found in Appendix D : DE3_HSTC Utility.

- **Configurable I/O Standards:**
  The I/O pins of the HSTC connector support many I/O standards with different voltage level, as the V_{CCIO} supplied to FPGA bank I/O is configurable. Users can choose the I/O standard of HSTC connector in the software utility "**DE3 System Builder**".

- **Compatible with HSMC Connector :**
  The HSTC connector is not only designed to be backward-compatible with the HSMC products, but also provides more I/O pins for further connection. The pin assignments of bank 1 and 2 are exactly the same. The only difference between the HSMC and HSTC connector is the pin assignments for bank 3. For HSTC connector, all the I/O pins on the bank 3 are well defined. Figure 2.13 shows the I/O distribution of the bank3 for the HSTC and HSMC connector. Table B-1 shows the pin compatible list for HSTC and HSMC connector.

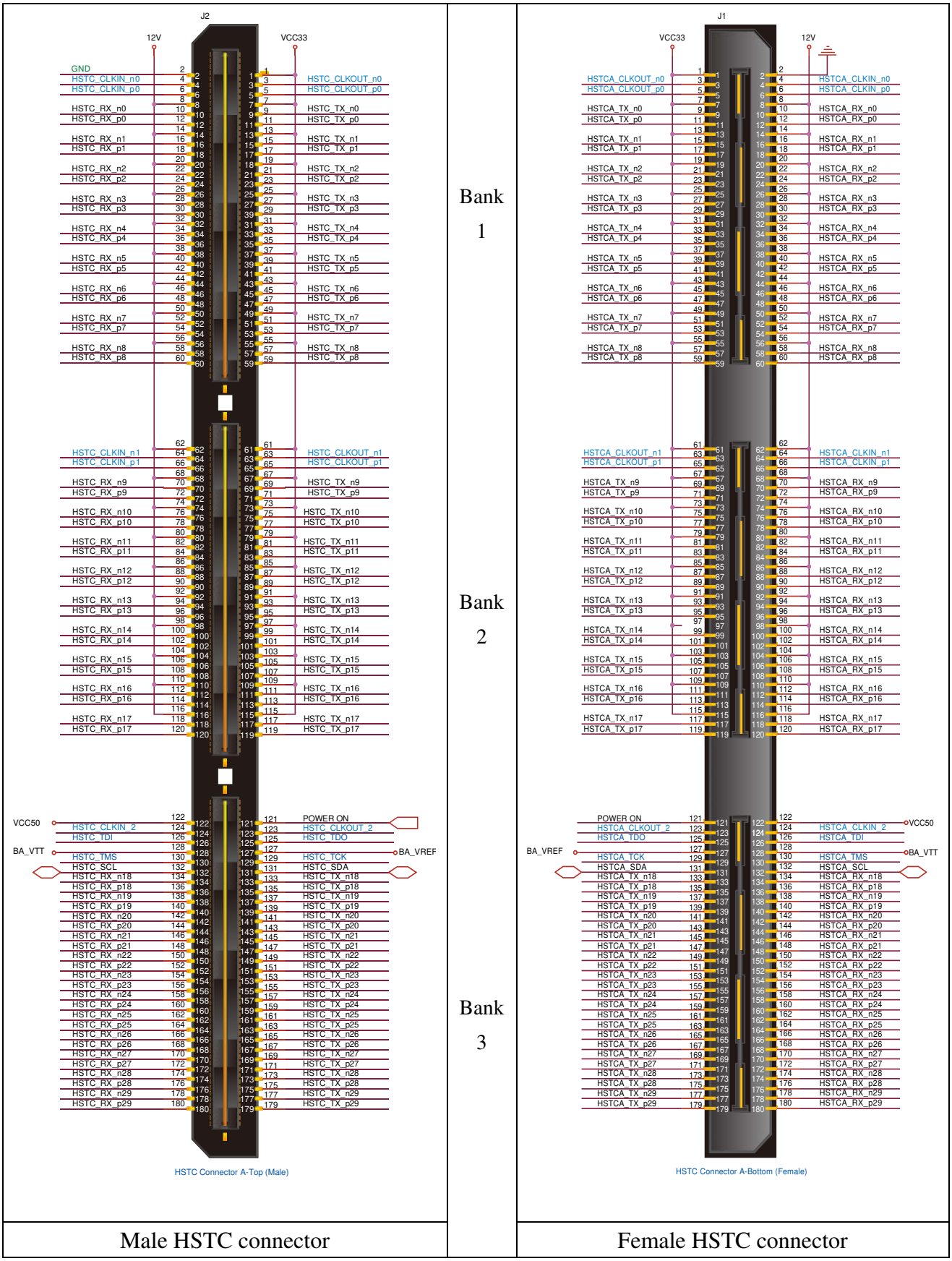
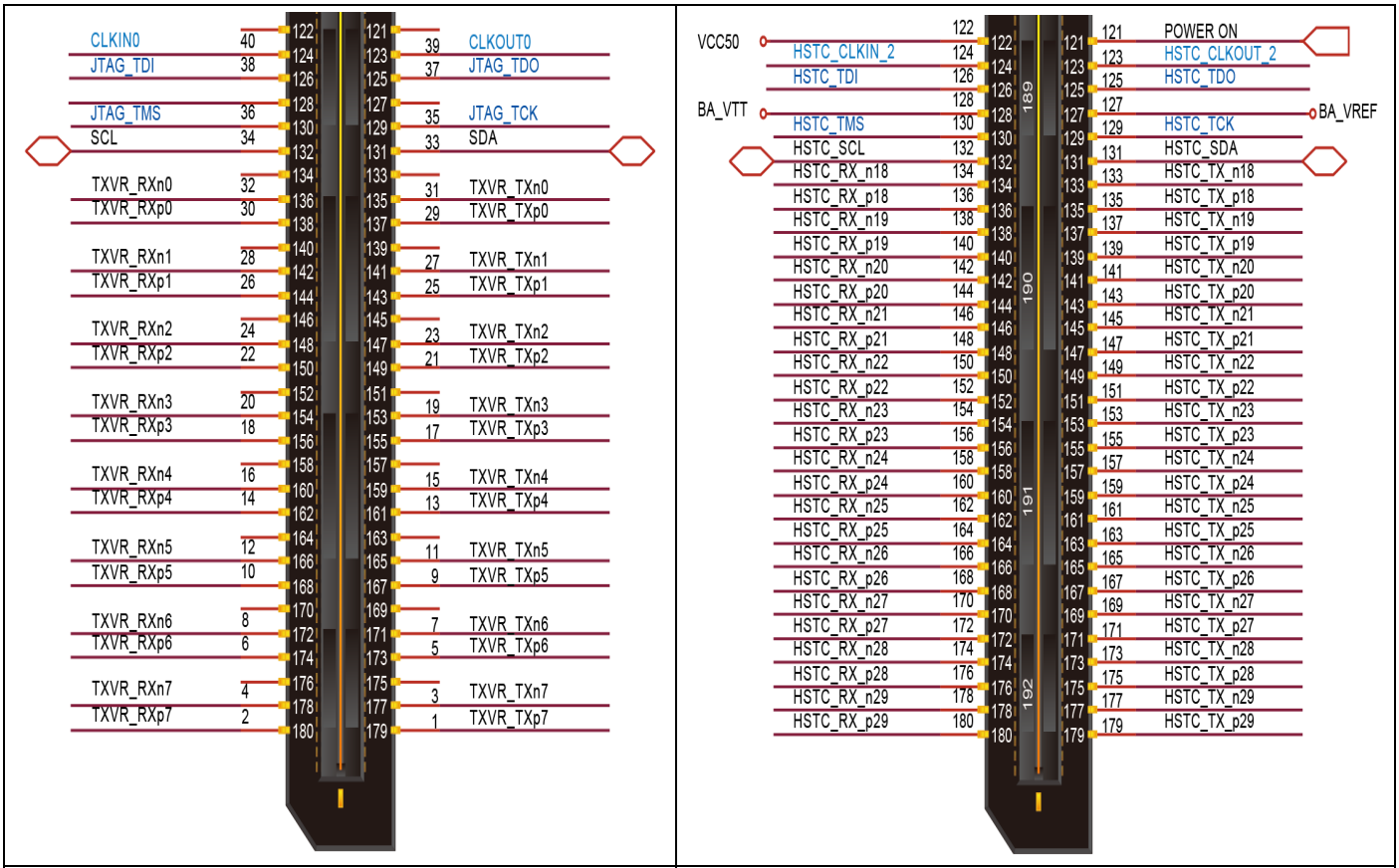


Figure 2.12. The male and female HSTC connectors

- **Share the same I/O pins with other connectors:**
  The HSTC connector group HSTCA (J1, J2) and HSTCB (J3, J4) share the same I/O pins with the GPIO expansion headers (J13, J14) and DDR2 SO-DIMM socket (J9), respectively. Hence none of the combinations above is allowed to be used at the same time.

- **Power Supply:**
  The HSTC connector provides 12, 5, and 3.3 volt for power supply purpose. There are also two power input pin named B<*HSTC Group*>_VTT and B<*HSTC Group*>_VREF, which are connected to the input reference voltage(V_{REF}) and termination voltage pin (V_{TT}) of the Stratix III FPGA, respectively.

Finally, Table A-6 to Table A-11 shows the connections between the HSTC connectors and the FPGA.



HSMC	HSTC

Figure 2.13. The difference between the HSMC and HSTC connectors

2.6 Connecting HSTC/HSMC Daughter Boards to DE3 HSTC connectors

It is important when the HSTC/HSMC daughter boards are connected to the DE3 HSTC connector is to ensure the I/O pins are properly matched between the daughter board and the DE3 connector in particular the 12V, 5V, and 3.3V power pins. If there are mismatch in pins between the two connectors, not only would it cause damage to the daughter board but more importantly the FPGA itself. Please note daughter boards can only be connected to the TOP HSTC connector of the DE3 board, therefore the bottom HSTC connector are only used to establish connection for stacking purposes.

2.7 Using the GPIO Expansion Headers

The DE3 Board provides two 40-pin expansion headers as shown in Figure 2.14. Each header has 36 pins connected to the Stratix III FPGA, and the two headers share the same I/O pins with HSTC connector A. The other 4 pins provide DC +5V (VCC5), DC +3.3V (VCC33), and two GND pins. Among these 36 I/O pins, there are 4 pins connected to the PLL clock input and output pins of the FPGA.

The I/O pins on the expansion headers have a great flexibility in selecting the I/O standards. The voltage level of the V_{CCIO} can be configured as 3.3V, 2.5V, 1.8V, or 1.5V.

Finally, Figure 2.15 shows the connections between the GPIO expansion headers and Stratix III. The pin assignments are given in Table A-12 and Table A-13.

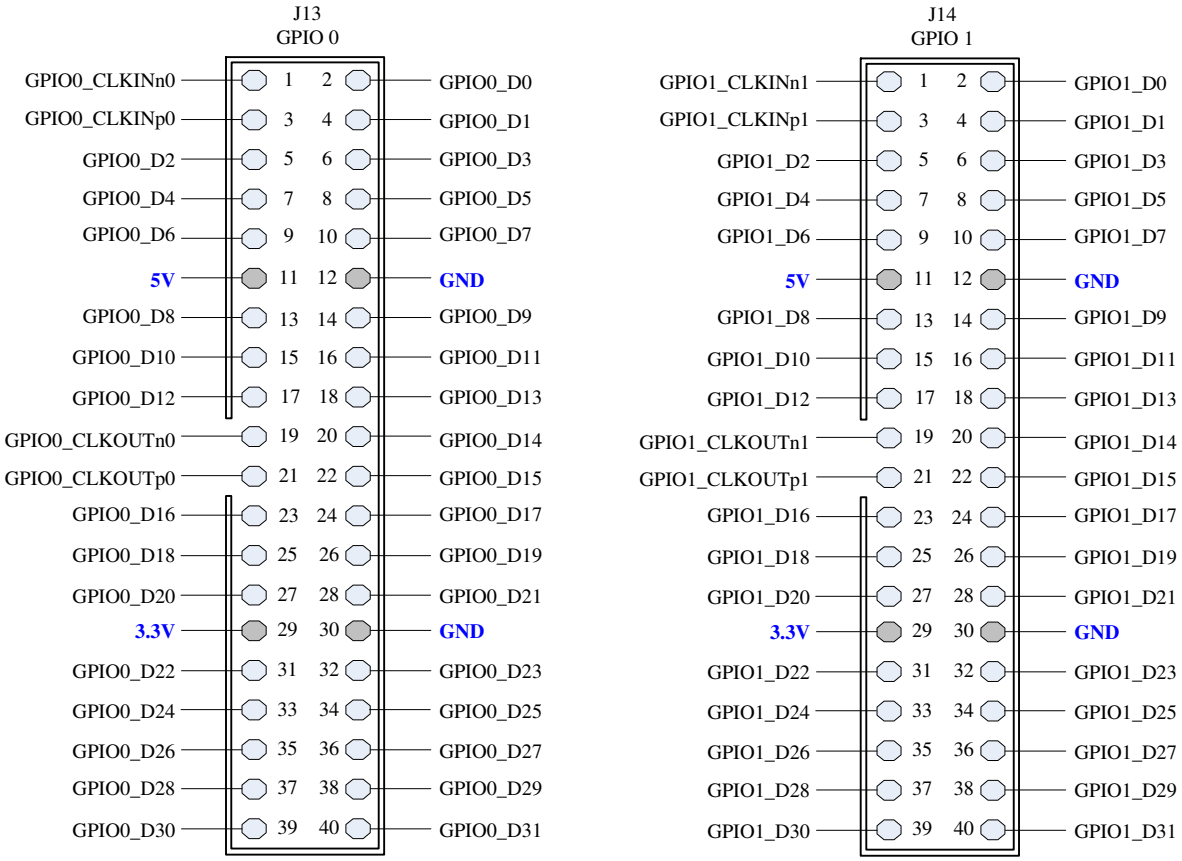


Figure 2.14. Pin distribution of the GPIO expansion headers

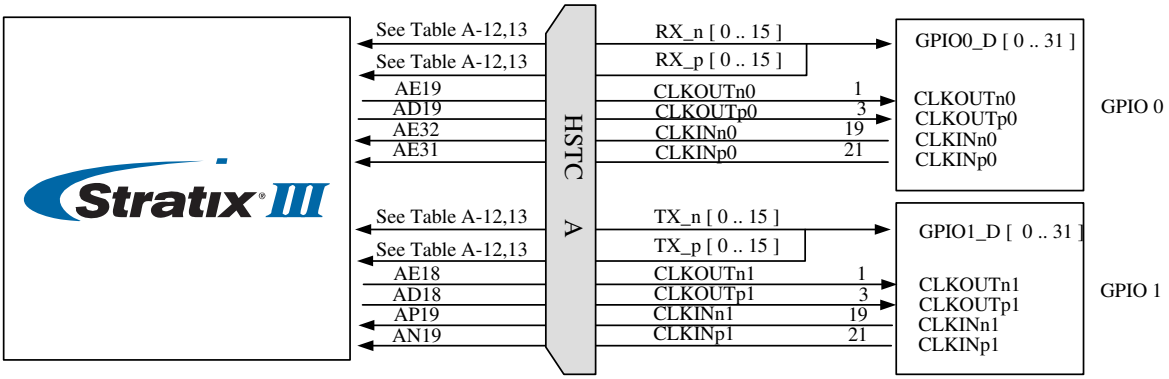


Figure 2.15. Connections between the GPIO expansion headers and Stratix III

2.8 Using the DDR2 SO-DIMM

The DE3 board provides a 200-pin DDR2 SO-DIMM socket. The maximum capacity supported is 4GB. The DDR2 SO-DIMM shares the same I/O pins with the HSTC connector B, except the