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PCI-X

Development Board

User Manual



Terasic PCI-X Development Board

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Chapter 1

PCI Package

The PCI package contains all components needed to use the PCI board in conjunction with a computer that runs the Microsoft Windows software.

1.1 Package contents

The PCI Package includes:

- Cyclone III PCI development board
- Terasic USB Blaster
- USB Cable for FPGA programming and control
- CD-ROM containing the User Manual, the Control Panel utility, the PCI System Builder and reference designs.
- THDB_HLB
- THDB_HFF
- Screw and Copper Pillar Package
- Power Cable

1.2 Getting Help

Here are the addresses where you can get help if you encounter problems:

- Altera Corporation
101 Innovation Drive
San Jose, California, 95134 USA
Email: mysupport@altera.com
- Terasic Technologies
No. 356, Sec. 1, Fusing E. Rd.
Jhubei City, HsinChu County, Taiwan, 302
Email: support@terasic.com
Web: www.terasic.com

1.3 Revision History

Date	Version	Changes
2008.12	First publication	

Chapter 2

Introduction

This chapter provides an introduction of the PCI Board features and design characteristic.

2.1 General Description

The Cyclone[®] III PCI development board provides a hardware platform for developing and prototyping low-power, high-performance, logic-intensive PCI-based designs. The board provides a high-density of the memory to facilitate the design and development of FPGA designs which need huge memory storage, and also includes Low-Voltage Differential Signaling (LVDS) interface of the High-Speed Terasic Connectors (HSTCs) for extra high-speed interface application.

Based on Cyclone[®] III FPGA and using Altera MegaCore functions, Terasic IP and the reference design, Cyclone III PCI Development Board allows users to quickly implement the design and solve design problems that require time-consuming, custom solutions.

Finally, to simplify the design process, we provide the software which calls “PCI System Builder” that provides a convenient way to build interfaces between host PC and user logic on FPGA, and also supports the interface of multi-port controller which allows shared access to a unique external memory. For more details about PCI System Builder, refer to *Chapter 4 PCI System Builder*.

2.2 Layout and Components

A photograph of the Cyclone[®] III PCI development board is shown in Figure 2.1 and 2.2. They depict the layout of the board and indicate the location of the connectors and key components.

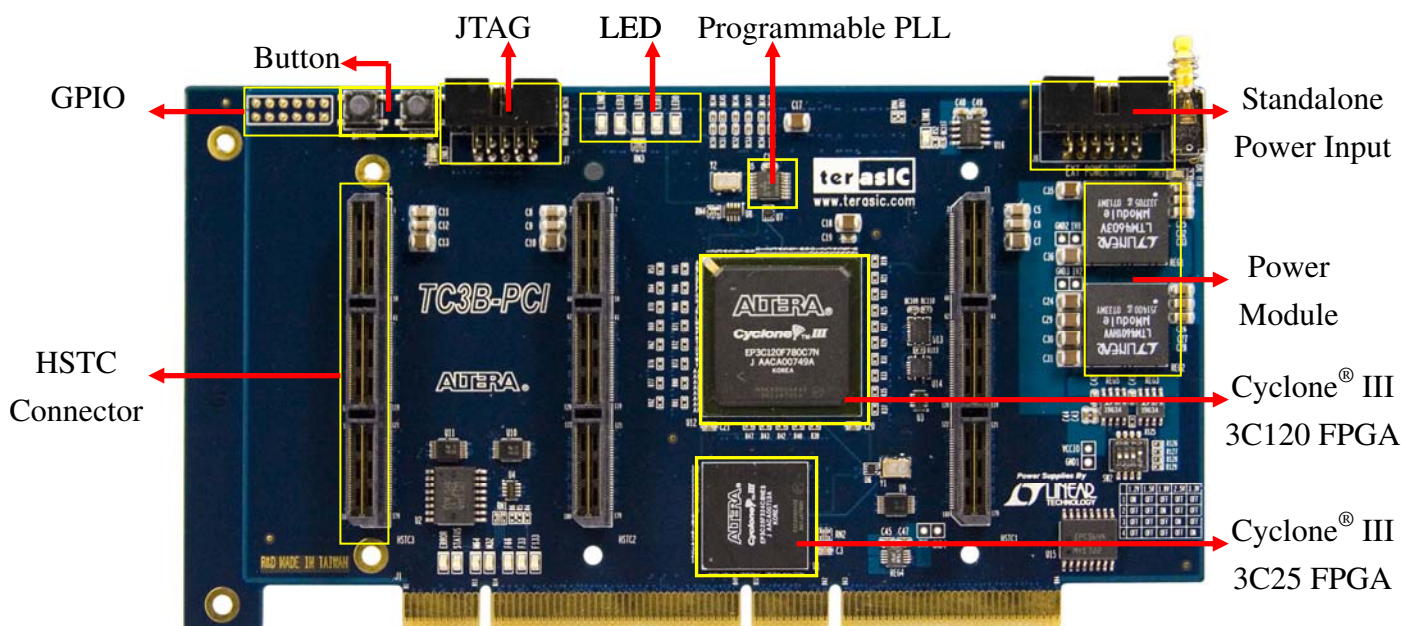


Figure 2.1 Cyclone[®] III PCI development board

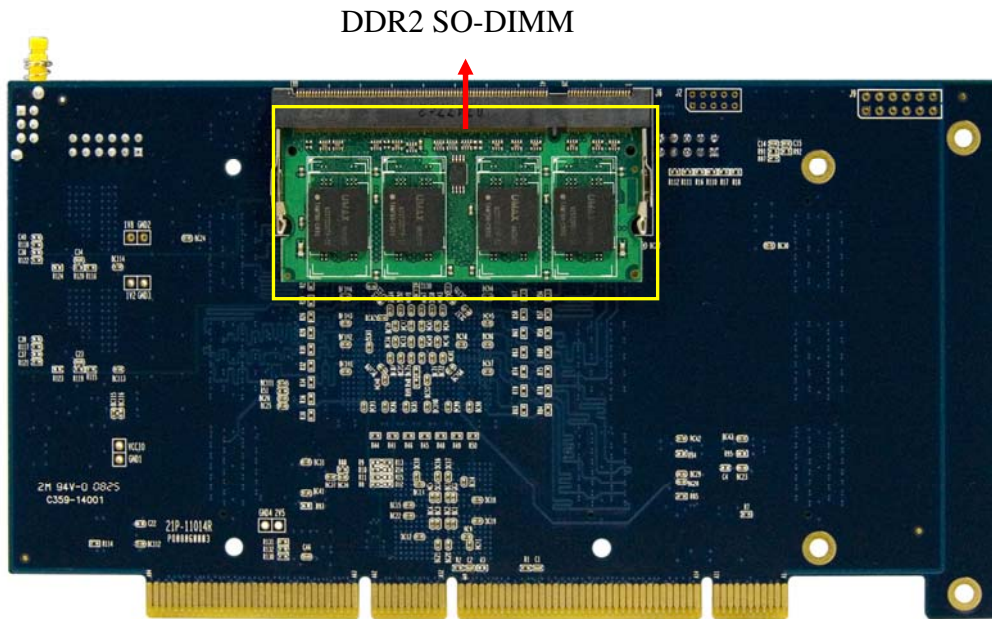


Figure 2.2 Cyclone[®] III PCI development board

The following hardware is provided on the PCI board:

- Altera Cyclone[®] III 3C120 FPGA device
 - 119,088 logic elements (LEs)
 - 3,981,312 total RAM bits
 - 288 18 x 18 multiplier blocks
- Altera Cyclone[®] III 3C25 FPGA device (PCI Bridge).
- Altera Serial Configuration device
 - EPCS64
 - EPCS16
- On-board memories
 - Up to 4GBytes DDR2 SO-DIMM
- Three HSTCs
 - 120 differential pair signals
 - 20 dedicated clock signals (8 differential pair & 4 single-end)
- PCI bus interfaces.

These features allow the user to implement the designs that need an enormous memory and high-speed data transfer. In addition to these hardware features, the PCI board has software support for PCI bus DMA, bus interrupt functions and a control panel facility to access various components.

In order to use the TC3B-PCI board, the user has to be familiar with the Quartus II software. The necessary knowledge can be acquired by reading the tutorials *Quartus II Introduction* (which exists in three versions based on the design entry method used, namely Verilog, VHDL or schematic entry).

2.3 Block Diagram of the PCI Board

Figure 2.3 gives the high-level block diagram of the PCI board. To provide maximum flexibility for the user, all connections are made through the Cyclone® III FPGA device. Thus, the user can configure the FPGA to implement any system design.

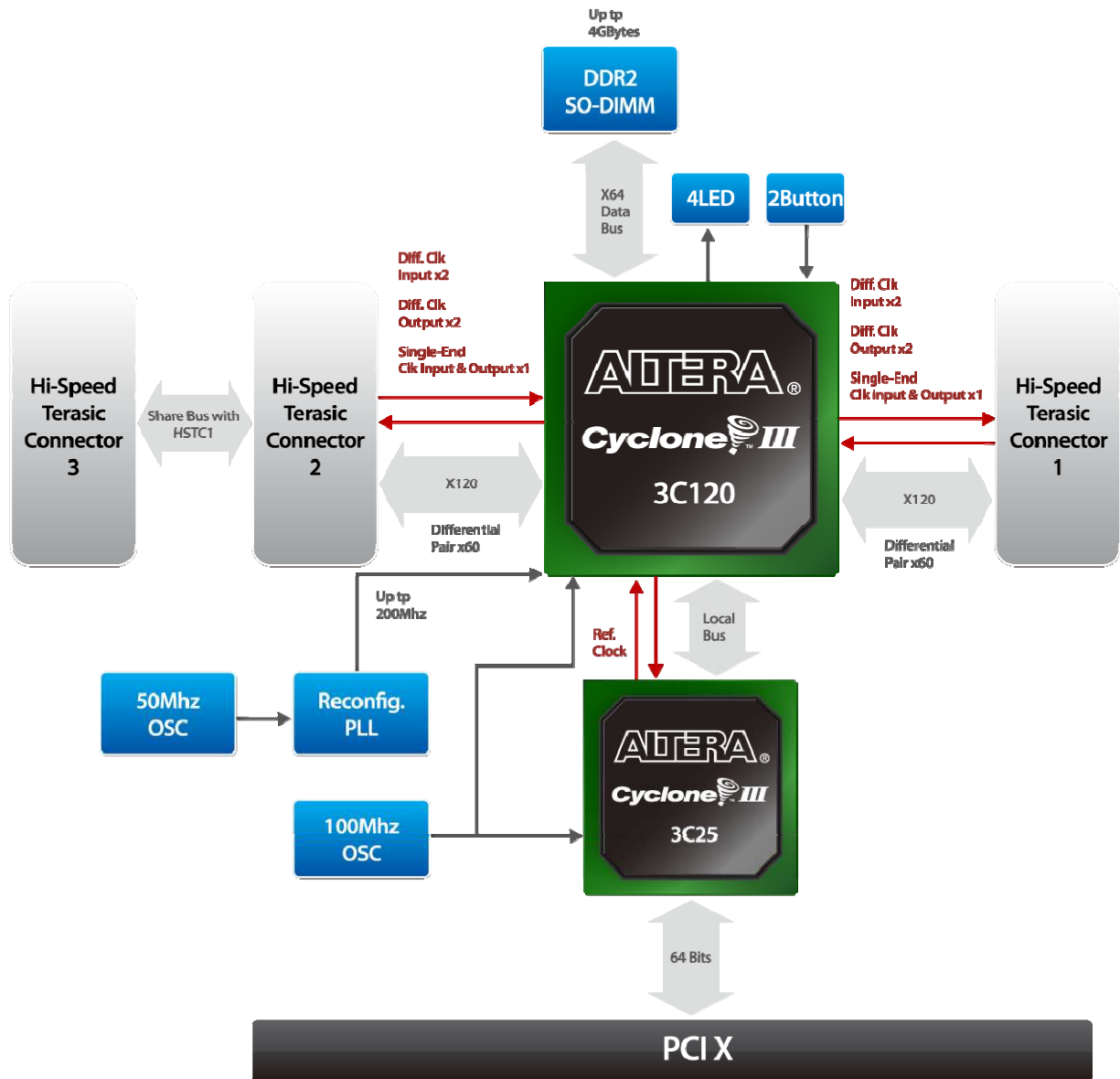


Figure 2.3 High level block diagram of the PCI board

Following is more detailed information about the blocks in Figure 2.3:

Cyclone® III 3C120 FPGA

- 119,088 LEs
- 432 M4K RAM blocks
- 3,981,312 total RAM bits
- 288 18x18 multiplier blocks
- Four phase locked loops (PLLs)

Cyclone® III 3C25 FPGA

- 24,624 LEs
- 66 M4K RAM blocks
- 608,256 total RAM bits
- 66 18x18 multiplier blocks
- Four PLLs

Serial Configuration device

- Altera's EPCS64 & EPCS16 serial configuration device
- In-system programming mode via JTAG interface ⁽¹⁾

DDR2 SDRAM

- 64-bits DDR2 SO-DIMM
- Up to 4GBytes

LED & button

- 4 user-controlled LEDs
- 2 user-controlled Buttons

Clock inputs

- Programmable PLL (80kHz ~ 200MHz)
- 100MHz oscillator

Three 180-pin HSTC expansion connectors

- 260 Cyclone[®] III I/O pins
- High-Speed connector up to GHz frequency

2.4 Power-up the PCI Board

The PCI Board contains the following ways to power-up:

1. Plug into PCI bus
2. Connect external power cable

After the PCI board powers up, the on-board configuration device which ships pre-programmed with the factory design, automatically configures the Cyclone[®] III device and the user-controlled LEDs will flash in a "Knight Rider" pattern.

Chapter 3

Components & Interfaces

This chapter describes functions of the components and interfaces on the development board, including detailed pin-out information to enable designers to create custom FPGA designs.

3.1 Clocking Circuitry

In order to achieve the design requirement which needs different frequency clock sources, the development board provides two clock sources that connect to dedicated clock input pins of Cyclone[®] III FPGA. One of the clock sources is a 100MHz oscillator and another is a programmable PLL.

For LVDS clocking, the expansion connectors (HSTCs) include the dedicated differential clock inputs and PLL output pins of Cyclone[®] III FPGA to implement high-speed clocking interface. Figure 3.1 shows the clocking diagram of the PCI board.

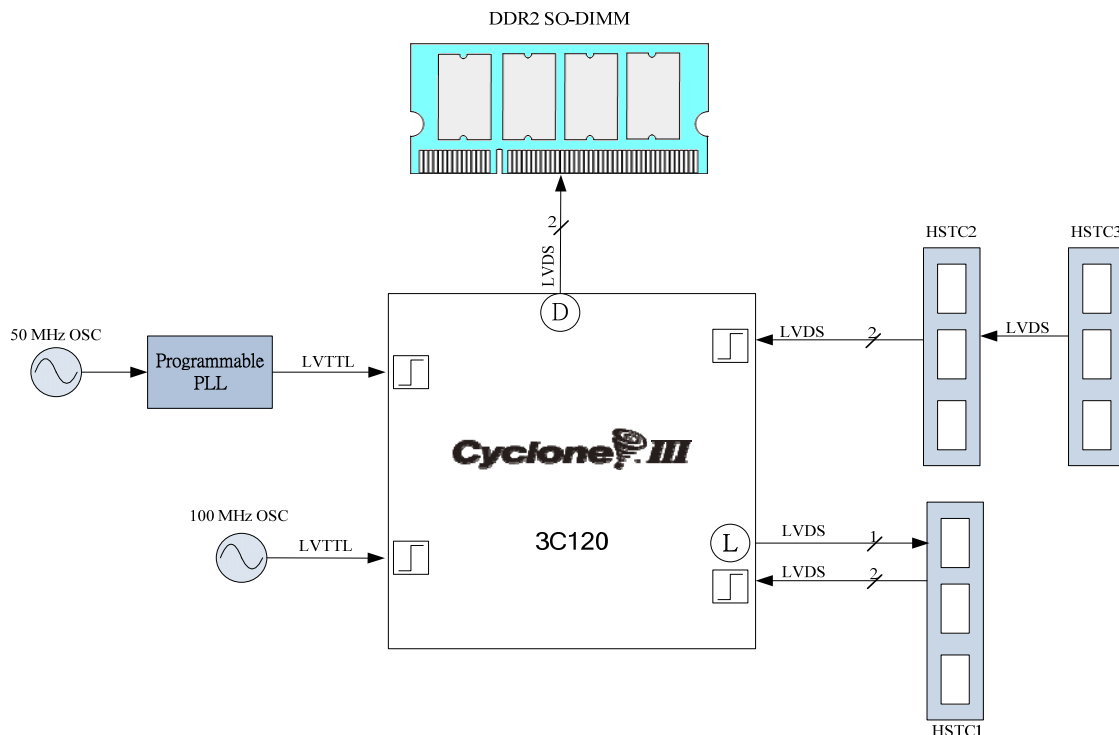


Figure 3.1 Clocking diagram of the PCI Board

Ⓛ : Dedicated PLL Output

Ⓜ : Dedicated Clock Input

ⓓ : Differential IO

3.1.1 Clock & Programmable PLL

The Cyclone® III PCI development board provides a programmable PLL which is driven by a 50 MHz oscillator and utilizes 2-wire serial interface SDAT and SCLK that operates up to 400 kbits/sec in read or write mode. The output frequency range of the PLL is 80 KHz to 200 MHz. A block diagram of the clock and on-board PLL showing connections to the Cyclone III FPGA is given in Figure 3.2. The associated pin assignments appear in Table 3.1

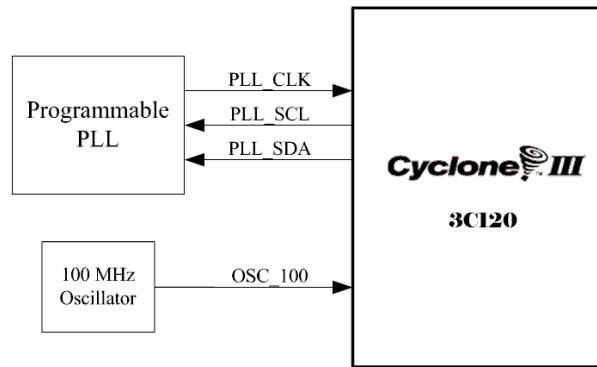


Figure 3.2 Block diagram of the clock and on-board PLL

Signal Name	FPGA Pin No.	Description
OSC_100	PIN_AG14	100 MHz Oscillator
PLL_CLK	PIN_B15	PLL Clock Output
PLL_SCL	PIN_AB24	PLL Serial Interface - Clock
PLL_SDA	PIN_AB23	PLL Serial Interface - Data

Table 3.1 Pin assignments of clock and on-board PLL

3.2 Switch

The Switch of Cyclone III PCI Board is used to select the expansion connectors IO voltage. Table 3.2 lists voltage selection by jumper.

Expansion IO Voltage	Pin number			
	1	2	3	4
1.2V	On	Off	Off	Off
1.5V	Off	Off	Off	Off
1.8V	Off	On	Off	Off
2.5V	Off	Off	On	Off
3.3V	Off	Off	Off	On

Table 3.2 Voltage selection of the expansion IO

3.3 HSTC Expansion Connectors

The Cyclone® III PCI development board contains three HSTC connectors (HSTC1, HSTC2 and HSTC3). The HSTC2 fully shares pins with HSTC3. These expansion connectors have total 240 bi-directional I/Os, 10 dedicated clock inputs and 10 PLL outputs of the Cyclone® III FPGA, and also provides DC +12V, DC +5V, DC +3.3V and GND pins. Furthermore, the voltage level of the I/O pins on the expansion connectors can be adjusted to 3.3V, 2.5V, 1.8V, 1.5V, 1.2V by using on-board switch.

High-speed differential I/O standards have become popular in high-speed interfaces because of their significant advantages over single-ended I/O standards. In response to the current market need, the PCI board supports LVDS channel up to 60 transmitters and 60 receivers on the expansion connectors. The channels had already achieved data rates of 600Mbps on Cyclone® III PCI development board. In summary, these features of the expansion connectors give applications the most flexibility for a variety of users. Figure 3.3 shows the schematic of HSTC expansion connector. Table 3.3 and 3.4 gives the pin assignment.

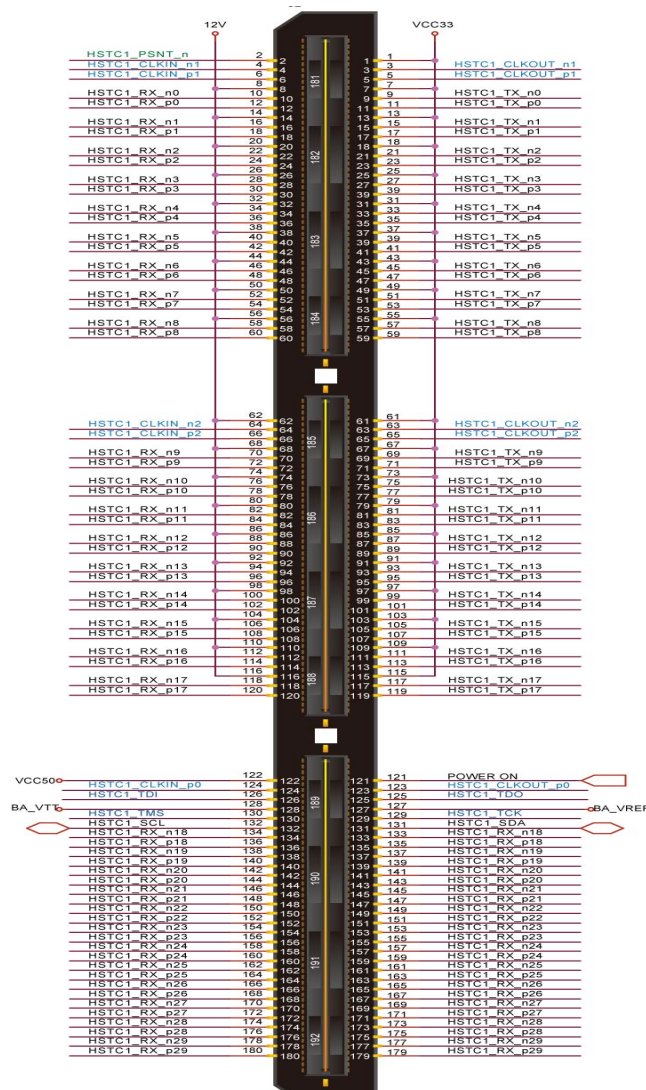


Figure 3.3 Schematic of the HSTC expansion connector

Schematic Signal Name		Connector pin no.	FPGA Pin Name
HSTC3_CLKIN_n0	HSTC2_CLKIN_n0	4	PIN_J1
HSTC3_CLKIN_p0	HSTC2_CLKIN_p0	6	PIN_J2
HSTC3_RX_n0	HSTC2_RX_n0	10	PIN_C2
HSTC3_RX_p0	HSTC2_RX_p0	12	PIN_D3
HSTC3_RX_n1	HSTC2_RX_n1	16	PIN_D1
HSTC3_RX_p1	HSTC2_RX_p1	18	PIN_D2
HSTC3_RX_n2	HSTC2_RX_n2	22	PIN_F3
HSTC3_RX_p2	HSTC2_RX_p2	24	PIN_E3
HSTC3_RX_n3	HSTC2_RX_n3	28	PIN_F1
HSTC3_RX_p3	HSTC2_RX_p3	30	PIN_F2
HSTC3_RX_n4	HSTC2_RX_n4	34	PIN_G3
HSTC3_RX_p4	HSTC2_RX_p4	36	PIN_G4
HSTC3_RX_n5	HSTC2_RX_n5	40	PIN_H3
HSTC3_RX_p5	HSTC2_RX_p5	42	PIN_H4
HSTC3_RX_n6	HSTC2_RX_n6	46	PIN_J3
HSTC3_RX_p6	HSTC2_RX_p6	48	PIN_J4
HSTC3_RX_n7	HSTC2_RX_n7	52	PIN_G5
HSTC3_RX_p7	HSTC2_RX_p7	54	PIN_G6
HSTC3_RX_n8	HSTC2_RX_n8	58	PIN_N3
HSTC3_RX_p8	HSTC2_RX_p8	60	PIN_N4
HSTC3_CLKIN_n1	HSTC2_CLKIN_n1	64	PIN_Y1
HSTC3_CLKIN_p1	HSTC2_CLKIN_p1	66	PIN_Y2
HSTC3_RX_n9	HSTC2_RX_n9	70	PIN_H24
HSTC3_RX_p9	HSTC2_RX_p9	72	PIN_H23
HSTC3_RX_n10	HSTC2_RX_n10	76	PIN_G26
HSTC3_RX_p10	HSTC2_RX_p10	78	PIN_G25
HSTC3_RX_n11	HSTC2_RX_n11	82	PIN_J24
HSTC3_RX_p11	HSTC2_RX_p11	84	PIN_J23
HSTC3_RX_n12	HSTC2_RX_n12	88	PIN_K22
HSTC3_RX_p12	HSTC2_RX_p12	90	PIN_K21
HSTC3_RX_n13	HSTC2_RX_n13	94	PIN_L22
HSTC3_RX_p13	HSTC2_RX_p13	96	PIN_L21
HSTC3_RX_n14	HSTC2_RX_n14	100	PIN_V22
HSTC3_RX_p14	HSTC2_RX_p14	102	PIN_U22
HSTC3_RX_n15	HSTC2_RX_n15	106	PIN_M1
HSTC3_RX_p15	HSTC2_RX_p15	108	PIN_M2
HSTC3_RX_n16	HSTC2_RX_n16	112	PIN_P1

HSTC3_RX_p16	HSTC2_RX_p16	114	PIN_P2
HSTC3_RX_n17	HSTC2_RX_n17	118	PIN_R1
HSTC3_RX_p17	HSTC2_RX_p17	120	PIN_R2
HSTC3_CLKIN_2	HSTC2_CLKIN_2	124	PIN_R5
HSTC3_RX_n18	HSTC2_RX_n18	134	PIN_T3
HSTC3_RX_p18	HSTC2_RX_p18	136	PIN_T4
HSTC3_RX_n19	HSTC2_RX_n19	138	PIN_R6
HSTC3_RX_p19	HSTC2_RX_p19	140	PIN_R7
HSTC3_RX_n20	HSTC2_RX_n20	142	PIN_AA3
HSTC3_RX_p20	HSTC2_RX_p20	144	PIN_AA4
HSTC3_RX_n21	HSTC2_RX_n21	146	PIN_R4
HSTC3_RX_p21	HSTC2_RX_p21	148	PIN_R3
HSTC3_RX_n22	HSTC2_RX_n22	150	PIN_V5
HSTC3_RX_p22	HSTC2_RX_p22	152	PIN_V6
HSTC3_RX_n23	HSTC2_RX_n23	154	PIN_U4
HSTC3_RX_p23	HSTC2_RX_p23	156	PIN_U3
HSTC3_RX_n24	HSTC2_RX_n24	158	PIN_AC1
HSTC3_RX_p24	HSTC2_RX_p24	160	PIN_AC2
HSTC3_RX_n25	HSTC2_RX_n25	162	PIN_V7
HSTC3_RX_p25	HSTC2_RX_p25	164	PIN_V8
HSTC3_RX_n26	HSTC2_RX_n26	166	PIN_AD1
HSTC3_RX_p26	HSTC2_RX_p26	168	PIN_AD2
HSTC3_RX_n27	HSTC2_RX_n27	170	PIN_W3
HSTC3_RX_p27	HSTC2_RX_p27	172	PIN_W4
HSTC3_RX_n28	HSTC2_RX_n28	174	PIN_AE1
HSTC3_RX_p28	HSTC2_RX_p28	176	PIN_AE2
HSTC3_RX_n29	HSTC2_RX_n29	178	PIN_AD3
HSTC3_RX_p29	HSTC2_RX_p29	180	PIN_AC3
HSTC3_CLKOUT_n0	HSTC2_CLKOUT_n0	3	PIN_G1
HSTC3_CLKOUT_p0	HSTC2_CLKOUT_p0	5	PIN_G2
HSTC3_TX_n0	HSTC2_TX_n0	9	PIN_K1
HSTC3_TX_p0	HSTC2_TX_p0	11	PIN_K2
HSTC3_TX_n1	HSTC2_TX_n1	15	PIN_K3
HSTC3_TX_p1	HSTC2_TX_p1	17	PIN_K4
HSTC3_TX_n2	HSTC2_TX_n2	21	PIN_L8
HSTC3_TX_p2	HSTC2_TX_p2	23	PIN_K8
HSTC3_TX_n3	HSTC2_TX_n3	27	PIN_K7
HSTC3_TX_p3	HSTC2_TX_p3	29	PIN_J7

HSTC3_TX_n4	HSTC2_TX_n4	33	PIN_L6
HSTC3_TX_p4	HSTC2_TX_p4	35	PIN_L7
HSTC3_TX_n5	HSTC2_TX_n5	39	PIN_J5
HSTC3_TX_p5	HSTC2_TX_p5	41	PIN_J6
HSTC3_TX_n6	HSTC2_TX_n6	45	PIN_M3
HSTC3_TX_p6	HSTC2_TX_p6	47	PIN_M4
HSTC3_TX_n7	HSTC2_TX_n7	51	PIN_L3
HSTC3_TX_p7	HSTC2_TX_p7	53	PIN_L4
HSTC3_TX_n8	HSTC2_TX_n8	57	PIN_M7
HSTC3_TX_p8	HSTC2_TX_p8	59	PIN_M8
HSTC3_CLKOUT_n1	HSTC2_CLKOUT_n1	63	PIN_L1
HSTC3_CLKOUT_p1	HSTC2_CLKOUT_p1	65	PIN_L2
HSTC3_TX_n9	HSTC2_TX_n9	69	PIN_F25
HSTC3_TX_p9	HSTC2_TX_p9	71	PIN_F24
HSTC3_TX_n10	HSTC2_TX_n10	75	PIN_G24
HSTC3_TX_p10	HSTC2_TX_p10	77	PIN_G23
HSTC3_TX_n11	HSTC2_TX_n11	81	PIN_K26
HSTC3_TX_p11	HSTC2_TX_p11	83	PIN_K25
HSTC3_TX_n12	HSTC2_TX_n12	87	PIN_U26
HSTC3_TX_p12	HSTC2_TX_p12	89	PIN_U25
HSTC3_TX_n13	HSTC2_TX_n13	93	PIN_V26
HSTC3_TX_p13	HSTC2_TX_p13	95	PIN_V25
HSTC3_TX_n14	HSTC2_TX_n14	99	PIN_V24
HSTC3_TX_p14	HSTC2_TX_p14	101	PIN_V23
HSTC3_TX_n15	HSTC2_TX_n15	105	PIN_W21
HSTC3_TX_p15	HSTC2_TX_p15	107	PIN_V21
HSTC3_TX_n16	HSTC2_TX_n16	111	PIN_Y22
HSTC3_TX_p16	HSTC2_TX_p16	113	PIN_W22
HSTC3_TX_n17	HSTC2_TX_n17	117	PIN_Y7
HSTC3_TX_p17	HSTC2_TX_p17	119	PIN_W8
HSTC3_CLKOUT_2	HSTC2_CLKOUT_2	123	PIN_AB3
HSTC3_TX_n18	HSTC2_TX_n18	133	PIN_V1
HSTC3_TX_p18	HSTC2_TX_p18	135	PIN_V2
HSTC3_TX_n19	HSTC2_TX_n19	137	PIN_U1
HSTC3_TX_p19	HSTC2_TX_p19	139	PIN_U2
HSTC3_TX_n20	HSTC2_TX_n20	141	PIN_V3
HSTC3_TX_p20	HSTC2_TX_p20	143	PIN_V4
HSTC3_TX_n21	HSTC2_TX_n21	145	PIN_U5
HSTC3_TX_p21	HSTC2_TX_p21	147	PIN_U6

HSTC3_TX_n22	HSTC2_TX_n22	149	PIN_Y5
HSTC3_TX_p22	HSTC2_TX_p22	151	PIN_Y6
HSTC3_TX_n23	HSTC2_TX_n23	153	PIN_W1
HSTC3_TX_p23	HSTC2_TX_p23	155	PIN_W2
HSTC3_TX_n24	HSTC2_TX_n24	157	PIN_AB1
HSTC3_TX_p24	HSTC2_TX_p24	159	PIN_AB2
HSTC3_TX_n25	HSTC2_TX_n25	161	PIN_Y3
HSTC3_TX_p25	HSTC2_TX_p25	163	PIN_Y4
HSTC3_TX_n26	HSTC2_TX_n26	165	PIN_AA5
HSTC3_TX_p26	HSTC2_TX_p26	167	PIN_AA6
HSTC3_TX_n27	HSTC2_TX_n27	169	PIN_AB5
HSTC3_TX_p27	HSTC2_TX_p27	171	PIN_AB6
HSTC3_TX_n28	HSTC2_TX_n28	173	PIN_AF2
HSTC3_TX_p28	HSTC2_TX_p28	175	PIN_AE3
HSTC3_TX_n29	HSTC2_TX_n29	177	PIN_AC4
HSTC3_TX_p29	HSTC2_TX_p29	179	PIN_AC5

Table 3.3 Pin assignments of the HSTC2 and HSTC3

Schematic Signal Name	Board Reference	FPGA Pin Name
HSTC1_CLKIN_n0	4	PIN_J28
HSTC1_CLKIN_p0	6	PIN_J27
HSTC1_RX_n0	10	PIN_L24
HSTC1_RX_p0	12	PIN_L23
HSTC1_RX_n1	16	PIN_R21
HSTC1_RX_p1	18	PIN_P21
HSTC1_RX_n2	22	PIN_C27
HSTC1_RX_p2	24	PIN_D26
HSTC1_RX_n3	28	PIN_R23
HSTC1_RX_p3	30	PIN_R22
HSTC1_RX_n4	34	PIN_E26
HSTC1_RX_p4	36	PIN_F26
HSTC1_RX_n5	40	PIN_H26
HSTC1_RX_p5	42	PIN_H25
HSTC1_RX_n6	46	PIN_AA13
HSTC1_RX_p6	48	PIN_Y13
HSTC1_RX_n7	52	PIN_AB14
HSTC1_RX_p7	54	PIN_AA14
HSTC1_RX_n8	58	PIN_AD11

HSTC1_RX_p8	60	PIN_AC11
HSTC1_CLKIN_n1	64	PIN_Y28
HSTC1_CLKIN_p1	66	PIN_Y27
HSTC1_RX_n9	70	PIN_AA10
HSTC1_RX_p9	72	PIN_AA8
HSTC1_RX_n10	76	PIN_AB8
HSTC1_RX_p10	78	PIN_AB9
HSTC1_RX_n11	82	PIN_AB12
HSTC1_RX_p11	84	PIN_AC12
HSTC1_RX_n12	88	PIN_AC7
HSTC1_RX_p12	90	PIN_AD8
HSTC1_RX_n13	94	PIN_AF11
HSTC1_RX_p13	96	PIN_AE11
HSTC1_RX_n14	100	PIN_AF14
HSTC1_RX_p14	102	PIN_AE14
HSTC1_RX_n15	106	PIN_AF12
HSTC1_RX_p15	108	PIN_AE12
HSTC1_RX_n16	112	PIN_AH10
HSTC1_RX_p16	114	PIN_AG10
HSTC1_RX_n17	118	PIN_AH8
HSTC1_RX_p17	120	PIN_AG8
HSTC1_CLKIN_2	124	PIN_L26
HSTC1_RX_n18	134	PIN_AC10
HSTC1_RX_p18	136	PIN_AB10
HSTC1_RX_n19	138	PIN_AC8
HSTC1_RX_p19	140	PIN_AB7
HSTC1_RX_n20	142	PIN_AH6
HSTC1_RX_p20	144	PIN_AG6
HSTC1_RX_n21	146	PIN_AH12
HSTC1_RX_p21	148	PIN_AG12
HSTC1_RX_n22	150	PIN_AF8
HSTC1_RX_p22	152	PIN_AE8
HSTC1_RX_n23	154	PIN_AF13
HSTC1_RX_p23	156	PIN_AE13
HSTC1_RX_n24	158	PIN_AH4
HSTC1_RX_p24	160	PIN_AG4
HSTC1_RX_n25	162	PIN_AH11
HSTC1_RX_p25	164	PIN_AG11
HSTC1_RX_n26	166	PIN_AH7

HSTC1_RX_p26	168	PIN_AG7
HSTC1_RX_n27	170	PIN_AF10
HSTC1_RX_p27	172	PIN_AE10
HSTC1_RX_n28	174	PIN_AA12
HSTC1_RX_p28	176	PIN_Y12
HSTC1_RX_n29	178	PIN_AF7
HSTC1_RX_p29	180	PIN_AE7
HSTC1_CLKOUT_n0	3	PIN_J26
HSTC1_CLKOUT_p0	5	PIN_J25
HSTC1_TX_n0	9	PIN_D28
HSTC1_TX_p0	11	PIN_D27
HSTC1_TX_n1	15	PIN_E28
HSTC1_TX_p1	17	PIN_E27
HSTC1_TX_n2	21	PIN_F28
HSTC1_TX_p2	23	PIN_F27
HSTC1_TX_n3	27	PIN_G28
HSTC1_TX_p3	29	PIN_G27
HSTC1_TX_n4	33	PIN_K28
HSTC1_TX_p4	35	PIN_K27
HSTC1_TX_n5	39	PIN_M28
HSTC1_TX_p5	41	PIN_M27
HSTC1_TX_n6	45	PIN_P28
HSTC1_TX_p6	47	PIN_P27
HSTC1_TX_n7	51	PIN_L28
HSTC1_TX_p7	53	PIN_L27
HSTC1_TX_n8	57	PIN_M26
HSTC1_TX_p8	59	PIN_M25
HSTC1_CLKOUT_n1	63	PIN_AF5
HSTC1_CLKOUT_p1	65	PIN_AE5
HSTC1_TX_n9	69	PIN_N26
HSTC1_TX_p9	71	PIN_N25
HSTC1_TX_n10	75	PIN_P26
HSTC1_TX_p10	77	PIN_P25
HSTC1_TX_n11	81	PIN_R28
HSTC1_TX_p11	83	PIN_R27
HSTC1_TX_n12	87	PIN_T26
HSTC1_TX_p12	89	PIN_T25
HSTC1_TX_n13	93	PIN_R26

HSTC1_TX_p13	95	PIN_R25
HSTC1_TX_n14	99	PIN_U28
HSTC1_TX_p14	101	PIN_U27
HSTC1_TX_n15	105	PIN_V28
HSTC1_TX_p15	107	PIN_V27
HSTC1_TX_n16	111	PIN_W27
HSTC1_TX_p16	113	PIN_W28
HSTC1_TX_n17	117	PIN_T22
HSTC1_TX_p17	119	PIN_T21
HSTC1_CLKOUT_2	123	PIN_H22
HSTC1_TX_n18	133	PIN_W26
HSTC1_TX_p18	135	PIN_W25
HSTC1_TX_n19	137	PIN_AC28
HSTC1_TX_p19	139	PIN_AC27
HSTC1_TX_n20	141	PIN_Y26
HSTC1_TX_p20	143	PIN_Y25
HSTC1_TX_n21	145	PIN_AA26
HSTC1_TX_p21	147	PIN_AA25
HSTC1_TX_n22	149	PIN_AB28
HSTC1_TX_p22	151	PIN_AB27
HSTC1_TX_n23	153	PIN_AB26
HSTC1_TX_p23	155	PIN_AB25
HSTC1_TX_n24	157	PIN_AD28
HSTC1_TX_p24	159	PIN_AD27
HSTC1_TX_n25	161	PIN_AD26
HSTC1_TX_p25	163	PIN_AC26
HSTC1_TX_n26	165	PIN_AF27
HSTC1_TX_p26	167	PIN_AE26
HSTC1_TX_n27	169	PIN_AE28
HSTC1_TX_p27	171	PIN_AE27
HSTC1_TX_n28	173	PIN_AC25
HSTC1_TX_p28	175	PIN_AC24
HSTC1_TX_n29	177	PIN_Y24
HSTC1_TX_p29	179	PIN_Y23

Table 3.4 Pin assignments of the HSTC1

3.4 Off-Chip Memory

The Cyclone[®] III PCI development board provides the large-capacity and high-speed memory interface.

3.4.1 DDR2 SO-DIMM Module

The board has a DDR2 SDRAM SO-DIMM memory interface with 64-bit data width. The target speed is 200 MHz DDR for a total theoretical bandwidth of nearly 25 Gb/s. Table 3.5 lists DDR2 SDRAM SO-DIMM pin-out as well as corresponding FPGA pin numbers.

Schematic Signal Name	Connector pin no.	FPGA Pin Name
DDR2_A0	102	PIN_G11
DDR2_A1	101	PIN_D15
DDR2_A2	100	PIN_E10
DDR2_A3	99	PIN_H15
DDR2_A4	98	PIN_A10
DDR2_A5	97	PIN_J15
DDR2_A6	94	PIN_F8
DDR2_A7	92	PIN_D7
DDR2_A8	93	PIN_F14
DDR2_CLK_P0	30	PIN_D8
DDR2_CLK_P1	164	PIN_J19
DDR2_CLK_N0	32	PIN_C8
DDR2_CLK_N1	166	PIN_H19
DDR2_A9	91	PIN_J13
DDR2_A10	105	PIN_F15
DDR2_A11	90	PIN_C7
DDR2_A12	89	PIN_B12
DDR2_A13	116	PIN_D24
DDR2_A14	86	PIN_A6
DDR2_A15	84	PIN_C6
DDR2_DQ0	5	PIN_C10
DDR2_DQ1	7	PIN_E11
DDR2_DQ2	17	PIN_C11
DDR2_DQ3	19	PIN_H13
DDR2_DQ4	4	PIN_B7
DDR2_DQ5	6	PIN_B6
DDR2_DQ6	14	PIN_A7
DDR2_DQ7	16	PIN_D10

DDR2_DQ8	23	PIN_D13
DDR2_DQ9	25	PIN_C13
DDR2_DQ10	35	PIN_E14
DDR2_DQ11	37	PIN_C14
DDR2_DQ12	20	PIN_C12
DDR2_DQ13	22	PIN_A12
DDR2_DQ14	36	PIN_B11
DDR2_DQ15	38	PIN_A11
DDR2_DQ16	43	PIN_C17
DDR2_DQ17	45	PIN_B18
DDR2_DQ18	55	PIN_A19
DDR2_DQ19	57	PIN_D20
DDR2_DQ20	44	PIN_C16
DDR2_DQ21	46	PIN_E17
DDR2_DQ22	56	PIN_C19
DDR2_DQ23	58	PIN_B19
DDR2_DQ24	61	PIN_C22
DDR2_DQ25	63	PIN_C21
DDR2_DQ26	73	PIN_A22
DDR2_DQ27	75	PIN_C24
DDR2_DQ28	62	PIN_E18
DDR2_DQ29	64	PIN_D21
DDR2_DQ30	74	PIN_B21
DDR2_DQ31	76	PIN_A21
DDR2_DQ32	123	PIN_A23
DDR2_DQ33	125	PIN_D22
DDR2_DQ34	135	PIN_E22
DDR2_DQ35	137	PIN_F21
DDR2_DQ36	124	PIN_B25
DDR2_DQ37	126	PIN_C25
DDR2_DQ38	134	PIN_A26
DDR2_DQ39	136	PIN_B26
DDR2_DQ40	141	PIN_AG17
DDR2_DQ41	143	PIN_AG18
DDR2_DQ42	151	PIN_AF15
DDR2_DQ43	153	PIN_AF16
DDR2_DQ44	140	PIN_AH17
DDR2_DQ45	142	PIN_AH18
DDR2_DQ46	152	PIN_AB16

DDR2_DQ47	154	PIN_AE17
DDR2_DQ48	157	PIN_AD17
DDR2_DQ49	159	PIN_AE19
DDR2_DQ50	173	PIN_AG22
DDR2_DQ51	175	PIN_AF24
DDR2_DQ52	158	PIN_AG21
DDR2_DQ53	160	PIN_AH21
DDR2_DQ54	174	PIN_AH22
DDR2_DQ55	176	PIN_AH23
DDR2_DQ56	179	PIN_AD18
DDR2_DQ57	181	PIN_AF20
DDR2_DQ58	189	PIN_AE21
DDR2_DQ59	191	PIN_AF22
DDR2_DQ60	180	PIN_AE24
DDR2_DQ61	182	PIN_AE25
DDR2_DQ62	192	PIN_AG26
DDR2_DQ63	194	PIN_AH25
DDR2_DQS0	13	PIN_E12
DDR2_DQS1	31	PIN_D12
DDR2_DQS2	51	PIN_B17
DDR2_DQS3	70	PIN_D17
DDR2_DQS4	131	PIN_A25
DDR2_DQS5	148	PIN_AF17
DDR2_DQS6	169	PIN_AE18
DDR2_DQS7	188	PIN_AF26
DDR2_DM0	10	PIN_A8
DDR2_DM1	26	PIN_B10
DDR2_DM2	52	PIN_E15
DDR2_DM3	67	PIN_C20
DDR2_DM4	130	PIN_B23
DDR2_DM5	147	PIN_AC15
DDR2_DM6	170	PIN_AH19
DDR2_DM7	185	PIN_AF25
DDR2_CS_N0	110	PIN_G18
DDR2_CS_N1	115	PIN_D25
DDR2_CKE0	79	PIN_H8
DDR2_CKE1	80	PIN_E8
DDR2_BA0	107	PIN_D16

DDR2_BA1	106	PIN_A17
DDR2_BA2	85	PIN_H12
DDR2_RAS_N	108	PIN_J16
DDR2_CAS_N	113	PIN_D19
DDR2_WE_N	109	PIN_H16
DDR2_ODT0	114	PIN_E21
DDR2_ODT1	119	PIN_C26
DDR2_SCL	197	PIN_J17
DDR2_SDA	195	PIN_C23

Table 3.5 Pin assignments of the DDR2 SO-DIMM

Chapter 4

Setup PCI Board

This chapter describes how to setup the PCI board and driver on users' PC.

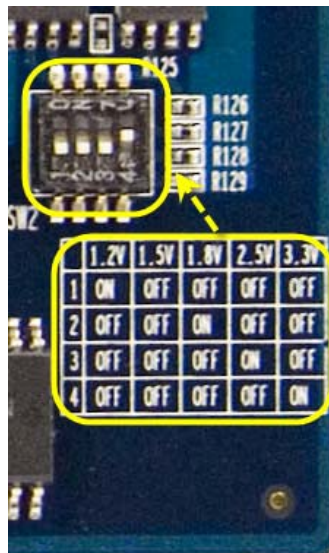
4.1 System Requirement

- Windows, 32-bits
- One 32 or 64 PCI slot
- Quartus Installed. Quartus 8.0 or 8.1 is recommended.
- USB-Blaster and USB Cable

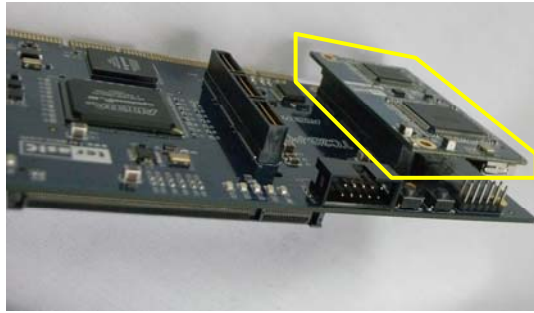
4.2 Hardware Installation: PCI Board

Follow these steps to install your PCI board into your computer:

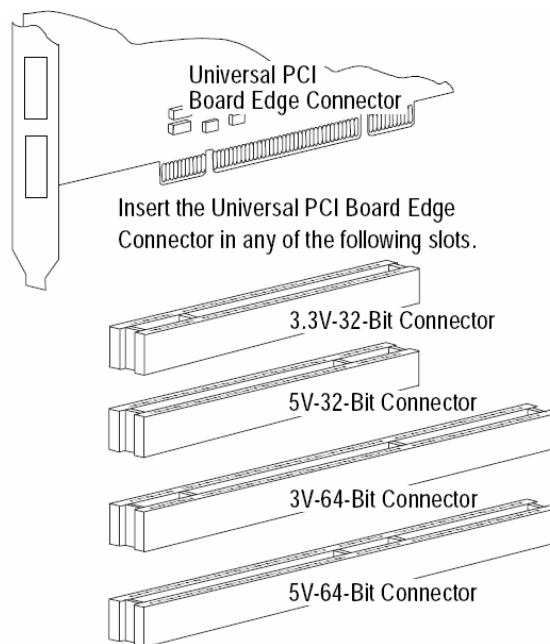
1. Switch SW2 to select the IO voltage level of HSTC on PCI board.



2. Make the connection between the daughter board and PCI board if your design needs it.



3. Switch off the computer and disconnect from the power socket.
4. Remove the cover of the PC.
5. Choose any open slot and insert PCI board.
 - * The Cyclone[®] III PCI development board has a Universal PCI Board edge connector. It can be inserted into any of the PCI slots.



6. Insert bracket screw and ensure that the board sits firmly in the PCI socket.
7. Replace the cover of the PC.
8. Reconnect all power cables and switch the power on.
9. The hardware installation is now complete.

4.3 Software Installation: PCI Kernel Driver

Before users can use Terasic's PCI library to communicate the PCI board, PCI kernel mode driver should be installed in users' PC first.

The kernel driver is located in the "Install PCI Driver" folder of PCI CD-ROM. Please follow below procedures to install the kernel driver:

10. Copy the folder "Install PCI Driver" to your hard-disk.
11. Double click "PCI_DriverInstall.exe" to launch the installation program.