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Data Conversion HSMC

Reference Manual

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I.S. EN ISO 9001

Part Number MNL-01016-1.0

Contents

Additional Information

1. Overview

General Description

This manual provides technical information about the Data Conversion HSMC. This High Speed Mezzanine Card (HSMC) can be used for developing DSP applications with Altera Development boards that feature the High Speed Mezzanine Card (HSMC) connector. Figure 1–1. shows a topside view of the Data Conversion HSMC.

The Data Conversion HSMC was created to provide a set of Analog to Digital and Digital to Analog interfaces including an Audio Codec interface. The purpose of this reference manual is to describe each of the hardware interfaces on the Data Conversion HSMC.

For the latest information about High Speed Mezzanine Cards (HSMCs), go to **www.altera.com/products/devkits/kit-index.html**.

Figure 1–1. Data Conversion HSMC Topside View

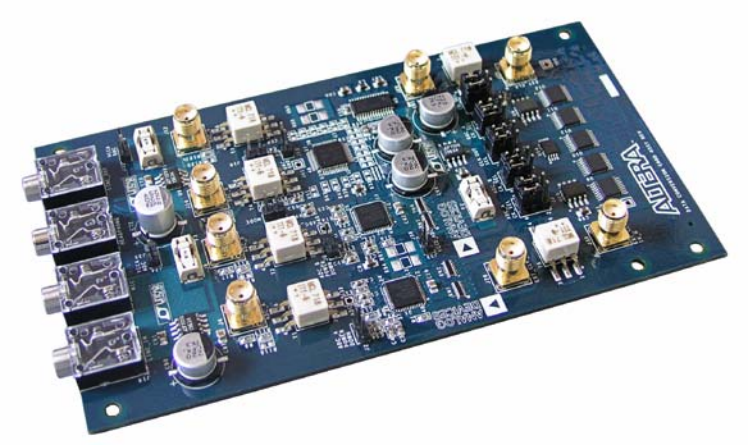


Figure 1–2 shows the Data Conversion HSMC in the DSP Development Kit, Cyclone III edition.

Figure 1–2. Data Conversion HSMC in the DSP Development Kit, Cyclone III Edition

For more information, refer *DSP Development Kit, Cyclone III Edition, Getting Started User Guide*.

Components and Block Diagram

Components

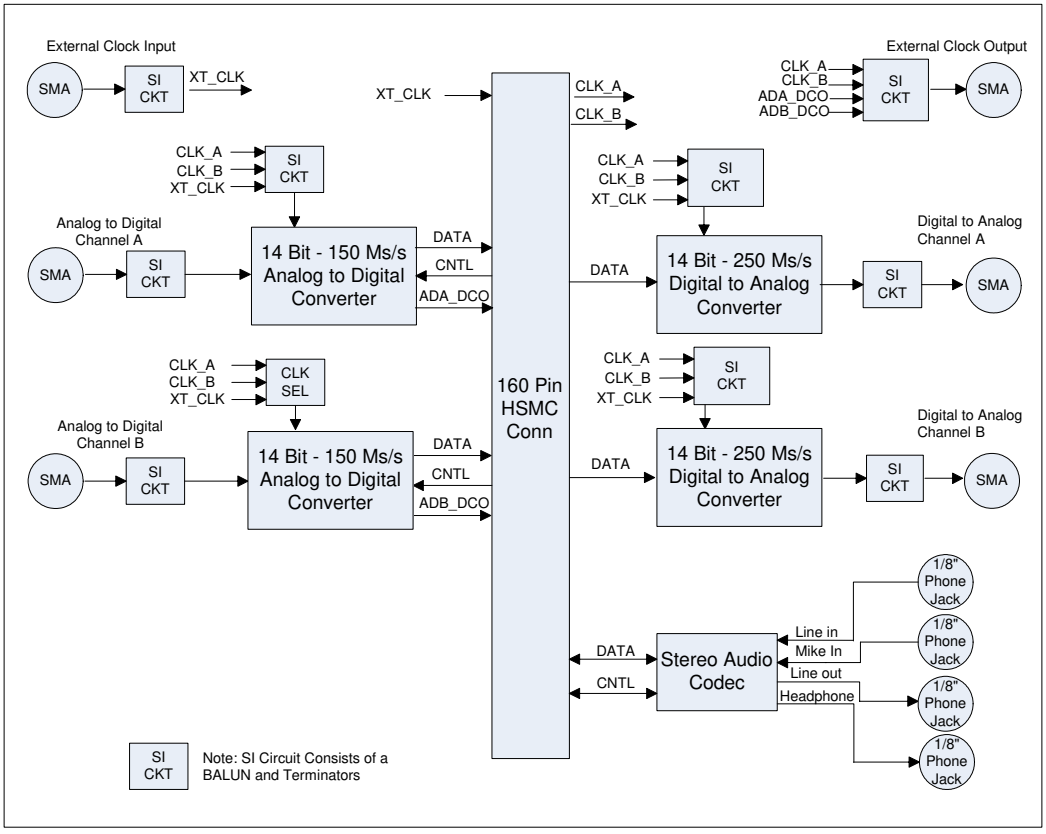
The Data Conversion HSMC contains the following components.

- Interfaces
  - HSMC Interface
  - Audio CODEC Interface
  - External Clock In Interface
  - External Clock Out Interface
  - ADC Channel A and B Input Interface
  - DAC Channel A and B Output Interface
- Power supply
- I2C Serial EEPROM

Block Diagram

Figure 1–3 shows a functional block diagram of the Data Conversion HSMC.

Figure 1–3. Data Conversion HSMC Block Diagram



2. Board Components and Interfaces

Board Overview

This chapter provides operational and connectivity details for the Data Conversion HSMC's major components and interfaces.

Board schematics, board layout database, and assembly files for the Data Conversion HSMC are included in the board_design_files subdirectory of the installed kit directory.

For information on powering-up the Data Conversion HSMC and installing the demo software and examples, refer to the user guide provided with your kit.

Figure 2–1 shows the top view of the Data Conversion HSMC.

Figure 2–1. Top View of the the Data Conversion HSMC

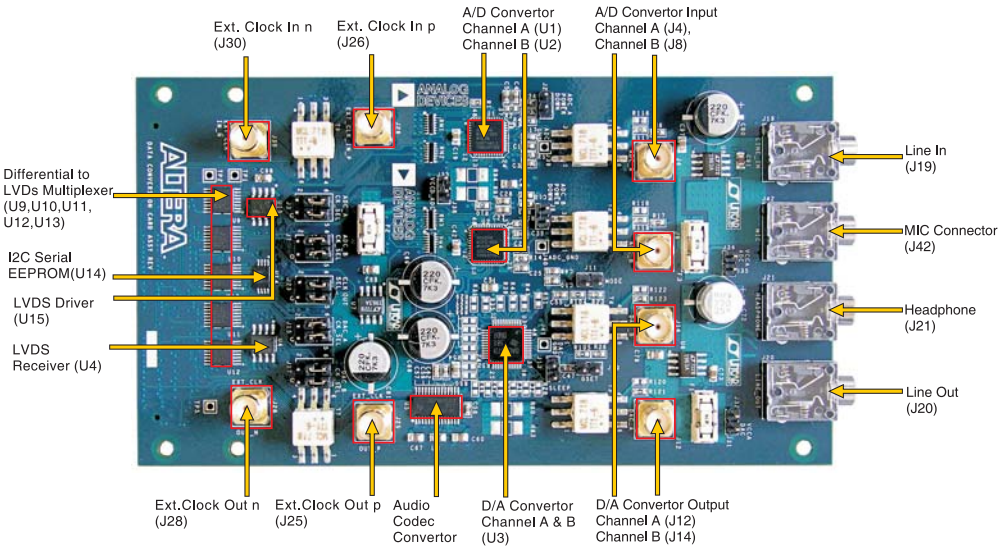


Figure 2–2 shows the back view of the Data Conversion HSMC.

Figure 2–2. Back View of the the Data Conversion HSMC

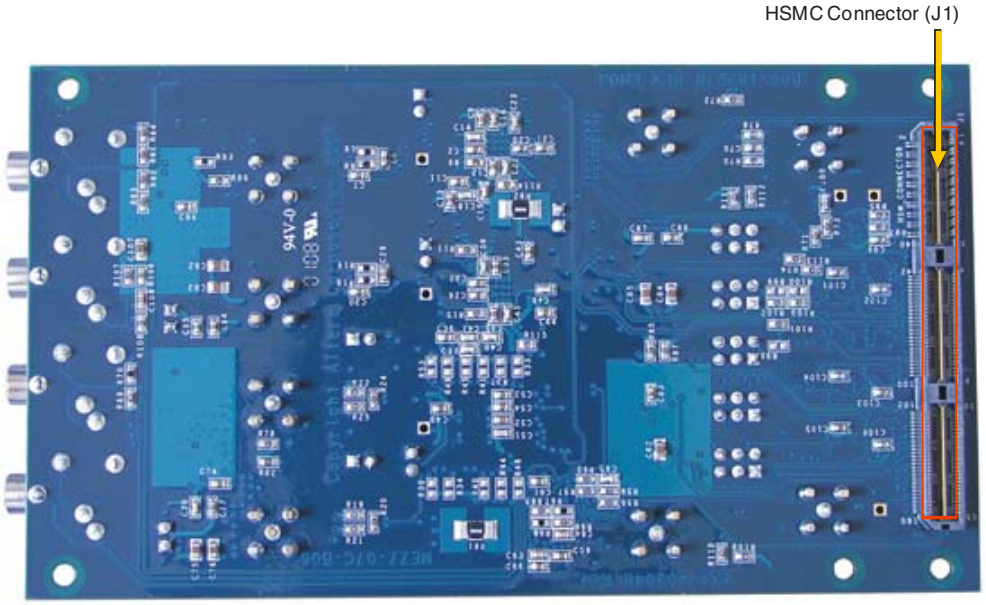


Table 2–1 lists the components and their corresponding board references.

Table 2–1. Data Conversion HSMC Feature Overview

Board Reference	Name	Description	Page
Configuration, Status and Setup Elements			
J3 (Channel A) J7 (Channel B)	A/D converter clock select jumper	Controls which of the three input clock signals (FPGA clock A, B, or the external SMA clock) is routed to the A/D converter	2–4
J2 (Channel A) J6 (Channel B)	Power down select jumper	Controls whether the ADC operates in power down or power up state	2–4
J15 (Channel A) J17 (Channel B)	D/A converter clock select jumper	Controls which of the three input clock signals (FPGA clock A, B, or the external SMA clock) is routed to the D/A converter	2–5
J11	Mode select jumper	Controls whether the DAC operates in dual bus mode or interleaved mode	2–5
J10	Gain setting select jumper	Controls whether the DAC channel's gain is set through one or two resistors	2–6

Table 2–1. Data Conversion HSMC Feature Overview

Board Reference	Name	Description	Page
J13	Sleep select jumper	Controls whether the DAC operates in power down or power up state	2–6
J23	External clock output select jumper	Selects which of the four input clocks (FPGA clock A, B or A/D converter Data Clock Output) is routed to the SMA clock out (J28)	2–6
Clock			
J26 (External Clock In-p) J30 (External Clock In-n)	External clock input SMA connectors	SMA connectors for a differential clock input	2–7
J25 (External Clock In-p) J28 (External Clock In-n)	External clock output SMA connectors	SMA connectors for a differential clock output	2–8
Components and Interfaces			
U1 (Channel A) U2 (Channel B)	A/D converter	Analog Devices AD9254. 14 bit, 150MS/s Analog to Digital converter	2–8
J4 (Channel A) J8 (Channel B)	A/D converter input SMA's	SMA's that drive the A/D converter inputs	2–13
U3 (Channel A and B)	D/A converter	Texas Instruments DAC5672. 14 bit, 175 MS/s Digital to Analog converter	2–13
J12 (Channel A) J14 (Channel B)	D/A converter output SMA's	SMA outputs for the D/A converters	2–17
U5	Audio CODEC	Texas Instruments TLV320AK23. Stereo Audio CODEC, 96KHz, with integrated headphone amplifier	2–17
J19	Line-in audio jack	3.5mm audio connector for line-in	2–18
J20	Line-out audio jack	3.5mm audio connector for line-out	2–18
J21	Headphone jack	3.5mm audio connector for headphones	2–18
J42	MIC jack	3.5mm audio connector for MIC	2–18
J1	HSMC	Expansion connector used to interface with Altera development boards	2–19
U14	I2C EEPROM	ISSI EEPROM IS24C02B, 2kbit	2–20

Configuration, Status and Setup Elements

This section describes configuration, status, and setup elements.

A/D Converter Clock Select Jumper (J3, J7)

Table 2–2 lists the J3 (channel A) and J7 (channel B) jumper settings used to select the A/D converter clock.

Table 2–2. A/D Converter Clock Select Jumper (J3,J7) Settings

Clock Source	Board Reference	Schematic Signal Name (1) (2) (3)	A/D Converter Clock Select (J3 or J7) Jumper Setting
FPGA Clock	HSMC Connector	FPGA_CLK_A_P FPGA_CLK_A_N	Pins 3 and 5, Pins 4 and 6
FPGA Clock	HSMC Connector	FPGA_CLK_B_P FPGA_CLK_B_N	Pins 1 and 3, Pins 4 and 6
External Clock	External Clock Input SMA	XT_IN_P XT_IN_N	Pins 3 and 5, Pins 2 and 4
No Clock	-	NO_CLK_P NO_CLK_N	Pins 1 and 3, Pins 2 and 4

Notes:
(1) See the appendices for FPGA pin-numbers for specific development boards.
(2) On the schematic MUX (U9) output signal names are ADA_CLK_SEL_P, ADA_CLK_SEL_N
(3) On the schematic MUX (U10) output signal names are ADB_CLK_SEL_P, ADB_CLK_SEL_N

Power Down Select Jumper (J2, J6)

The power down configuration of A/D converter is selectable through J2 (channel A) or J6 (channel B). Table 2–3 lists the jumper settings for power down options. A/D converters should be powered down when not used to reduce spurious noise output.

Table 2–3. Power Down Select Jumper Settings for AD9254 A/D Converter (U1, U2)

A/D Converter	Jumper Settings (1)	Description
U1 (Channel A)	J2 Jumper OFF	ADC channel A in normal (operational) state
U1 (Channel A)	J2 Jumper ON	ADC channel A in power down
U2 (Channel B)	J6 Jumper OFF	ADC channel B in normal (operational) state
U2 (Channel B)	J6 Jumper ON	ADC channel B in power down

Notes:
(1) If jumper pins are left open, ADC will be in normal state.

D/A Converter Clock Select Jumper (J15, J17)

Table 2–4 lists the J15 (channel A) and J17 (channel B) jumper settings used to select the D/A converter clock.

Table 2–4. D/A Converter Clock Select Jumper (J15, J17) Settings

Clock Source	Board Reference	Schematic Signal Name (1) (2)	D/A Converter Clock Select (J15 or J17) Jumper Setting
FPGA Clock	HSMC Connector	FPGA_CLK_A_P FPGA_CLK_A_N	Pins 3 and 5, Pins 4 and 6
FPGA Clock	HSMC Connector	FPGA_CLK_B_P FPGA_CLK_B_N	Pins 1 and 3, Pins 4 and 6
External Clock	External Clock Input SMA	XT_IN_P XT_IN_N	Pins 3 and 5, Pins 2 and 4
No Clock	-	NO_CLK_P NO_CLK_N	Pins 1 and 3, Pins 2 and 4

Notes:
(1) On the schematic MUX (U11) output signal names are DAC_CLK_1_P, DAC_CLK_1_N
(2) On the schematic MUX (U12) output signal names are DAC_CLK_2_P, DAC_CLK_2_N

Mode Select Jumper (J11)

The mode select jumper is used to put D/A converter in either dual bus or interleaved mode. It is selectable through J11 (channel A & channel B) Table 2–5 lists the jumper settings for mode select options.

Table 2–5. Mode Select Jumper (J11) Settings for DAC5672 D/A Converter

Jumper Settings (J11)	Description
Jumper ON	Interleaved mode
Jumper OFF	Dual bus mode

Gain Select Jumper (J10)

The Gain setting select jumper is used to set gain of D/A converter's channels. It is selectable through J10 (channel A & channel B) Table 2–6 lists the jumper settings for gain settings options.

Table 2–6. Gain Select Jumper (J10) Settings for DAC5672 D/A Converter

Jumper Settings (J10)	Description
Jumper ON	Sets gain of channel A through Rset on BiasJ_A pin and of channel B through Rset on BiasJ_B pin
Jumper OFF	Gain of channel A and B is set through Rset on BIASJ_a pin only and Rset on BIASJ_B pin is ignored

Sleep Select Jumper (J13)

The sleep select jumper is used to put D/A converter in power down mode. It is selectable through J13 (channel A & channel B). Table 2–7 lists the jumper settings for sleep select options. The D/A when not in use should be put in sleep mode.

Table 2–7. Sleep Select Jumper (J13) Settings for DAC5672 D/A Converter

Jumper Settings (J13)	Description
Jumper ON	Puts DAC in power down mode
Jumper OFF	DAC in normal state

External Clock Output Select Jumper (J23)

Table 2–8 lists External Clock Output Select Jumper (J23) Settings.

Table 2–8. External Clock Output Select Jumper (J23) Settings

Clock Source	Board Reference	Schematic Signal Name (1)	External Clock Output Select Jumper (J23) Settings
FPGA Clock	HSMC Connector	FPGA_CLK_A_P FPGA_CLK_A_N	Pins 3 and 5, Pins 4 and 6
FPGA Clock	HSMC Connector	FPGA_CLK_B_P FPGA_CLK_B_N	Pins 1 and 3, Pins 4 and 6
A/D A DCO	A/D Channel A	ADA_DCO_P ADA_DCO_N	Pins 3 and 5, Pins 2 and 4

Table 2–8. External Clock Output Select Jumper (J23) Settings			
Clock Source	**Board Reference**	**Schematic Signal Name (1)**	**External Clock Output Select Jumper (J23) Settings**
A/D B DCO	A/D Channel B	ADB_DCO_P ADB_DCO_N	Pins 1 and 3, Pins 2 and 4
Notes: (1) On the schematic MUX (U13) output signal names are RX_CLK_P, RX_CLK_N			

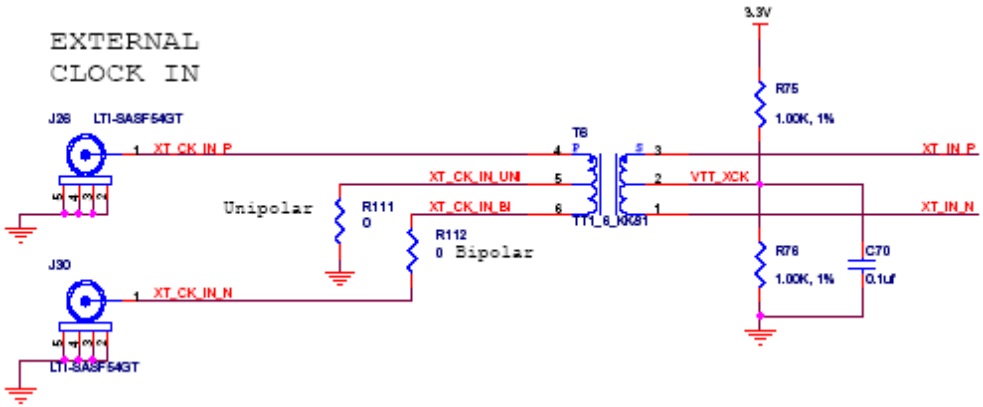
Clocks

This section describes External Clock Input and Output SMA connectors.

External Clock Input SMA Connectors (J26, J30)

The CLK SMA connector (J26, J30) provides an external clock input. It can be selected to be the input to U1, U2 and U3. See Figure 2–3. An external clock input provides designers, while using a particular design, the flexibility to use the same external clock source for the entire system under test. If you choose to use a single ended clock, R112 should be removed and R111 should be installed.

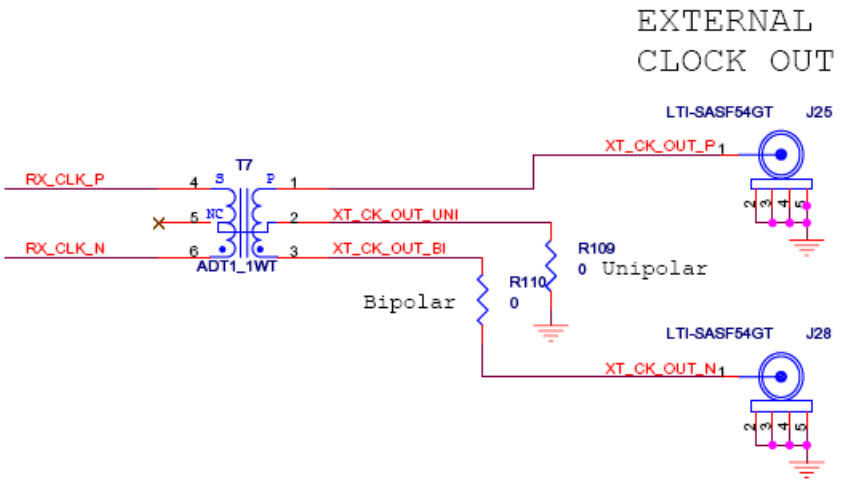
Figure 2–3. External Clock Input Schematic



External Clock Output SMA Connectors (J25, J28)

The CLK SMA connector (J25, J28) provides an external clock output. Different clocks can be selected by using differential LVDS multiplexer (U13) and clock select jumper (J23). See Figure 2–4. The external clock source provides designers, while using a particular design, the flexibility to alter the input frequency to verify FMAX tolerances. If you choose to use a single ended clock, R110 should be removed and R109 should be installed.

Figure 2–4. External Clock Output Schematic



Component Interfaces

This section describes the user interfaces, which consist of A/D converter, D/A converter, Audio Codec Converter, HSMC Connector, and I2C Serial EEPROM.

A/D Converter (U1, U2)

The Data Conversion HSMC contains two AD9254 14-bit 150 MSPS A/D converters. This device is designed for high speed and high-performance applications.

The inputs to these A/D converters are transformer-coupled in order to create a balanced input. The signal-to-noise ratio for the system is up to 72 dB for input signals from 1 MHz to the Nyquist frequency of the

converter. The maximum differential input voltage to the converter is 2 VPP. Usable voltage input to the SMA connector is approximately 512 mV when driven from a 50 Ohm source.

Table 2–9 lists the A/D converter references.

Table 2–9. A/D Converter Component Reference

Item	Description
Board reference	U1, U2
Part Number	AD9254
Device description	14 bit, 150 MSPS Analog to Digital converter
Manufacturer	Analog Device
Manufacturer web site	www.analog.com

Table 2–10 lists the pinouts of ADC Channel A.

Table 2–10. ADC Channel A (U1) Pinouts

HSMC Signal	HSMC Pin	Device Signal	Device Pin No.	Description
ADA_D0	79	D0	45	Data Output Bit 0
ADA_D1	77	D1	46	Data Output Bit1
ADA_D2	73	D2	1	Data Output Bit 2
ADA_D3	71	D3	2	Data Output Bit 3
ADA_D4	67	D4	3	Data Output Bit 4
ADA_D5	65	D5	4	Data Output Bit 5
ADA_D6	61	D6	5	Data Output Bit 6
ADA_D7	59	D7	6	Data Output Bit 7
ADA_D8	55	D8	9	Data Output Bit 8
ADA_D9	53	D9	10	Data Output Bit 9
ADA_D10	49	D10	11	Data Output Bit 10
ADA_D11	47	D11	12	Data Output Bit 11
ADA_D12	43	D12	13	Data Output Bit 12
ADA_D13	41	D13	14	Data Output Bit 13
ADA_OR	83	OR	15	Out-of-Range Indicator
AD_SDIO	91	SDIO/DCS	18	Serial Port Interface (SPI) Data Input/Output (Serial Port Mode)
AD_SCLK	92	SCLK/DFS	19	Serial Port Interface Clock (Serial Port Mode)

Table 2–10. ADC Channel A (U1) Pinouts

HSMC Signal	HSMC Pin	Device Signal	Device Pin No.	Description
ADA_SPI_CS	89	CSB	20	Serial Port Interface Chip Select (Active Low)
ADA_OE	85	OEB	43	Output Enable (Active Low)
ADA_DCO	156	DCO	44	Data Clock Output
-	-	ADA_CLK_P	38 (1)	Clock Input
-	-	ADA_CLK_N	39 (2)	Clock Input
-	-	ADA_PWDN	36 (3)	Power-Down Function Select

Notes:
(1) This pin is connected to Multiplexer pin U9.15.
(2) This pin is connected to Multiplexer pin U9.14.
(3) This pin is connected to Jumper pin J2.2.

Table 2–11 shows the pinout details of ADC Channel B.

Table 2–11. ADC Channel B (U2) Pinouts

HSMC Signal	HSMC Pin	Device Signal	Device Pin No.	Description
ADB_D0	80	D0	45	Data Output Bit 0
ADB_D1	78	D1	46	Data Output Bit1
ADB_D2	74	D2	1	Data Output Bit 2
ADB_D3	72	D3	2	Data Output Bit 3
ADB_D4	68	D4	3	Data Output Bit 4
ADB_D5	66	D5	4	Data Output Bit 5
ADB_D6	62	D6	5	Data Output Bit 6
ADB_D7	60	D7	6	Data Output Bit 7
ADB_D8	56	D8	9	Data Output Bit 8
ADB_D9	54	D9	10	Data Output Bit 9
ADB_D10	50	D10	11	Data Output Bit 10
ADB_D11	48	D11	12	Data Output Bit 11
ADB_D12	44	D12	13	Data Output Bit 12
ADB_D13	42	D13	14	Data Output Bit 13
ADB_OR	84	OR	15	Out-of-Range Indicator
AD_SDIO	91	SDIO/DCS	18	Serial Port Interface (SPI) Data Input/Output (Serial Port Mode)
AD_SCLK	92	SCLK/DFS	19	Serial Port Interface Clock (Serial Port Mode)

Table 2–11. ADC Channel B (U2) Pinouts

HSMC Signal	HSMC Pin	Device Signal	Device Pin No.	Description
ADB_SPI_CS	90	CSB	20	Serial Port Interface Chip Select (Active Low)
ADB_OE	86	OEB	43	Output Enable (Active Low)
ADB_DCO	158	DCO	44	Data Clock Output
-	-	ADB_CLK_P	38 (1)	Clock Input
-	-	ADB_CLK_N	39 (2)	Clock Input
-	-	ADB_PWDN	36 (3)	Power-Down Function Select

Notes:
(1) This pin is connected to Multiplexer pin U10.15.
(2) This pin is connected to Multiplexer pin U10.14.
(3) This pin is connected to Jumper pin J6.2.

A/D Converter Clocks

Figure 2–5 shows the components involved in selecting the clock signal to be sent to the AD9254 A/D converter (U1 for channel A, U2 for channel B). J3 (channel A) or J7 (channel B) selects the A/D clock from the FPGA clock A, the FPGA clock B or the External SMA clock (J26 and J30). The selected A/D clock passes through a differential to LVDS clock multiplexer (U9 for channel A, U10 for channel B), which provides the clock signal to the AD9254.

Figure 2–5. A/D Converter Clocking Options

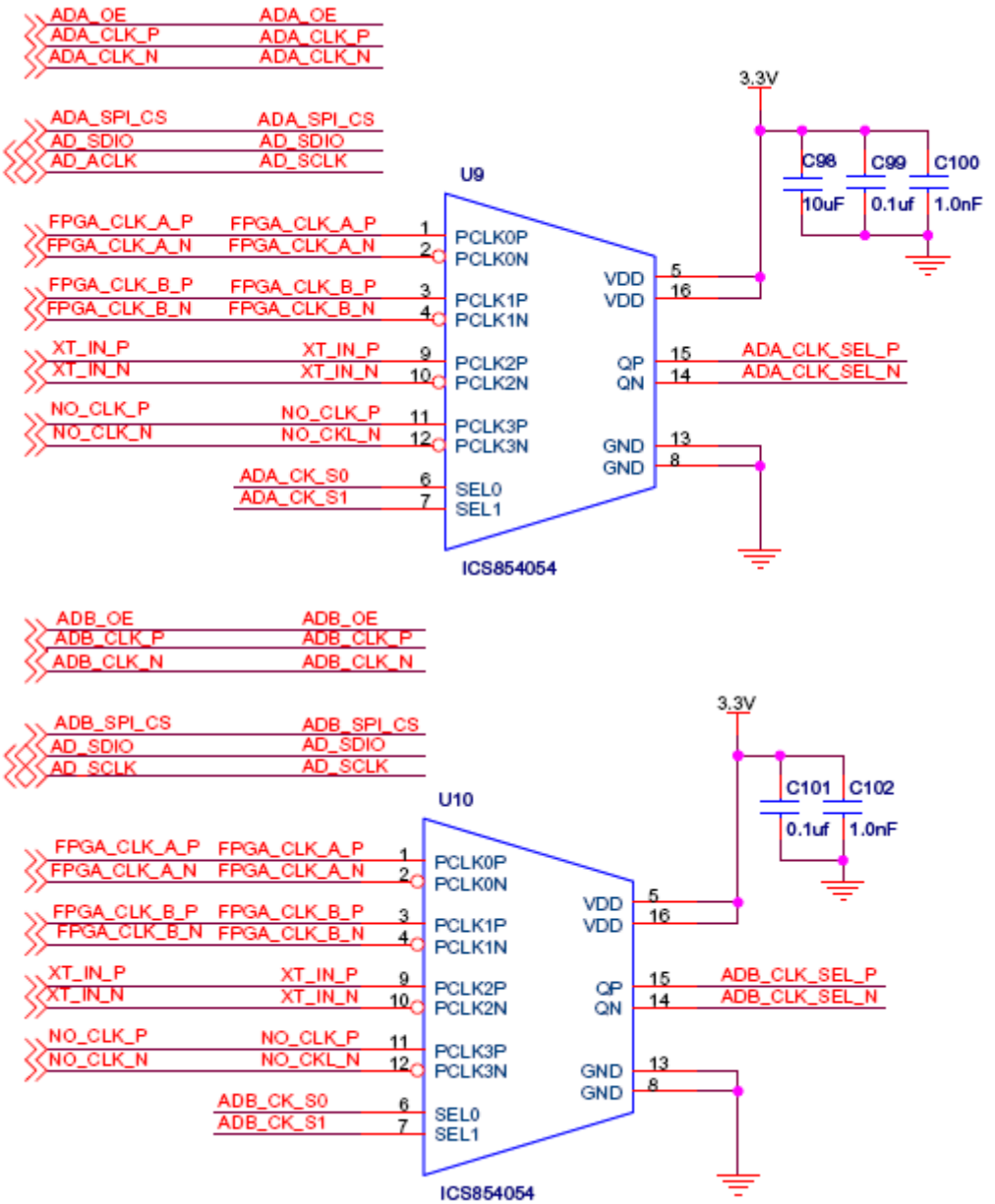


Table 2–12 lists the differential to LVDS clock multiplexer pinouts.

Table 2–12. Differential to LVDS Clock Multiplexer (U9, U10) Pinouts

Schematic Signal	HSMC Connector Pin Number	Device Signal	Device Pin No.	Description
FPGA_CLK_A_P	95	PCLK0P	1	Non-inverting Differential clock input
FPGA_CLK_A_N	97	PCLK0N	2	Inverting Differential clock input
FPGA_CLK_B_P	155	PCLK1P	3	Non-inverting Differential clock input
FPGA_CLK_B_N	157	PCLK1N	4	Inverting Differential clock input
XT_IN_P	96	PCLK2P	9	Non-inverting Differential clock input
XT_IN_N	98	PCLK2N	10	Inverting Differential clock input
AD(A,B)_CLK_SEL_P	-	QP	15	Non-inverting Differential Clock Output
AD(A,B)_CLK_SEL_N	-	QN	14	Inverting Differential Clock Output

A/D Converter Input SMA Connector (J4, J8)

J4 (channel A) and J8 (channel B) are standard through-hole SMA connectors used to interface the AD9254 A/D converter input with SMA cables.

D/A Converter (U3)

The D/A converter (U3 for channel A and B) on the Data Conversion HSMC provides 14-bit resolution and produces samples at rates up to 275 MSPS. It is a high-speed TI DAC5672 D/A converter and is set up to drive a differential-to-single output through a transformer. The output is transformer coupled and can be found on the SMA connector (J12 for channel A, J14 for channel B). The output of the TI DAC5672 D/A converter is set to the maximum output current of 20 mA. The signal-to-noise ratio for the system is up to 60 dB for output signals from 1 MHz to the Nyquist frequency of the converter.

Table 2–13 lists the D/A converter references.

Table 2–13. D/A Converter Component Reference

Item	Description
Board reference	U3
Part Number	DAC5672
Device description	14 bit, 275 MSPS Digital to Analog converter

Table 2–13. D/A Converter Component Reference	
Item	**Description**
Manufacturer	Texas Instruments
Manufacturer web site	www.ti.com

Table 2–14 lists the pinouts of DAC Channel A and Channel B.

Table 2–14. DAC Channel A and Channel B (U3) Pinouts				
HSMC Signal	**HSMC Pin**	**Device Signal**	**Device Pin No.**	**Description**
DA0	139	DA0	14	Data port A0
DA1	137	DA1	13	Data port A1
DA2	133	DA2	12	Data port A2
DA3	131	DA3	11	Data port A3
DA4	127	DA4	10	Data port A4
DA5	125	DA5	9	Data port A5
DA6	121	DA6	8	Data port A6
DA7	119	DA7	7	Data port A7
DA8	115	DA8	6	Data port A8
DA9	113	DA9	5	Data port A9
DA10	109	DA10	4	Data port A10
DA11	107	DA11	3	Data port A11
DA12	103	DA12	2	Data port A12
DA13	101	DA13	1	Data port A13
DB0	140	DB0	36	Data port B0
DB1	138	DB1	35	Data port B1
DB2	134	DB2	34	Data port B2
DB3	132	DB3	33	Data port B3
DB4	128	DB4	32	Data port B4
DB5	126	DB5	31	Data port B5
DB6	122	DB6	30	Data port B6
DB7	120	DB7	29	Data port B7
DB8	116	DB8	28	Data port B8
DB9	114	DB9	27	Data port B9
DB10	110	DB10	26	Data port B10
DB11	108	DB11	25	Data port B11

Table 2–14. DAC Channel A and Channel B (U3) Pinouts

HSMC Signal	HSMC Pin	Device Signal	Device Pin No.	Description
DB12	104	DB12	24	Data port B12
DB13	102	DB13	23	Data port B13
-	-	CLKA	18 (1)	Clock input for DACA, CLKIQ in interleaved mode
-	-	CLKB	19 (2)	Clock input for DACB, RESETIQ in interleaved mode
-	-	GSET	42 (3)	Gain-setting mode: H – 1 resistor, L – 2 resistors. Internal pull-up.
-	-	MODE	48 (4)	Mode Select: H – Dual Bus, L – Interleaved. Internal pull-up.
-	-	SLEEP	37 (5)	Sleep function control input: H – DAC in power-down mode, L – DAC in operating mode. Internal pull-down.

Notes:
(1) This pin is connected to Differential Receiver pin U4.7.
(2) This pin is connected to Differential Receiver pin U4.6.
(3) This pin is connected to Jumper pin J10.1.
(4) This pin is connected to Jumper pin J11.1.
(5) This pin is connected to Jumper Pin J13.2.

D/A Converter Clocks

Figure 2–6 shows the components involved in selecting the clock signal to be sent to the DAC5672 (U3 for channel A and B). J15 (channel A) or J17 (channel B) selects the D/A clock from the FPGA clock A, the FPGA clock B, or the SMA clock (J26 and J30). The selected D/A clock passes through a differential to LVDS clock multiplexer (U11 for channel A, U12 for channel B), which provides the clock signal to 2 bit high speed differential receiver FIN1028 which in turn outputs clock to the DAC5672. (see "D/A Converter Clock Select Jumper (J15, J17)" on page 2–5.)

Figure 2–6. D/A Converter Clocking Options

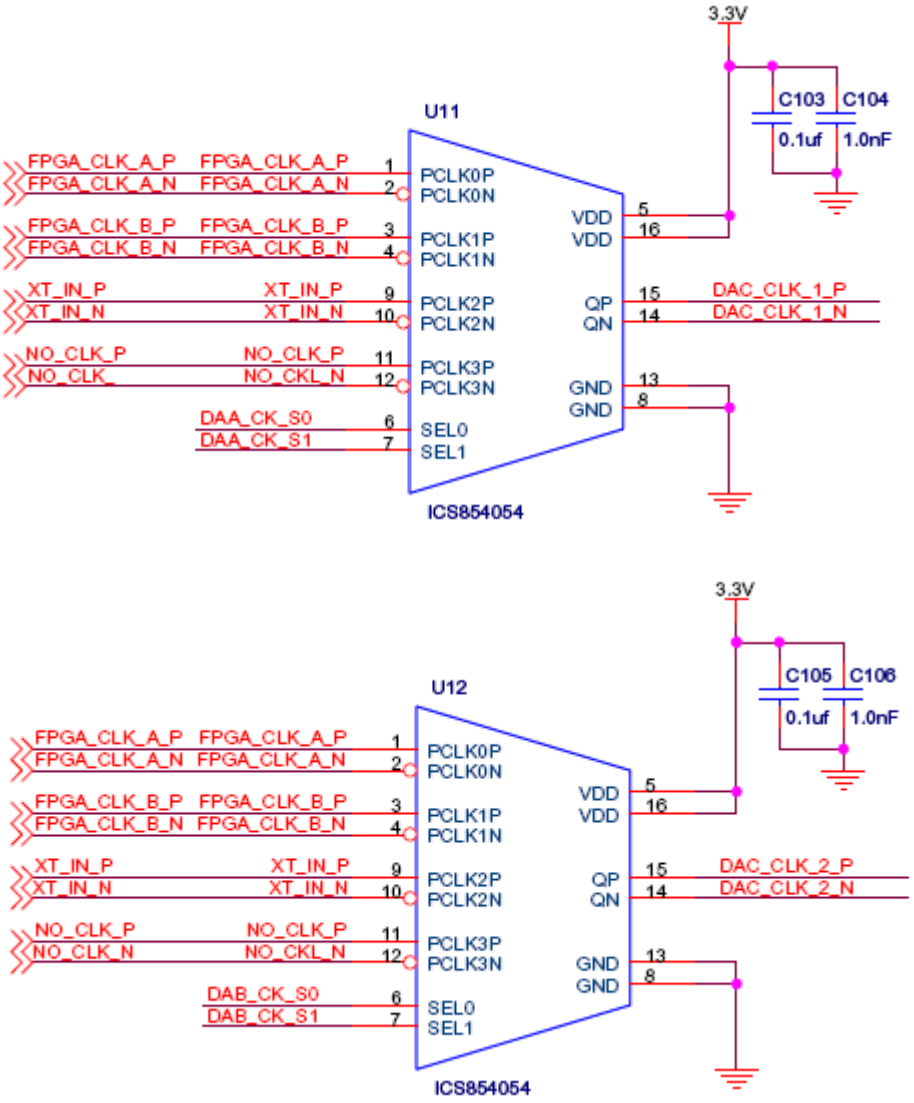


Table 2–15 lists the differential to LVDS clock multiplexer pinouts.

Table 2–15. Differential to LVDS Clock Multiplexer (U11, U12) Pinouts

Schematic Signal	HSMC Connector Pin Number	Device Signal	Device Pin No.	Description
FPGA_CLK_A_P	95	PCLK0P	1	Non-inverting Differential clock input
FPGA_CLK_A_N	97	PCLK0N	2	Inverting Differential clock input
FPGA_CLK_B_P	155	PCLK1P	3	Non-inverting Differential clock input
FPGA_CLK_B_N	157	PCLK1N	4	Inverting Differential clock input
XT_IN_P	96	PCLK2P	9	Non-inverting Differential clock input
XT_IN_N	98	PCLK2N	10	Inverting Differential clock input
DA(A,B)_CLK_SEL_P	-	QP	15	Non-inverting Differential Clock Output
DA(A,B)_CLK_SEL_N	-	QN	14	Inverting Differential Clock Output

D/A Converter Output SMA Connector (J12, J14)

J12 (channel A) and J14 (channel B) are standard through-hole SMA connectors used to interface the DAC5672 D/A converter output with SMA cables.

Audio CODEC Converter (U5)

The Data Conversion HSMC contains three stereo jack and one mic jack connectors which provide one stereo output, one stereo input, one amplified stereo headphone output, and one microphone input. The stereo jacks are driven by a stereo audio CODEC running at 8-96 kHz. Table 2–16 lists the audio CODEC references.

Table 2–16. Audio CODEC Converter Component Reference

Item	Description
Board reference	U5
Part Number	TLV320AIC23
Device description	Stereo Audio Codec, 8 to 96 KHz, with Integrated Headphone Amplifier
Manufacturer	Texas Instruments
Manufacturer web site	www.ti.com

Table 2–17 lists the TI TLV320AIC23 audio CODEC pin-outs.

Table 2–17. Audio CODEC Converter (U5) Pinouts

HSMC Signal	HSMC Pin	Device Signal	Device Pin No.	Description
AIC_XCLK	150	XTI/MCLK	25	Crystal or external-clock input. Used for derivation of all internal clocks on the AIC23B
AIC_LRCOUT	146	LRCOUT	7	I2S ADC-word clock signal. In audio master mode, the AIC23B generates this framing signal and sends it to the DSP. In audio slave mode, the signal is generated by the DSP.
AIC_LRCIN	145	LRCIN	5	I2S DAC-word clock signal. In audio master mode, the AIC23B generates this framing signal and sends it to the DSP. In audio slave mode, the signal is generated by the DSP.
AIC_DIN	143	DIN	4	I2S format serial data input to the sigma-delta stereo DAC
AIC_DOUT	144	DOUT	6	I2S format serial data output from the sigma-delta stereo ADC
AD_SCLK	92	SCLK	24	Control-port serial-data clock. For SPI and 2-wire control modes this is the serial-clock input.
AD_SDIO	91	SDIN	23	I2S format serial data input to the sigma-delta stereo DAC
AIC_SPI_CS	151	CS_n	21	Serial Control Interface Chip Select (Active Low)
AIC_BCLK	149	BCLK	3	I2S serial-bit clock. In audio master mode, the AIC23B generates this signal and sends it to the DSP. In audio slave mode, the signal is generated by the DSP

Audio Jacks (J19, J20, J21, J42)

The Data Conversion HSMC contains the following audio connectors:

- J19—an audio connector for line-in
- J20—an audio connector for line-out
- J21—an audio connector for amplified line-out
- J42—an audio connector for mic