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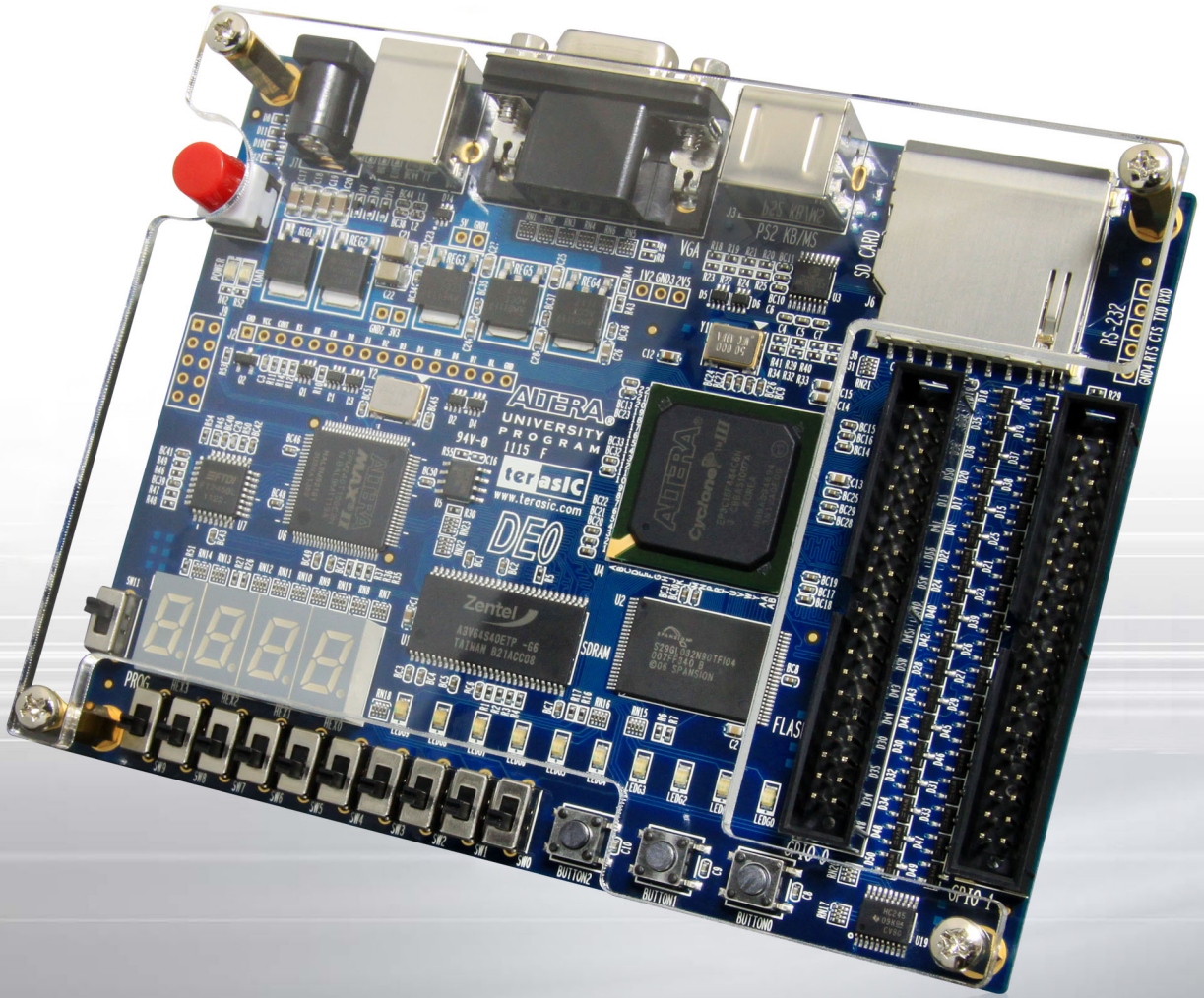

ALTERA
UNIVERSITY
PROGRAM

DE0 User Manual

Development and Education Board

CONTENTS

Chapter 1
DE0 Package

The DE0 package contains all the components needed to use the DE0 board in conjunction with a computer that runs the Microsoft Windows software.

1.1 Package Contents

Figure 1-1shows a photograph of the DE0 package.

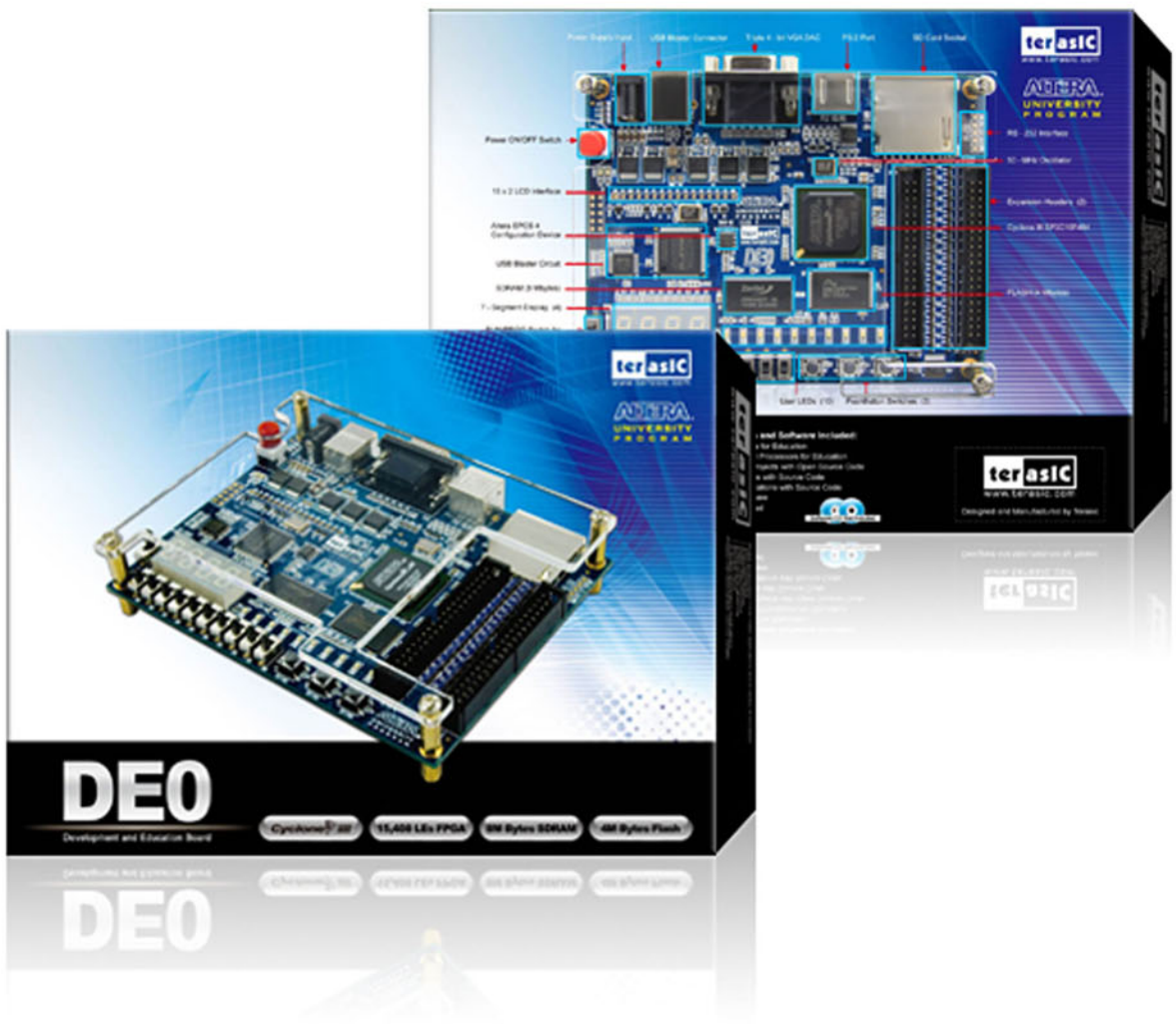

Figure 1-1 The DE0 package contents.

The DE0 package includes:

- The DE0 board
- USB Cable for FPGA programming and control
- DE0 System CD containing :
    - Altera's Quartus® II Web Edition and the Nios® II Embedded Design Suit Evaluation Edition software
    - the DE0 documentation and supporting materials, including the User Manual, the Control Panel utility, reference designs and demonstrations, device datasheets, tutorials, and a set of laboratory exercises
- Clear plastic cover for the board
- 7.5 DC wall-mount power supply

1.2 The DE0 Board Assembly

To assemble the included stands for the DE0 board:

- Assemble a rubber (silicon) cover, as shown in Figure 1-2, for each of the four copper stands on the DE0 board
- The clear plastic cover provides extra protection, and is mounted over the top of the board by using additional stands and screws

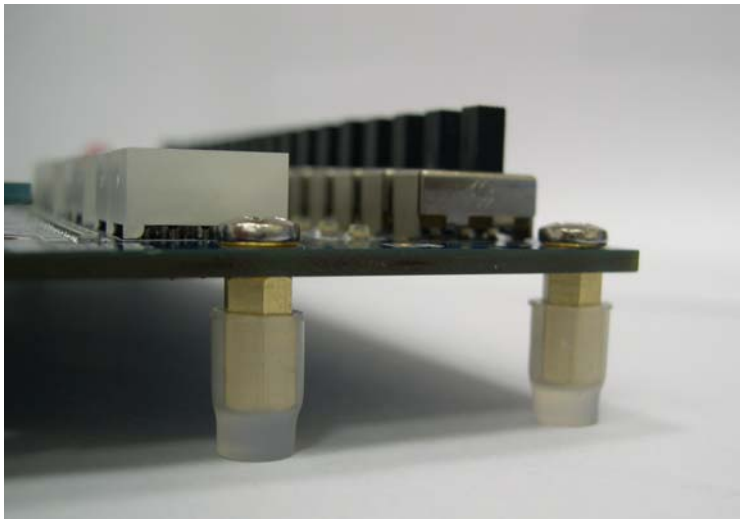

Figure 1-2 The feet for the DE0 board.

■ Getting Help

Here are the addresses where you can get help if you encounter problems:

- Altera Corporation
  101 Innovation Drive

San Jose, California, 95134 USA
Email: university@altera.com

- Terasic Technologies
  No. 356, Sec. 1, Fusing E. Rd.
  Jhubei City, HsinChu County, Taiwan, 302
  Email: support@terasic.com
  Web: DE0.terasic.com

Chapter 2
Altera DE0 Board

This chapter presents the features and design characteristics of the DE0 board.

2.1 Layout and Components

A photograph of the DE0 board is shown in Figure 2-1. It depicts the layout of the board and indicates the location of the connectors and key components.

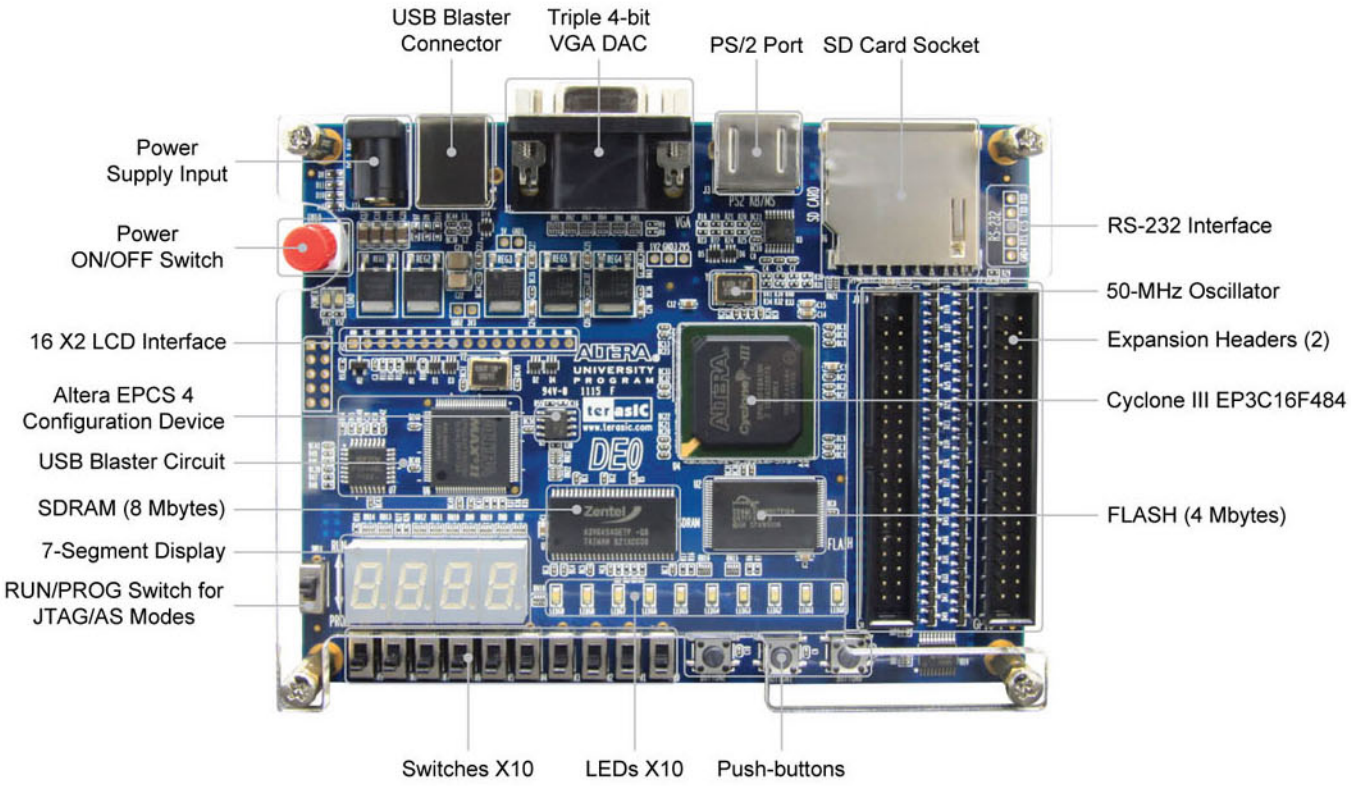

Figure 2-1 The DE0 board.

The DE0 board has many features that allow the user to implement a wide range of designed circuits, from simple circuits to various multimedia projects.

The following hardware is provided on the DE0 board:

- Altera Cyclone® III 3C16 FPGA device
- Altera Serial Configuration device – EPCS4
- USB Blaster (on board) for programming and user API control; both JTAG and Active Serial (AS) programming modes are supported
- 8-Mbyte SDRAM
- 4-Mbyte Flash memory
- SD Card socket
- 3 pushbutton switches
- 10 toggle switches
- 10 green user LEDs
- 50-MHz oscillator for clock sources
- VGA DAC (4-bit resistor network) with VGA-out connector
- RS-232 transceiver
- PS/2 mouse/keyboard connector
- Two 40-pin Expansion Headers

2.2 Block Diagram of the DE0 Board

Figure 2-2 gives the block diagram of the DE0 board. To provide maximum flexibility for the user, all connections are made through the Cyclone IIII FPGA device. Thus, the user can configure the FPGA to implement any system design.

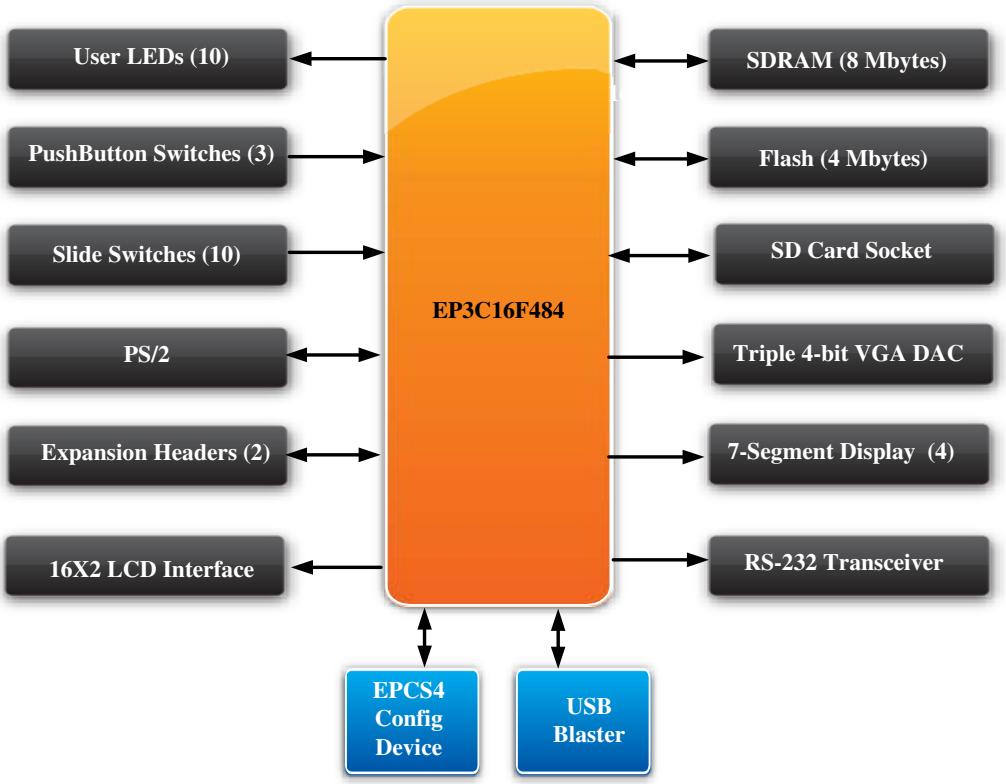

Figure 2-2 Block diagram of the DE0 board.

Following is more detailed information about the blocks in Figure 2-2:

Cyclone IIII 3C16 FPGA

- 15,408 LEs
- 56 M9K Embedded Memory Blocks
- 504K total RAM bits
- 56 embedded multipliers
- 4 PLLs
- 346 user I/O pins
- FineLine BGA 484-pin package

Built-in USB Blaster circuit

- On-board USB Blaster for programming and user API (Application programming interface) control
- Using the Altera EPM240 CPLD

SDRAM

- One **8**-Mbyte Single Data Rate Synchronous Dynamic RAM memory chip
- Supports 16-bits data bus

Flash memory

- 4-Mbyte NOR Flash memory
- Support Byte (8-bits)/Word (16-bits) mode

SD card socket

- Provides both SPI and SD 1-bit mod SD Card access

Pushbutton switches

- 3 pushbutton switches
- Normally high; generates one active-low pulse when the switch is pressed

Slide switches

- 10 Slide switches
- A switch causes logic 0 when in the DOWN position and logic 1 when in the UP position

General User Interfaces

- 10 Green color LEDs (Active high)
- 4 seven-segment displays (Active low)
- 16x2 LCD Interface (Not include LCD module)

Clock inputs

- 50-MHz oscillator

VGA output

- Uses a 4-bit resistor-network DAC
- With 15-pin high-density D-sub connector
- Supports up to 1280x1024 at 60-Hz refresh rate

Serial ports

- One RS-232 port (Without DB-9 serial connector)
- One PS/2 port (Can be used through a PS/2 Y Cable to allow you to connect a keyboard and mouse to one port)

Two 40-pin expansion headers

- 72 Cyclone III I/O pins, as well as 8 power and ground lines, are brought out to two 40-pin expansion connectors
- 40-pin header is designed to accept a standard 40-pin ribbon cable used for IDE hard drives

2.3 Power-up the DE0 Board

The DE0 board comes with a preloaded configuration bit stream to demonstrate some features of the board. This bit stream also allows users to see quickly if the board is working properly. To power-up the board perform the following steps:

1. Connect the provided USB cable from the host computer to the USB Blaster connector on the DE0 board. For communication between the host and the DE0 board, it is necessary to install the Altera USB Blaster driver software. If this driver is not already installed on the host computer, it can be installed as explained in the tutorial *Getting Started with Altera's DE0 Board*. This tutorial is available in the directory ***DE0\DE0_user_manual*** on the **DE0 System CD-ROM**.
2. Connect the 7.5V adapter to the DE0 board
3. Connect a VGA monitor to the VGA port on the DE0 board
4. Turn the RUN/PROG switch on the left edge of the DE0 board to RUN position; the PROG position is used only for the AS Mode programming
5. Turn the power on by pressing the ON/OFF switch on the DE0 board

At this point you should observe the following:

- All user LEDs are flashing
- All 7-segment displays are cycling through the numbers 0 to F
- The VGA monitor displays the image shown in Figure 2-3.

Figure 2-3 The default VGA output pattern.

Chapter 3
DE0 Control Panel

The DE0 board comes with a Control Panel facility that allows users to access various components on the board from a host computer. The host computer communicates with the board through an USB connection. The facility can be used to verify the functionality of components on the board or be used as a debug tool while developing RTL code.

This chapter first presents some basic functions of the Control Panel, then describes its structure in block diagram form, and finally describes its capabilities.

3.1 Control Panel Setup

The Control Panel Software Utility is located in the "DE0_*Control_panel*" folder in the **DE0 System CD-ROM**. To install it, just copy the whole folder to your host computer.

To activate the Control Panel, perform the following steps:

1. Make sure Quartus II and USB-Blaster Driver are installed successfully on your PC.
2. Connect the supplied USB cable to the USB Blaster port, connect the 7.5V power supply, and turn the power switch ON
3. Set the RUN/PROG switch to the RUN position
4. Start the executable *DE0_ControlPanel.exe* on the host computer. The Control Panel user interface shown in Figure 3-1will appear.

When the control panel window appears, it will automatically download the bit stream file .sof into the FPGA. If any error message shows up as shown in Figure 3-2, please check steps 1 to 3 has been performed. Then, click *Download Code* button to program FPGA again. Note, the Control Panel will occupy the USB port until you close that port; you cannot use Quartus II to download a configuration file into the FPGA until you close the USB port.

5. The Control Panel is now ready to be use; experiment by setting the value of the LEDs display and observe the result on the DE0 board.

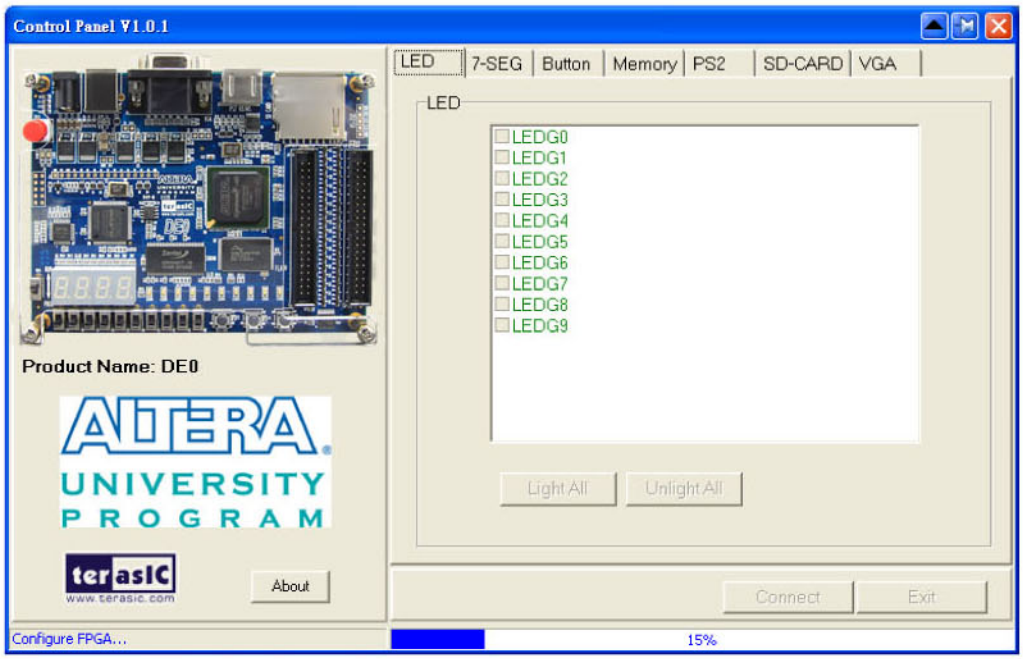

Figure 3-1. The DE0 Control Panel.

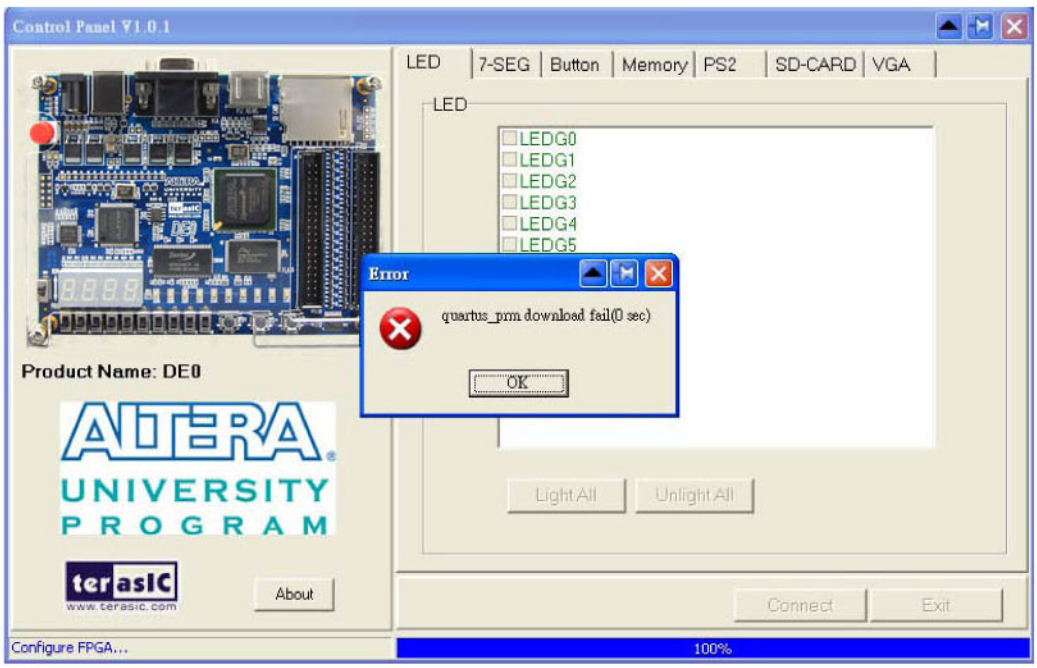

Figure 3-2. The error message of the DE0 Control Panel.

The concept of the DE0 Control Panel is illustrated in Figure 3-3. The "Control Codes" that perform the control functions is implemented in the FPGA board. It communicates with the Control Panel window, which is active on the host computer, via the USB Blaster link. The graphical interface is used to issue commands to the control codes. It handles all requests and performs data transfers between the computer and the DE0 board.

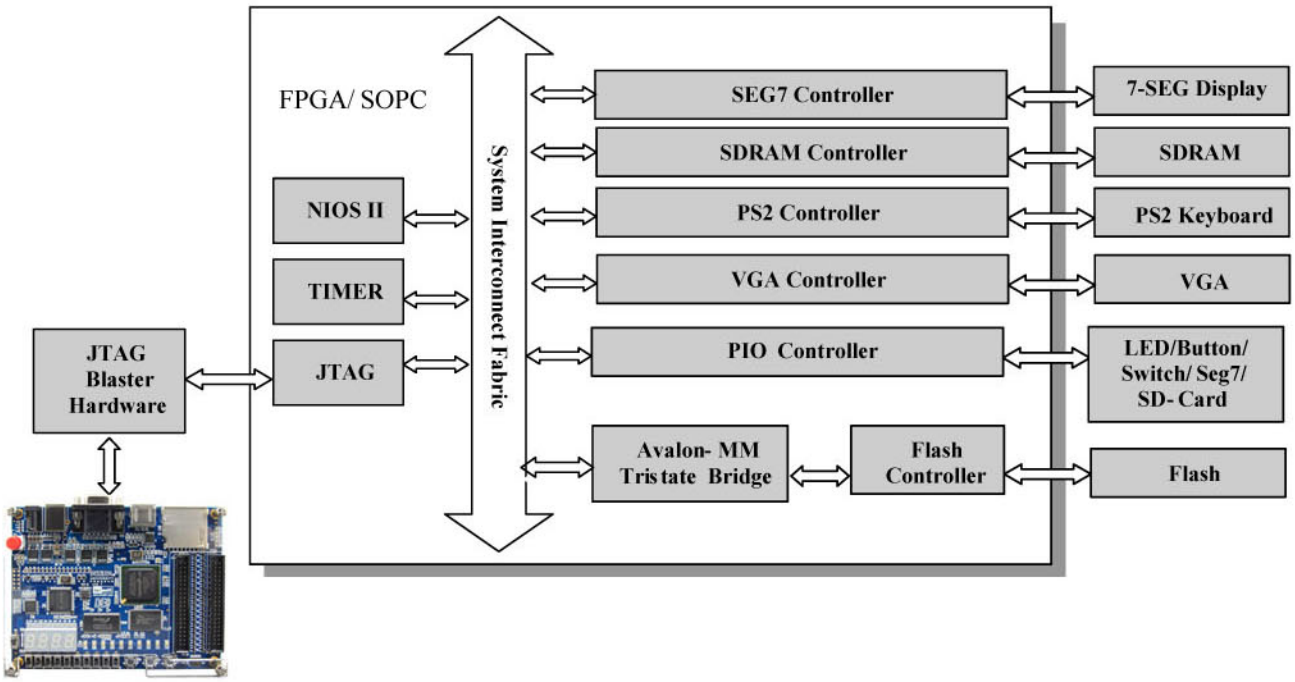

Figure 3-3. The DE0 Control Panel concept.

The DE0 Control Panel can be used to light up the LEDs, change the values displayed on 7-segment, monitor buttons/switches status, read/write the SDRAM and Flash Memory, read data from a PS/2 keyboard, output color pattern to LCD monitor via VGA connector, and read SD-CARD specification information. The feature of reading/writing a word or an entire file from/to the Flash Memory allows the user to develop multimedia application (Flash Picture Viewer) without worrying about how to build a Memory Programmer.

3.2 Controlling the LEDs and 7-Segment Displays

A simple function of the Control Panel is to allow setting the values displayed on LEDs and the 7-segment displays.

Choosing the **LED** tab leads to the window in Figure 3-4. Here, you can directly turn the individual LEDs on or off by selecting they individually or by clicking “Light All” or “Unlight All”.

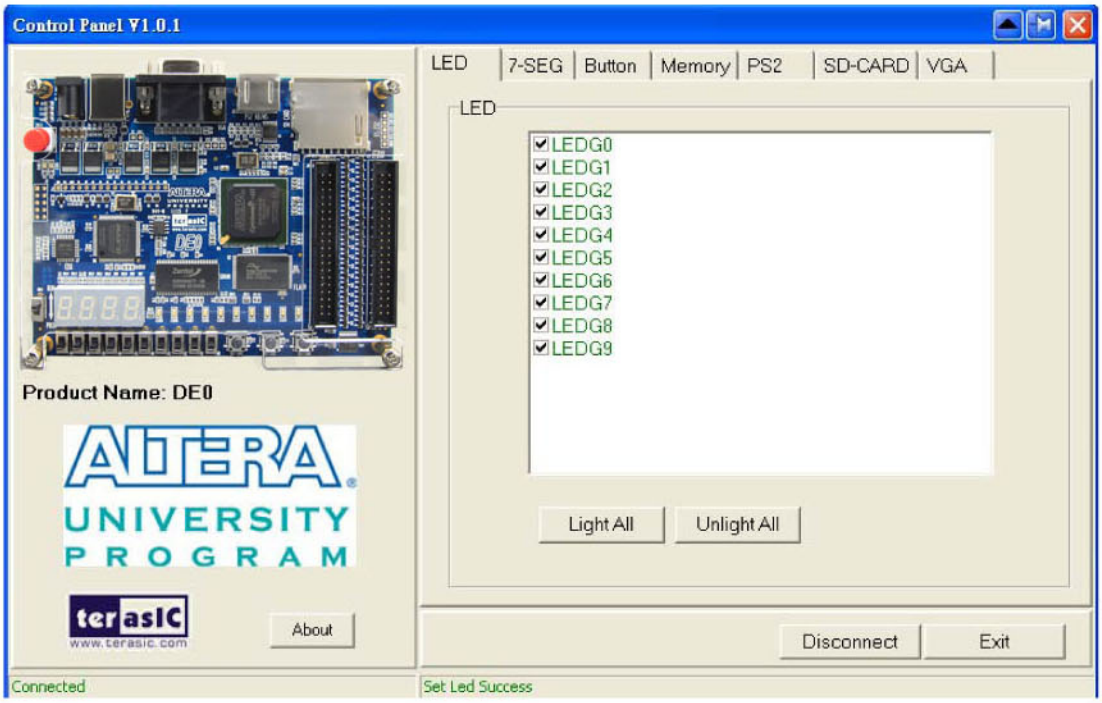

Figure 3-4. Controlling LEDs

Choosing the **7-SEG** tab leads to the window in Figure 3-5. In the tab sheet, directly use the **Up-Down** control and **Dot** Check box to specified desired patterns, the 7-SEG patterns on the board will be updated immediately.

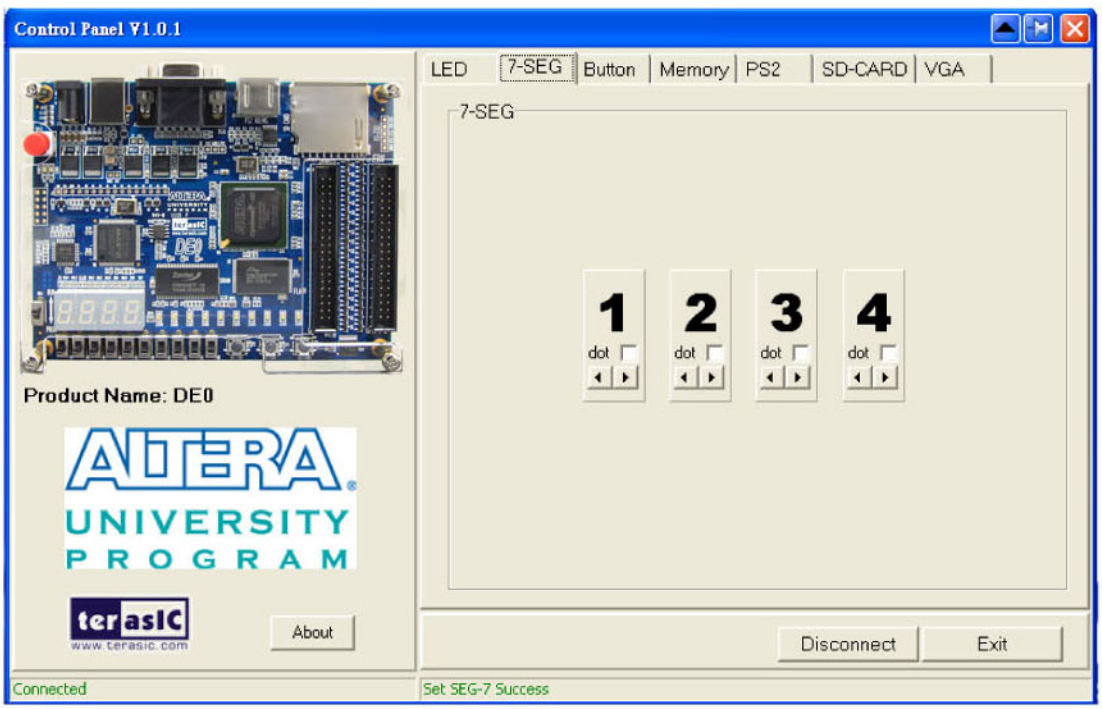

Figure 3-5. Controlling 7-SEG display.

The ability to set arbitrary values into simple display devices is not needed in typical design activities. However, it gives the user a simple mechanism for verifying that these devices are functioning correctly in case a malfunction is suspected. Thus, it can be used for troubleshooting purposes.

3.3 Switches and Buttons

Choosing the **Button** tab leads to the window in Figure 3-6. The function is designed to monitor the status of switches and buttons in real time and show the status in a graphical user interface. It can be used to verify the functionality of the switches and buttons.

Press the **Start** button to start button/switch status monitoring process, and button caption is changed from **Start** to **Stop**. In the monitoring process, the status of buttons and switches on the board is shown in the GUI window and updated in real time. Press **Stop** to end the monitoring process.

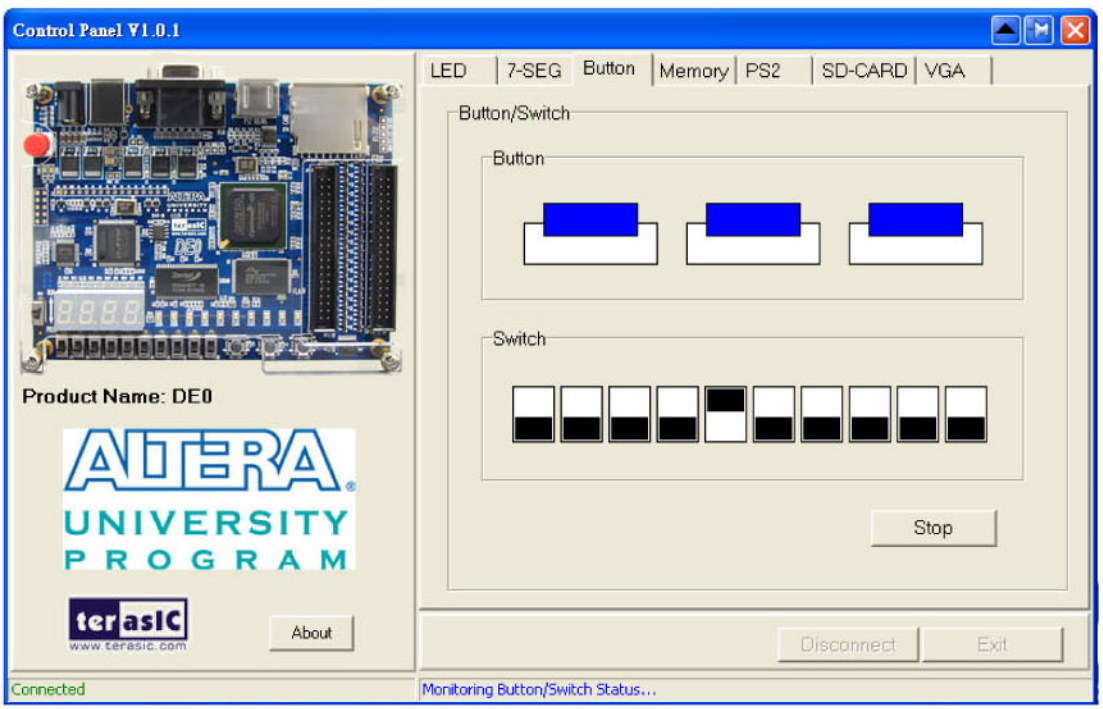

Figure 3-6. Monitoring switches and buttons.

The ability to check the status of button and switch is not needed in typical design activities. However, it provides users a simple mechanism for verifying if the buttons and switches are functioning correctly. Thus, it can be used for troubleshooting purposes.

3.4 SDRAM and Flash Controller and Programmer

The Control Panel can be used to write/read data to/from the SDRAM and FLASH chips on the DE0 board. Click on the **Memory** tab and select "SDRAM" to reach the window in Figure 3-7. Please note to erase the flash memory before writing data to it.

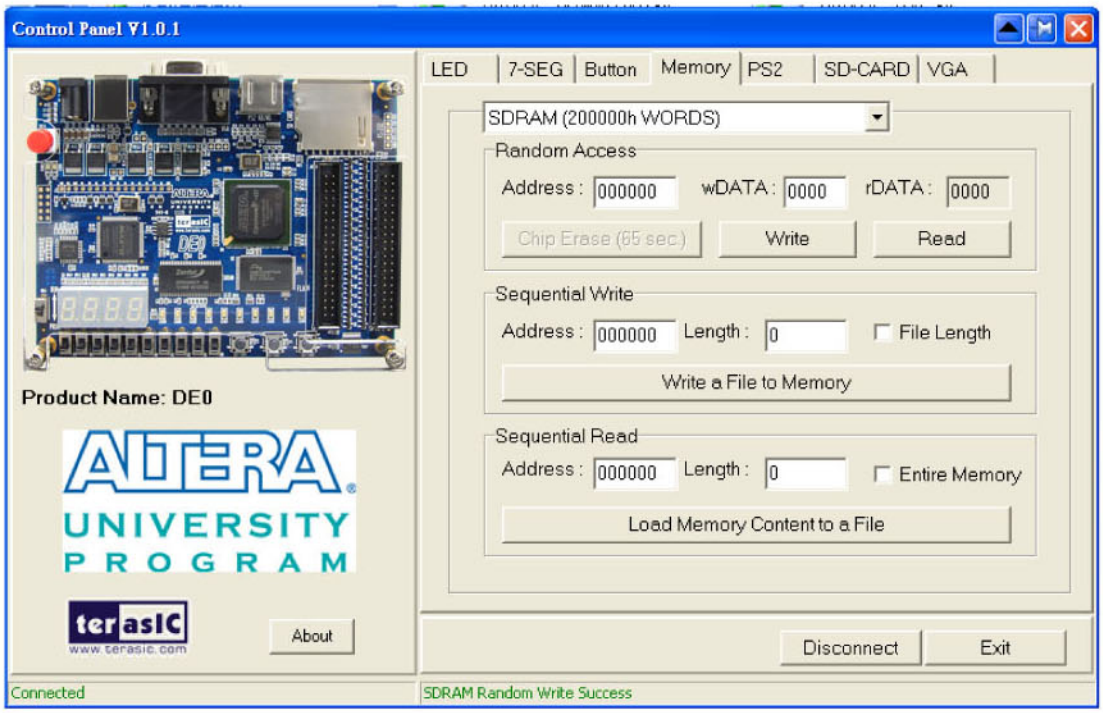

Figure 3-7. Accessing the SDRAM

A 16-bit word can be written into the SDRAM by entering the address of the desired location, specifying the data to be written, and pressing the **Write** button. Contents of the location can be read by pressing the **Read** button. Figure 3-7 depicts the result of writing the hexadecimal value 7eff into location 000000, followed by reading the same location.

The Sequential Write function of the Control Panel is used to write the contents of a file into the SDRAM as follows:

1. Specify the starting address in the **Address** box.
2. Specify the number of bytes to be written in the **Length** box. If the entire file is to be loaded, then a checkmark may be placed in the **File Length** box instead of giving the number of bytes.
3. To initiate the writing of data, click on the **Write a File to Memory** button.
4. When the Control Panel responds with the standard Windows dialog box asking for the source file, specify the desired file in the usual manner.

The Control Panel also supports loading files with a *.hex* extension. Files with a *.hex* extension are ASCII text files that specify memory values using ASCII characters to represent hexadecimal values. For example, a file containing the line

0123456789ABCDEF

defines four 8-bit values: 01, 23, 45, 67, 89, AB, CD, EF. These values will be loaded consecutively into the memory.

The Sequential Read function is used to read the contents of the SDRAM and place them into a file as follows:

1. Specify the starting address in the **Address** box.
2. Specify the number of bytes to be copied into the file in the **Length** box. If the entire contents of the SDRAM are to be copied (which involves all 8 Mbytes), then place a checkmark in the **Entire Memory** box.
3. Press **Load Memory Content to a File** button.
4. When the Control Panel responds with the standard Windows dialog box asking for the destination file, specify the desired file in the usual manner.

Users can use the similar way to access the Flash. Please note that users need to erase the flash before writing data to it.

3.5 PS2 Device

The Control Panel provides users a tool to receive the inputs from a PS2 keyboard in real time. The received scan-codes are translated to ASCII code and displayed in the control window. Only visible ASCII codes are displayed. For control key, only “Carriage Return/ENTER” key is implemented. This function can be used to verify the functionality of the PS2 Interface. Please follow the steps below to exercise the PS2 device:

1. Choosing the **PS2** tab leads to the window in Figure 3-8.
2. Plug a PS2 Keyboard to the FPGA board. Then,
3. Press the **Start** button to start PS2Keyboard input receiving process; Button caption is changed from **Start** to **Stop**.
4. In the receiving process, users can start to press the attached keyboard. The input data will be displayed in the control window in real time. Press **Stop** to terminate the monitoring process.

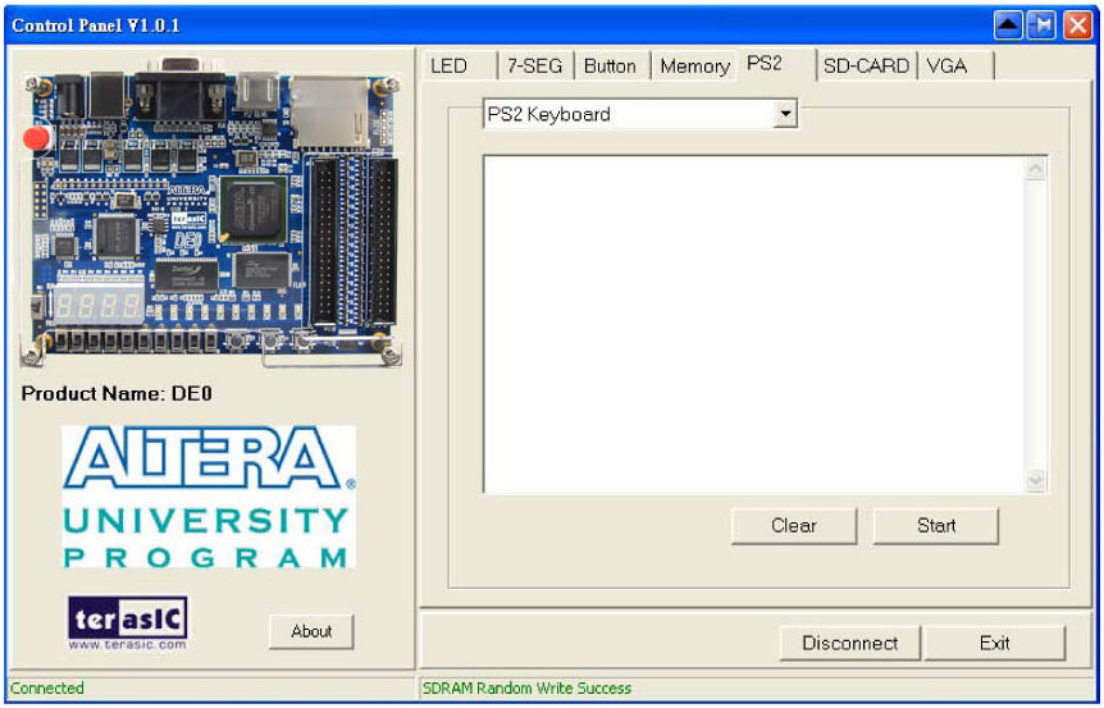

Figure 3-8. Reading the PS2 Keyboards

3.6 SD CARD

The function is designed to read the identification and specification of the SD card. The 1-bit SD MODE is used to access the SD card. This function can be used to verify the functionality of SD-CARD Interface. Follow the steps below to exercise the SD card:

1. Choosing the **SD-CARD** tab leads to the window in Figure 3-9.
2. Insert a SD card to the DE0 board, then press the **Read** button to read the SD card. The SD card's identification and specification will be displayed in the control window.

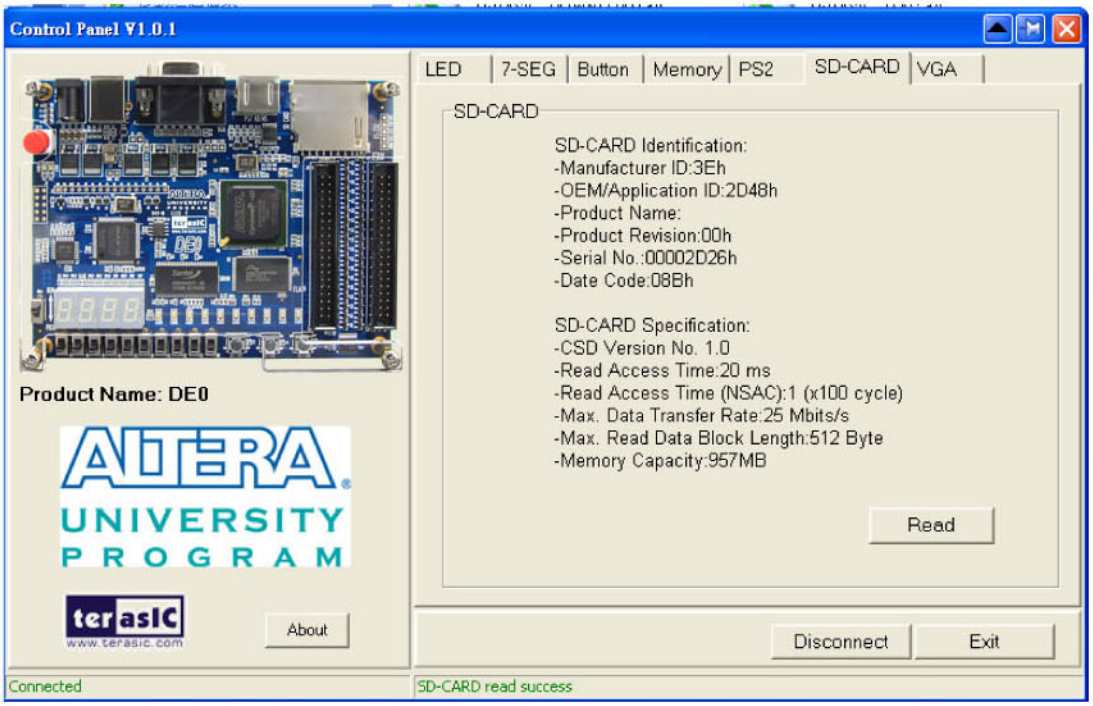

Figure 3-9. Reading the SD card Identification and Specification

3.7 VGA

DE0 control panel provides VGA pattern function that allows users to output color pattern to LCD/CRT monitor using the DE0 FPGA board. Please follow the steps below to generate the VGA pattern function:

1. Choosing the VGA tab leads to the window in Figure 3-10.
2. Plug a D-sub cable to the VGA connector of the DE0 board and LCD/CRT monitor.
3. The LCD/CRT monitor will display the same color pattern on the control panel window.
4. Click the drop down menu shown in Figure 3-10 where you can output the selected color individually.

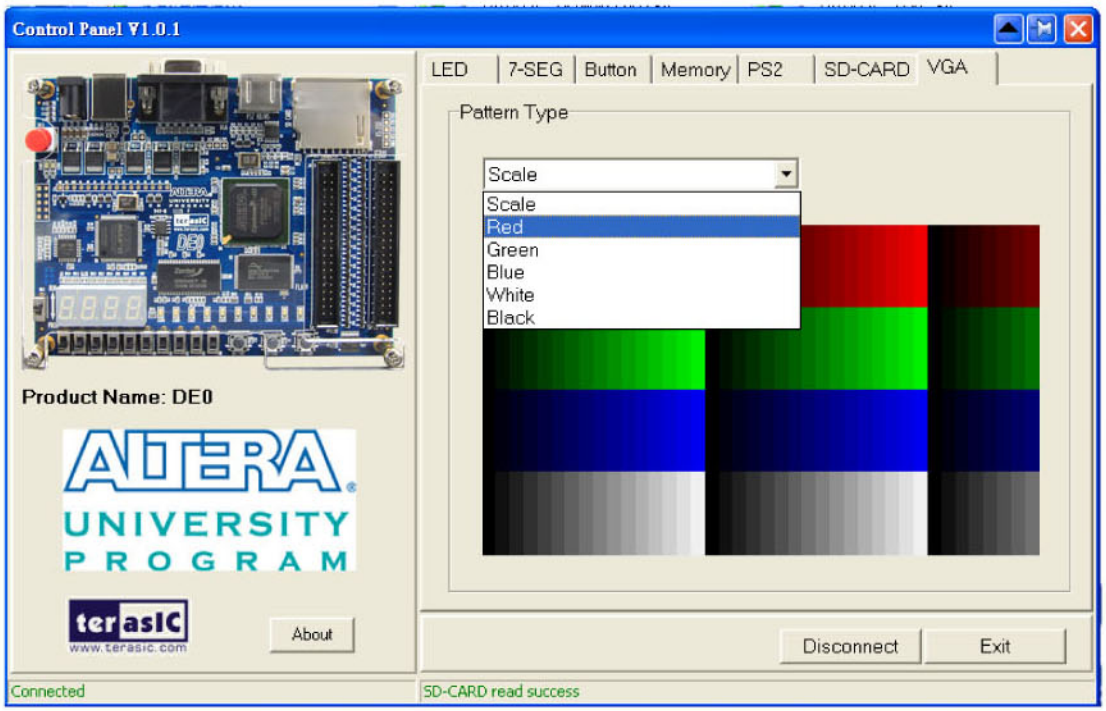

Figure 3-10. Controlling VGA display

Chapter 4
Using the DE0 Board

This chapter gives instructions for using the DE0 board and describes each of its I/O devices.

4.1 Configuring the Cyclone III FPGA

The procedure for downloading a circuit from a host computer to the DE0 board is described in the tutorial *Getting Started with Altera's DE0 Board*. This tutorial is found in the *user_manaul* folder on the **DE0 System CD-ROM**. The user is encouraged to read the tutorial first, and to treat the information below as a short reference.

The DE0 board contains a serial EEPROM chip that stores configuration data for the Cyclone III FPGA. This configuration data is automatically loaded from the EEPROM chip into the FPGA each time power is applied to the board. Using the Quartus II software, it is possible to reprogram the FPGA at any time, and it is also possible to change the non-volatile data that is stored in the serial EEPROM chip. Both types of programming methods are described below.

1. *JTAG* programming: In this method of programming, named after the IEEE standards *Joint Test Action Group*, the configuration bit stream is downloaded directly into the Cyclone III FPGA. The FPGA will retain this configuration as long as power is applied to the board; the configuration is lost when the power is turned off.
2. *AS* programming: In this method, called *Active Serial* programming, the configuration bit stream is downloaded into the Altera EPCS4 serial EEPROM chip. It provides non-volatile storage of the bit stream, so that the information is retained even when the power supply to the DE0 board is turned off. When the board's power is turned on, the configuration data in the EPCS4 device is automatically loaded into the Cyclone III FPGA.

The sections below describe the steps used to perform both JTAG and AS programming. For both methods the DE0 board is connected to a host computer via a USB cable. Using this connection, the board will be identified by the host computer as an Altera *USB Blaster* device. The process for installing on the host computer the necessary software device driver that communicates with the USB Blaster is described in the tutorial *Getting Started with Altera's DE0 Board*. This tutorial is available on the **DE0 System CD-ROM**.

Configuring the FPGA in JTAG Mode

Figure 4-1 illustrates the JTAG configuration setup. To download a configuration bit stream into the Cyclone III FPGA, perform the following steps:

- Ensure that power is applied to the DE0 board
- Connect the supplied USB cable to the USB Blaster port on the DE0 board (see Figure 2-1)
- Configure the JTAG programming circuit by setting the RUN/PROG switch (see Figure 4-2) to the RUN position.
- The FPGA can now be programmed by using the Quartus II Programmer module to select a configuration bit stream file with the *.sof* filename extension

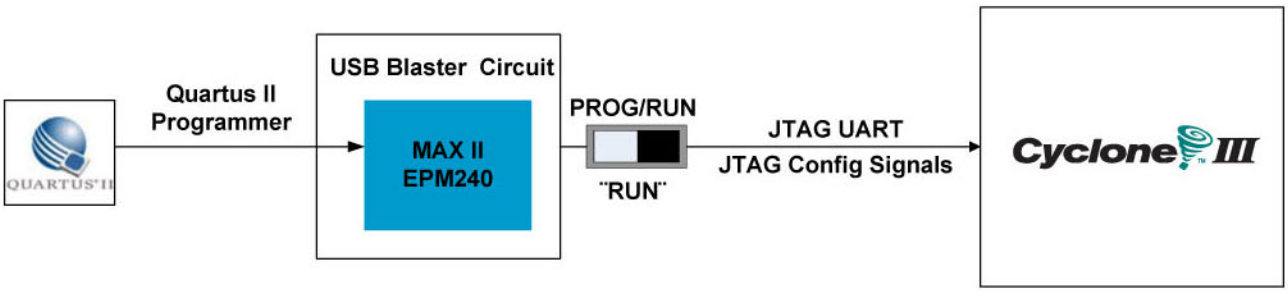

Figure 4-1. The JTAG configuration scheme

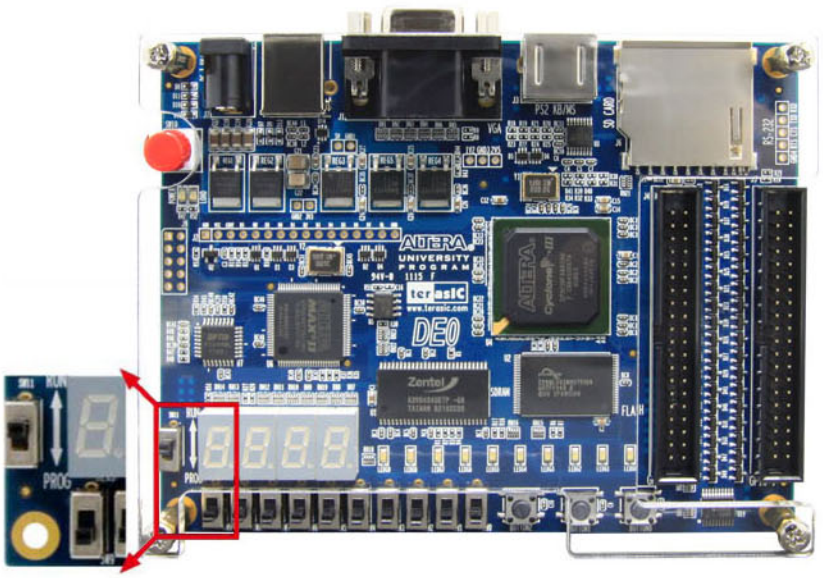

Figure 4-2. The RUN/PROG switch (SW11) is set in JTAG mode

Configuring the EPCS4 in AS Mode

Figure 4-3 illustrates the AS configuration set up. To download a configuration bit stream into the EPCS4 serial EEPROM device, perform the following steps:

- Ensure that power is applied to the DE0 board

- Connect the supplied USB cable to the USB Blaster port on the DE0 board (see Figure 2-1)
- Configure the JTAG programming circuit by setting the RUN/PROG switch (see Figure 4-4) to the PROG position.
- The EPCS4 chip can now be programmed by using the Quartus II Programmer module to select a configuration bit stream file with the *.pof* filename extension
- Once the programming operation is finished, set the RUN/PROG switch back to the RUN position and then reset the board by turning the power switch off and back on; this action causes the new configuration data in the EPCS4 device to be loaded into the FPGA chip.

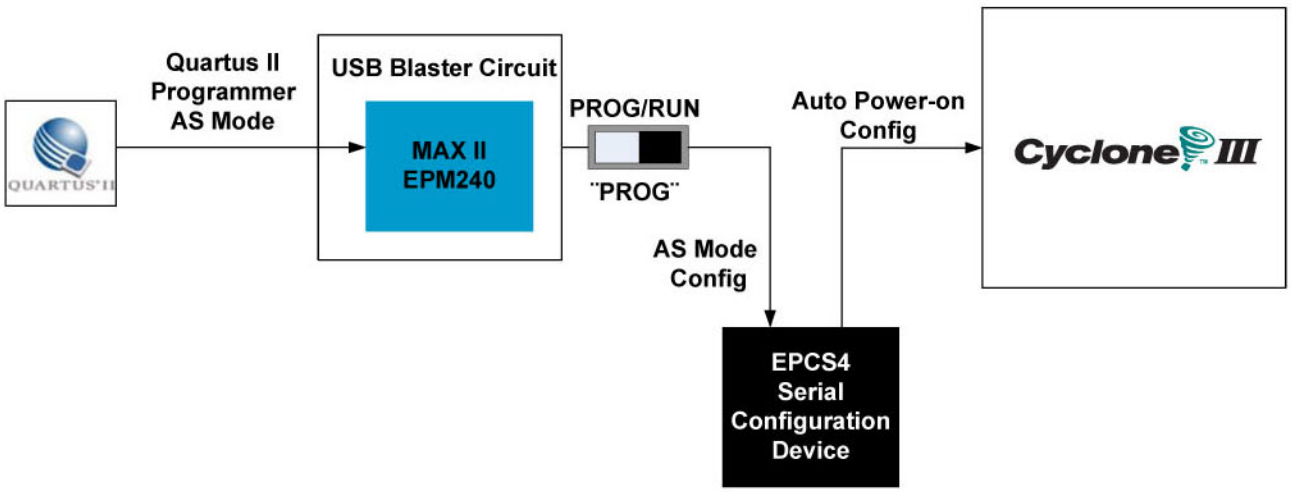

Figure 4-3. The AS configuration scheme

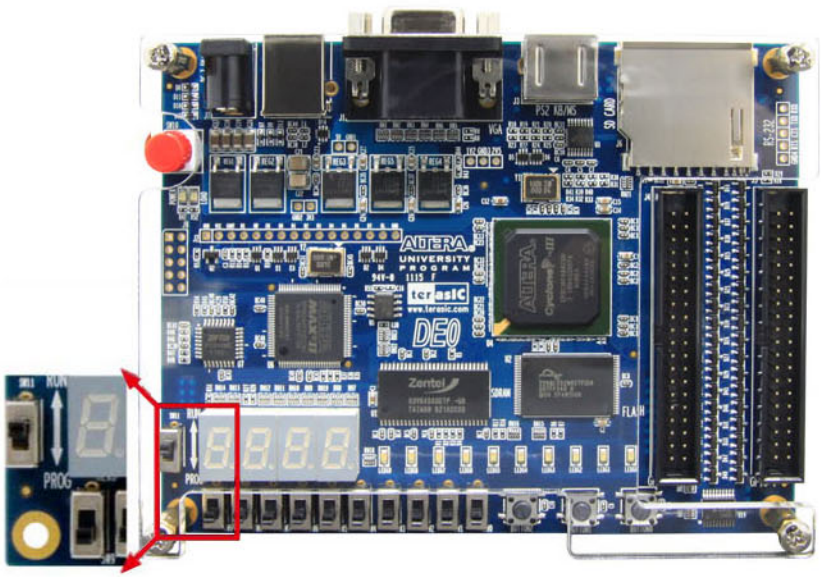

Figure 4-4. The RUN/PROG switch (SW11) is set in AS mode