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# DE0-Nano

## User Manual

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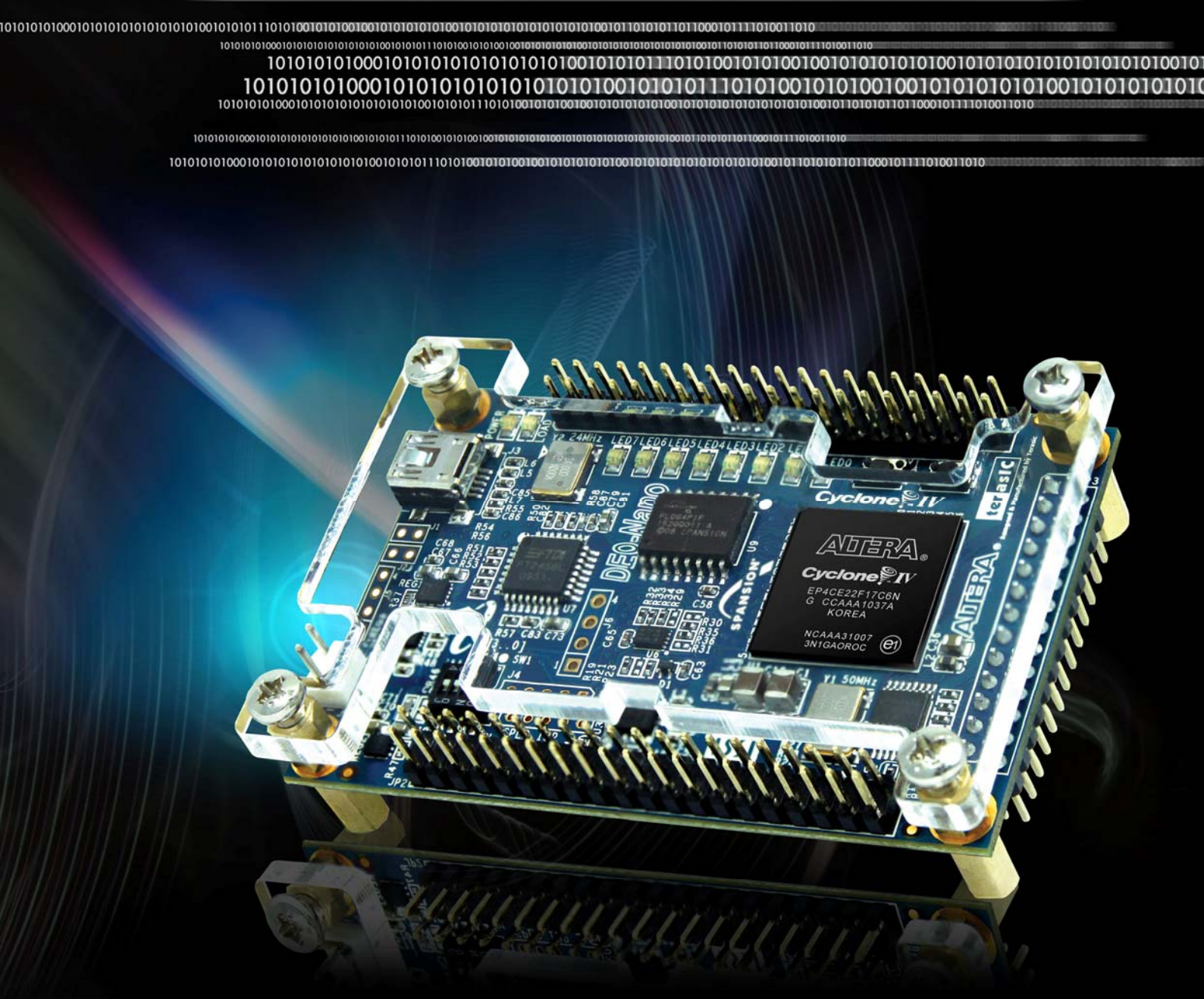


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# CONTENTS

# Chapter 1

# Introduction

The DE0-Nano board introduces a compact-sized FPGA development platform suited for to a wide range of portable design projects, such as robots and mobile projects.

The DE0-Nano is ideal for use with embedded soft processors—it features a powerful Altera Cyclone IV FPGA (with 22,320 logic elements), 32 MB of SDRAM, 2 Kb EEPROM, and a 64 Mb serial configuration memory device. For connecting to real-world sensors the DE0-Nano includes a National Semiconductor 8-channel 12-bit A/D converter, and it also features an Analog Devices 13-bit, 3-axis accelerometer device.

The DE0-Nano board includes a built-in USB Blaster for FPGA programming, and the board can be powered either from this USB port or by an external power source. The board includes expansion headers that can be used to attach various Terasic daughter cards or other devices, such as motors and actuators. Inputs and outputs include 2 pushbuttons, 8 user LEDs and a set of 4 dip-switches.

## 1.1 Features

Figure 1-1 shows a photograph of the DE0-Nano Board.

**Figure 1-1 The DE0-Nano Board**

The key features of the board are listed below:

- Featured device
  - Altera Cyclone® IV EP4CE22F17C6N FPGA
  - 153 maximum FPGA I/O pins

- Configuration status and set-up elements
  - On-board USB-Blaster circuit for programming
  - Spansion EPCS64

- Expansion header
  - Two 40-pin Headers (GPIOs) provide 72 I/O pins, 5V power pins, two 3.3V power pins and four ground pins

- Memory devices
  - 32MB SDRAM
  - 2Kb I2C EEPROM

- General user input/output
  - 8 green LEDs
  - 2 debounced pushbuttons
  - 4-position DIP switch

- G-Sensor
  - ADI ADXL345, 3-axis accelerometer with high resolution (13-bit)

- A/D Converter
  - NS ADC128S022, 8-Channel, 12-bit A/D Converter
  - 50 Ksps to 200 Ksps

- Clock system
  - On-board 50MHz clock oscillator

- Power Supply
  - USB Type mini-AB port (5V)
  - DC 5V pin for each GPIO header (2 DC 5V pins)
  - 2-pin external power header (3.6-5.7V)

## 1.2 About the KIT

The kit comes with the following contents:

- DE0-Nano board
- System CD-ROM.
- USB Cable

The system CD contains technical documents for the DE0-Nano board, which includes component datasheets, demonstrations, schematic, and user manual.

Figure 1-2 shows the photograph of the DE0-Nano kit contents.


**Figure 1-2 DE0-Nano kit package contents**

## 1.3 Getting Help

Here is information of how to get help if you encounter any problem:

- Terasic Technologies
- Tel: +886-3-575-0880
- Email: support@terasic.com

- Altera Corporation
- Email: university@altera.com

Chapter 2

# DE0-Nano Board Architecture

This chapter describes the architecture of the DE0-Nano board including block diagram and components.

## 2.1 Layout and Components

The picture of the DE0-Nano board is shown in Figure 2-1 and Figure 2-2. It depicts the layout of the board and indicates the locations of the connectors and key components.

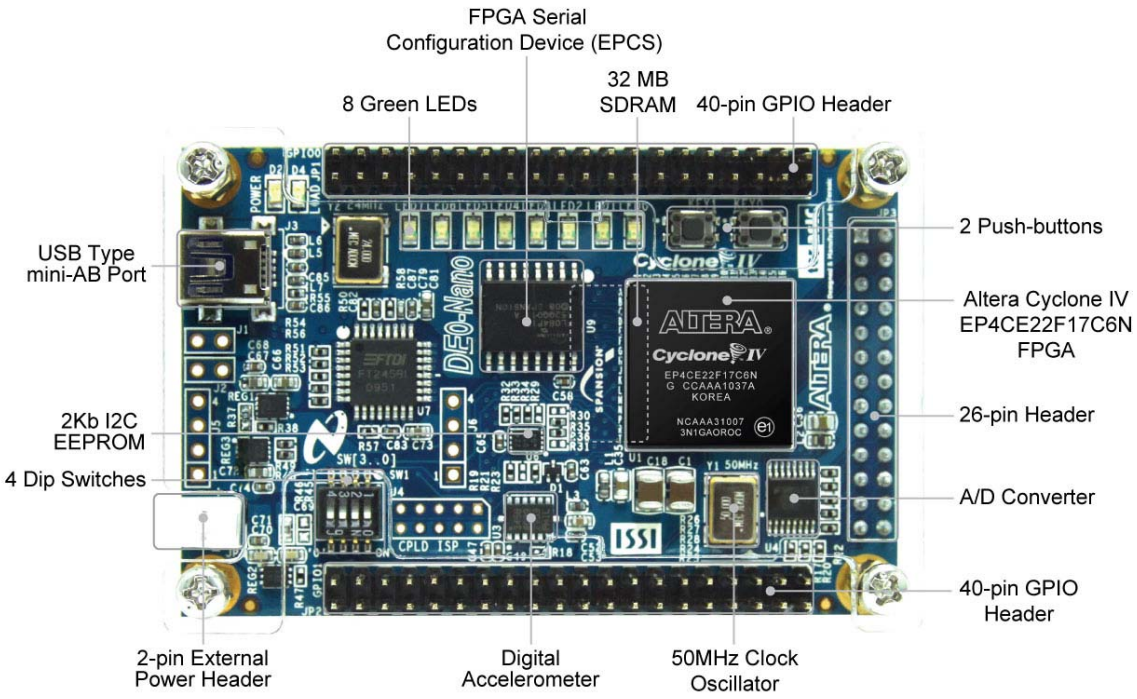


**Figure 2-1 The DE0-Nano Board PCB and component diagram (top view)**

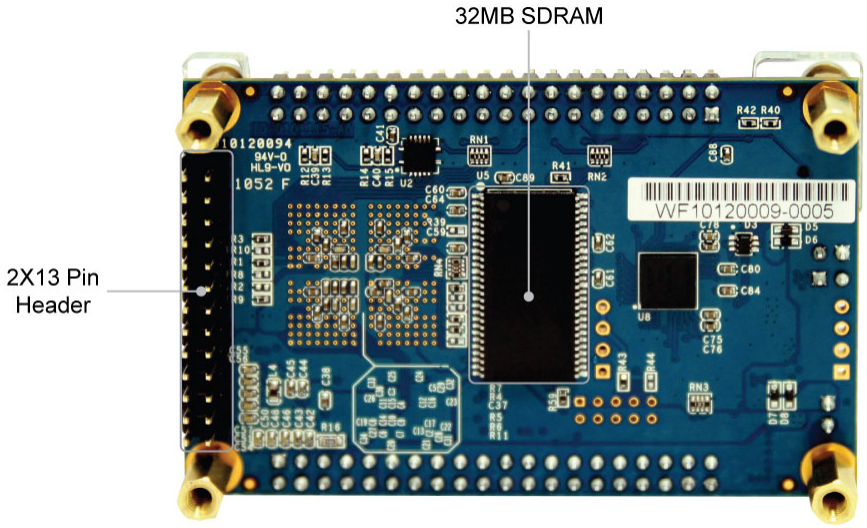


**Figure 2-2 The DE0-Nano Board PCB and component diagram (bottom view)**

## 2.2 Block Diagram of the DE0-Nano Board

Figure 2-3 shows the block diagram of the DE0-Nano board. To provide maximum flexibility for the user, all connections are made through the Cyclone IV FPGA device. Thus, the user can configure the FPGA to implement any system design.

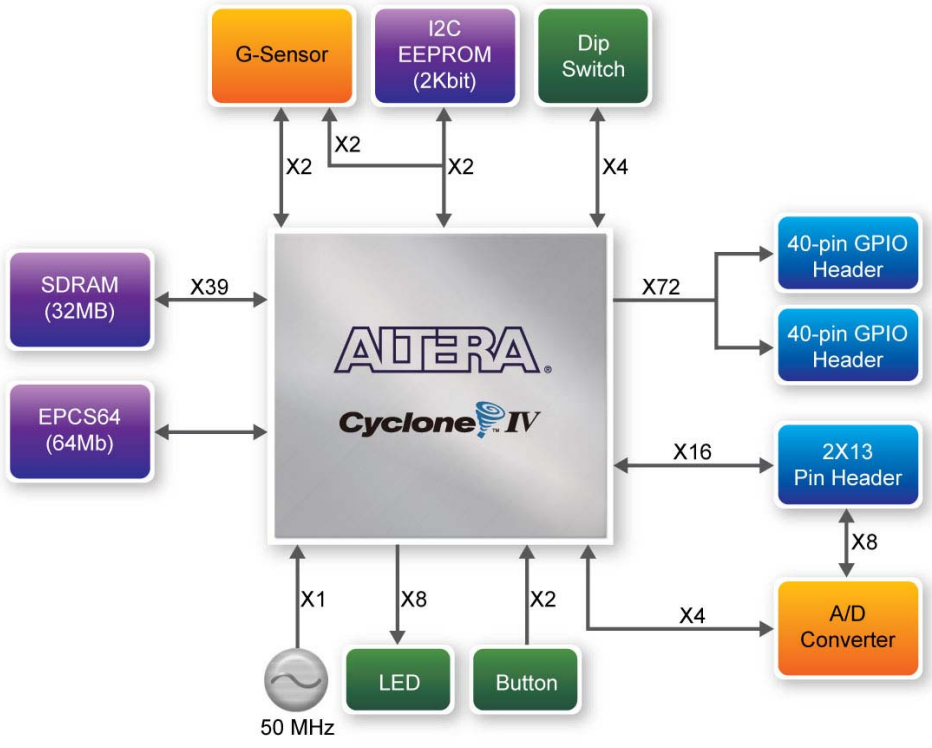


**Figure 2-3 Block diagram of DE0-Nano Board**

## 2.3 Power-up the DE0-Nano Board

The DE0-Nano board comes with a preloaded configuration bit stream to demonstrate some features of the board. This allows users to see quickly if the board is working properly. To power-up the board two options are available which are described below:

1. Connect a USB Mini-B cable between a USB (Type A) host port and the board. For communication between the host and the DE0-Nano board, it is necessary to install the Altera USB Blaster driver software.

2. Alternatively, users can power-up the DE0-Nano board by supplying 5V to the two DC +5 (VCC5) pins of the GPIO headers or supplying (3.6-5.7V) to the 2-pin header.

At this point you should observe flashing LEDs on the board.

Chapter 3

# Using the DE0-Nano Board

This chapter gives instructions for using the DE0-Nano board and describes in detail its components and connectors, along with the required pin assignments.

## 3.1 Configuring the Cyclone IV FPGA

The DE0-Nano board contains a Cyclone IV E FPGA which can be programmed using JTAG programming. This allows users to configure the FPGA with a specified design using Quartus II software. The programmed design will remain functional on the FPGA as long as the board is powered on, or until the device is reprogrammed. The configuration information will be lost when the power is turned off.

To download a configuration bit stream file using JTAG Programming into the Cyclone IV FPGA, perform the following steps:

1. Connect a USB Mini-B cable between a host computer and the DE0-Nano.
2. The FPGA can now be programmed through the Quartus II Programmer by selecting a configuration bit stream file with the .sof filename extension.

### ■ Configuring the Spansion EPCS64 device

The DE0-Nano board contains a Spansion EPCS64 serial configuration device. This device provides non-volatile storage of the configuration bit-stream, so that the information is retained even when the power supply to the DE0-Nano board is turned off. When the board's power is turned on, the configuration data in the EPCS64 device is automatically loaded into the Cyclone IV E FPGA.

The Cyclone IV E device supports in-system programming of a serial configuration device using the JTAG interface via the serial flash loader design. The serial flash loader is a bridge design for the Cyclone IV E device that uses its JTAG interface to access the EPCS .jic file and then uses the AS interface to program the EPCS device. **Figure 3-1** illustrates the programming method when adopting a serial flash loader solution. Chapter 9 of this document describes how to load a circuit to the serial configuration device.


**Figure 3-1 Programming a serial configuration device with serial flash loader solution**

## ■ JTAG Chain on DE0-Nano Board

The JTAG Chain on the DE0-Nano board is connected to a host computer using an on-board USB-blaster. The USB-blaster consists of a USB Mini-B connector, a FTDI USB 2.0 Controller, and an Altera MAX II CPLD.

Figure 3-2 illustrates the JTAG configuration setup.

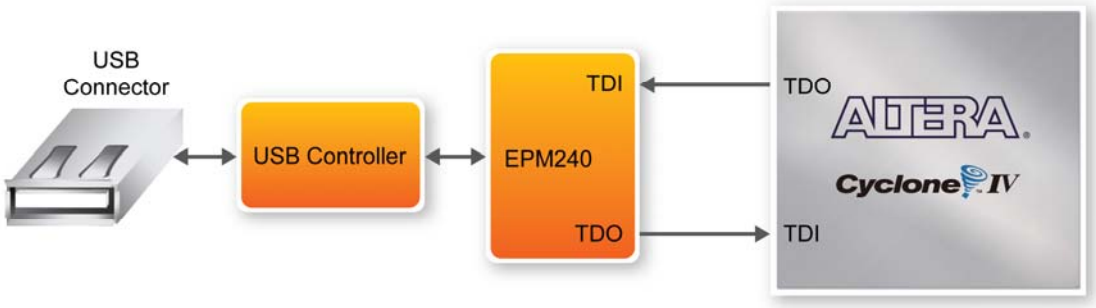


**Figure 3-2 JTAG Chain**

# 3.2 General User Input/Output

## ■ Pushbuttons

The DE0-Nano board contains two pushbuttons shown in Figure 3-3. Each pushbutton is debounced using a Schmitt Trigger circuit, as indicated in Figure 3-4. The two outputs called KEY0, and KEY1 of the Schmitt Trigger devices are connected directly to the Cyclone IV E FPGA. Each pushbutton provides a high logic level when it is not pressed, and provides a low logic level when pressed. Since the pushbuttons are debounced, they are appropriate for using as clock or reset inputs.

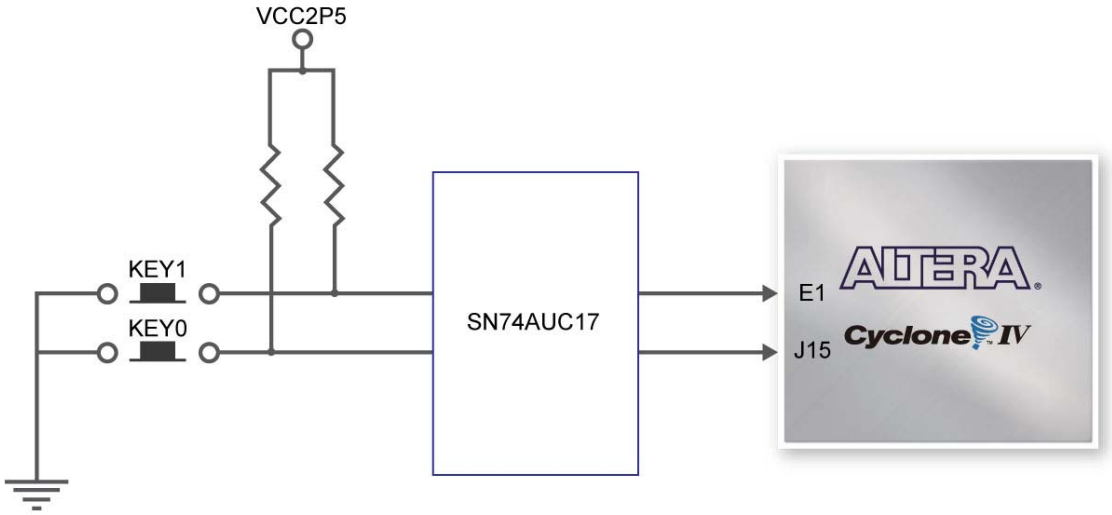


**Figure 3-3 Connections between the push-buttons and Cyclone IV FPGA**

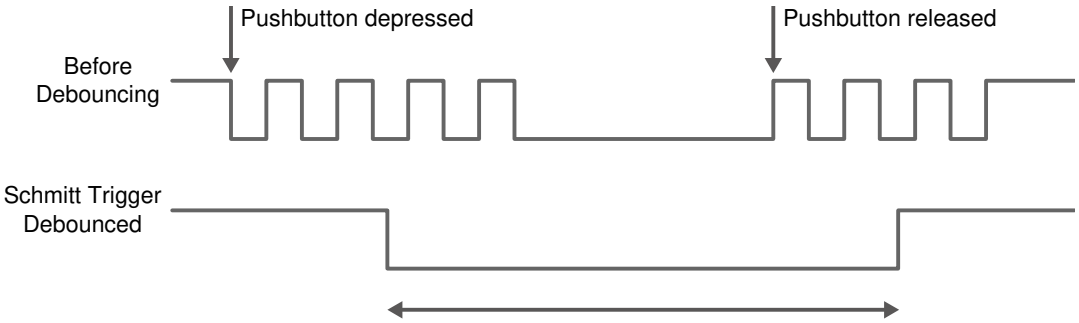


**Figure 3-4 Pushbuttons debouncing**

## ■ LEDs

There are 8 green user-controllable LEDs on the DE0-Nano board. The eight LEDs, which are presented in Figure 3-4, allow users to display status and debugging information. Each LED is driven directly by the Cyclone IV E FPGA. Each LED is driven directly by a pin on the Cyclone IV E FPGA; driving its associated pin to a high logic level turns the LED on, and driving the pin low turns it off.

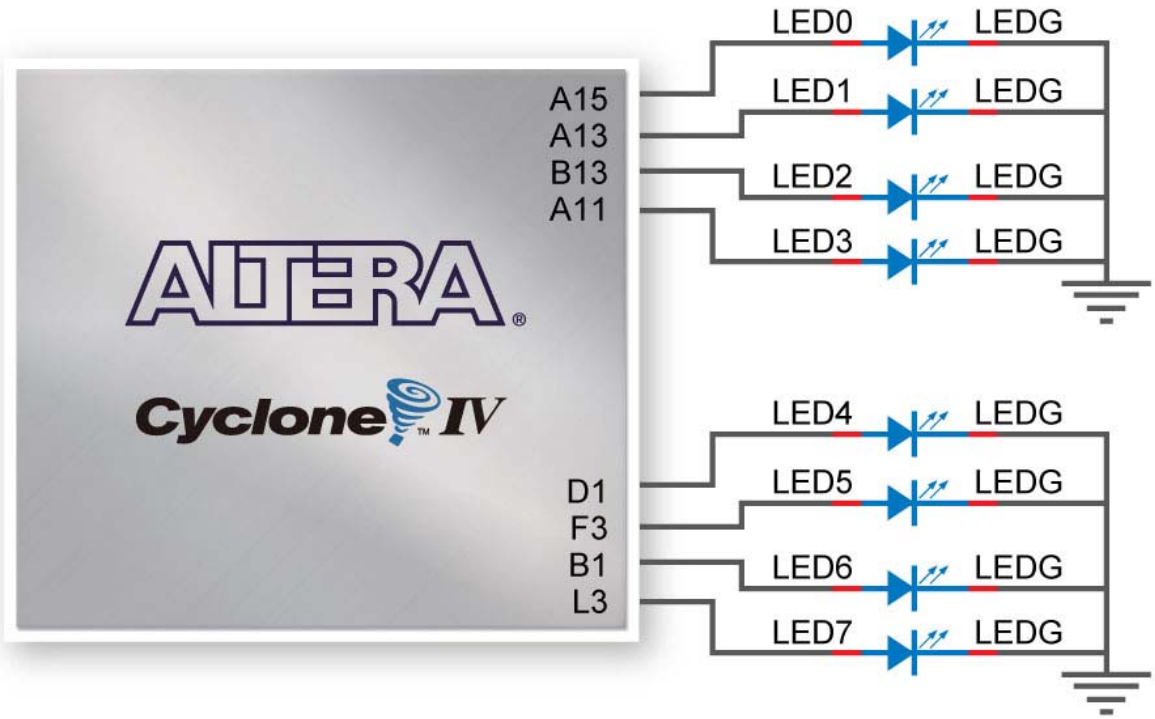


**Figure 3-5 Connections between the LEDs and Cyclone IV FPGA**

## ■ DIP Switch

The DE0-Nano board contains a 4 dip switches. A DIP switch provides, to the FPGA, a high logic level when it is in the DOWN position, and a low logic level when in the UPPER position.

**Table 3-1 Pin Assignments for Push-buttons**

| *Signal Name* | *FPGA Pin No.* | *Description* | *I/O Standard* |
|---|---|---|---|
| KEY[0] | PIN_J15 | Push-button[0] | 3.3V |
| KEY[1] | PIN_E1 | Push-button[1] | 3.3V |

**Table 3-2 Pin Assignments for LEDs**

| *Signal Name* | *FPGA Pin No.* | *Description* | *I/O Standard* |
|---|---|---|---|
| LED[0] | PIN_A15 | LED Green[0] | 3.3V |
| LED[1] | PIN_A13 | LED Green[1] | 3.3V |
| LED[2] | PIN_B13 | LED Green[2] | 3.3V |
| LED[3] | PIN_A11 | LED Green[3] | 3.3V |
| LED[4] | PIN_D1 | LED Green[4] | 3.3V |
| LED[5] | PIN_F3 | LED Green[5] | 3.3V |
| LED[6] | PIN_B1 | LED Green[6] | 3.3V |
| LED[7] | PIN_L3 | LED Green[7] | 3.3V |

Table 3-3 Pin Assignments for DIP Switches

| *Signal Name* | *FPGA Pin No.* | *Description* | *I/O Standard* |
|---|---|---|---|
| DIP Switch[0] | PIN_M1 | DIP Switch[0] | 3.3V |
| DIP Switch[1] | PIN_T8 | DIP Switch[1] | 3.3V |
| DIP Switch[2] | PIN_B9 | DIP Switch[2] | 3.3V |
| DIP Switch[3] | PIN_M15 | DIP Switch[3] | 3.3V |

## 3.3 SDRAM Memory

The board features a Synchronous Dynamic Random Access Memory (SDRAM) device providing 32MB with a 16-bit data lines connected to the FPGA. The chip uses 3.3V LVCMOS signaling standard. All signals are registered on the positive edge of the clock signal, DRAM_CLK. Connections between the FPGA and SDRAM chips are shown in Figure 3-6.

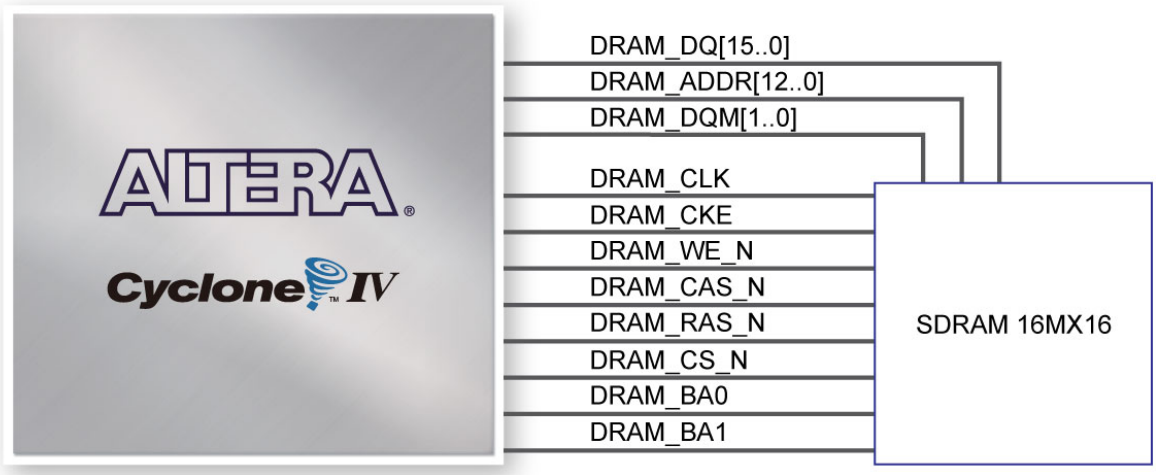


Figure 3-6 Connections between FPGA and SDRAM

Table 3-4 SDRAM Pin Assignments

| *Signal Name* | *FPGA Pin No.* | *Description* | *I/O Standard* |
|---|---|---|---|
| DRAM_ADDR[0] | PIN_P2 | SDRAM Address[0] | 3.3V |
| DRAM_ADDR[1] | PIN_N5 | SDRAM Address[1] | 3.3V |
| DRAM_ADDR[2] | PIN_N6 | SDRAM Address[2] | 3.3V |
| DRAM_ADDR[3] | PIN_M8 | SDRAM Address[3] | 3.3V |
| DRAM_ADDR[4] | PIN_P8 | SDRAM Address[4] | 3.3V |
| DRAM_ADDR[5] | PIN_T7 | SDRAM Address[5] | 3.3V |
| DRAM_ADDR[6] | PIN_N8 | SDRAM Address[6] | 3.3V |
| DRAM_ADDR[7] | PIN_T6 | SDRAM Address[7] | 3.3V |
| DRAM_ADDR[8] | PIN_R1 | SDRAM Address[8] | 3.3V |
| DRAM_ADDR[9] | PIN_P1 | SDRAM Address[9] | 3.3V |
| DRAM_ADDR[10] | PIN_N2 | SDRAM Address[10] | 3.3V |
| DRAM_ADDR[11] | PIN_N1 | SDRAM Address[11] | 3.3V |

| | | | |
|---|---|---|---|
| DRAM_ADDR[12] | PIN_L4 | SDRAM Address[12] | 3.3V |
| DRAM_DQ[0] | PIN_G2 | SDRAM Data[0] | 3.3V |
| DRAM_DQ[1] | PIN_G1 | SDRAM Data[1] | 3.3V |
| DRAM_DQ[2] | PIN_L8 | SDRAM Data[2] | 3.3V |
| DRAM_DQ[3] | PIN_K5 | SDRAM Data[3] | 3.3V |
| DRAM_DQ[4] | PIN_K2 | SDRAM Data[4] | 3.3V |
| DRAM_DQ[5] | PIN_J2 | SDRAM Data[5] | 3.3V |
| DRAM_DQ[6] | PIN_J1 | SDRAM Data[6] | 3.3V |
| DRAM_DQ[7] | PIN_R7 | SDRAM Data[7] | 3.3V |
| DRAM_DQ[8] | PIN_T4 | SDRAM Data[8] | 3.3V |
| DRAM_DQ[9] | PIN_T2 | SDRAM Data[9] | 3.3V |
| DRAM_DQ[10] | PIN_T3 | SDRAM Data[10] | 3.3V |
| DRAM_DQ[11] | PIN_R3 | SDRAM Data[11] | 3.3V |
| DRAM_DQ[12] | PIN_R5 | SDRAM Data[12] | 3.3V |
| DRAM_DQ[13] | PIN_P3 | SDRAM Data[13] | 3.3V |
| DRAM_DQ[14] | PIN_N3 | SDRAM Data[14] | 3.3V |
| DRAM_DQ[15] | PIN_K1 | SDRAM Data[15] | 3.3V |
| DRAM_BA[0] | PIN_M7 | SDRAM Bank Address[0] | 3.3V |
| DRAM_BA[1] | PIN_M6 | SDRAM Bank Address[1] | 3.3V |
| DRAM_DQM[0] | PIN_R6 | SDRAM byte Data Mask[0] | 3.3V |
| DRAM_DQM[1] | PIN_T5 | SDRAM byte Data Mask[1] | 3.3V |
| DRAM_RAS_N | PIN_L2 | SDRAM Row Address Strobe | 3.3V |
| DRAM_CAS_N | PIN_L1 | SDRAM Column Address Strobe | 3.3V |
| DRAM_CKE | PIN_L7 | SDRAM Clock Enable | 3.3V |
| DRAM_CLK | PIN_R4 | SDRAM Clock | 3.3V |
| DRAM_WE_N | PIN_C2 | SDRAM Write Enable | 3.3V |
| DRAM_CS_N | PIN_P6 | SDRAM Chip Select | 3.3V |

## 3.4 I2C Serial EEPROM

The DE0-Nano contains a 2Kbit Electrically Erasable PROM (EEPROM). The EEPROM is configured through a 2-wire I2C serial interface. The device is organized as one block of 256 x 8-bit memory. The I2C write and read address are 0xA0 and 0xA1, respectively. **Figure 3-7** illustrates its connections with the Cyclone IV FPGA.

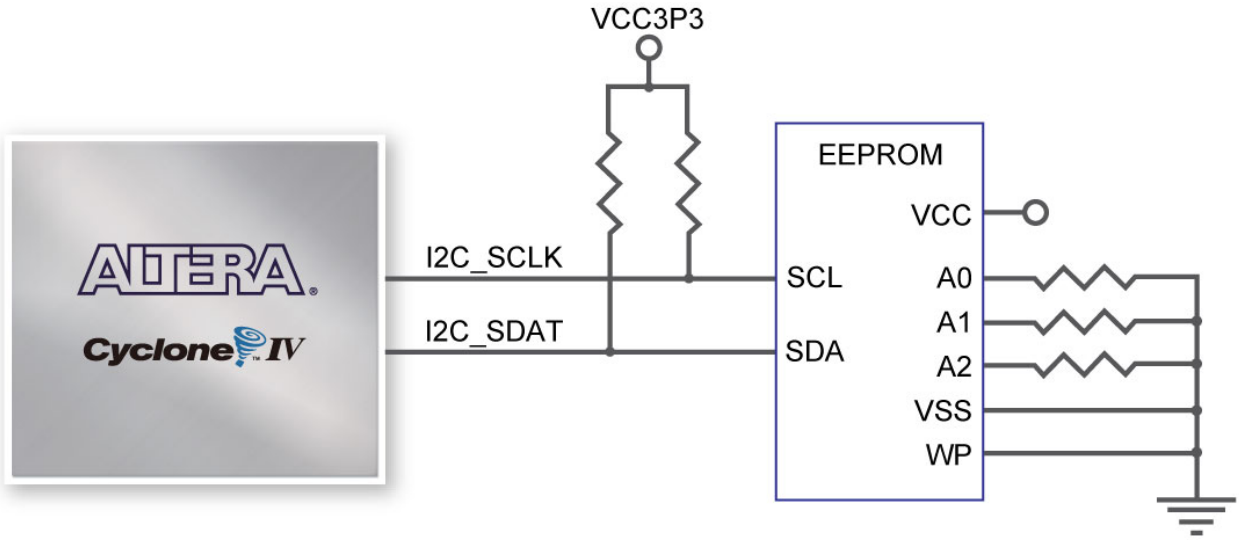


**Figure 3-7 Connections between FPGA and EEPROM**

**Table 3-5 Pin Assignments for I2C Serial EEPROM**

| *Signal Name* | *FPGA Pin No.* | *Description* | *I/O Standard* |
|---|---|---|---|
| I2C_SCLK | PIN_F2 | EEPROM clock | 3.3V |
| I2C_SDAT | PIN_F1 | EEPROM data | 3.3V |

## 3.5 Expansion Headers

The DE0-Nano board provides two 40-pin expansion headers. Each header connects directly to 36 pins of the Cyclone IV E FPGA, and also provides DC +5V (VCC5), DC +3.3V (VCC33), and two GND pins. Figure 3-8 shows the I/O distribution of the GPIO connectors.

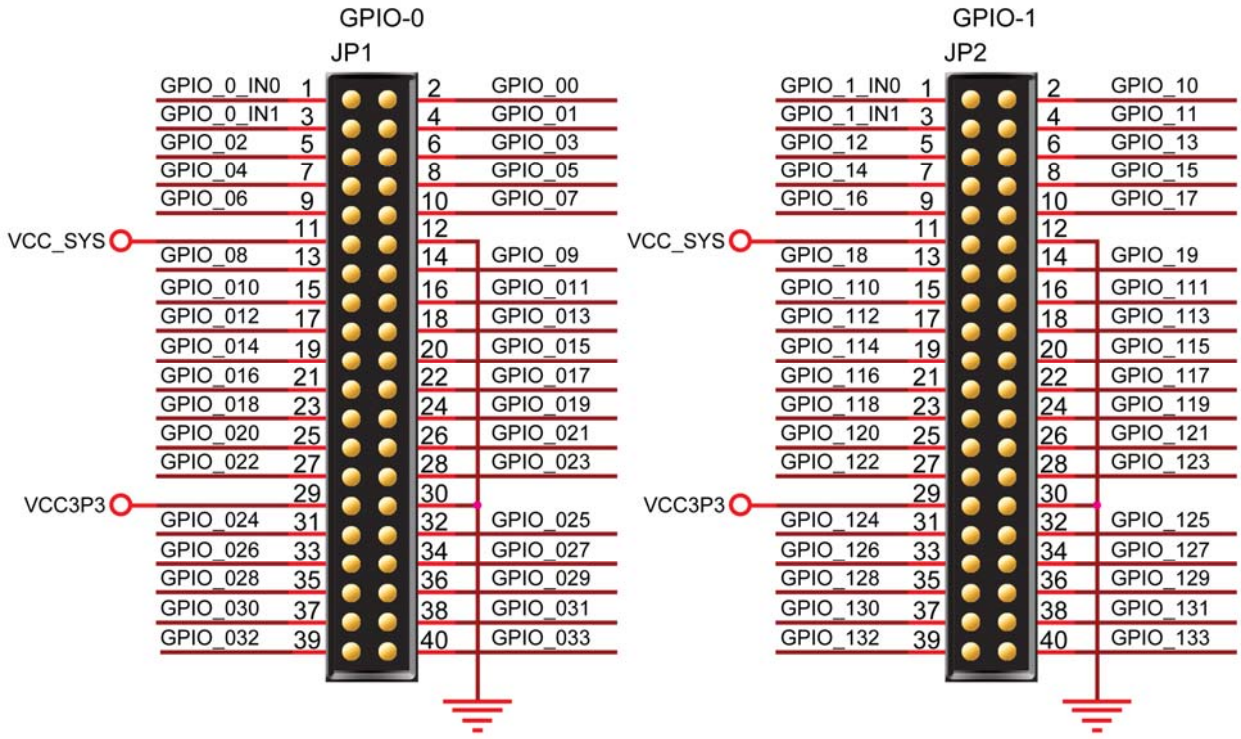


**Figure 3-8 Pin arrangement of the GPIO expansion headers**

The pictures below indicate the pin 1 location of the expansion headers.

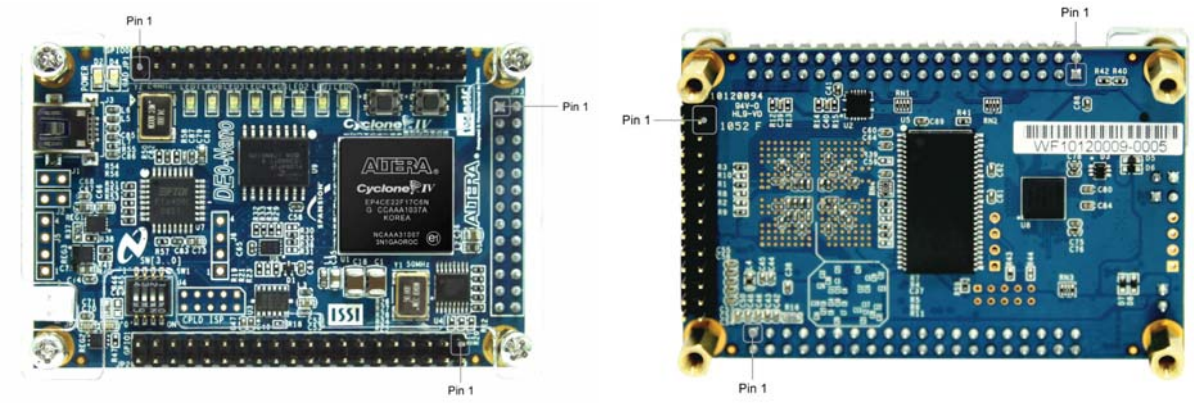


**Figure 3-9 Pin1 locations of the GPIO expansion headers**

**Table 3-6 GPIO-0 Pin Assignments**

| *Signal Name* | *FPGA Pin No.* | *Description* | *I/O Standard* |
|---|---|---|---|
| GPIO_0_IN0 | PIN_A8 | GPIO Connection DATA | 3.3V |
| GPIO_00 | PIN_D3 | GPIO Connection DATA | 3.3V |
| GPIO_0_IN1 | PIN_B8 | GPIO Connection DATA | 3.3V |
| GPIO_01 | PIN_C3 | GPIO Connection DATA | 3.3V |
| GPIO_02 | PIN_A2 | GPIO Connection DATA | 3.3V |

| | | | |
|---|---|---|---|
| GPIO_03 | PIN_A3 | GPIO Connection DATA | 3.3V |
| GPIO_04 | PIN_B3 | GPIO Connection DATA | 3.3V |
| GPIO_05 | PIN_B4 | GPIO Connection DATA | 3.3V |
| GPIO_06 | PIN_A4 | GPIO Connection DATA | 3.3V |
| GPIO_07 | PIN_B5 | GPIO Connection DATA | 3.3V |
| GPIO_08 | PIN_A5 | GPIO Connection DATA | 3.3V |
| GPIO_09 | PIN_D5 | GPIO Connection DATA | 3.3V |
| GPIO_010 | PIN_B6 | GPIO Connection DATA | 3.3V |
| GPIO_011 | PIN_A6 | GPIO Connection DATA | 3.3V |
| GPIO_012 | PIN_B7 | GPIO Connection DATA | 3.3V |
| GPIO_013 | PIN_D6 | GPIO Connection DATA | 3.3V |
| GPIO_014 | PIN_A7 | GPIO Connection DATA | 3.3V |
| GPIO_015 | PIN_C6 | GPIO Connection DATA | 3.3V |
| GPIO_016 | PIN_C8 | GPIO Connection DATA | 3.3V |
| GPIO_017 | PIN_E6 | GPIO Connection DATA | 3.3V |
| GPIO_018 | PIN_E7 | GPIO Connection DATA | 3.3V |
| GPIO_019 | PIN_D8 | GPIO Connection DATA | 3.3V |
| GPIO_020 | PIN_E8 | GPIO Connection DATA | 3.3V |
| GPIO_021 | PIN_F8 | GPIO Connection DATA | 3.3V |
| GPIO_022 | PIN_F9 | GPIO Connection DATA | 3.3V |
| GPIO_023 | PIN_E9 | GPIO Connection DATA | 3.3V |
| GPIO_024 | PIN_C9 | GPIO Connection DATA | 3.3V |
| GPIO_025 | PIN_D9 | GPIO Connection DATA | 3.3V |
| GPIO_026 | PIN_E11 | GPIO Connection DATA | 3.3V |
| GPIO_027 | PIN_E10 | GPIO Connection DATA | 3.3V |
| GPIO_028 | PIN_C11 | GPIO Connection DATA | 3.3V |
| GPIO_029 | PIN_B11 | GPIO Connection DATA | 3.3V |
| GPIO_030 | PIN_A12 | GPIO Connection DATA | 3.3V |
| GPIO_031 | PIN_D11 | GPIO Connection DATA | 3.3V |
| GPIO_032 | PIN_D12 | GPIO Connection DATA | 3.3V |
| GPIO_033 | PIN_B12 | GPIO Connection DATA | 3.3V |

**Table 3-7 GPIO-1 Pin Assignments**

| *Signal Name* | *FPGA Pin No.* | *Description* | *I/O Standard* |
|---|---|---|---|
| GPIO_1_IN0 | PIN_T9 | GPIO Connection DATA | 3.3V |
| GPIO_10 | PIN_F13 | GPIO Connection DATA | 3.3V |
| GPIO_1_IN1 | PIN_R9 | GPIO Connection DATA | 3.3V |
| GPIO_11 | PIN_T15 | GPIO Connection DATA | 3.3V |
| GPIO_12 | PIN_T14 | GPIO Connection DATA | 3.3V |
| GPIO_13 | PIN_T13 | GPIO Connection DATA | 3.3V |
| GPIO_14 | PIN_R13 | GPIO Connection DATA | 3.3V |
| GPIO_15 | PIN_T12 | GPIO Connection DATA | 3.3V |
| GPIO_16 | PIN_R12 | GPIO Connection DATA | 3.3V |

| | | | |
|---|---|---|---|
| GPIO_17 | PIN_T11 | GPIO Connection DATA | 3.3V |
| GPIO_18 | PIN_T10 | GPIO Connection DATA | 3.3V |
| GPIO_19 | PIN_R11 | GPIO Connection DATA | 3.3V |
| GPIO_110 | PIN_P11 | GPIO Connection DATA | 3.3V |
| GPIO_111 | PIN_R10 | GPIO Connection DATA | 3.3V |
| GPIO_112 | PIN_N12 | GPIO Connection DATA | 3.3V |
| GPIO_113 | PIN_P9 | GPIO Connection DATA | 3.3V |
| GPIO_114 | PIN_N9 | GPIO Connection DATA | 3.3V |
| GPIO_115 | PIN_N11 | GPIO Connection DATA | 3.3V |
| GPIO_116 | PIN_L16 | GPIO Connection DATA | 3.3V |
| GPIO_117 | PIN_K16 | GPIO Connection DATA | 3.3V |
| GPIO_118 | PIN_R16 | GPIO Connection DATA | 3.3V |
| GPIO_119 | PIN_L15 | GPIO Connection DATA | 3.3V |
| GPIO_120 | PIN_P15 | GPIO Connection DATA | 3.3V |
| GPIO_121 | PIN_P16 | GPIO Connection DATA | 3.3V |
| GPIO_122 | PIN_R14 | GPIO Connection DATA | 3.3V |
| GPIO_123 | PIN_N16 | GPIO Connection DATA | 3.3V |
| GPIO_124 | PIN_N15 | GPIO Connection DATA | 3.3V |
| GPIO_125 | PIN_P14 | GPIO Connection DATA | 3.3V |
| GPIO_126 | PIN_L14 | GPIO Connection DATA | 3.3V |
| GPIO_127 | PIN_N14 | GPIO Connection DATA | 3.3V |
| GPIO_128 | PIN_M10 | GPIO Connection DATA | 3.3V |
| GPIO_129 | PIN_L13 | GPIO Connection DATA | 3.3V |
| GPIO_130 | PIN_J16 | GPIO Connection DATA | 3.3V |
| GPIO_131 | PIN_K15 | GPIO Connection DATA | 3.3V |
| GPIO_132 | PIN_J13 | GPIO Connection DATA | 3.3V |
| GPIO_133 | PIN_J14 | GPIO Connection DATA | 3.3V |

## 3.6 A/D Converter and 2x13 Header

The DE0-Nano contains an ADC128S022 lower power, eight-channel CMOS 12-bit analog-to-digital converter. This A-to-D provides conversion throughput rates of 50 ksps to 200 ksps. It can be configured to accept up to eight input signals at inputs IN0 through IN7. This eight input signals are connected to the 2x13 header, as shown in Figure 3-10. The remaining I/Os of the 2x13 header are a DC +3.3V (VCC33), a GND and 13 pins, which are connect directly to the Cyclone IV E device.

For more detailed information on the A/D converter chip, please refer to its datasheet which is available on manufacturer's website or under the /datasheet folder of the system CD.

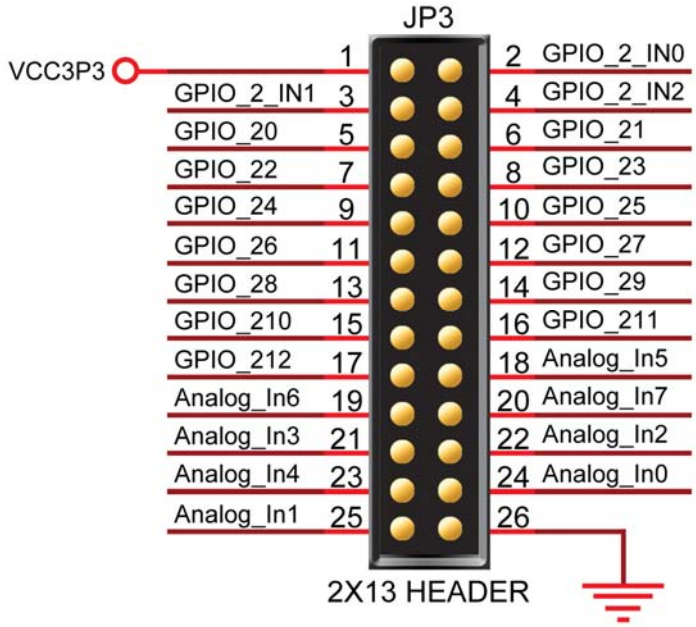


**Figure 3-10 Pin distribution of the 2x13 Header**

Figure 3-11 shows the connections on the 2x13 header, A/D converter and Cyclone IV device.

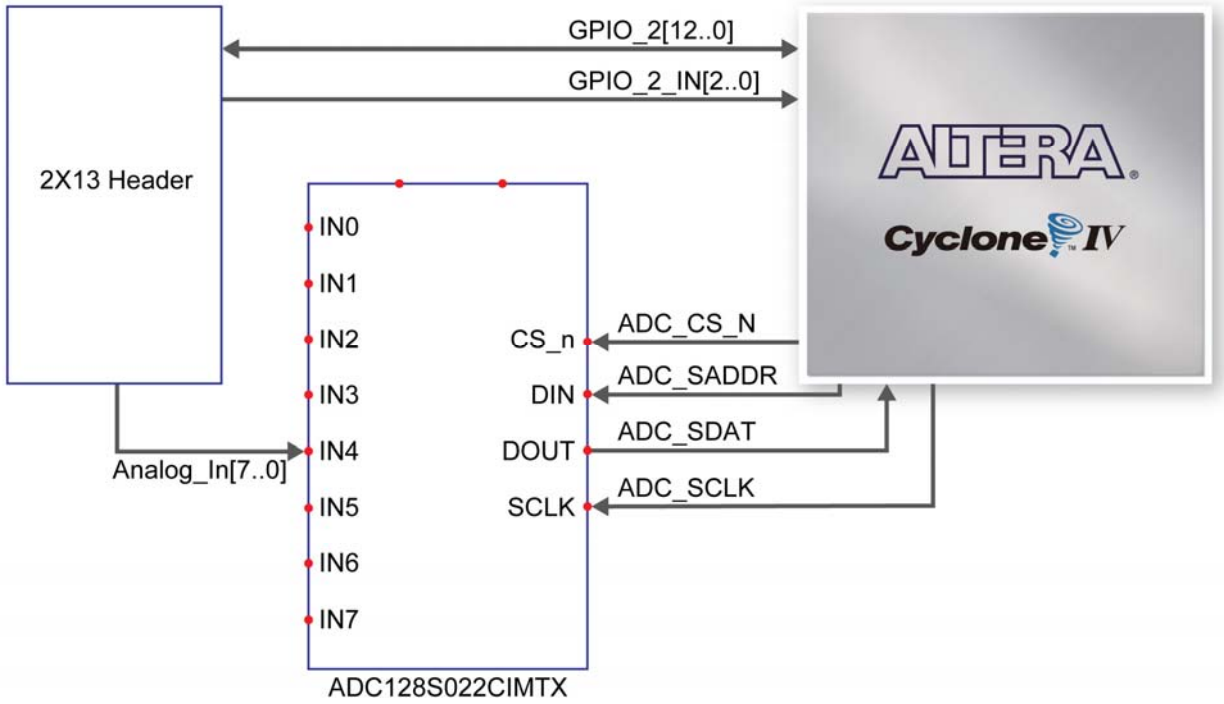


**Figure 3-11 Wiring for 2x13 header and A/D converter**

The pictures below indicate the pin 1 location of the 2x13 header.

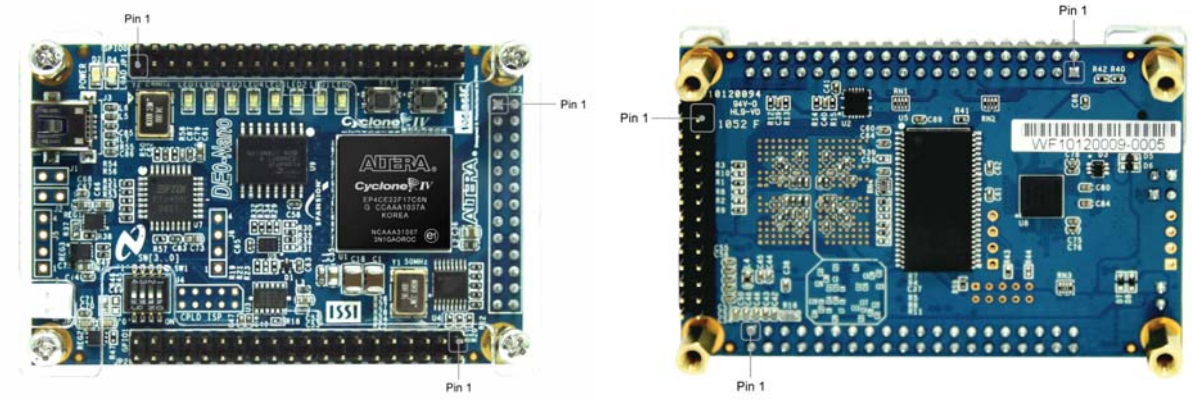


**Figure 3-12 Pin1 locations of the 2x13 header**

**Table 3-8 Pin Assignments for 2x13 Header**

| *Signal Name* | *FPGA Pin No.* | *Description* | *I/O Standard* |
|---|---|---|---|
| GPIO_2[0] | PIN_A14 | GPIO Connection DATA[0] | 3.3V |
| GPIO_2[1] | PIN_B16 | GPIO Connection DATA[1] | 3.3V |
| GPIO_2[2] | PIN_C14 | GPIO Connection DATA[2] | 3.3V |
| GPIO_2[3] | PIN_C16 | GPIO Connection DATA[3] | 3.3V |
| GPIO_2[4] | PIN_C15 | GPIO Connection DATA[4] | 3.3V |
| GPIO_2[5] | PIN_D16 | GPIO Connection DATA[5] | 3.3V |
| GPIO_2[6] | PIN_D15 | GPIO Connection DATA[6] | 3.3V |
| GPIO_2[7] | PIN_D14 | GPIO Connection DATA[7] | 3.3V |
| GPIO_2[8] | PIN_F15 | GPIO Connection DATA[8] | 3.3V |
| GPIO_2[9] | PIN_F16 | GPIO Connection DATA[9] | 3.3V |
| GPIO_2[10] | PIN_F14 | GPIO Connection DATA[10] | 3.3V |
| GPIO_2[11] | PIN_G16 | GPIO Connection DATA[11] | 3.3V |
| GPIO_2[12] | PIN_G15 | GPIO Connection DATA[12] | 3.3V |
| GPIO_2_IN[0] | PIN_E15 | GPIO Input | 3.3V |
| GPIO_2_IN[1] | PIN_E16 | GPIO Input | 3.3V |
| GPIO_2_IN[2] | PIN_M16 | GPIO Input | 3.3V |

**Table 3-9 Pin Assignments for ADC**

| *Signal Name* | *FPGA Pin No.* | *Description* | *I/O Standard* |
|---|---|---|---|
| ADC_CS_N | PIN_A10 | Chip select | 3.3V |
| ADC_SADDR | PIN_B10 | Digital data input | 3.3V |
| ADC_SDAT | PIN_A9 | Digital data output | 3.3V |
| ADC_SCLK | PIN_B14 | Digital clock input | 3.3V |

## 3.7 Digital Accelerometer

The ADXL345 is a small, thin, ultralow power, 3-axis accelerometer with high resolution measurement. This digital accelerometer can be accessed through a SPI 3-wire digital interface or I2C 2-wire digital interface. Main applications include medical instrumentation, industrial instrumentation, personal electronic aid and hard disk drive protection etc. Some of the key features of this device are listed below. For more detailed information, please refer to its datasheet which is available on manufacturer's website or under the /datasheet folder of the system CD.

- Up to 13-bit resolution at +/- 16g
- SPI (3- wire) or I2C (2-wire) digital interface
- Flexible interrupts modes

Figure 3-13 shows the connections between the ADXL345 and the Cyclone IV E device.

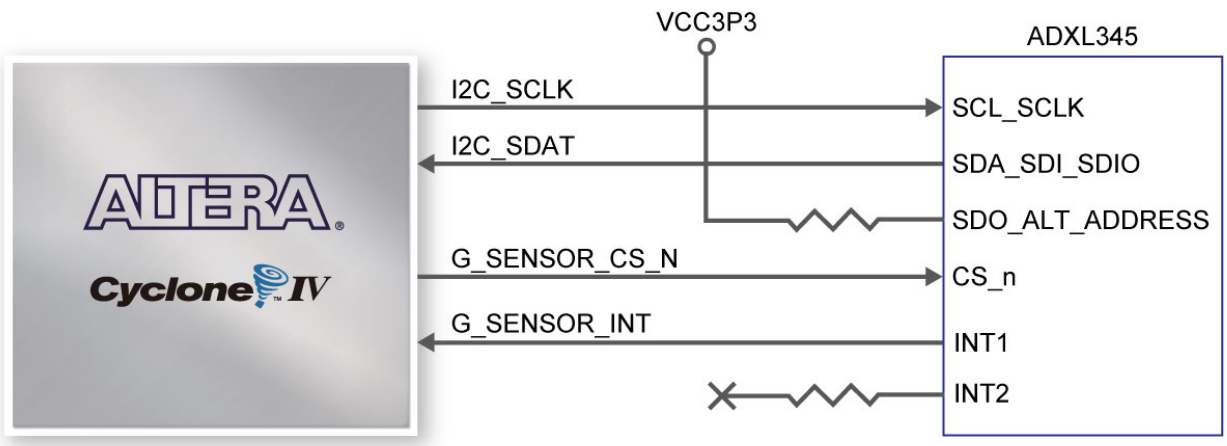


**Figure 3-13 Wiring between the ADXL345 and the Cyclone IV E device**

**Table 3-10 Pin Assignments for Digital Accelerometer**

| *Signal Name* | *FPGA Pin No.* | *Description* | *I/O Standard* |
|---|---|---|---|
| I2C_SCLK | PIN_F2 | EEPROM clock | 3.3V |
| I2C_SDAT | PIN_F1 | EEPROM data | 3.3V |
| G_SENSOR_INT | PIN_M2 | G_Sensor Interrupt | 3.3V |
| G_SENSOR_CS_N | PIN_G5 | G_Sensor chip select | 3.3V |

## 3.8 Clock Circuitry

The DE0-Nano board includes a 50 MHz oscillator. The oscillator is connected directly to a dedicated clock input pin of the Cyclone IV E FPGA. The 50MHz clock input can be used as a source clock to drive the phase lock loops (PLL) circuit. The clock distribution on the DE0-Nano board is shown in Figure 3-14.


**Figure 3-14 Block diagram of the clock distribution**

## 3.9 Power Supply

The DE0-Nano board's power is provided through the USB 5V power, the 5V VCC pins on the two 40-pin headers or the 2-pin power header. The DC voltage is then stepped down to various required voltages. For portable project applications, connect a battery power supply (3.6~5.7V) to the 2-pin external power header shown in Figure 3-15.

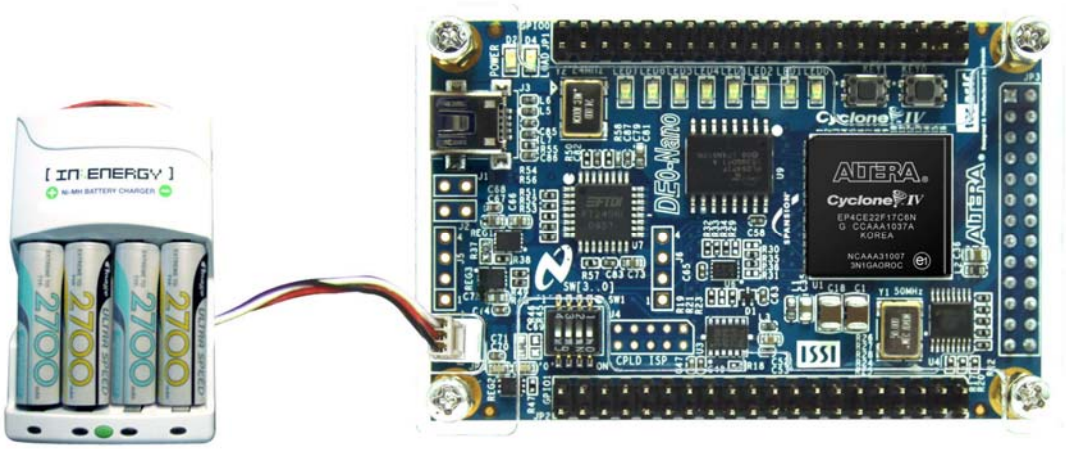


**Figure 3-15 Portable Battery Connection**

## ■ Power Distribution System

Figure 3-16 shows the power distribution system on the DE0-Nano board.

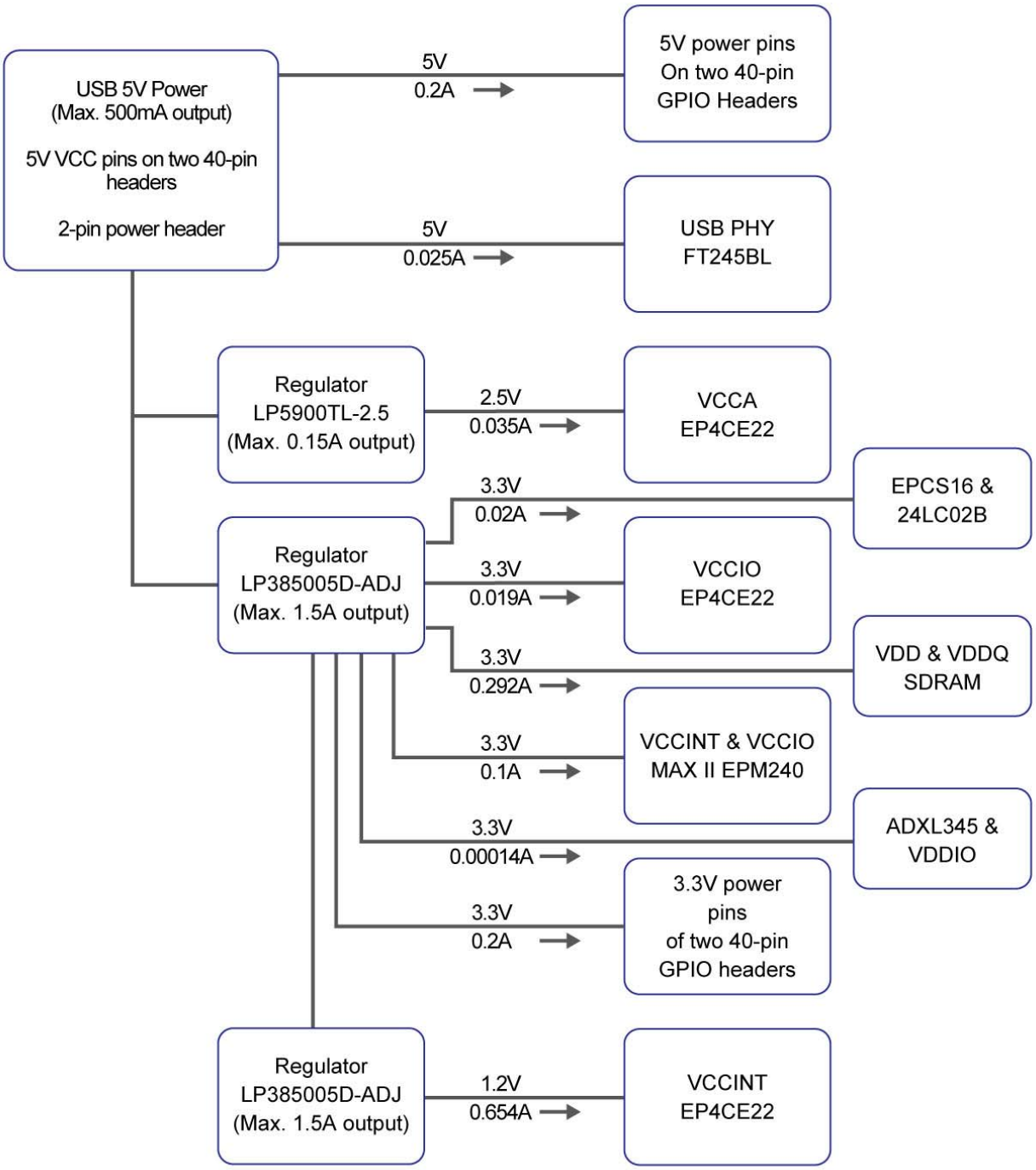


**Figure 3-16 DE0-Nano Power Distribution System**

Chapter 4

# DE0-Nano Control Panel

The DE0-Nano board comes with a Control Panel facility that allows users to access various components on the board from a host computer. The host computer communicates with the board through a USB connection. The facility can be used to verify the functionality of components on the board or be used as a debug tool while developing RTL code.

This chapter first presents some basic functions of the Control Panel, then describes its structure in block diagram form, and finally describes its capabilities.

## 4.1 Control Panel Setup

The Control Panel Software Utility is located in the directory *"tools/DE0_NANO_ControlPanel"* in the **DE0-Nano System CD**. It's free of installation, just copy the whole folder to your host computer and launch the control panel by executing the "DE0_NANO_ControlPanel.exe".

When Control Panel starts it will attempt to download a configuration file onto the DE0-Nano board. The configuration file contains a design that communicates with the peripheral devices on the board that are attached to the FPGA device. Perform the following steps to ensure that the control panel starts up successfully:

1. Make sure Quartus II 10.0 or later version is installed successfully on your PC.
2. Connect a USB A to Mini-B cable to a USB (Type A) host port and to the board.
3. Start the executable DE0_NANO_ControlPanel.exe on the host computer. The Control Panel user interface shown in **Figure 4-1** will appear.
5. The DE0_NANO_ControlPanel.sof bit stream is loaded automatically as soon as the DE0_NANO_ControlPanel.exe is launched.
6. In case the connection is disconnected, click on CONNECT where the .sof will be re-loaded onto the board.

*Note: the Control Panel will occupy the USB port until you choose to close the program or disconnect it from the board by clicking the Disconnect button. While the Control Panel is connected to the board, you will be unable to use Quartus II to download a configuration file into the FPGA.*