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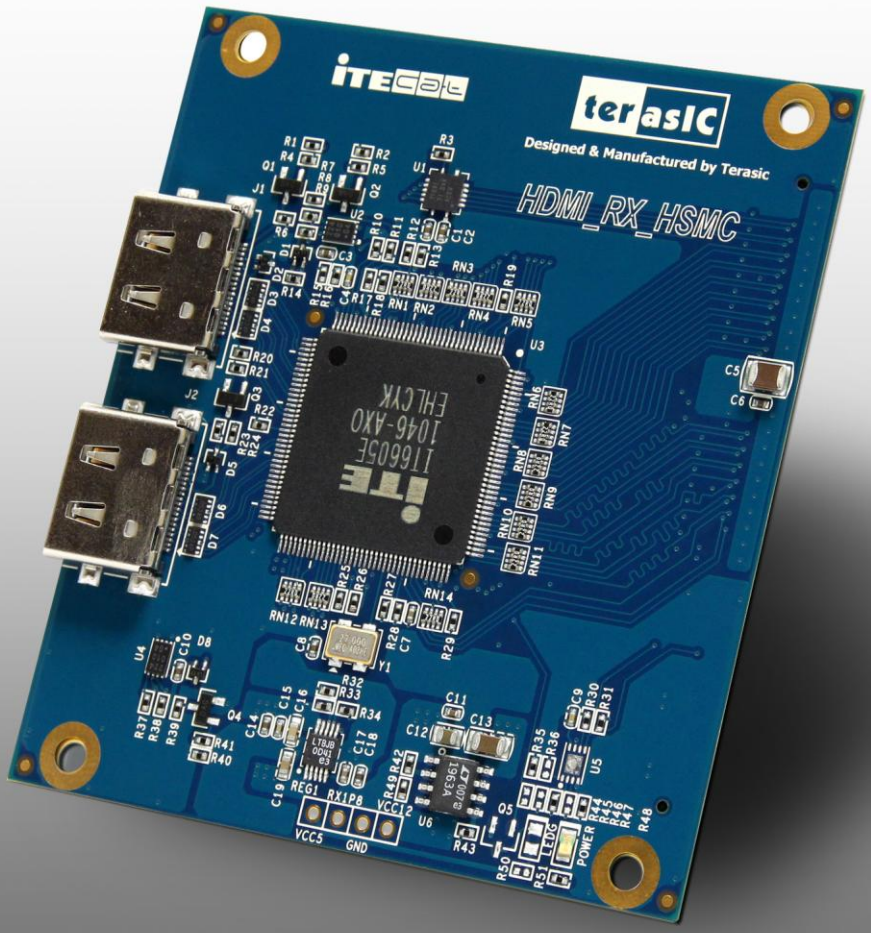
HDMI_RX_HSMC

Terasic HDMI Video Receiver Daughter Board

User Manual



CONTENTS

Chapter 1

Introduction

HDMI_RX_HSMC is a HDMI receiver daughter board with HSMC (High Speed Mezzanine Connector) interface. Host boards, supporting HSMC-compliant connectors, can control the HDMI daughter board through the HSMC interface.

This HDMI_RX_HSMC kit contains complete reference design with source code written in Verilog and C, for HDMI signal receiving. Based on reference design, users can easily and quickly develop their applications.

1.1 About the KIT

This section describes the package content.

The HDMI_RX_HSMC package, as shown in **Figure 1-1**, contains:

- HDMI_RX_HSMC board x 1
- System CD-ROM x 1

The CD contains technical documents of the HDMI receiver, and one reference design for HDMI receiving with source code.

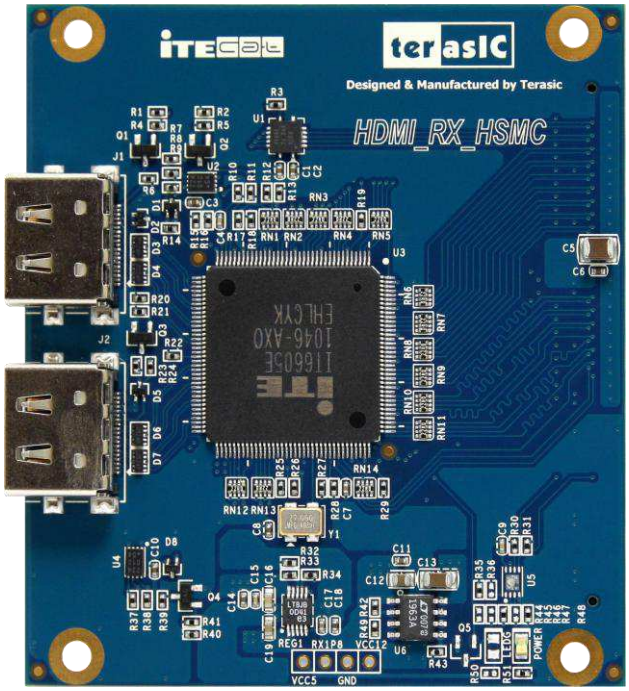


Figure 1-1 HDMI_RX_HSMC Package

1.2 Assemble the HDMI_RX_HSMC Board

This section describes how to connect the HDMI_RX_HSMC daughter board to a main board, and uses DE4 as an example.

The HDMI_RX_HSMC board connects to main boards through the HSMC interface. For DE4, the HDMI_RX_HSMC daughter board can be connected to any one of the two HSMC connectors on DE4.

Figure 1-2 shows a HDMI_RX_HSMC daughter board connected to the HSMC connector of DE4. Due to high speed data rate in between, users are strongly recommended to screw the two boards together.

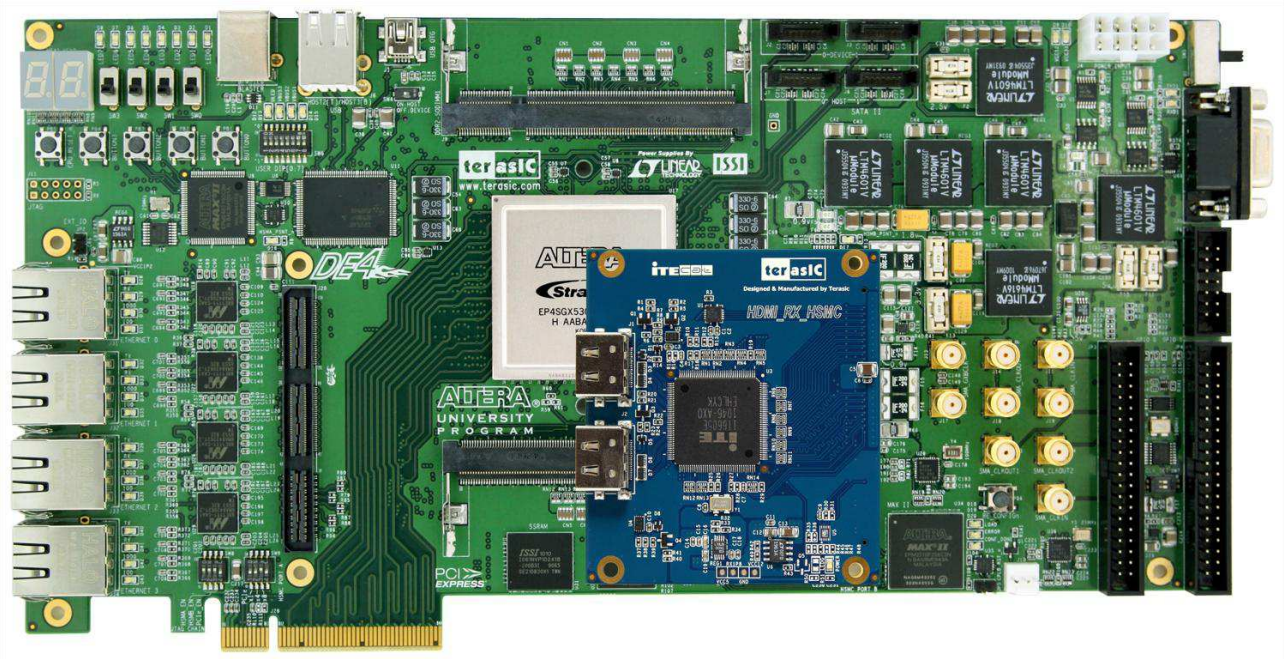


Figure 1-2 Connect HDMI_RX_HSMC daughter board to DE4 board

Note. We need to use the THCB-HMF2 card in between to make the HDMI_RX_HSMC daughter board connected to the HSMC connector of DE4. The photo of the THCB-HMF2 card is shown in Figure 1-3.

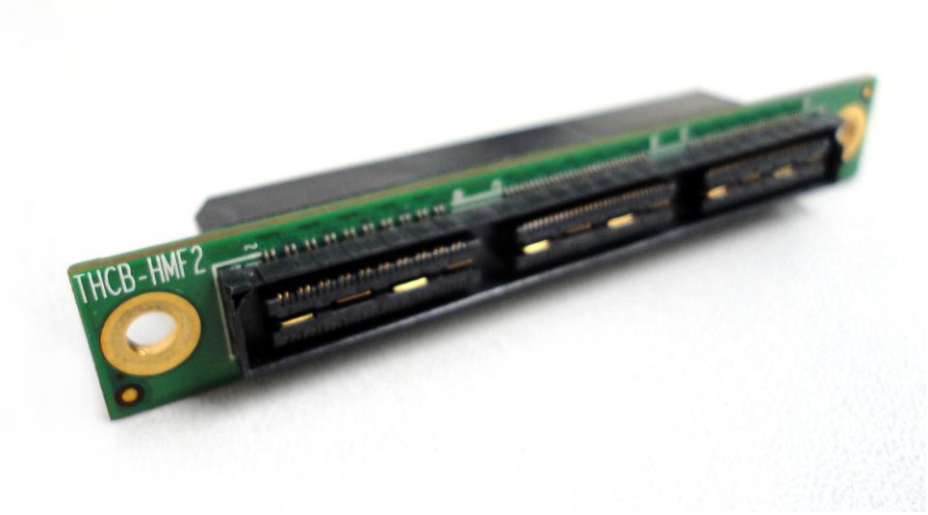


Figure 1-3 THCB-HMF2 card

1.3 Getting Help

Here are some places to get help if you encounter any problem:

- Email to support@terasic.com
- Taiwan : +886-3-550-8800
- China : +0086-13971483508
- Korea : +82-2-512-7661
- English Support Line: +1-408-512-12336

Chapter 2

Features

This chapter will illustrate technical details of HDMI_RX_HSMC board.

2.1 Features

This section describes the major features of the HDMI_RX_HSMC board.

Board Features:

- One HSMC interface for connection purpose
- One HDMI receiver with dual receiving ports
- Two 2K EEPROM for storing EDID of two receiver ports separately
- Powered by 3.3V power pins of HSMC connector

HDMI Receiver Features:

1. Dual-Port HDMI 1.4 receiver, Pin compliant with CAT6023
2. Compliant with HDMI 1.3, HDMI 1.4a 3D, HDCP 1.4 and DVI 1.0 specifications
3. Supporting link speeds up to 2.25 Gbps (link clock rate of 225MHZ)
4. Supporting diverse 3D formats which are compliant with HDMI 1.4a 3D specification.
   - Supporting 3D video up to 1080P@23.98/24/30Hz, 1080i@50/59.94/60/Hz, 720P@50/59.94/60Hz
   - Supporting formats: framing packing, side-by-side (half), top-and-bottom.
5. Various video input interface supporting digital video standards such as:
   - 24/30/36-bit RGB/YCbCr 4:4:4

- 16/20/24-bit YCbCr 4:2:2
- 8/10/12-bit YCbCr 4:2:2 (ITU BT-656)
- 12/15/18-bit double data rate interface (data bus width halved, clocked with both rising and falling edges) for RGB/YCbCr 4:4:4
- 24/30/36-bit double data rate interface (full bus width, pixel clock rate halved, clocked with both rising and falling edges)
- Input channel swap
- MSB/LSB swap

6. Bi-direction Color Space Conversion (CSC) between RGB and YCbCr color space with programmable coefficients
7. Up/down sampling between YCbCr 4:4:4 and YCbCr 4:2:2
8. Dither for conversion from 12-bit/10-bit to component to 10-bit/8-bit
9. Support Gammat Metadata packet
10. Digital audio output interface supporting:

    - Up to four I2S interface supporting 8-channel audio, with sample rates of 32~192 kHz and sample accuracy of 16~24 bits
    - S/PDIF interface supporting PCM, Dolby Digital, DTS digital audio at up to 192kHz frame rate
    - Optional support for 8-channel DSD audio up to 8 channels at 88.2kHz sample rate
    - Support for high-bit-rate (HBR) audio such as DTS-HD and Dolby TrueHD through the four I2S interface or the S/PDIF interface, with frame rates as high as 768kHz
    - Automatic audio error detection for programmable soft mute, preventing annoying harsh output sound due to audio error or hot-unplug

11. Auto-calibrated input termination impedance provides process-, voltage- and temperature-invariant matching to the input transmission lines
12. Integrated pre-programmed HDCP keys
13. Intelligent, programmable power management

2.2 Layout and Components

The photos of the HDMI_RX_HSMC board are shown in Figure 2-1 and Figure 2-2. They indicate the location of the connectors and key components.

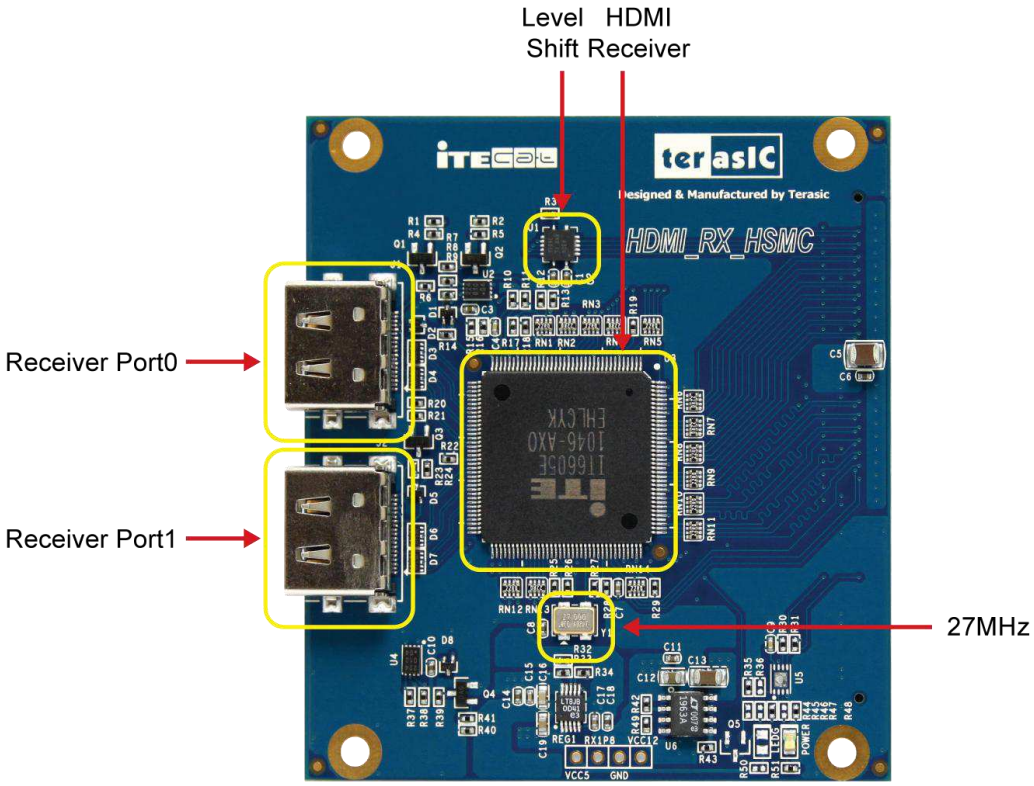


Figure 2-1 HDMI receiver on the front of the HDMI_RX_HSMC board

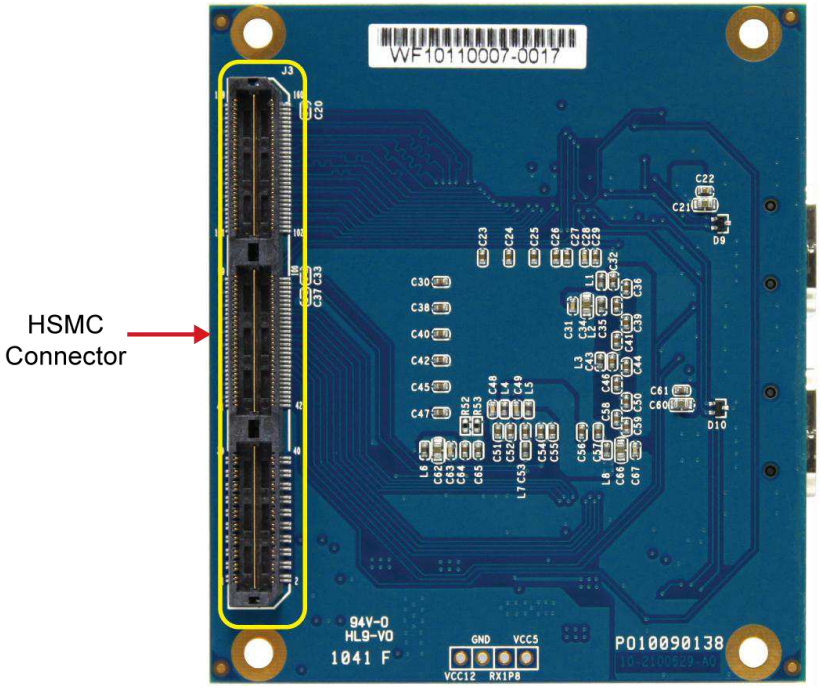


Figure 2-2 On the back of the HDMI_RX_HSMC board with HSMC connector

The HDMI_RX_HSMC board includes the following key components:

- Receiver (U3)
- Receiver port 0/1 (J1/J2)
- 27MHZ OSC (Y1)
- HSMC expansion connector (J3)
- Receiver I2C EEPORM (U2/U4)
- RX Regulator (REG1/U6)
- Level shifter (U1)

2.3 Block Diagram of HDMI Signal Receiving

This section describes the block diagram of HDMI signal receiving.

Figure 2-3 shows the block diagram of HDMI signal receiving. Please refer to the schematic included in the CD for more details. The HDMI receiver is controlled through the I2C interface, where the host works as master and the transmitter works as a slave. Because the pin PCADR is pulled low, the transmitter I2C device address is set to 0x90. Through the I2C interface, the host board can access the internal registers of receiver to control its behavior. The receiver can support two receiving ports, but only one port can be activated at the same time.

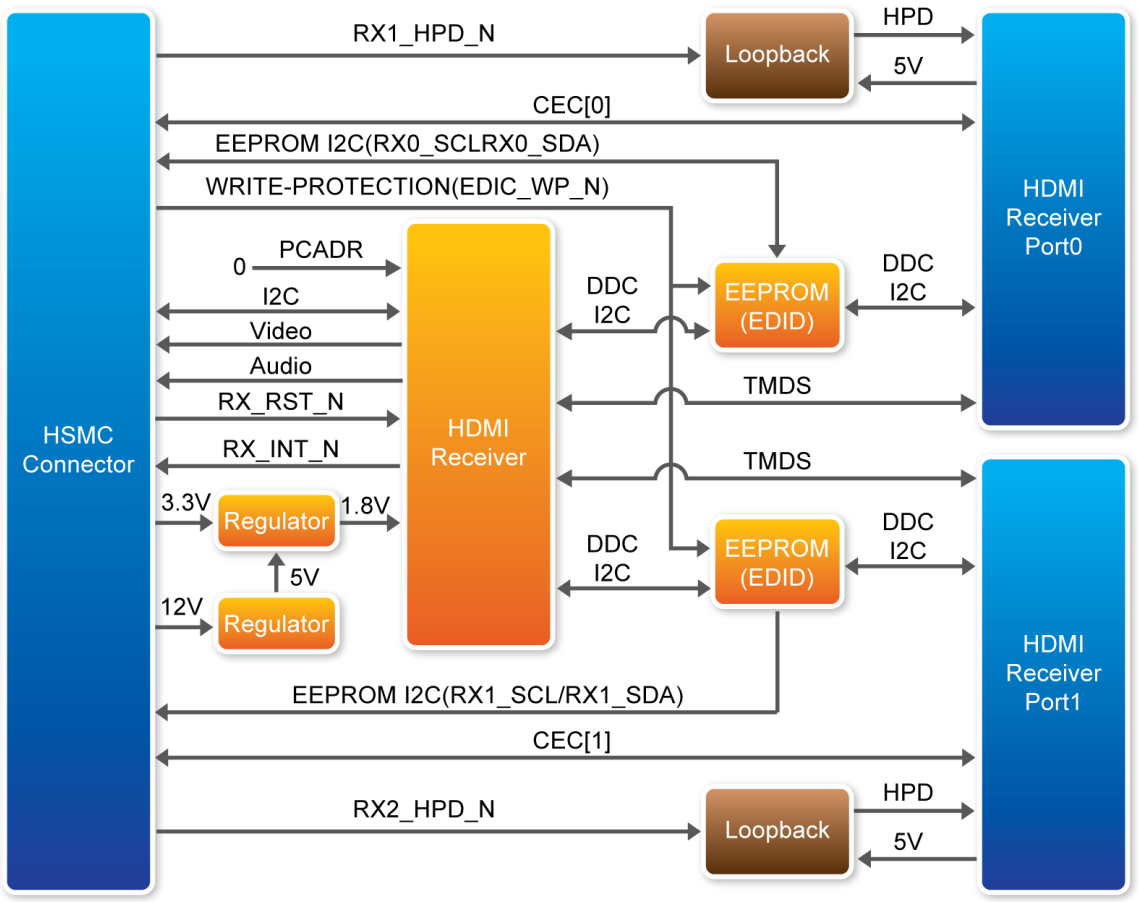


Figure 2-3 Block diagram of HDMI signal receiving

The host can use the reset pin RX_RST_N to reset the receiver, and listen to the interrupt pin RX_INT_N to detect change of the receiver status. When interrupt happens, the host needs to read the internal register to find out which event is triggered and perform proper actions for the interrupt.

Here are the steps to control the receiver:

1. Reset the receiver from the RX_RST_N pin
2. Read the EEPROM (EDID) to check whether the EEPROM contents need to be updated. When writing data to EEPROM, remember to pull-low the EEPROM write protection pin EDID_WP(please refer to the part schematic of the EEPROM circuit). Finally, make sure EDID_WP is pulled high and configure the both I2C pins as input pins, so the attached HSMC source device can read the EDID successfully
3. Initialize the receiver through the I2C interface
4. Pull-Low the RX1_HPD_N and RX2_PHD_N pins to enable HPD pins of receiving ports
5. Set receiver port 1 as active port
6. Polling the interrupt pin RX_INT_N. Switch to another receiver port every three seconds and

activate it if no HDMI source device found on the current active port

- **If a HDMI source device is detected:**

  - Perform HDCP authentication
  - Read the input video format, including color space and color depth
  - Configure input and output color space

2.4 Generate Pin Assignments

This section describes how to automatically generate a top-level project, including HDMI pin assignments.

Users can easily create the HDMI_RX_HSMC board pin assignments by utilizing the Terasic System Builder (Please visit http://www.terasic.com.tw/en/ to download the latest version of System Builder). Here are the procedures to generate a top-level project for HDMI_RX_HSMC.

- Launch Terasic System Builder(from the following path on the HDMI_RX system CD:HDMI_RX_Tool\DE4_SystemBuilder.exe)
- Select CLOCK,LED x 8,Button x 4
- Select HDMI TX and HDMI RX on the HSMC Expansion options, which is shown in **Figure 2-4**
- Input desired pin Prefix Name in the dialog of DE4 Configuration

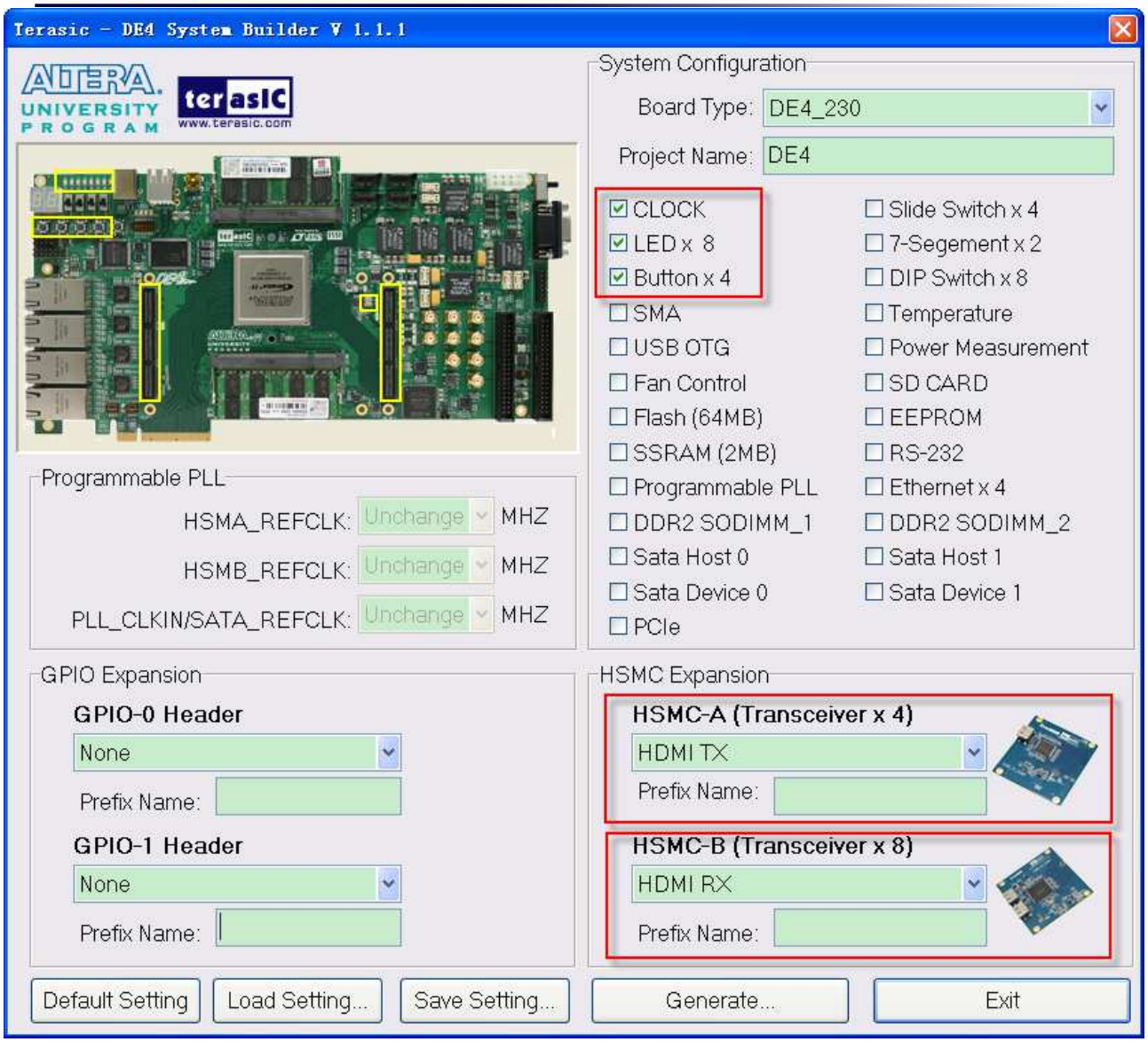


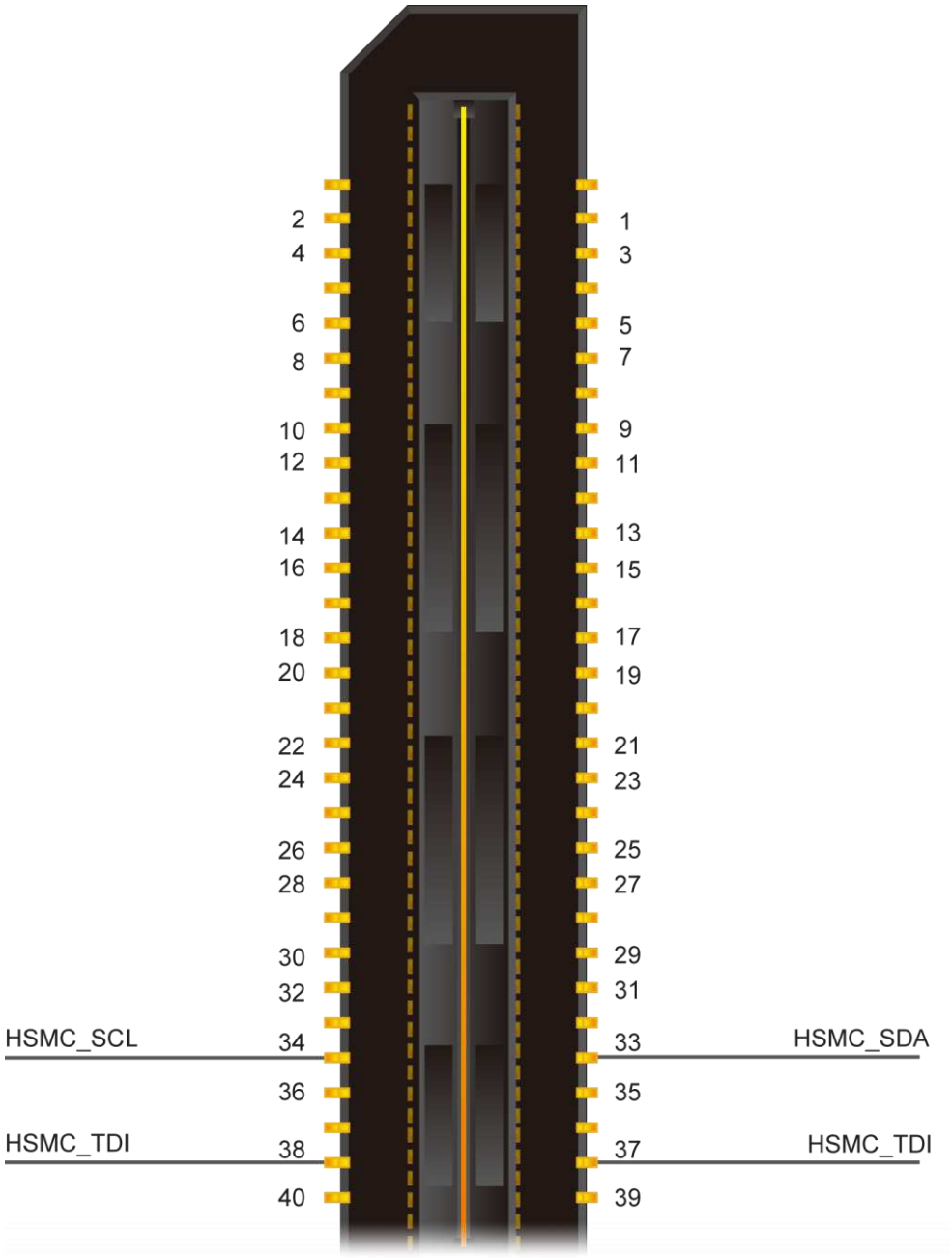
Figure 2-4 Select the DE4 Board

Click "Generate" to generate the desired top-level and pin assignments for a HDMI project.

2.5 Pin Definition of HSMC Connector

This section describes pin definition of the HSMC interface onboard.

All the control and data signals of HDMI receiver are connected to the HSMC connector, so users can fully control the HDMI_RX_HSMC daughter board through the HSMC interface. Power is derived from 3.3V and 12V pins of the HSMC connector. Figure 2-5 shows the physical pin location and signal name on the HSMC connector.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HSMC_SCL
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HSMC_TDI
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31
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HSMC_SDA
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HSMC_TDI
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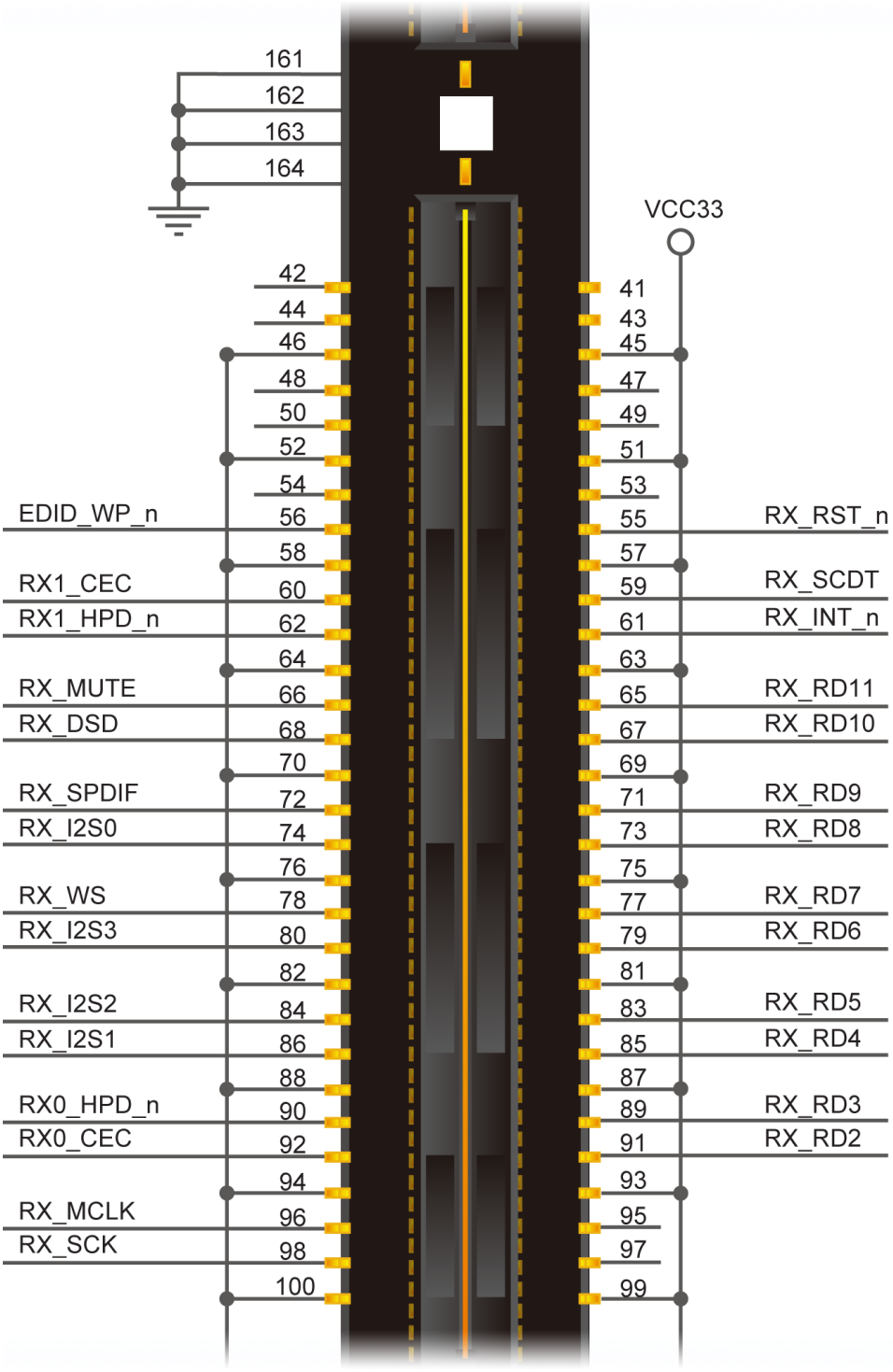
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VCC33
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EDID_WP_n
RX1_CEC
RX1_HPD_n
RX_MUTE
RX_DSD
RX_SPDIF
RX_I2S0
RX_WS
RX_I2S3
RX_I2S2
RX_I2S1
RX0_HPD_n
RX0_CEC
RX_MCLK
RX_SCK
RX_RST_n
RX_SCDT
RX_INT_n
RX_RD11
RX_RD10
RX_RD9
RX_RD8
RX_RD7
RX_RD6
RX_RD5
RX_RD4
RX_RD3
RX_RD2

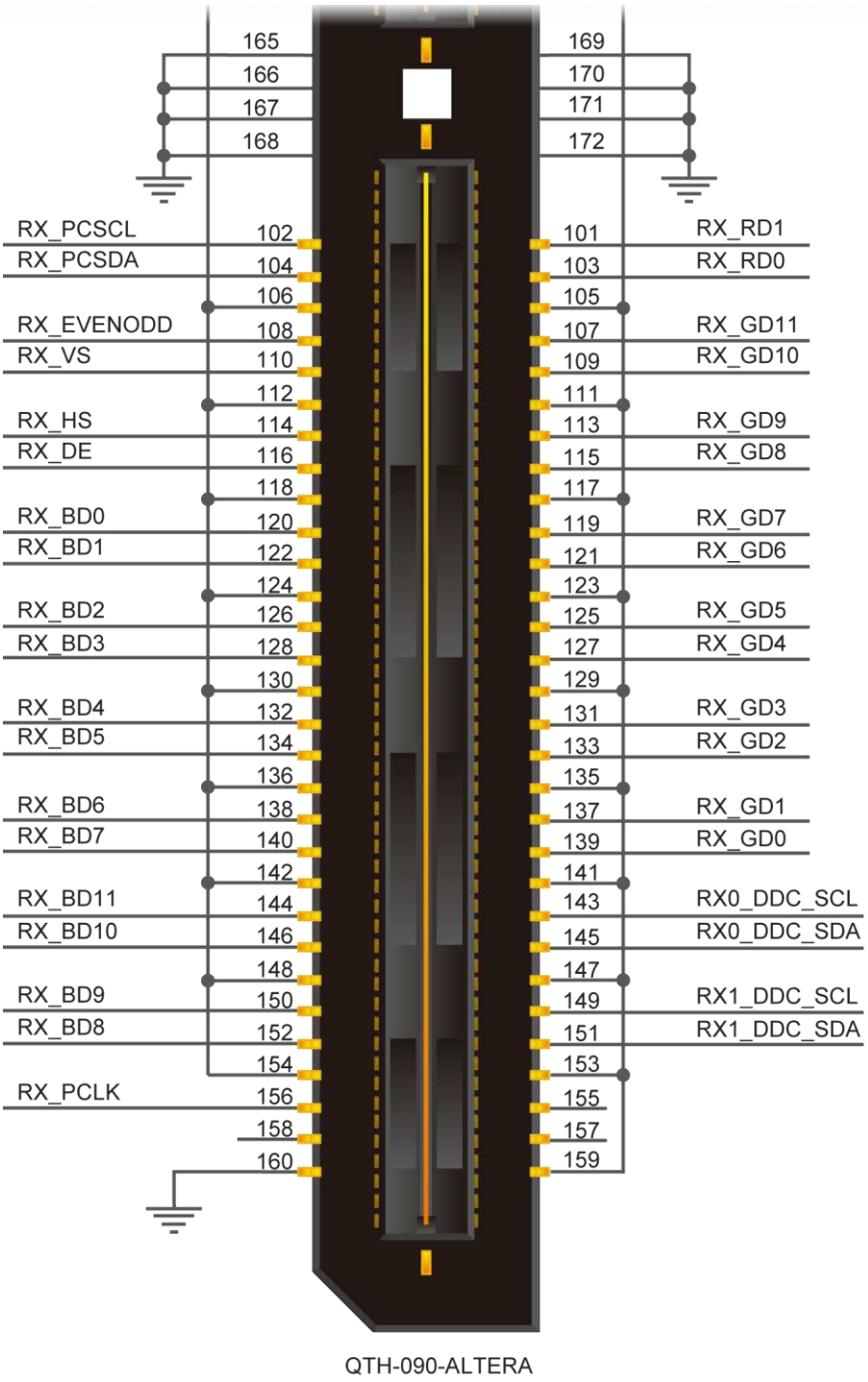

Figure 2-5 HSMC Connector of HDMI_RX_HSMC board

Table 2-1 below lists the HSMC signal direction and description.

Note. The power pins are not shown in the table.

Table 2-1 The HSMC pin definition of the HDMI_RX_HSMC board

Signal Name	*Pin NO.*	*Direction (FPGA View)*	*Description*
HSMC_SDA	33	inout	I2C serial data for on-board EEPROM
HSMC_SCL	34	output	I2C serial clock for onboard EEPROM
RX_RST_n	55	input	Hardware reset pin. Active LOW
EDID_WP_n	56	output	EEPROM Write Protection(active high)
RX_SCDT	59	input	Indication for active HDMI signal at input port
RX1_CEC	60	inout	CEC (Consumer Electronics Control) for HDMI Port 1
RX_INT_n	61	input	Interrupt output. Default active-low
RX1_HPD_n	62	output	Enable Hardware Plug Detection for HDMP Port 1, Low Active
RX_RD11	65	Input	Digital Video Input Pins
RX_MUTE	66	input	Mute output, doubles as DSD Serial Right CH3 data output
RX_RD10	67	Input	Digital Video Input Pins
RX_DSD	68	input	DSD Serial Left CH3 data output
RX_RD9	71	Input	Digital Video Input Pins
RX_SPDIF	72	input	S/PDIF audio output, doubles as DSD Serial Left CH2 data output
RX_RD8	73	Input	Digital Video Input Pins
RX_I2S0	74	input	I2S serial data output, doubles as DSD
RX_RD7	77	Input	Digital Video Input Pins
RX_WS	78	input	I2S word select output, doubles as DSD Serial Right CH0 data output
RX_RD6	79	Input	Digital Video Input Pins
RX_I2S3	80	input	I2S serial data output, doubles as DSD
RX_RD5	83	Input	Digital Video Input Pins
RX_I2S2	84	input	I2S serial data output, doubles as DSD
RX_RD4	85	Input	Digital Video Input Pins
RX_I2S1	86	input	I2S serial data output, doubles as DSD
RX_RD3	89	Input	Digital Video Input Pins
RX0_HPD_n	90	output	Enable Hardware Plug Detection for HDMP Port 0, Low Active
RX_RD2	91	Input	Digital Video Input Pins
RX0_CEC	92	inout	CEC (Consumer Electronics Control) for HDMI Port 0
RX_MCLK	96	input	Audio master clock
RX_SCK	98	input	I2S serial clock output, doubles as DSD clock
RX_RD1	101	Input	Digital Video Input Pins
RX_PCSCL	102	inout	Serial Programming Clock for chip programming
RX_RD0	103	Input	Digital Video Input Pins
RX_PCSDA	104	inout	Serial Programming Data for chip programming
RX_GD11	107	Input	Digital Video Input Pins
RX_EVENODD	108	input	Indicates whether the current field is Even or Odd

			for interlaced format
RX_GD10	109	Input	Digital Video Input Pins
RX_VS	110	output	Vertical sync. signal
RX_GD9	113	Input	Digital Video Input Pins
RX_HS	114	output	Horizontal sync. signal
RX_GD8	115	Input	Digital Video Input Pins
RX_DE	116	input	Data enable
RX_GD7	119	Input	Digital Video Input Pins
RX_BD0	120	Input	Digital Video Input Pins
RX_GD6	121	Input	Digital Video Input Pins
RX_BD1	122	Input	Digital Video Input Pins
RX_GD5	125	Input	Digital Video Input Pins
RX_BD2	126	Input	Digital Video Input Pins
RX_GD4	127	Input	Digital Video Input Pins
RX_BD3	128	Input	Digital Video Input Pins
RX_GD3	131	Input	Digital Video Input Pins
RX_BD4	132	Input	Digital Video Input Pins
RX_GD2	133	Input	Digital Video Input Pins
RX_BD5	134	Input	Digital Video Input Pins
RX_GD1	137	Input	Digital Video Input Pins
RX_BD6	138	Input	Digital Video Input Pins
RX_GD0	139	Input	Digital Video Input Pins
RX_BD7	140	Input	Digital Video Input Pins
RX0_DDC_SCL	143	inout	DDC I2C Clock for HDMI Port 0
RX_BD11	144	Input	Digital Video Input Pins
RX0_DDC_SDA	145	inout	DDC I2C Data for HDMI Port 0
RX_BD10	146	input	Digital Video Input Pins
RX1_DDC_SCL	149	input	DDC I2C Clock for HDMI Port 1
RX_BD9	150	input	Digital Video Input Pins
RX1_DDC_SDA	151	inout	DDC I2C Data for HDMI Port 1
RX_BD8	152	input	Digital Video Input Pins
RX_PCLK	156	input	Output data clock.

Chapter 3

Demonstration

This chapter illustrates the video/audio demonstration for the HDMI_RX_HSMC board. Users may modify the reference design for various purposes accordingly.

3.1 Introduction

This section describes the functionality of the demonstrations briefly.

This demonstration shows how to use DE4 to control the HDMI_RX_HSMC board.

The demonstration includes:

■ Loopback HDMI_RX to HDMI_TX:

Loopback (internal bypass) the HDMI Video and Audio Signals. The audio and video output pins of the receiver are directly connected to the input audio and video pins of the transmitter.

3.2 System Requirements

The following items are required for Loopback HDMI_RX to HDMI_TX demonstration.

■ Loopback HDMI_RX to HDMI_TX

- HDMI_RX_HSMC board x 1
- HDMI_TX_ HSMC board x 1
- DE4 Board x 1
- LCD monitor with at least one HDMI input x 1
- HDMI Source Device x 1
- HDMI Cable x 2
- THCB-HMF2 board x2

3.3 Setup the Demonstration

Figure 3-1 shows how to setup hardware for Loopback HDMI_RX to HDMI_TX demonstration.

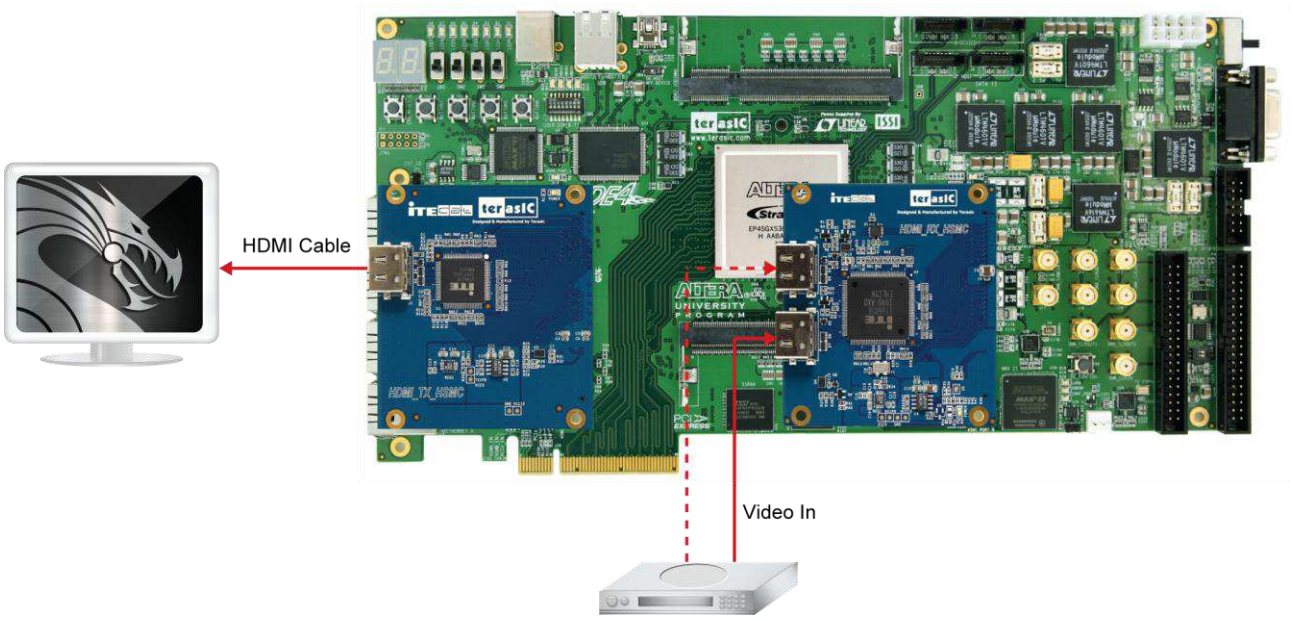

Figure 3-1 Loopback HDMI_RX to HDMI_TX Demonstration Setup

3.4 Operation

This section describes the procedures of running the demonstrations.

■ FPGA Configuration

Please follow the steps below to configure the FPGA.

- Make sure hardware setup is completed
- Connect PC with DE4 via a USB cable
- Power on DE4
- Make sure Quartus II has been installed on your PC
- Execute the batch file hdmi_demo.bat under the folder "HDMI_RX_Demonstration\DE4_230_HDMI_TX_RX\demo batch"(for the Loopback demonstration)

■ Internal Loopback HDMI_RX to HDMI_TX

Note. Do not attempt to connect/remove the HSMC_HDMI daughter board to/from the main board when the power is on, or the hardware could be damaged.

After FPGA is configured, please follow the steps below to run the Loopback HDMI_RX to HDMI_TX demonstration.

- Connect the HDMI LCD and the HDMI TX port with a HDMI Cable
- Power on the LCD monitor and make sure the LCD monitor is set to the mode where HDMI input is the source
- Connect the HDMI source device and HDMI RX port on the HDMI_RX_HSMC board with a HDMI Cable
- Power on the HDMI source device and make sure its HDMI port is selected as the output
- Users will be able to see the video displayed on the LCD monitor and hear the sound, if there is a speaker built-in
- Users can change the RX port connected to the HDMI source device. The demonstration can automatically detect the RX port and activate it

Figure 3-2 shows the Nios II program trace log when a HDMI LCD source device is detected. It indicates the input video resolution is 1280 x 720 (VIC=4) with color space RGB444 and 36-bits color depth.

Both input color and output color of the receiver and transmitter are configured as RGB444. In another words, the color format doesn't change from the source to the LCD monitor during the loopback process. The output color depth of the transmitter is configured as 24-bits.

```
[TERASIC-00016.656]++++++++++ RX HW Reset +++++++++
[TERASIC-00016.658]RX hardware Reset
[TERASIC-00016.815]Revision of Receiver:A2h
[TERASIC-00016.907]InitCAT6023(): reg07 = 1C, ucCurrentHDMIPort = 1
[TERASIC-00019.882][RX]Active Port: B
[TERASIC-00022.950]++++++++++ RX HW Reset +++++++++
[TERASIC-00022.953]RX hardware Reset
[TERASIC-00023.109]Revision of Receiver:A2h
[TERASIC-00023.200]InitCAT6023(): reg07 = 0C, ucCurrentHDMIPort = 0
[TERASIC-00026.175][RX]Active Port: A
[TERASIC-00027.256]CDR_RESET, reg10 = 01
[TERASIC-00027.521][RX] VState = 1, VSTATE_SyncWait
[TERASIC-00027.970]RXINT_VideoMode_Chg, -> VSTATE_SyncWait
[TERASIC-00028.059][RX] VState = 3, VSTATE_SyncChecking
[TERASIC-00028.334][RX] VState = 6, VSTATE_ModeDetecting
[TERASIC-00028.506]RXINT_VideoMode_Chg, -> VSTATE_SyncWait
[TERASIC-00028.558][RX] VState = 3, VSTATE_SyncChecking
[TERASIC-00028.620][RX] VState = 6, VSTATE_ModeDetecting
[TERASIC-00028.847]==== RX Video On ====
[TERASIC-00029.488][RX] VState = 7, VSTATE_VideoOn
[TERASIC-00029.490][RX] AState = 4, ASTATE_AudioOn
[TERASIC-00029.523]===== Input Display Res.: 1920 x 1080 @36bps =====
[TERASIC-00029.539]===== Input Audio: Rate=48000, Valid-Channel Mask=01h =====
[TERASIC-00029.551]H_Total    = 2200
[TERASIC-00029.553]H_Display  = 1920
[TERASIC-00029.563]H_FPorch   = 88
[TERASIC-00029.573]H_Sync     = 44
[TERASIC-00029.614]H_BPorch   = 148
[TERASIC-00029.629]V_Total    = 1125
[TERASIC-00029.631]V_Display  = 1080
[TERASIC-00029.650]V_FPorch   = 4
[TERASIC-00029.661]V_Sync     = 44
[TERASIC-00029.707]V_BPorch   = 5
[TERASIC-00029.713]V_SycnToDE = 41
[TERASIC-00029.776]VIC: 16 (1920x1080p@60)
[TERASIC-00029.778]Aspect Ratio = 16:9
[TERASIC-00029.779]ITU709 = No
[TERASIC-00029.781]Color Space = RGB444
[TERASIC-00029.782]========
[TERASIC-00029.783][RX]Video On:Yes
[TERASIC-00029.990]HDMITX_SetOutput
[TERASIC-00030.717]ConfigAVIInfoFrame, VIC=16
[TERASIC-00033.109]Set Rx Color Convert:RGB444->RGB444
[TERASIC-00033.156]Set Tx Color Depth: 24 bits
[TERASIC-00033.158]Set Tx Color Convert:RGB444->RGB444
[TERASIC-00033.886]ConfigAVIInfoFrame, VIC=16
```

Figure 3-2 Nios II program trace log of Loopback HDMI_RX to HDMI_TX demonstration

Chapter 4

Case Study

This chapter describes the design concepts for the Loopback HDMI_RX to HDMI_TX demonstration in the previous chapter.

4.1 Overview

This section describes the overview of the reference design.

This reference design shows how to use DE4 to control HDMI_RX_HSMC board. Please refer to the previous chapter for the demonstration of this reference design.

The source code of the reference design can be found under the directory of Examples folder in the CD of the HDMI_RX_HSMC board. The demonstration includes the following function:

- **Loopback HDMI_RX to HDMI_TX:**

Loopback (internal bypass) the HDMI Video and Audio Signals. The audio and video output pins of the receiver are directly connected to the input audio and video pins of the transmitter.

4.2 System Function Block

This section will describe the system behavior in function blocks.

Figure 4-1 shows the system function block diagram of this demonstration. In the design, SOPC is included because Nios II processor is used to control receiver through I2C interface. The Nios II program is designed to run on the on-chip memory.

The source selector circuit is designed to select the desired video source between the video pattern generator and the video from the receiver. Four LEDs on DE4 are used for human interface. LEDs are designed to indicate the HDMI status, which is illustrated in Table 4-1. BUTTONs are designed to change the video format and color space of the build-in video pattern generator, which is illustrated in Table 4-2

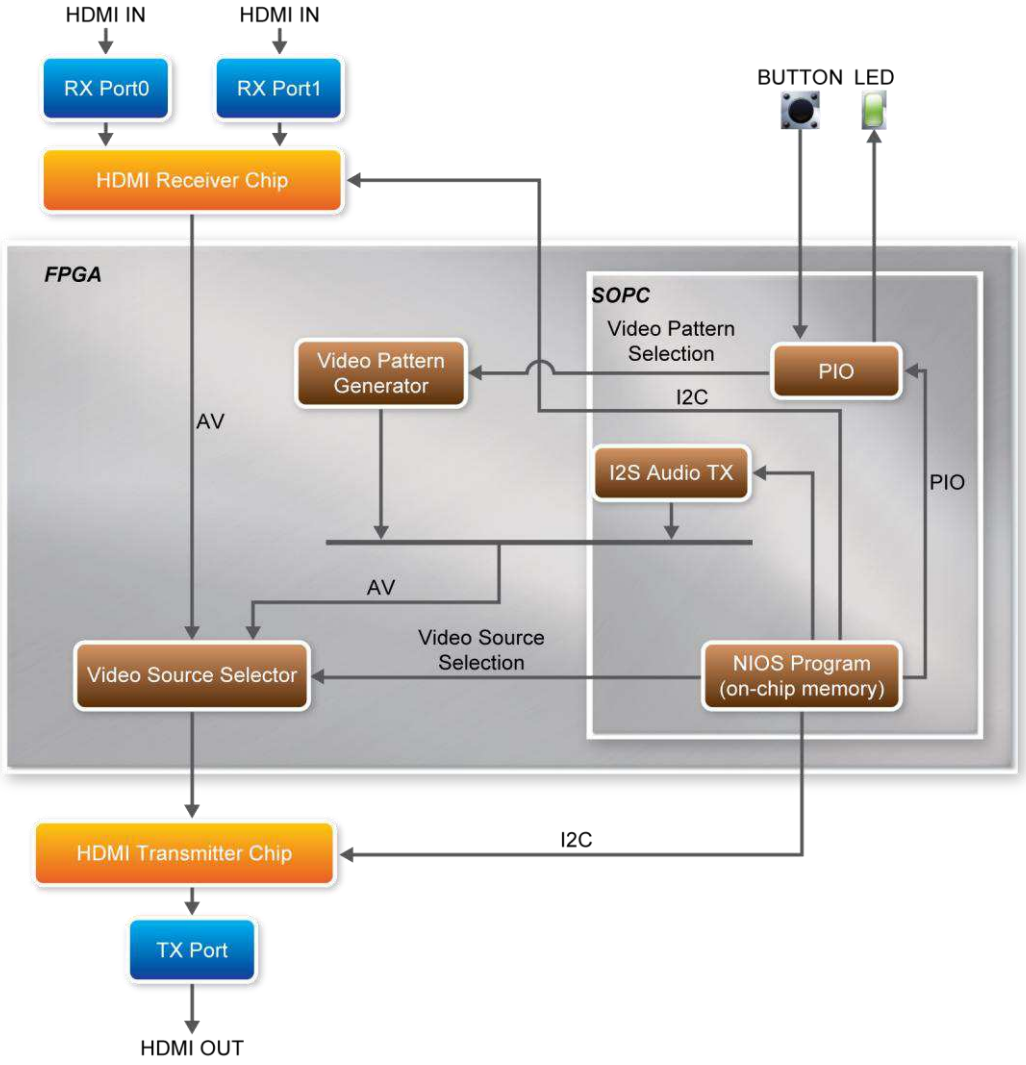

Figure 4-1 System Function Block Diagram

Table 4-1 LED Indications

LED	*Description*
	**System is running.**
	**HDMI sink device is detected and synchronized.**
	**HDMI source device is detected and synchronized.**

Table 4-2 Button Operation Definition

BUTTON	Description
 BUTTON0	Press to change active video format of the built-in video pattern generator.
 BUTTON1	Press to change active video color space of the built-in video pattern generator.

■ Receiver Controlled by Nios II Processor

The receiver is controlled by Nios II program through I2C interface. Based on I2C protocol, the Nios II program can read/write the internal registers of the receiver, and control the behavior of the receiver. The revision number of receiver is either A1 or A2, which can be determined by querying the register 4 of receiver.

The major differences between both revisions are:

1. Receiver initialization process
2. Video synchronization process

Please search the global variable “Is_A2” in it6605.c for detail information.

The Nios II program controls the receiver to perform the following procedures step by step:

- Initialize the HDMI receiver chip
- Detect if a HDMI source device is attached or detached
- Select one of the receiving ports and activate it
- Read and parse the EDID content to find the capability of the HDMI source device. The capability includes supported color space, video format (VIC code), and color depth etc
- Perform HDCP authentication
- Report the input video (VIC) and audio format of the attached HDMI source device
- Configure the color space of input and output. The receiver can provide color space transformation

■ Video Source Selector

The source selector is implemented using Megafunction LPM_MUX.