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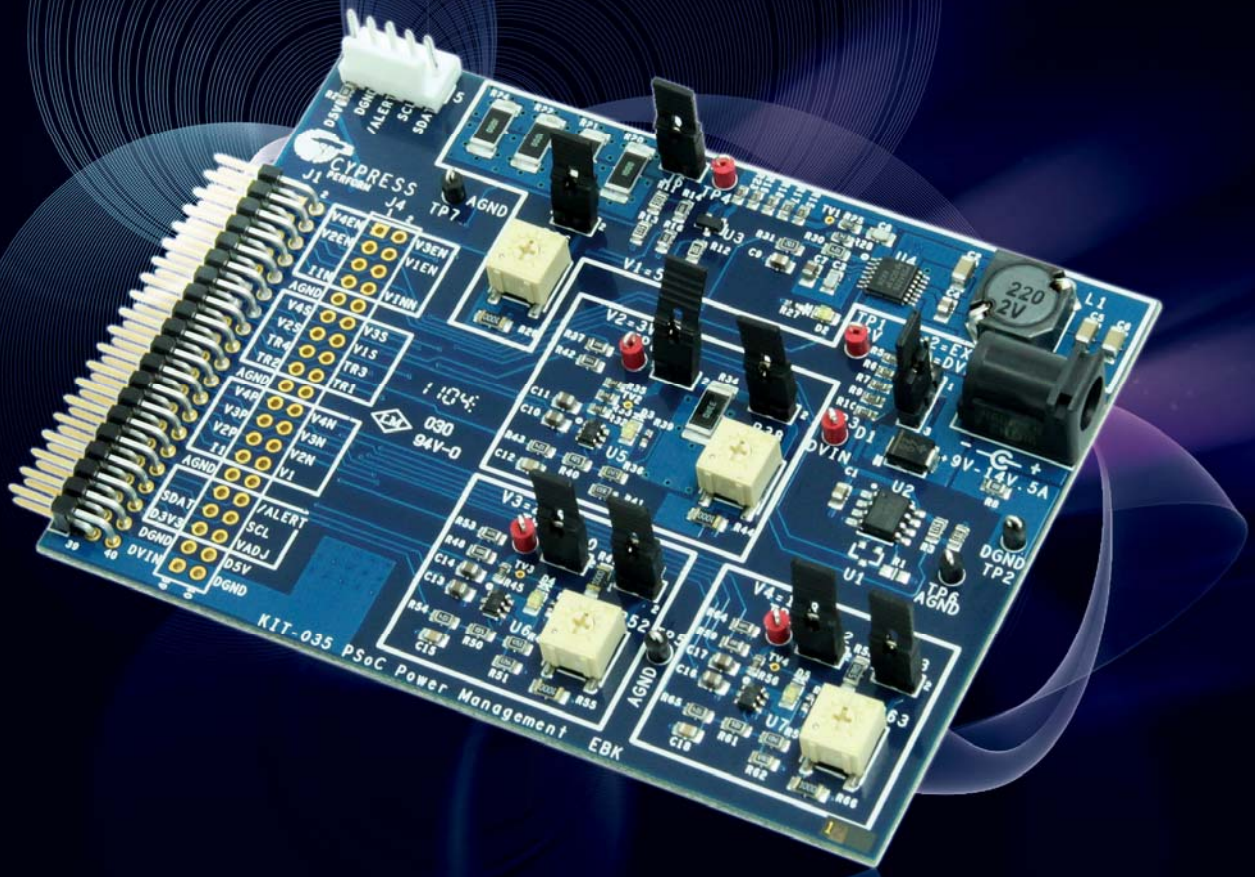
PSoC

Power Management Expansion Board Kit CY8CKIT-035

User's Guide



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CONTENTS

Chapter 1

Introduction to the PME EBK

In general terms, power management or power supervision is a combination of sequencing, monitoring and control of multiple regulators and/or point-of-load DC power converters in a system. Typical solutions for power management include multiple devices such as CPLDs, mixed-signal ASICs and/or limited-functionality and inflexible discrete devices. Power management solutions require: (1) rapid fault detection capabilities for high-availability systems of the power converters in the system; (2) accurate and reliable power rail sequencing of the power converters during power-on and power-off events; (3) voltage and current measurement of the power converters to optimize power consumption and/or for data logging; and, (4) closed-loop control of the power converters through trimming and, for development and manufacturing test purposes, margining of voltage rails in the system.

The PSoC Power Management Expansion Board Kit (PME EBK) is part of the PSoC development kit ecosystem and is designed to work with the CY8CKIT-001 PSoC Development Kit (DVK) and the CY8CKIT-030 PSoC 3 Development Kit (DVK). It enables you to evaluate the system power management functions and capabilities of PSoC 3 devices. You can evaluate the example projects described in this guide or design and customize your own system power management solution using components in Cypress's PSoC Creator™ software (included in this kit) or by altering example projects provided with this kit.

The PSoC Power Management Expansion Board Kit (PME EBK) is used with the PSoC family of devices and is specifically designed and packaged for use with the PSoC 3 device family. PSoC 3 is a programmable system-on-chip platform that combines precision analog and digital logic with a high performance, single-cycle, 67MHz 8051 processor. With the flexibility of the PSoC architecture, you can easily create your own custom power management solution on chip with the exact functionality you need, in the way you want it—no more, no less.

1.1 Features

The PSoC Power Management Expansion Board Kit (PME EBK) is intended to provide a demonstration and development platform for Cypress and customers in developing power management/supervisor solutions including:

- Power Supply Sequencing
- Power Supply Voltage and Current Measurement
- Power Supply Voltage Trimming and Margining
- Power Supply Over-Voltage and Under-Voltage Fault Detection
- EEPROM Data Recording
- I2C/SMBus/PMBus Host Communications Interface

Figure 1-1 shows a simplified block diagram of the most fundamental components on the PME EBK and how they interact to aid in understanding of the hardware. Not all hardware components are shown.

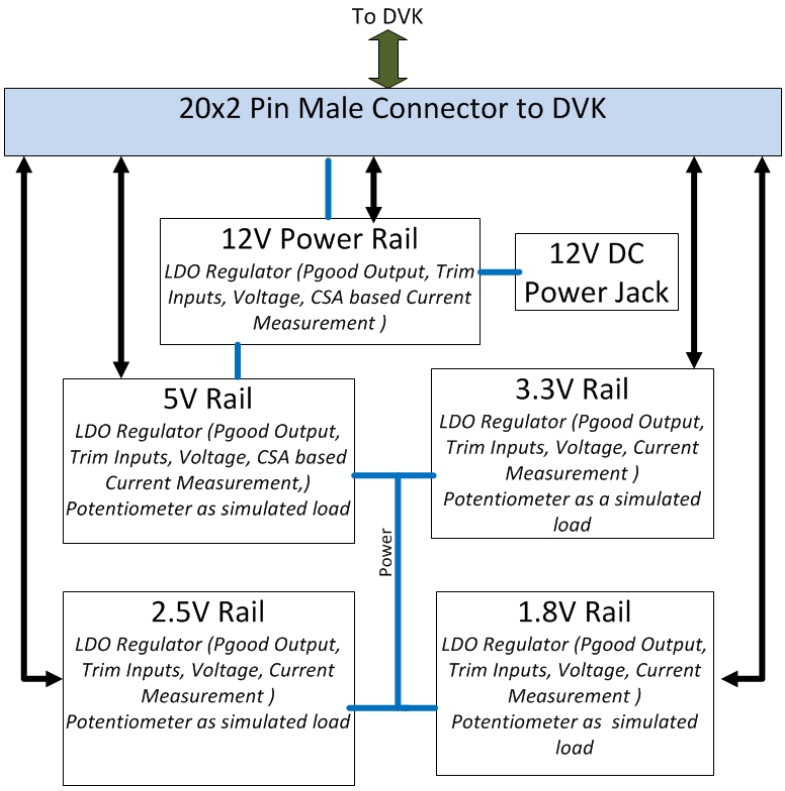

Figure 1-1 PME EBK Block Diagram

1.2 About the KIT

The PSoC Power Management Expansion board kit (PME) consists of:

- Cypress PME EBK
- Quick Start Guide
- Power DC Adaptor 12V/2A
- System CD containing:
  - User's Guide (this document)
  - PSoC Creator and pre-requisite software
  - PSoC Programmer and pre-requisite software
  - PME Example Firmware for the CY8CKIT-001 PSoC Development Kit
    - Advanced Sequencer
    - Power Supervisor

- PME Example Firmware for the CY8CKIT-030 PSoC 3 Development Kit
  - Advanced Sequencer
  - Power Supervisor
- Application Note (AN62496) “Voltage Sequencing with PSoC ® 3 and PSoC ® 5”
- Application Note (AN60220) “Multiplexed Comparator using PSoC ® 3”
- Datasheets for key PME EBK components

Figure 1-2 shows a photograph of the PME EBK contents.

Figure 1-2 PME EBK Package Contents

1.3 PSoC Creator

Cypress's PSoC Creator software is a state-of-the-art, easy-to-use integrated development environment (IDE) that introduces a game changing, hardware and software design environment based on classic schematic entry and revolutionary embedded design methodology.

With PSoC Creator, you can:

- Draw a schematic of the hardware circuit you would like to build inside PSoC and the tool will automatically place and route the components for you
- Eliminate external CPLDs or standard logic ICs by integrating state machines and simple glue logic in your design
  Trade-off architecture decisions between hardware and software, allowing you to focus on what matters and getting you to market faster

PSoC Creator also enables you to tap into an entire tools ecosystem with integrated compiler tool chains, RTOS solutions, and production programmers to support PSoC 3.

1.4 Getting Help

Certified as a Cypress Authorized Design Partner, Terasic offers design expertise in rapidly developing PSoC Solutions to get your products into production quickly and reducing your development and BOM costs. Terasic provides customized board designs for academia and industry.

For additional information visit:

www.cypress.com/go/CY8CKIT-035
or
http://pme.terasic.com

For support please contact:

Online: www.cypress.com/go/support
Telephone (24x7): +1-800-541-4736 ext. 8 (USA)
+1-408-943-2600 ext. 8 (International)

Chapter 2

PME EBK Architecture

This chapter provides information about the architecture and block diagram of the PME EBK.

2.1 Layout and Components

Photos of the PME EBK are shown in **Figure 2-1** and **Figure 2-2**. They depict the layout of the board and indicate the locations of the connectors and key components.

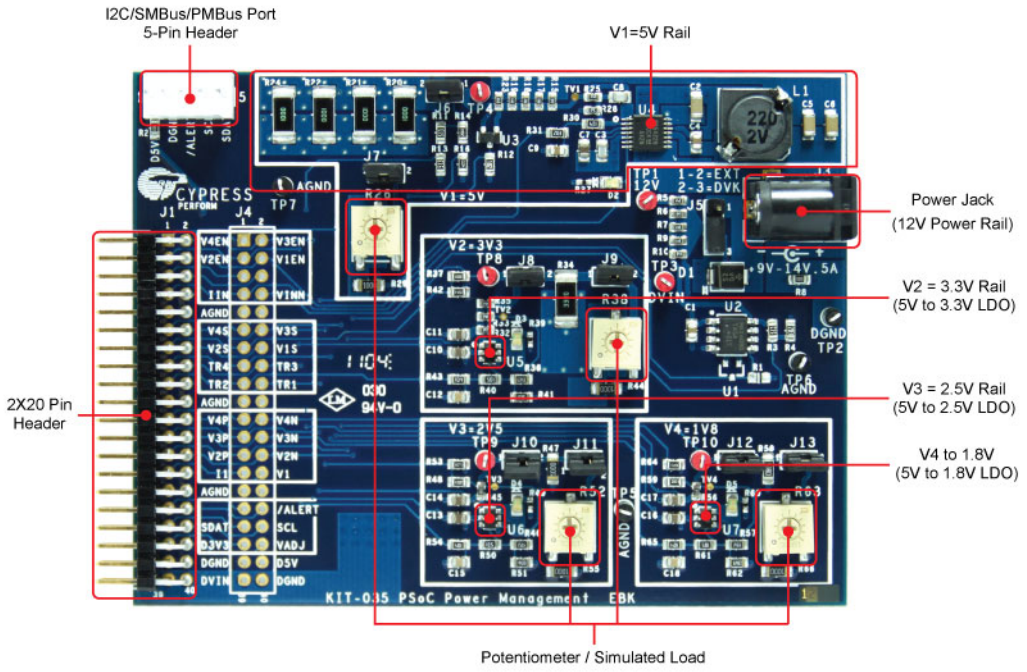

Figure 2-1 PME PCB (Top)

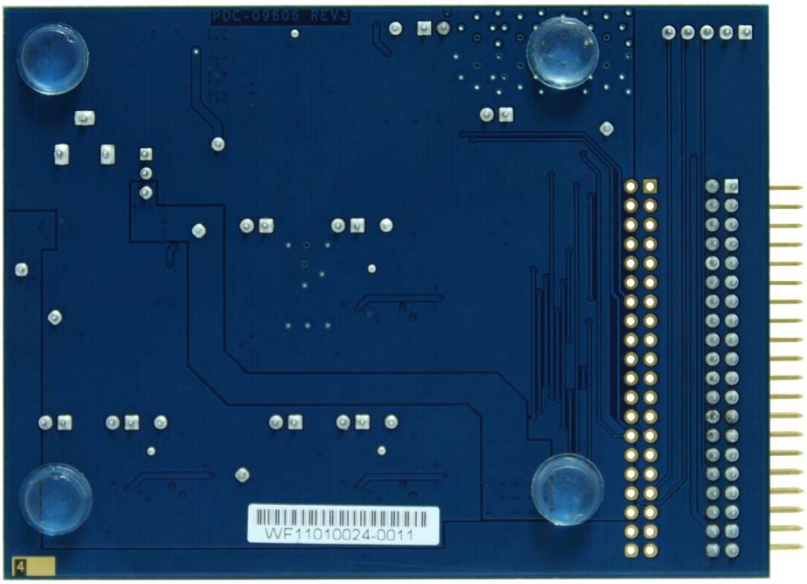

Figure 2-2 PME PCB (Bottom)

2.2 PSoC 4+1 Power Supervisor Solution on the PME

The PSoC Power Management EBK contains 4 DC voltage regulator circuits. They all have enable inputs to allow PSoC to control the power up and power down sequencing of the regulators as well as the necessary passive components to enable PSoC to measure their output voltage and load currents using its built-in ADC converter. The regulators chosen support having their output voltage trimmed (or margined) by PSoC and the necessary passive components to enable PSoC to detect under and over voltage fault conditions using its internal window comparator hardware. PME EBK also provides an I2C/SMBus/PMBus compatible header to support systems that have a requirement for communication with a host controller. All of this functionality is implemented on a single PSoC 3. The PME routes all the input/output signals for power management/supervision to a PSoC 3 mounted on a development kit platform such as the CY8CKIT-001 PSoC Development Kit or CY8CKIT-030 PSoC 3 Development Kit. PSoC 3 is not mounted on the PME EBK itself.

Figure 2-3 shows a high-level overview of the 4+1 Power Management solution that can be implemented using the PME. Up to 4 secondary regulators can be sequenced through the logic-level enable outputs (labeled as EN[4]). The 4 secondary voltage rails along with one primary input power rail (labeled as V[4+1]) can be multiplexed into a 12 bit, differential Delta Sigma ADC configured for a single-ended input range of 0-4096 mV at 27 ksps with a 0.1% accurate internal reference. For load current measurements across a series shunt resistor (labeled as I[4+1]), the ADC configuration is dynamically changed to a differential input range of ±256mV at 22.9 ksps. A firmware interrupt service routine (ISR) running on PSoC is responsible for taking the raw ADC readings and converting them to actual voltages (in mV) and currents (in µA), performing simple IIR filtering and using this information to increase or decrease the duty cycles of the

pulse-width-modulated (PWM) outputs for regulator trimming and margining. The trim/margin PWM outputs from PSoC (labeled as TR[4]) are filtered with a single RC filter stage on PME EBK and fed into the voltage feedback input of the regulators. A single time-multiplexed window comparator is implemented in PSoC using 2 voltage DAC's (to set the under and over voltage limits for each rail), 2 comparators and a programmable glitch filter. This window comparator loops through each channel at 2µs per channel that it monitors (labeled as C[4+1]). Note that all 5 monitored supply rail voltages are connected to both the V[4+1] and C[4+1] input pins. Each voltage is connected to 2 pins to enable the hardware window comparator and the ADC with input multiplexer to run asynchronously to each other at different speeds in order to give the fastest possible fault detection time.

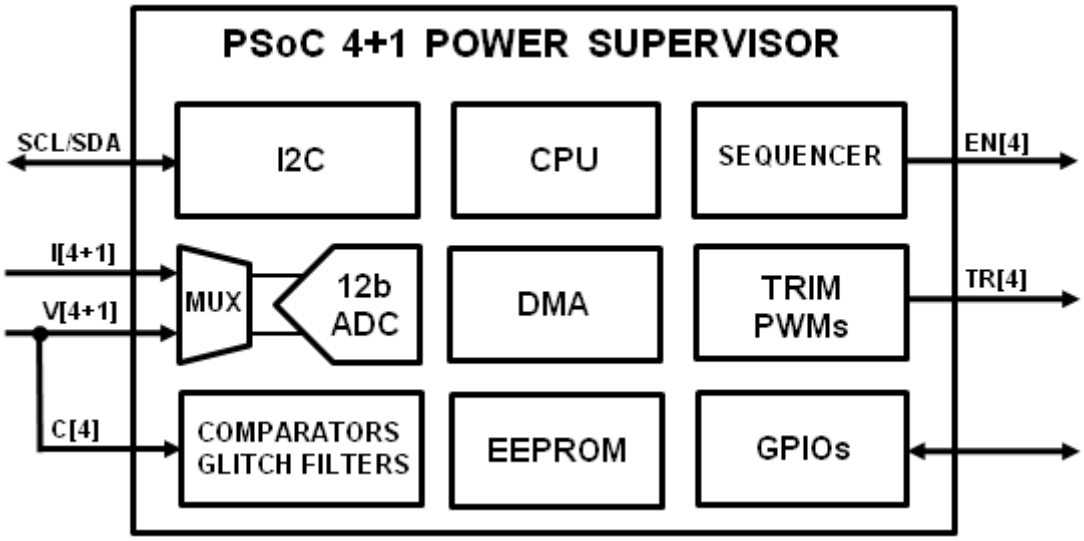

Figure 2-3 4+1 PSoC Power Management Functional Diagram

Note that PME EBK hardware limits support to a maximum of 4 secondary regulator circuits. The PSoC 3 Power Supervisor solution can be easily extended to support up to 12 secondary regulator circuits. Contact Cypress for further information on the full 12+1 PSoC Power Supervisor solution.

Chapter 3

PME EBK Hardware Overview

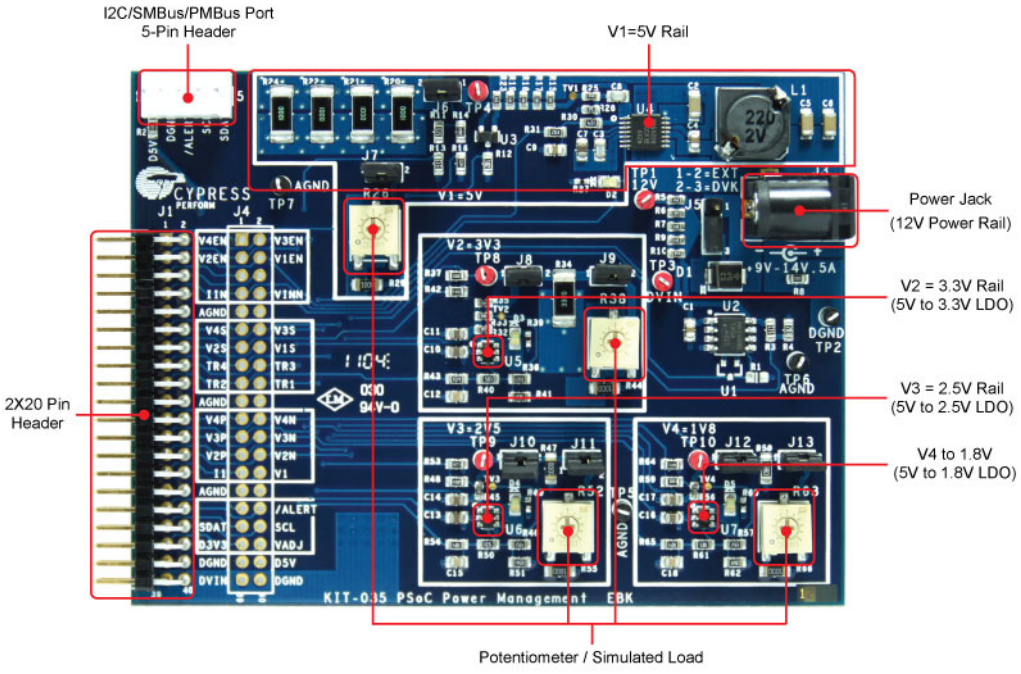

Figure 3-1 PME Hardware Components

The Power Management EBK Board consists of a 12V primary input power source and 4 secondary voltage rails: V1=5V, V2=3.3V, V3=2.5V and V4=1.8V. Voltage rail V1 feeds power to the other three rails V2, V3 and V4. Therefore, disabling V1 will disable V2-V4 as a result. Each secondary rail consists of a regulator with enable input, circuitry that enables PSoC to apply a DC control voltage to the regulator feedback or adjust pin, as well as fixed and adjustable (potentiometer) load elements. Two jumpers are provided for each rail to (1) disconnect all loads or (2) disconnect only the adjustable load.

PME EBK provides an I2C/SMBus/PMBus connector. A 40-pin (2×20) header J1 is provided to interface this board with the host PSoC on a development kit platform such as the CY8CKIT-001

PSoC Development Kit or CY8CKIT-030 PSoC 3 Development Kit. The header carries voltage enables, regulator voltage, regulator load currents and trim/margin control signals for each regulator on PME EBK. The I2C physical layer signals (SDA/SCL) from PSoC are also routed across this header to enable connection to an external host or management processor that supports standard I2C, SMBus or PMBus protocol interfaces.

3.1 2x20 pin Interface Header

The following table outlines the definition of the 40-pin J1 header interface.

Table 3-1 2x20 Header (J1) Pin Definition

Description	*Signal*	*Pin*	*Pin*	*Signal*	*Description*
Voltage Regulator 4, Enable	V4EN	1	2	V3EN	Voltage Regulator 3, Enable
Voltage Regulator 2, Enable	V2EN	3	4	V1EN	Voltage Regulator 1, Enable
-	NC	5	6	NC	-
Power Rail Current (measured as single ended voltage)	IIN	7	8	VIN	Power Rail Sensing Voltage
Analog Ground	AGND	9	10	NC	-
Voltage Regulator 4, Fault Sensing Voltage	C4	11	12	C3	Voltage Regulator 3, Fault Sensing Voltage
Voltage Regulator 2, Fault Sensing Voltage	C2	13	14	C1	Voltage Regulator 1, Fault Sensing Voltage
Voltage Regulator 4, Trim	TR4	15	16	TR3	Voltage Regulator 3, Trim
Voltage Regulator 2, Trim	TR2	17	18	TR1	Voltage Regulator 1, Trim
Analog Ground	AGND	19	20	NC	-
Voltage Regulator 4, Current (Measured as differential voltage)	I4	21	22	V4	Voltage Regulator 4
Voltage Regulator 3, Current (Measured as differential voltage)	I3	23	24	V3	Voltage Regulator 3
Voltage Regulator 2, Current (Measured as differential voltage)	I2	25	26	V2	Voltage Regulator 2
Voltage Regulator 1 Current (Measured as single ended voltage)	I1	27	28	V1	Voltage Regulator 1
Analog Ground	AGND	29	30	NC	-
-	NC	31	32	/ALERT	Alert Signal (I2C/SMBus/PMBus)
Serial Data (I2C/SMBus/PMBus)	SDAT	33	34	SCL	Serial Clock (I2C/SMBus/PMBus)
unused	D3V3	35	36	VADJ	*unused*
Digital Ground	DGND	37	38	D5V	*unused*
Optional 12V Power from DVK	DVIN	39	40	DGND	Digital Ground

3.2 PME EBK Headers and Jumpers

A number of headers and jumpers are provided on the PME EBK. The following table outlines the function of each item and the default configuration.

Table 3-2 PME Jumper Settings

PCB Designator	*Description*	*Factory Default Configuration*
J1	2×20 pin header for connecting to PSoC DVK	-
J2	5-pin header for connecting an external host or management processor via I2C/SMBus/PMBus	-
J3	Power Jack	-
J4	2×20 pin header that replicates signals on J1 for easy connection to a logic analyzer or oscilloscope	-
J5	3-pin header for primary input power source selection. Place jumper in 1-2 position to source power from the DC power jack J3. Place in 2-3 position to source power from the PSoC platform DVK	2-3 position
J6	2-pin header for connecting all loads on V1=5V rail (this includes the fixed and adjustable loads on V1 as well as the load presented by the V2, V3 and V4 rails)	Installed
J7	2-pin header for connecting the potentiometer load on V1=5V rail	Installed
J8	2-pin header for connecting both loads on V2=3.3V rail (fixed and adjustable)	Installed
J9	2-pin header for connecting potentiometer load on V2=3.3V rail	Installed
J10	2-pin header for connecting ALL loads on V3=2.5V rail (fixed and adjustable)	Installed
J11	2-pin header for connecting variable potentiometer on V3=2.5V rail	Installed
J12	2-pin header for connecting ALL loads on V4=1.8V rail (fixed and adjustable)	Installed
J13	2-pin header for connecting variable potentiometer on V4=1.8V rail	Installed

3.3 Development Kit (DVK) Compatibility

This kit contains an expansion board only and requires a Cypress development kit platform in order to use it. This kit is compatible with both the CY8CKIT-001 PSoC DVK and the CY8CKIT-030 PSoC 3 DVK.

NOTE: *Early revisions of the CY8CKIT-001 PSoC Development Kit contained an early engineering sample release (ES2) of the PSoC 3 CY8C38xxx Device Family Processor Module which is not compatible with the example projects that accompany this kit. If you have an early revision of the kit you can upgrade free of charge at www.cypress.com/go/psoc3kitupgrade.*

Chapter 4

Example Projects for the PME

4.1 Introduction

This section provides details on how to operate the hardware and run the example projects provided.

4.2 Software Installation

Perform the following steps to install the PSoC PME EBK software:
Insert the kit CD into the CD drive of your PC. The CD is designed to auto-run and the kit menu should appear. (See Figure 4-1)

Figure 4-1 CD Autorun Kit Menu

NOTE: *If auto-run does not execute, double-click* ***AutoRun*** *on the root directory of the CD. After the installation is complete, the kit contents are available at the following location: C:\Program Files\Terasic\PSoC Power Management EBK\1.0*

When installing the PSoC Power Management EBK software, the installer checks if your system has the required software. This includes PSoC Creator, PSoC Programmer, Windows Installer, .NET framework, Adobe Acrobat Reader, and KEIL Compiler. If these applications are not installed, then the installer prompts you to install all pre-requisite software, which is also available on the kit CD. The software can be uninstalled using one of the following methods:

- Go to **Start > Control Panel > Add or Remove Programs**; select appropriate software package; select the **Remove** button.
- Go to **Start > All Programs > Cypress > Cypress Update Manager > Cypress Update Manager**; select the Uninstall button for the appropriate software package.
- Insert the kit CD and click **Install the kit contents from CD** button. In the **CyInstaller for PSoC Power Management EBK 1.0 window**, select **Remove** from the Installation Type drop-down menu. Follow the instructions to uninstall. (**NOTE:** *this method will only un install the kit software and not all the other material/software that may have been installed along with the kit software*)

4.3 Hardware Setup

The kit includes example projects for both the CY8CKIT-001 PSoC DVK and the CY8CKIT-030 PSoC 3 DVK hardware platforms. The main difference between the projects for the two hardware platforms is the PSoC pin mapping. Other differences will be highlighted in the sections that describe details of the example projects. The following sections describe how to set up the hardware to run the example projects. For a given DVK base platform, the same hardware configuration applies to both example projects.

■ CY8CKIT-001 PSoC DVK

1. Using the pin header/breadboard area of the PSoC DVK base board, use jumper wires to make the following connections:

   - "SW1" to P1_4
   - "SW2" to P1_5

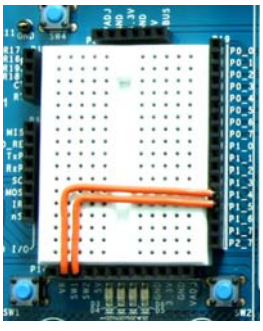

Figure 4-2 CY8CKIT-001 PSoC DVK Breadboard

2. Set the system to run at 5V using SW3 and set J6 “VDD DIG” and J7 “VDD ANLG” to VDD=5V using J6 and J7 as shown below:

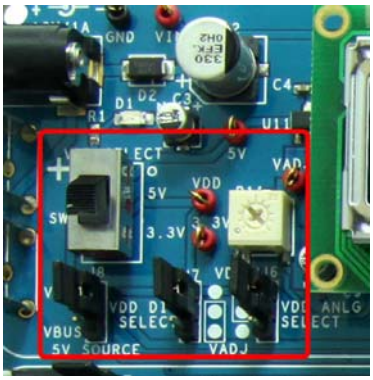

Figure 4-3 CY8CKIT-001 PSoC DVK Power Jumpers

3. Ensure that the LCD character display included with PSoC DVK is attached and that the LCD power jumper (J12) is in the ON position:

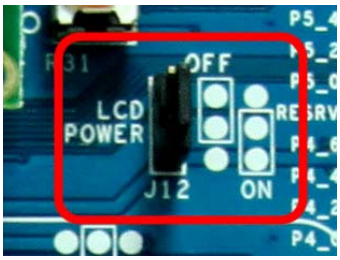

Figure 4-4 CY8CKIT-001 PSoC DVK LCD Power Jumper

CAUTION: *Do not attach the PSoC Power Management EBK to the PSoC DVK until you have programmed the PSoC with one of the example projects. The GPIOs routed to the PSoC Power Management EBK connect to the power regulator circuits which may be damaged if firmware previously programmed into PSoC drives those pins. Once the PSoC has been programmed, attach the PSoC Power Management EBK to PORT A of the PSoC DVK.*

■ CY8CKIT-030 PSoC 3 DVK

1. No jumper wires are required for the PSoC 3 DVK examples since the buttons and potentiometer are hardwired to GPIOs. Ensure that the LCD character display included with the PSoC 3 DVK is attached.

2. Set VDDD and VDDA to 5.0V using J10 and J11

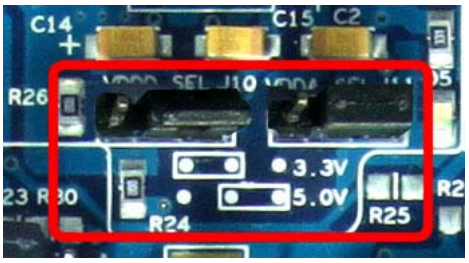

Figure 4-5 CY8CKIT-030 PSoC 3 DVK Power Jumpers

CAUTION: *Do not attach the PSoC Power Management EBK to the PSoC 3 DVK until you have programmed the PSoC with one of the example projects. The GPIOs routed to the PSoC Power Management EBK connect to the power regulator circuits which may be damaged if firmware previously programmed into PSoC drives those pins. Once the PSoC has been programmed, attach the PSoC Power Management EBK to PORT E of the PSoC 3 DVK.*

4.4 Example Projects

The PSoC Power Management EBK includes two example projects:
1. Advanced Sequencer
2. Power Supervisor

The kit includes project workspaces for both the CY8CKIT-001 PSoC DVK and the CY8CKIT-030 PSoC 3 DVK.

To begin, go to the ***Start Page*** in PSoC Creator and under the ***Examples and Tutorials*** section, expand the ***Kits and Solutions*** entry as shown below. Expand the PSoC Power Management EBK entry and double click on the workspace file that matches your development kit (***CY8CKIT-001_Examples.cywrk*** or ***CY8CKIT-030_Examples.cywrk)***. The example projects will be copied to any location you specify on your hard drive and then opened automatically.

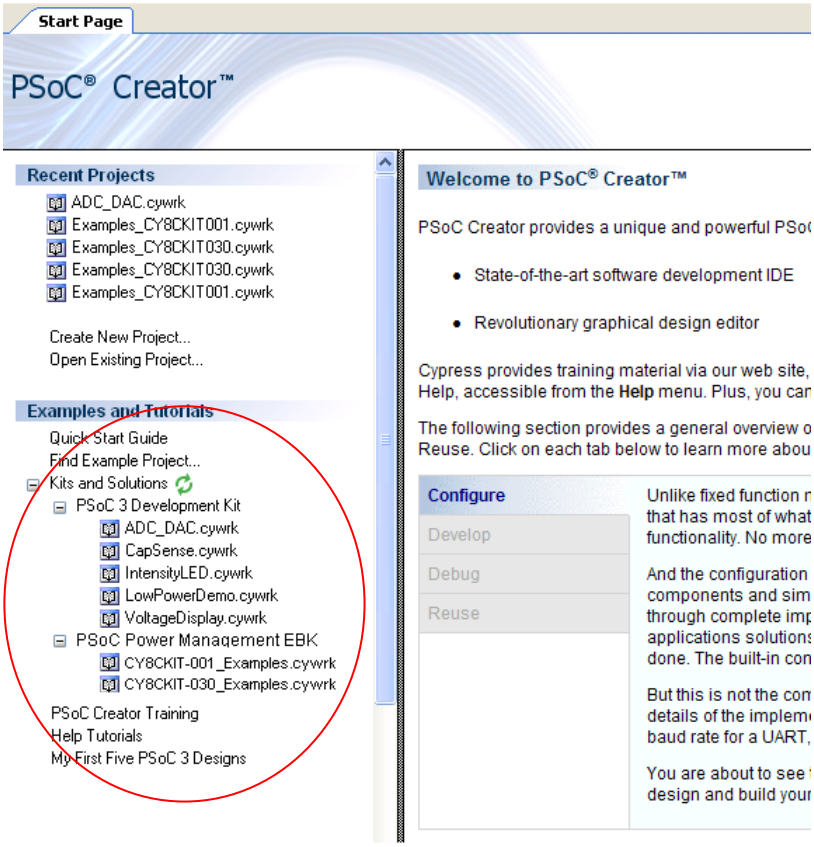

Figure 4-6 PSoC Creator Start Page showing Kits and Solutions

The example projects will be displayed in the ***Workspace Explorer*** window as shown in the example below for the CY8CKIT-001 PSoC DVK:

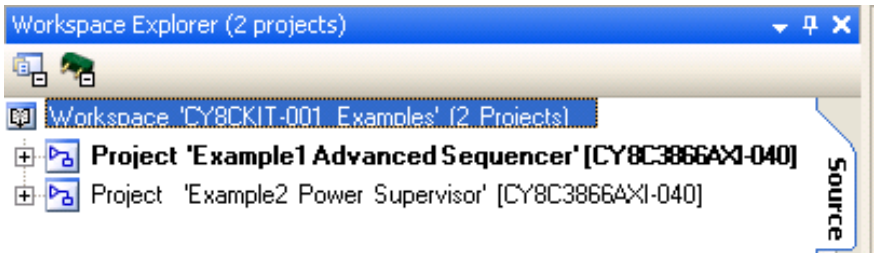

Figure 4-7 Workspace Explorer View

■ Running the Example Firmware: CY8CKIT-001 PSoC DVK

Make sure the hardware has been configured according to the Hardware Setup section.

1. If this is the first time that the example project firmware is being programmed into PSoC, make sure the PSoC Power Management EBK is not connected to the PSoC DVK
2. Apply 12 VDC power to the PSoC DVK
3. Attach the MiniProg3 first to a USB port on the PC and then to the PROG port on the

CY8CKIT-009 PSoC 3 Processor Module

4. In PSoC Creator, set the appropriate example project as active by right clicking on it in the Workspace Explorer and selecting ***Set As Active Project***
5. In PSoC Creator, select ***Debug*** > ***Program*** to program PSoC
6. Remove power from the PSoC DVK and attach the PSoC Power Management EBK to Port A of the PSoC DVK
7. On the PSoC Power Management EBK board, make sure the power jumper (J5) is set to "DVK" (the default setting)
8. Apply 12 VDC power to the PSoC DVK
9. If the PME EBK cannot be detected by PSoC, status debug messages will be displayed on the LCD to assist with rectifying the problem

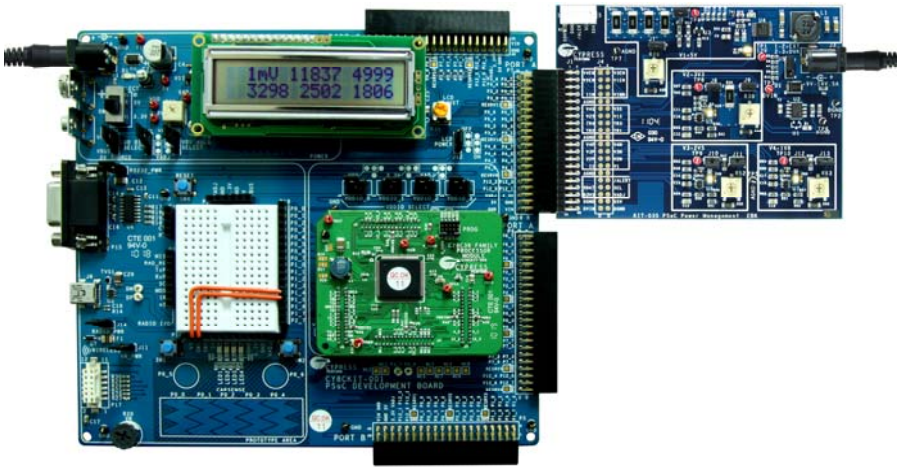

Figure 4-8 CY8CKIT-001 PSoC DVK with PSoC Power Management EBK Connected to Port A (Running Example 2)

■ Running the Example Firmware: CY8CKIT-030 PSoC 3 DVK

Make sure the hardware has been configured according to the Hardware Setup section.

1. If this is the first time that the example project firmware is being programmed into PSoC, make sure the PSoC Power Management EBK is not connected to the PSoC 3 DVK
2. Attach a USB cable from the PC to the PSoC 3 DVK Program/Debug USB port (use J1 - the USB connector closest to the corner of the board)
3. In PSoC Creator, set the appropriate example project as active by right clicking on it in the Workspace Explorer and selecting Set As Active Project
4. In PSoC Creator, select ***Debug*** > ***Program*** to program PSoC
5. Remove the USB cable from the PSoC 3 DVK and attach the PSoC Power Management EBK to Port E of the PSoC 3 DVK

6. On the PSoC Power Management EBK board, make sure the power jumper (J5) is set to “EXT”. Note that this is not the default setting for the J5 jumper.
7. Apply 12 VDC power to the PSoC Power Management EBK using J3
8. Re-attach the USB cable from the PC to the PSoC 3 DVK Program/Debug USB port (use J1 - the USB connector closest to the corner of the board)
9. If the PME EBK cannot be detected by PSoC, status debug messages will be displayed on the LCD to assist with rectifying the problem
10. Going forward, every time PSoC is re-programmed, press the Reset (SW1) button on the PSoC 3 DVK to run the newly programmed firmware image

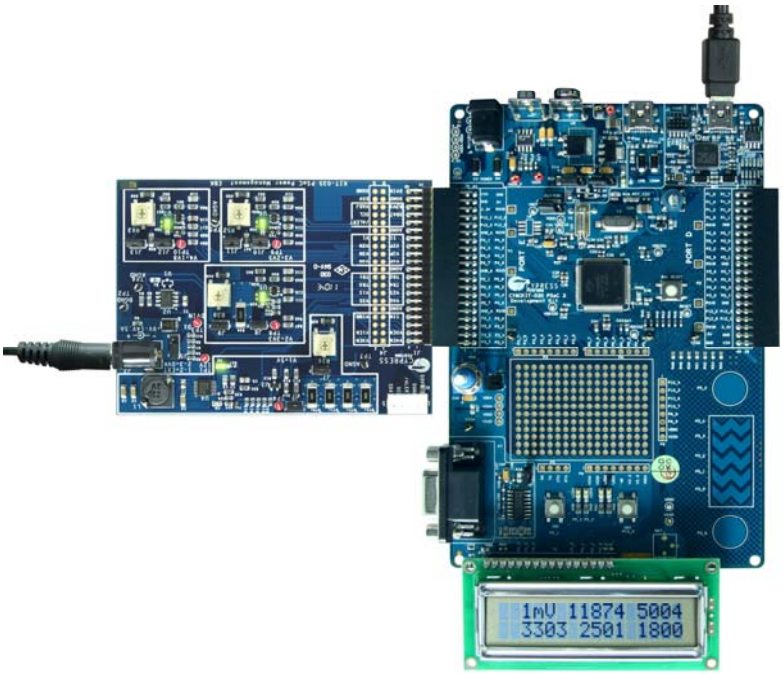

Figure 4-9 CY8CKIT-030 PSoC 3 DVK with PSoC Power Management EBK Connected to Port E (Running Example 2)

■ Example 1: Advanced Sequencer

Overview

This example demonstrates the following features:
1. Voltage sequencing
2. Under-voltage/over-voltage monitoring using the window comparator for rapid fault detection

If the project is running correctly, all 4 green LEDs on the PSoC Power Management EBK should be turned on and the debug LCD should display something like this: (See **Figure 4-10**)

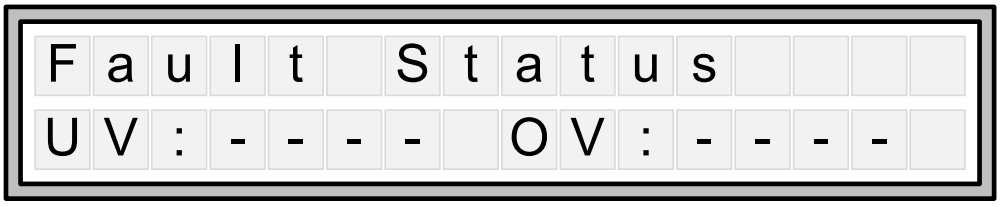

Figure 4-10 Example1 - LCD Display for Normal Operation

The 4 digits indicate the rail failure status (under-voltage=UV or over-voltage=OV). A dash '-' indicates that the rail is within defined operating limits (+/- 7.5% of nominal voltage). If a failure occurs on any rail, the rail number will be displayed next to the UV or OV indicator. For example, if you remove jumper J6, then you will remove power to regulators 2 through 4. This should cause an under-voltage (UV) fault on rails 2 through 4. In that case, the display should look like this: (see **Figure 4-11**)

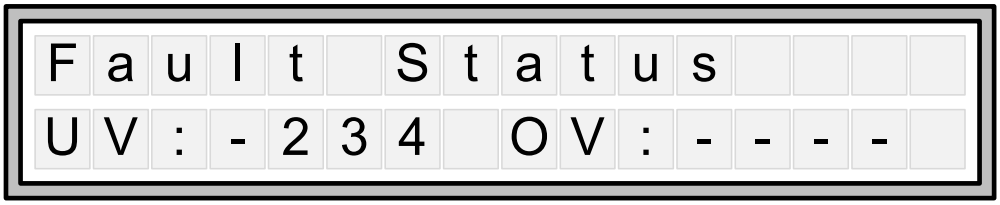

Figure 4-11 Example1 - LCD Display when J6 Removed

Note also that the ***Voltage Sequencer*** component has been configured to shut down all rails on any fault condition, so all 4 green LEDs on PME EBK should turn off when jumper J6 is removed. Changing this default behavior will be described in the next section. To power up the sequencer again, replace J6 and then press and hold the retry switch (SW2 on the CY8CKIT-001 PSoC DVK and SW3 on the CY8CKIT-030 PSoC 3 DVK).

Technical Details – Voltage Sequencing

This example builds upon the ***Voltage Sequencer*** component discussed in Cypress Application Note AN62496 "Voltage Sequencing with PSoC® 3 and PSoC® 5". The ***Voltage Sequencer*** component enables designers to control both the power-up and power-down sequence and timing of up to 16 secondary-side voltage supplies. It is designed to interface to regulators that provide a digital power good (PGOOD) status output. In this example project, the regulators on the PSoC Power Management EBK are monitored using the under-voltage/over-voltage window comparator logic inside PSoC with programmable thresholds on each rail which generate equivalent PGOOD signals internally that connect to the ***Voltage Sequencer*** component. (See **Figure 4-12**)

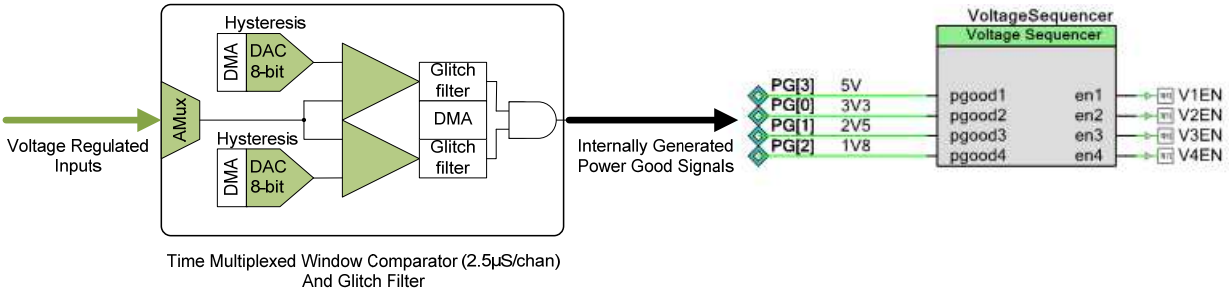

Figure 4-12 Advanced Sequencer Architecture

To change the behavior of the sequencer, double click on the ***Voltage Sequencer*** in the Example1 top-level design schematic file. (See **Figure 4-13**)

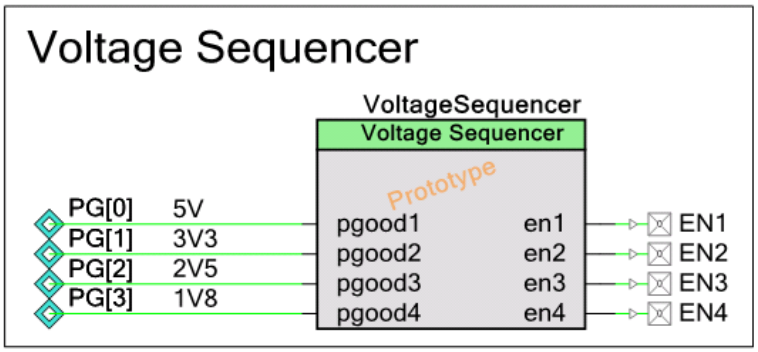

Figure 4-13 Voltage Sequencer Component

This will open the component customizer for the ***Voltage Sequencer***. The ***General Tab*** will be presented first by default. (See **Figure 4-14**)

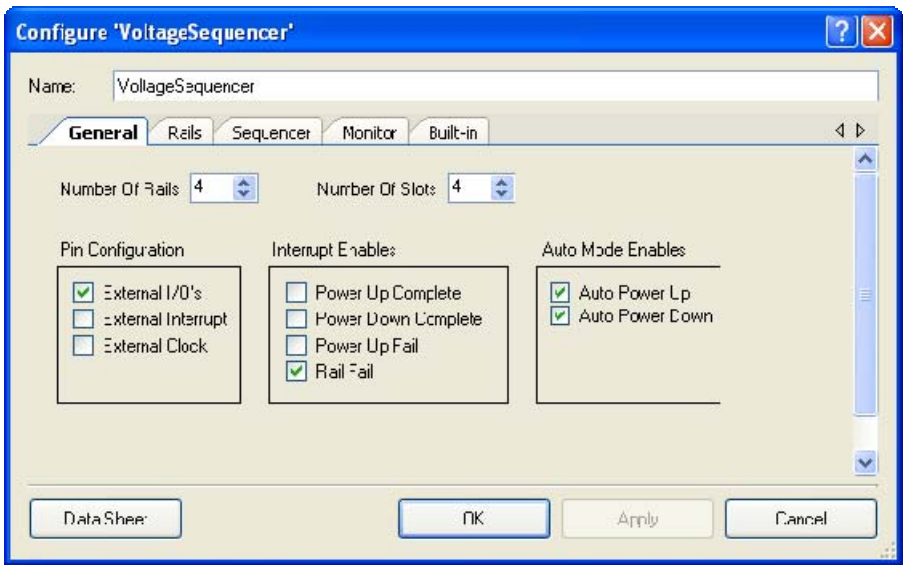

Figure 4-14 Voltage Sequencer Customizer General Tab

For this example project, the key parameter settings are the number of rails (4), Auto Power Up and Auto Power Down settings and Rail Fail interrupts. Those settings enable the component to automatically sequence the regulators up and down with minimal firmware. Refer to AN62496 for full details of the configuration options presented here.

Click on the ***Rails Tab*** to setup the voltage regulator controls, primarily used in this example project to set the polarity of the regulator enable signals to active high for compatibility with the regulators installed on the PSoC Power Management EBK. (See **Figure 4-15**)

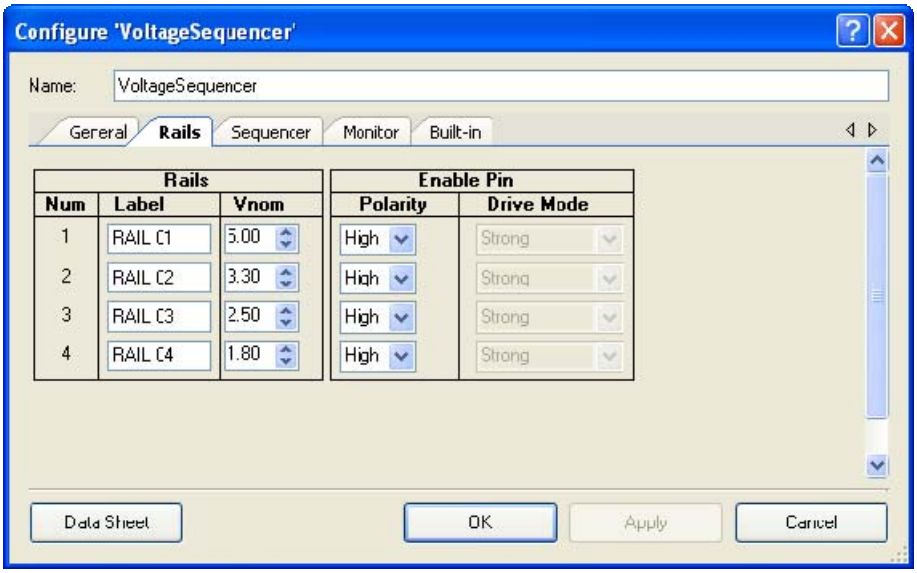

Figure 4-15 Voltage Sequencer Customizer Rails Tab

Click on the ***Sequencer Tab*** to configure the sequencing options. In this example project, each rail is assigned its own sequencing time slot. The matrix of checkboxes currently shows that timing slot

1 is associated with regulator 1. Timing slot 2 with regulator 2 etc. Changing the checkbox assignments will change the sequence of powering up the regulators on PME EBK. Since rails 2 through 4 derive their input power from the output of regulator 1 (this is a hardwired connection on PME EBK), we will always need to power up rail 1 first. Therefore, the checkbox assigning rail 1 to slot 1 will always need to be assigned that way when working with the PME EBK. Feel free to re-configure the power-up sequence of the other 3 rails (V2 through V4).

The timing of the power-up sequence is controlled by the ***Ramp*** and ***Up Delay*** parameters both expressed in units of 1 ms (**NOTE:** *this unit is customizable. Refer to Cypress application note AN62496* for more details). The ***Ramp*** parameter defines how long the Voltage Sequencer should wait after enabling a regulator before checking for pass or fail on the PGOOD input. The ***Up Delay*** parameter defines how long the ***Voltage Sequencer*** should wait once the timing slot has powered-up successfully before moving on to the next timing slot. This provides external components powered by the regulator the time needed to power up and initialize properly before moving to the next power/timing slot. (See **Figure 4-16** below for the correct configuration).

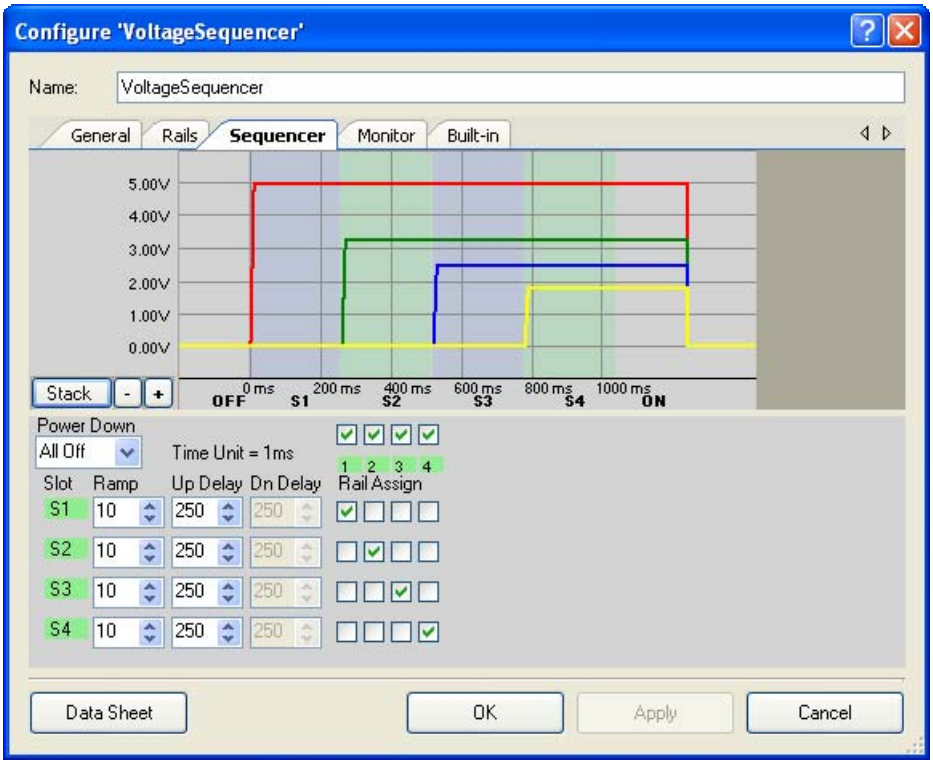

Figure 4-16 Voltage Sequencer Customizer Sequencer Tab

The ***Power Down*** pull-down menu control specifies how the regulators should be turned off in case of fault or system power down. The ***All Off*** setting sets it to simultaneous shutdown. ***Forward*** and ***Reverse*** are 2 other built-in options that enable designers to control the power-down sequence and timing (controlled by the ***Dn Delay*** parameter). The chart in the upper part of this tab displays the current sequencer configuration for visual confirmation that the settings have been entered correctly.

Finally, click on the ***Monitor Tab*** to configure the rail monitoring options. Setting the ***MonType*** parameter to ***PGood*** will cause the sequencer to shut down when there is any failure on that rail. Setting it to ***None*** will cause the sequencer to ignore the ***PGood*** status on that rail. Changing the ***MonType*** to ***None*** for Rails 2, 3 and 4 will prevent the sequencer from shutting down the regulators when jumper J6 is removed from PME EBK, for example. This will also prevent the system from reacting to UV and OV faults. Faults can still be reported and logged. (See **Figure 4-17**)

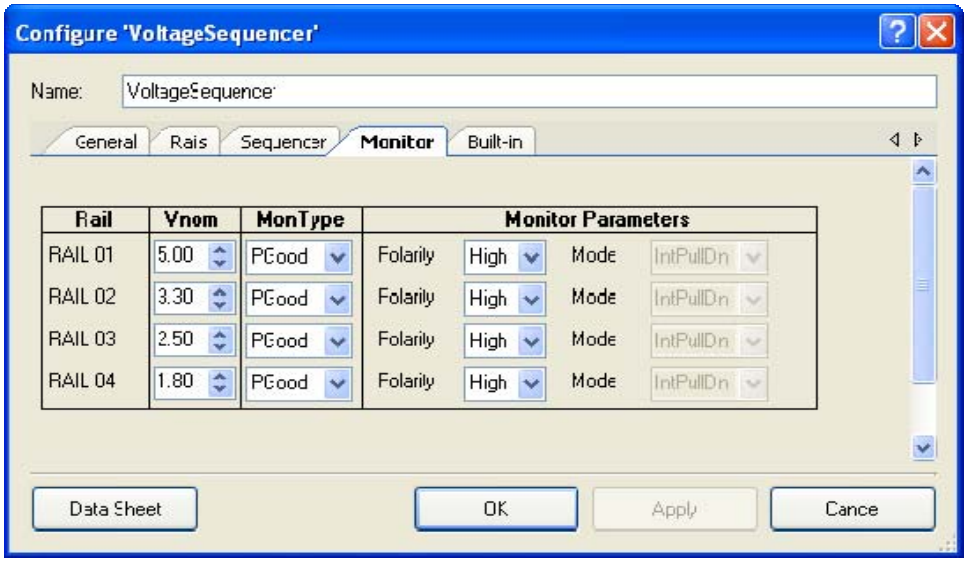

Figure 4-17 Voltage Sequencer Customizer Monitor Tab

Technical Details – Under-voltage/Over-voltage Monitoring using the Window Comparator

To support over-voltage and under-voltage detection on the four secondary power supply rails, eight comparators and eight programmable DACs would be required. As the number of regulators in the systems expands, the number of comparators and DACs required becomes excessive. To make more efficient use of analog hardware resources, an alternative implementation has been implemented based on the idea presented in Application Note AN60220 "Multiplexed Comparator using PSoC® 3".

As shown below, a single window comparator and glitch filter are rapidly time-multiplexed across all the rails requiring monitoring at the rate of approximately 2 µs per channel. (See **Figure 4-18**). Note the use of DMA controllers to control the under/over-voltage DACs and the glitch comparator circuits. The DMA controllers inside PSoC are extremely versatile and are able to transfer between SRAM, peripherals and non-volatile flash memory in any combination. Since the window comparator performs a time-critical fault detection function, it is highly desirable to have that block function with zero interaction with the CPU. The DMA controllers make that happen. Exactly how the DMA controllers are used is described on the next page.