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VEEK

User Manual

Video & Embedded Evaluation Kit

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CONTENTS

Chapter 1

Introduction of the VEEK

The VEEK FPGA Development Kit is a comprehensive design environment with everything embedded developers need to create processing-based systems. The VEEK delivers an integrated platform that includes hardware, design tools, intellectual property (IP) and reference designs for developing embedded software and hardware platform in a wide range of applications. The fully integrated kit allows developers to rapidly customize their processor and IP to best suit their specific application. The VEEK features the DE2-115 development board targeting the Cyclone IV E FPGA, as well as a LCD multimedia color touch panel and a 5-Megapixel digital image sensor module.

The VEEK is preconfigured with an FPGA hardware reference design including several Ready-to-Run demonstration applications stored on the provided SD-Card. Software developers can use these reference designs as their platform to quickly architect, develop and build complex embedded systems. By simply scrolling through the demo of your choice on the LCD multimedia color touch panel, you can evaluate numerous processor system designs.

The all-in-one embedded solution offered on the VEEK, in combination of the LCD touch panel and digital image module, provide embedded developers the ideal platform for multimedia applications with unparallel processing performance. Developers can benefit from the use of FPGA-based embedded processing system such as mitigate design risk and obsolescence, design reuse, reducing bill of material (BOM) costs by integrating powerful graphics engines within the FPGA, and lower cost.

Figure 1-1 shows a photograph of the VEEK.

Figure 1-1 The VEEK overview

The key features of the board are listed below:

■ DE2-115 Development Board

- Cyclone IV EP4CE115 FPGA
  - 114,480 LEs
  - 432 M9K memory blocks
  - 3,888 Kbits embedded memory
  - 4 PLLs
- Configuration
  - On-board USB-Blaster circuitry
  - JTAG and AS mode configuration supported
  - EPCS64 serial configuration device
- Memory Devices
  - 128MB SDRAM
  - 2MB SRAM
  - 8MB Flash with 8-bit mode
  - 32Kbit EEPROM
- Switches and Indicators
  - 18 switches and 4 push-buttons
  - 18 red and 9 green LEDs
  - Eight 7-segment displays

- Audio
  - 24-bit encoder/decoder (CODEC)
  - Line-in, line-out, and microphone-in jacks
- Display
  - 16x2 LCD module
- On-Board Clocking Circuitry
  - Three 50MHz oscillator clock inputs
  - SMA connectors (external clock input/output)
- SD Card Socket
  - Provides SPI and 4-bit SD mode for SD Card access
- Two Gigabit Ethernet Ports
  - Integrated 10/100/1000 Gigabit Ethernet
- High Speed Mezzanine Card (HSMC)
  - Configurable I/O standards (voltage levels: 3.3/2.5/1.8/1.5V)
- USB Type A and B
  - Provide host and device controller compliant with USB 2.0
  - Support data transfer at full-speed and low-speed
  - PC driver available
- 40-pin Expansion Port
  - Configurable I/O standards (voltage levels: 3.3/2.5/1.8/1.5V)
- VGA-out Connector
  - VGA DAC (high speed triple DACs)
- DB9 Serial Connector
  - RS232 port with flow control
- PS/2 Connector
  - PS/2 connector for connecting a PS2 mouse or keyboard
- TV-in Connector
  - TV decoder (NTSC/PAL/SECAM)
- Remote Control
  - Infrared receiver module

- Power
  - Desktop DC input
  - Switching and step-down regulators LM3150MH

■ LCD touch screen module

- Equipped with an 8-inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module
- Module composed of LED backlight
- Support 18-bit parallel RGB interface
- Converting the X/Y coordination of touch point to its corresponding digital data via the Analog Devices AD7843 A/D converter

Table 1-1 shows the general physical specifications of the LTC (Note*).

Table 1-1 General physical specifications of the LCD

Item	*Specification*	*Unit*
LCD size	8 inch (Diagonal)	-
Resolution	800 x3(RGB) x 600	dot
Dot pitch	0.0675(W) x 0.2025(H)	mm
Active area	162.0(W) x 121.5(H)	mm
Module size	183.0(W) x 141.0(H) x 7.2(D)	mm
Surface treatment	Anti-Glare	-
Color arrangement	RGB-stripe	-
Interface	Digital	-

■ 5-Megapixel digital image sensor module

- Superior low-light performance
- High frame rate
- Low dark current
- Global reset release, which starts the exposure of all rows simultaneously
- Bulb exposure mode, for arbitrary exposure times
- Snapshot mode to take frames on demand
- Horizontal and vertical mirror image
- Column and row skip modes to reduce image size without reducing field-of-view
- Column and row binning modes to improve image quality when resizing
- Simple two-wire serial interface
- Programmable controls: gain, frame rate, frame size, exposure

Table 1-2 shows the key parameters of the CMOS sensor (Note*).

Table 1-2 Key performance parameters of the CMOS sensor

Parameter		*Value*
Active Pixels		2592Hx1944V
Pixel size		2.2umx2.2um
Color filter array		RGB Bayer pattern
Shutter type		Global reset release(GRR)
Maximum data rate/master clock		96Mp/s at 96MHz
Frame rate	Full resolution	Programmable up to 15 fps
	VGA mode	Programmable up to 70 fps
ADC resolution		12-bit
Responsivity		1.4V/lux-sec(550nm)
Pixel dynamic range		70.1dB
SNRMAX		38.1dB
Supply Voltage	Power	3.3V
	I/O	1.7V～3.1V

■ Digital Accelerometer

- Up to 13-bit resolution at +/- 16g
- SPI (3- and 4-wire) digital interface
- Flexible interrupts modes

Note: for more detailed information of the LCD touch panel and CMOS sensor module, please refer to their datasheets respectively.

1.1 About the Kit

The kit contains all users needed to run the demonstrations and develop custom designs, as shown in Figure 1-2.

The system CD contains technical documents of the VEEK which includes component datasheets, demonstrations, schematic, and user manual.

Figure 1-2 VEEK kit package contents

1.2 Getting Help

Here is information of how to get help if you encounter any problem:

- Terasic Technologies
- Tel: +886-3-550-8800
- Email: support@terasic.com

Chapter 2

VEEK Architecture

This chapter describes the architecture of the VEEK including block diagram and components.

2.1 Layout and Components

The picture of the VEEK is shown in Figure 2-1 and Figure 2-2. It depicts the layout of the board and indicates the locations of the connectors and key components.

Figure 2-1 VEEK PCB and component diagram (top view)

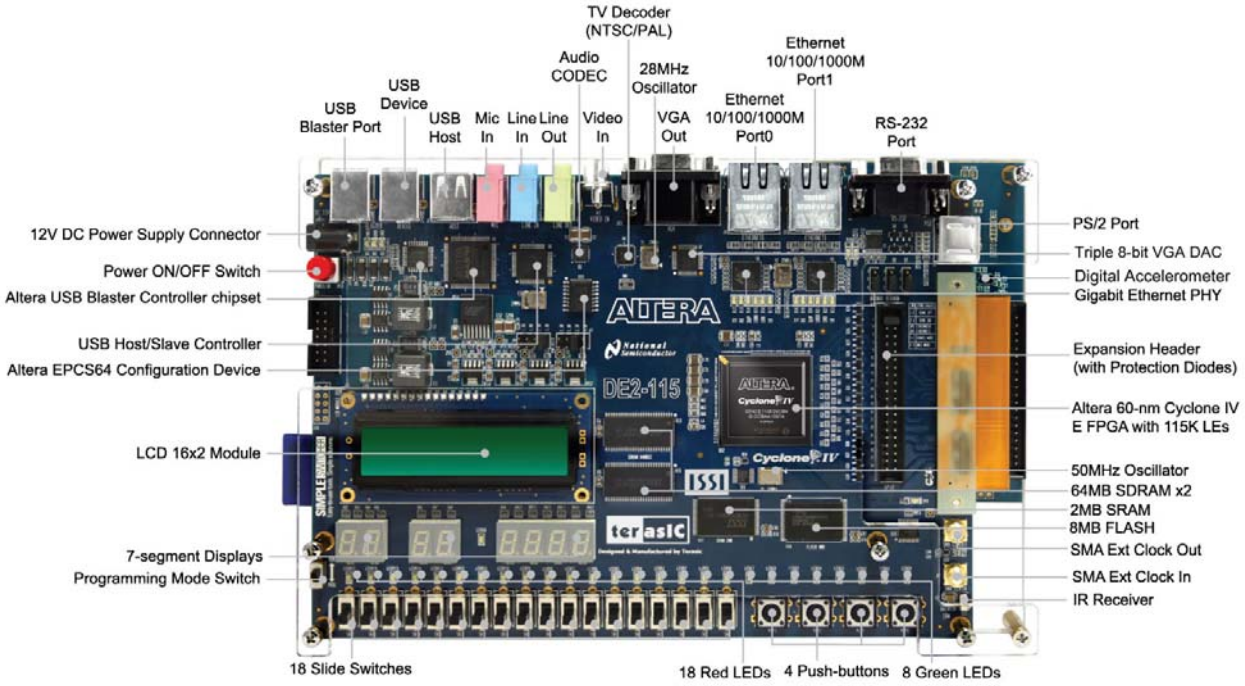

Figure 2-2 VEEK PCB and component diagram (bottom view)

2.2 Block Diagram of the VEEK

Figure 2-3 gives the block diagram of the VEEK board. To provide maximum flexibility for the user, all connections are made through the Cyclone IV E FPGA device. Thus, the user can configure the FPGA to implement any system design.

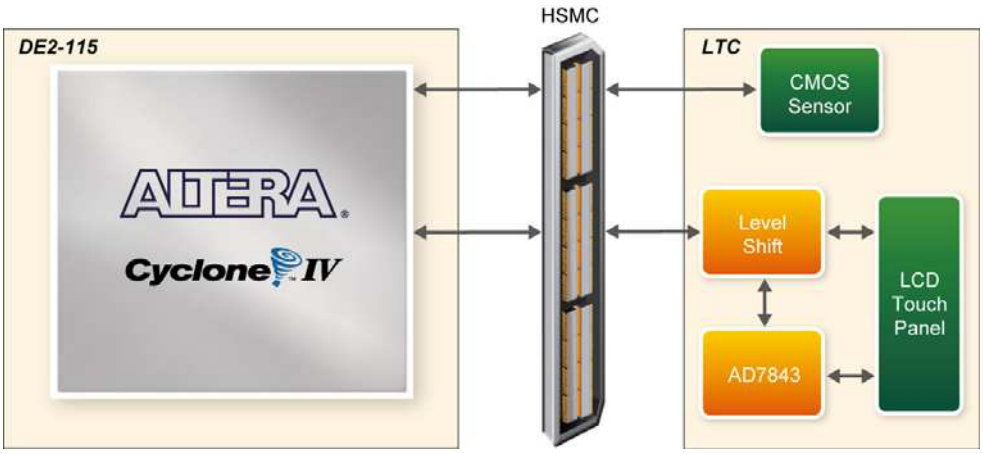

Figure 2-3 Block Diagram of VEEK

Chapter 3

Using the VEEK

This section describes the detailed information of the components, connectors, and pin assignments of the VEEK.

3.1 Configuring the Cyclone IV E FPGA

The VEEK board contains a serial configuration device that stores configuration data for the Cyclone IV E FPGA. This configuration data is automatically loaded from the configuration device into the FPGA every time while power is applied to the board. Using the Quartus II software, it is possible to reconfigure the FPGA at any time, and it is also possible to change the non-volatile data that is stored in the serial configuration device. Both types of programming methods are described below.

1. JTAG programming: In this method of programming, named after the IEEE standards Joint Test Action Group, the configuration bit stream is downloaded directly into the Cyclone IV E FPGA. The FPGA will retain this configuration as long as power is applied to the board; the configuration information will be lost when the power is turned off.
2. AS programming: In this method, called Active Serial programming, the configuration bit stream is downloaded into the Altera EPCS64 serial configuration device. It provides non-volatile storage of the bit stream, so that the information is retained even when the power supply to the VEEK board is turned off. When the board's power is turned on, the configuration data in the EPCS64 device is automatically loaded into the Cyclone IV E FPGA.

■ JTAG Chain on VEEK Board

To use JTAG interface for configuring FPGA device, the JTAG chain on the VEEK must form a close loop that allows Quartus II programmer to detect the FPGA device. **Figure 3-1** illustrates the JTAG chain on the VEEK board. Shorting pin1 and pin2 on JP3 can disable the JTAG signals on the HSMC connector that will form a close JTAG loopback on DE2-115 (See **Figure 3-2**). Thus, only the on board FPGA device (Cyclone IV E) will be detected by Quartus II programmer. By default, a jumper is placed on pin1 and pin2 of JP3. To prevent any changes to the bus controller (Max II EPM240) described in later sections, users should not adjust the jumper on JP3.

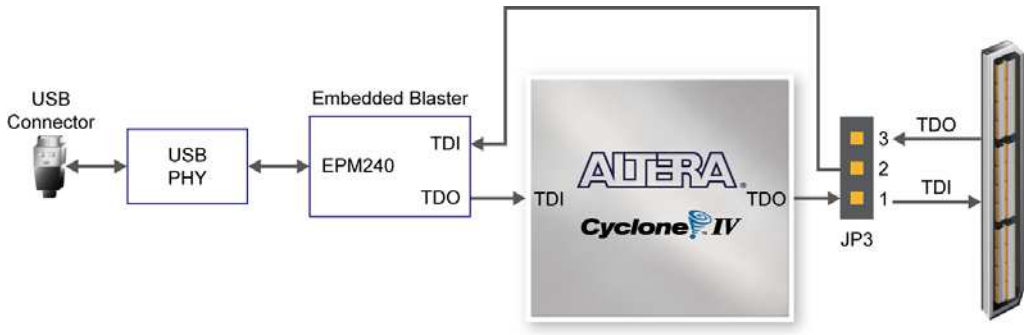

Figure 3-1 JTAG Chain

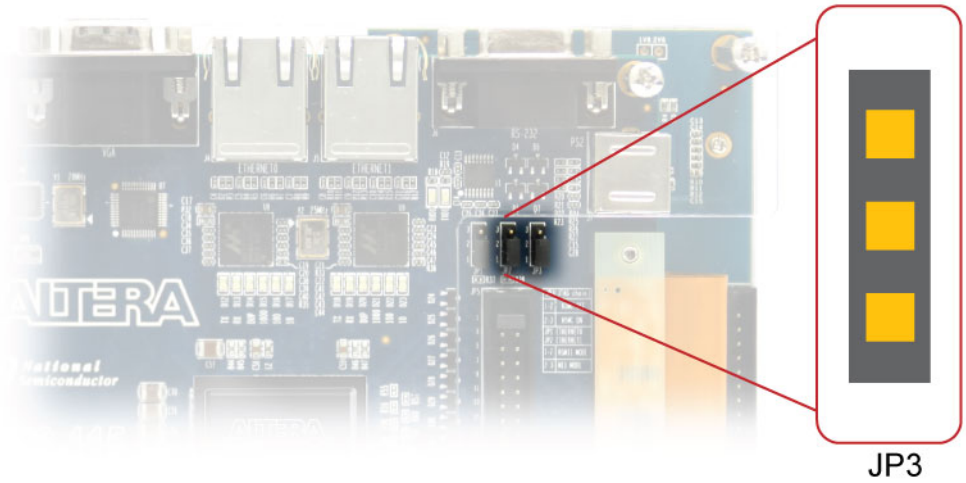

Figure 3-2 The JTAG chain configuration header

■ Configuring the FPGA in JTAG Mode

Figure 3-3 illustrates the JTAG configuration setup. To download a configuration bit stream into the Cyclone IV E FPGA, perform the following steps:

- Ensure that power is applied to the VEEK board
- Configure the JTAG programming circuit by setting the RUN/PROG slide switch (SW19) to the RUN position (See Figure 3-4)
- Connect the supplied USB cable to the USB-Blaster port on the VEEK board
- The FPGA can now be programmed by using the Quartus II Programmer module to select a configuration bit stream file with the .sof filename extension

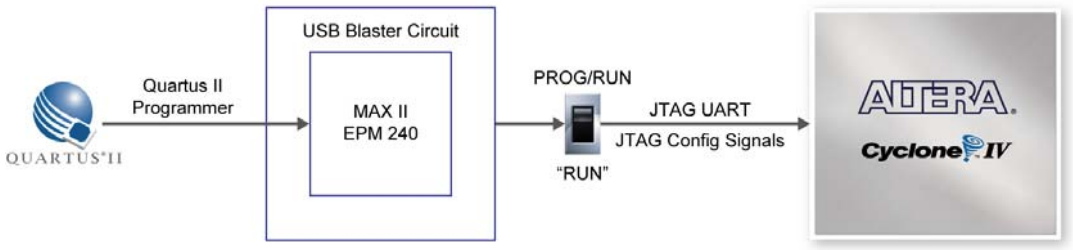

Figure 3-3 The JTAG chain configuration scheme

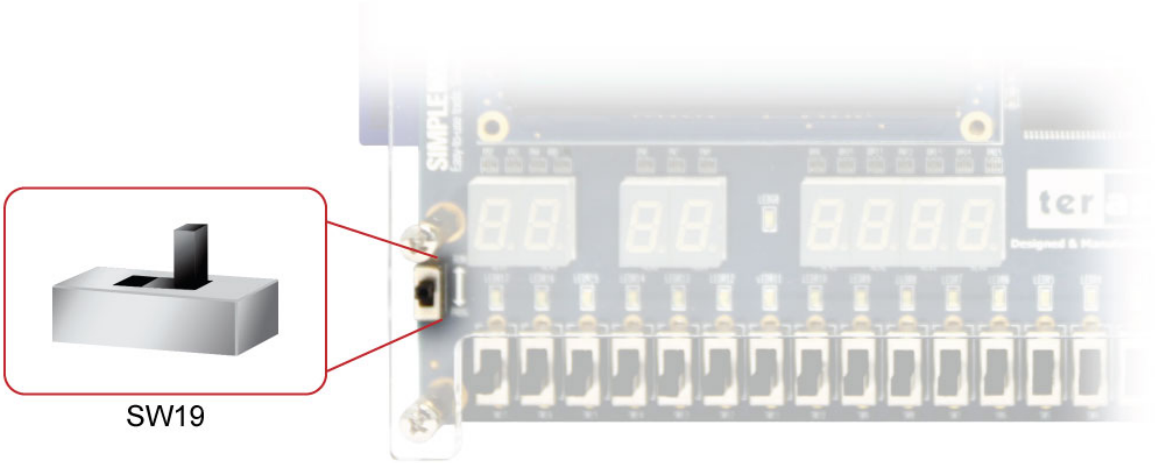

Figure 3-4 The RUN/PROG switch (SW19) is set to JTAG mode

■ Configuring the EPCS64 in AS Mode

Figure 3-5 illustrates the AS configuration set up. To download a configuration bit stream into the EPCS64 serial configuration device, perform the following steps:

- Ensure that power is applied to the VEEK board
- Connect the supplied USB cable to the USB-Blaster port on the VEEK board
- Configure the JTAG programming circuit by setting the RUN/PROG slide switch (SW19) to the PROG position
- The EPCS64 chip can now be programmed by using the Quartus II Programmer module to select a configuration bit stream file with the .pof filename extension
- Once the programming operation is finished, set the RUN/PROG slide switch back to the RUN position and then reset the board by turning the power switch off and back on; this action causes the new configuration data in the EPCS64 device to be loaded into the FPGA chip

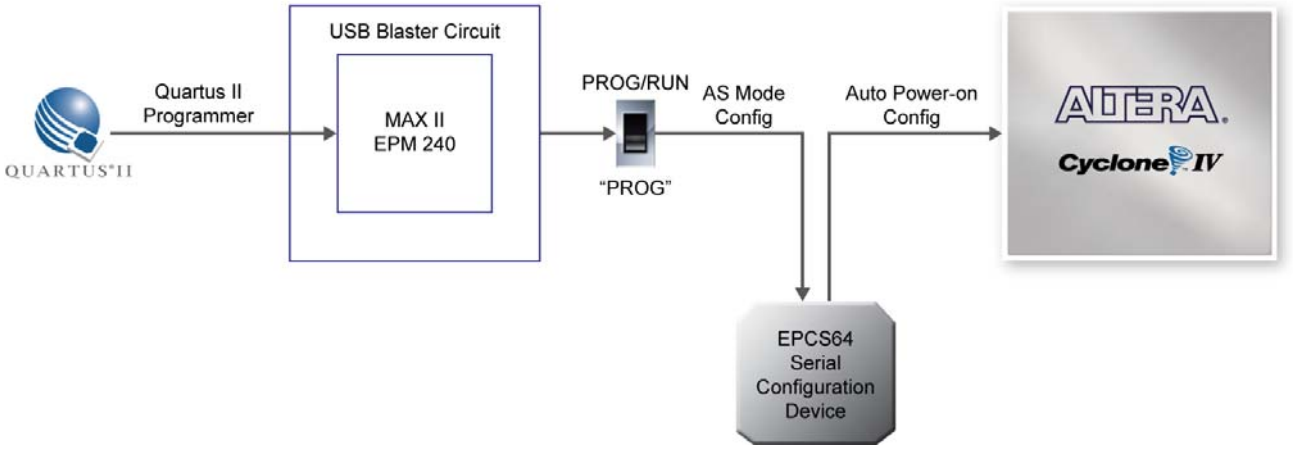

Figure 3-5 The AS configuration scheme

3.2 Bus Controller

The VEEK comes with a bus controller using the Max II EPM240 that allows user to access the touch screen module through the HSMC connector. This section describes its structure in block diagram form and its capabilities.

■ Bus Controller Introduction

The bus controller provides level shifting functionality from 2.5V (HSMC) to 3.3V domains.

■ Block Diagram of the Bus Controller

Figure 3-6 gives the block diagram of the connection setup from the HSMC connector to the bus controller on the Max II EPM240 to the touch screen module. To provide maximum flexibility for the user, all connections are established through the HSMC connector. Thus, the user can configure the Cyclone IV E FPGA on the VEEK to implement any system design.

Figure 3-6 Block Diagram of the Bus Controller

3.3 Using the 8” LCD Touch Screen Module

The VEEK features an 8-inch Amorphous-TFT-LCD panel. The LCD Touch Screen module offers resolution of (800x600) to provide users the best display quality for developing applications. The LCD panel supports 18-bit parallel RGB data interface.

The VEEK is also equipped with an Analog Devices AD7843 touch screen digitizer chip. The AD7843 is a 12-bit analog to digital converter (ADC) for digitizing x and y coordinates of touch points applied to the touch screen. The coordinates of the touch points can be read through the serial port interface on the AD7843.

To display images on the LCD panel correctly, the RGB color data along with the data enable and clock signals must act according to the timing specification of the LCD touch panel as shown in **Table 3-1.**

Table 3-2 gives the pin assignment information of the LCD touch panel.

Table 3-1 LCD timing specifications

Parameter	*Symbol*	*Values*			*Unit*
		Min.	*Typ.*	*Max.*	
CLK Frequency	FCPH	-	39.79	-	MHz
CLK Period	FCPH	-	25.13	-	Ns
CLK Pulse Duty	FCWH	40	50	60	%
DE Period	FDEH+ TDEL	1000	1056	-	TCPH
DE Pulse Width	FDH	-	800	-	TCPH
DE Frame Blanking	FHS	10	28	110	FDEH+TDEL
DE Frame Width	FEP	-	600	-	FDEH+TDEL
OEV Pulse Width	TOEV	-	150	-	TCPH
OKV Pulse Width	TCKV	-	133	-	TCPH
DE(internal)-STV Time	T1	-	4	-	TCPH
DE(internal)-CKV Time	T2	-	40	-	TCPH
DE(internal)-OEV Time	T3	-	23	-	TCPH
DE(internal)-POL Time	T4	-	157	-	TCPH
STV Pulse Width	-	-	1	-	TH
Note: THS + THA < TH					

Table 3-2 Pin assignment of the LCD touch panel

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
LCD_DIM	PIN_P27	LCD backlight enable	2.5V
LCD_NCLK	PIN_V24	LCD clock	2.5V
LCD_R0	PIN_V26	LCD red data bus bit 0	2.5V
LCD_R1	PIN_R27	LCD red data bus bit 1	2.5V

LCD_R2	PIN_R28	LCD red data bus bit 2	2.5V
LCD_R3	PIN_U27	LCD red data bus bit 3	2.5V
LCD_R4	PIN_U28	LCD red data bus bit 4	2.5V
LCD_R5	PIN_V27	LCD red data bus bit 5	2.5V
LCD_G0	PIN_P21	LCD green data bus bit 0	2.5V
LCD_G1	PIN_R21	LCD green data bus bit 1	2.5V
LCD_G2	PIN_R22	LCD green data bus bit 2	2.5V
LCD_G3	PIN_R23	LCD green data bus bit 3	2.5V
LCD_G4	PIN_T21	LCD green data bus bit 4	2.5V
LCD_G5	PIN_T22	LCD green data bus bit 5	2.5V
LCD_B0	PIN_V28	LCD blue data bus bit 0	2.5V
LCD_B1	PIN_U22	LCD blue data bus bit 1	2.5V
LCD_B2	PIN_V22	LCD blue data bus bit 2	2.5V
LCD_B3	PIN_V25	LCD blue data bus bit 3	2.5V
LCD_B4	PIN_L28	LCD blue data bus bit 4	2.5V
LCD_B5	PIN_J26	LCD blue data bus bit 5	2.5V
LCD _DEN	PIN_P25	LCD RGB data enable	2.5V
TOUCH _PENIRQ_N	PIN_L22	AD7843 pen interrupt	2.5V
TOUCH _DOUT	PIN_L21	AD7843 serial interface data out	2.5V
TOUCH _BUSY	PIN_U26	AD7843 serial interface busy	2.5V
TOUCH _DIN	PIN_U25	AD7843 serial interface data in	2.5V
TOUCH _CS_N	PIN_T26	AD7843 serial interface chip select input	2.5V
TOUCH _DCLK	PIN_T25	AD7843 interface clock	2.5V

3.4 Using 5-Megapixel Digital Image Sensor Module

The VEEK is equipped with a 5-Megapixel digital image sensor module that provides an active imaging array of 2,592H x 1,944V. It features low-noise CMOS imaging technology that achieves CCD image quality. In addition, it incorporates sophisticated camera functions on-chip such as windowing, column and row skip mode, and snapshot mode.

The sensor can be operated in its default mode or programmed by the user through a simple two-wire serial interface for frame size, exposure, gain settings, and other parameters. Table 3-3 contains the pin names and descriptions of the image sensor module.

Table 3-3 Pin assignment of the CMOS sensor

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
CAMERA_ PIXCLK	PIN_J27	Pixel clock	2.5V
CAMERA_ D0	PIN_F26	Pixel data bit 0	2.5V
CAMERA_ D1	PIN_E26	Pixel data bit 1	2.5V
CAMERA_ D2	PIN_G25	Pixel data bit 2	2.5V

CAMERA_ D3	PIN_G26	Pixel data bit 3	2.5V
CAMERA_ D4	PIN_H25	Pixel data bit 4	2.5V
CAMERA_ D5	PIN_H26	Pixel data bit 5	2.5V
CAMERA_ D6	PIN_K25	Pixel data bit 6	2.5V
CAMERA_ D7	PIN_K26	Pixel data bit 7	2.5V
CAMERA_ D8	PIN_L23	Pixel data bit 8	2.5V
CAMERA_ D9	PIN_L24	Pixel data bit 9	2.5V
CAMERA_ D10	PIN_M25	Pixel data bit 10	2.5V
CAMERA_ D11	PIN_M26	Pixel data bit 11	2.5V
CAMERA_ STROBE	PIN_G28	Snapshot strobe	2.5V
CAMERA_ LVAL	PIN_K27	Line valid	2.5V
CAMERA_ FVAL	PIN_K28	Frame valid	2.5V
CAMERA_ RESET_N	PIN_M28	Image sensor reset	2.5V
CAMERA_ SCLK	PIN_K22	Serial clock	2.5V
CAMERA_ TRIGGER	PIN_H23	Snapshot trigger	2.5V
CAMERA_ SDATA	PIN_H24	Serial data	2.5V
CAMERA_ XCLKIN	PIN_G23	External input clock	2.5V

3.5 Using the Digital Accelerometer

The VEEK is equipped with a digital accelerometer sensor module, the ADXL345 is a small, thin, ultralow power assumption 3-axis accelerometer with high resolution measurement. Digitalized output is formatted as 16-bit twos complement and could be accessed either using SPI interface or I2C interface. This chip uses the 3.3V CMOS signaling standard. Main applications include medical instrumentation, industrial instrumentation, personal electronic aid and hard disk drive protection etc. Some of the key features of this device are listed below. For more detailed information of better using this chip, please refer to its datasheet which is available on manufacturer's website or under the /datasheet folder of the system CD.Table 3-4 contains the pin names and descriptions of the G sensor module.

Table 3-4 Pin assignment of the Digital Accelerometer

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
GSENSOR_INT1	PIN_AE26	Interrupt 1 output	2.5V
GSENSOR_INT2	PIN_AE27	Interrupt 2 output	2.5V
GSENSOR_CS_n	PIN_D28	Chip Select	2.5V
GSENSOR_ALT_ADDR	PIN_E27	I2C Address Select	2.5V
GSENSOR_SDA_SDI_SDIO	PIN_E28	Serial Data	2.5V
GSENSOR_SCL_SCLK	PIN_F27	Serial Communications Clock	2.5V

Chapter 4

VEEK Demonstrations

This chapter gives detailed description of the provided bundles of exclusive demonstrations implemented on VEEK. These demonstrations are particularly designed (or ported) for VEEK, with the goal of showing the potential capabilities of the kit and showcase the unique benefits of FPGA-based SOPC systems such as reducing BOM costs by integrating powerful graphics and video processing circuits within the FPGA.

4.1 System Requirements

To run and recompile the demonstrations, you should:

- Install Altera Quartus II 10.0 and NIOS II EDS 10.0 or later edition on the host computer
- Install the USB-Blaster driver software. You can find instructions in the tutorial "Getting Started with Altera's DE2-115 Board" (tut_initialDE2-115.pdf) which is available on the DE2-115 system CD
- Copy the entire demonstrations folder from the VEEK system CD to your host computer

4.2 Factory Configuration

The VEEK development kit comes preconfigured with a default utility that boots up on power on and allows users to quickly select, load, and run different Ready-to-Run demonstrations stored on an SD Card using the VEEK touch panel. **Figure 4-1** gives a snapshot of the default application selector interface (Note*). Every demonstration consists of a FPGA hardware image and an application software image. When you select a demonstration the application selector copies the hardware image to EPCS device and software image to flash memory and reconfigures the FPGA with your selection. For more comprehensive information of the application selector factory configuration, please refer to chapter 5.

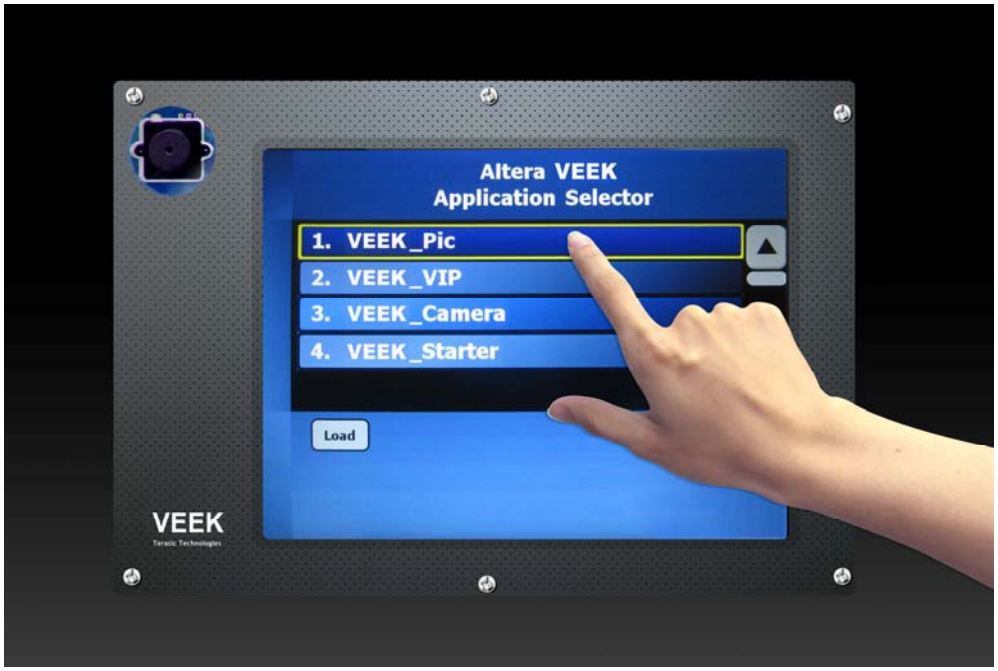

Figure 4-1 Application selector interface

Note: Please insert the supplied SD Card from this demonstration.

4.3 VEEK Starter Demonstration

The VEEK starter demonstration takes user the initial experience of an embedded system integrating a LCD Touch Panel. This demonstration consists of two sub item, Touch and Color pattern generator. The Touch segment draws a circle on where you touch the screen and updates its coordinates on the top left corner. The pattern generator can be treated as an upgrade version of the LCD test program. The software successively generates different color patterns after a fixed time delay. Users could use it to quickly investigate any flaw of the LCD.

Figure 4-2 shows the hardware system block diagram of this demonstration. The system is clocked by an external 50MHz Oscillator. Through the internal PLL module, the generated 100MHz clock is used for Nios II processor and other components, and there also a 40MHz pixel clock for the video pipeline and 10MHz for low-speed peripherals. The Nios II CPU runs the application software and controls all the peripherals. A scatter-gather DMA is used to transfer pixel data from the video buffer to the video pipeline.

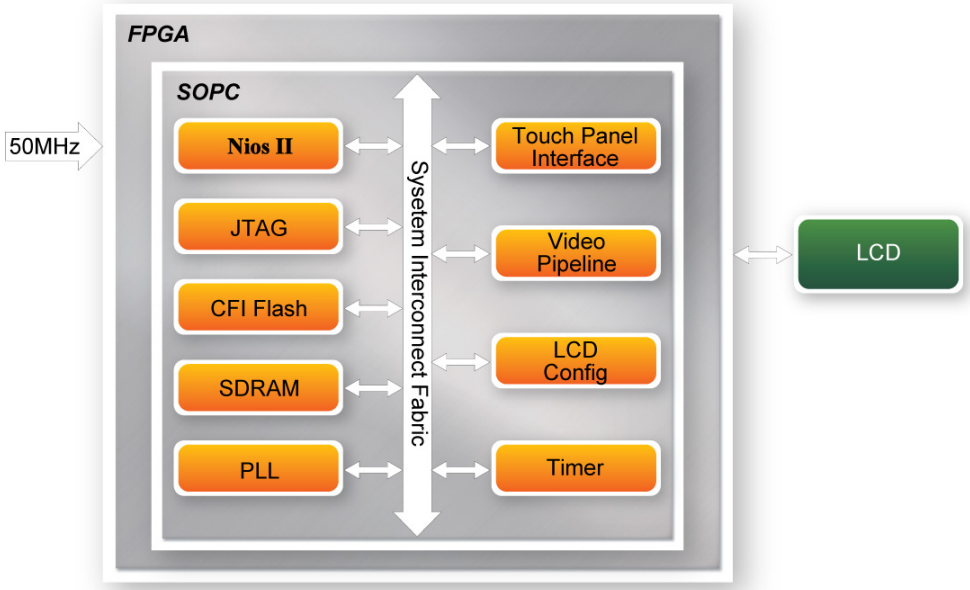

Figure 4-2 Block diagram of the VEEK Starter demonstration

Figure 4-3 illustrates the software structure of this demonstration. The touch panel's SPI HAL block responds to the bottom hardware requests and interface to upper layers. The SGDMA HAL allocates required frame/descriptor buffers to specified memory address and is responsible of handling frame buffer update issue.

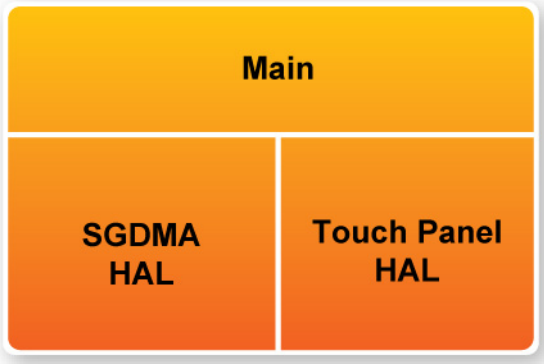

Figure 4-3 Software stack of the VEEK Starter demonstration

■ Demonstration Source Code

- Project directory: VEEK_Starter
- Bit stream used: VEEK_Starter.sof
- Nios II Workspace: VEEK_Starter\Software

■ Demonstration Batch File

Demo Batch File Folder:VEEK_Starter\demo_batch

The demo batch file includes the following files:

- Batch File: VEEK_Starter.bat, VEEK_Starter_bashrc
- FPGA Configure File: VEEK_Starter.sof
- Nios II Program: VEEK_Starter.elf

■ Demonstration Setup

- Make sure Quartus II and Nios II are installed on your PC
- Power on the DE2-115 board
- Connect USB-Blaster to the DE2-115 board and install USB-Blaster driver if necessary
- Execute the demo batch file "VEEK_Starter.bat" under the batch file folder, VEEK_Starter\demo_batch
- After Nios II program is downloaded and executed successfully, a prompt message will be displayed in nios2-terminal
- From on the touch panel, tap any icon of the main interface and start the experience, as shown in **Figure 4-4, Figure 4-5** and **Figure 4-6**
- Under each sub item, touch the **Exit** button on the left bottom corner will lead you back to the main interface

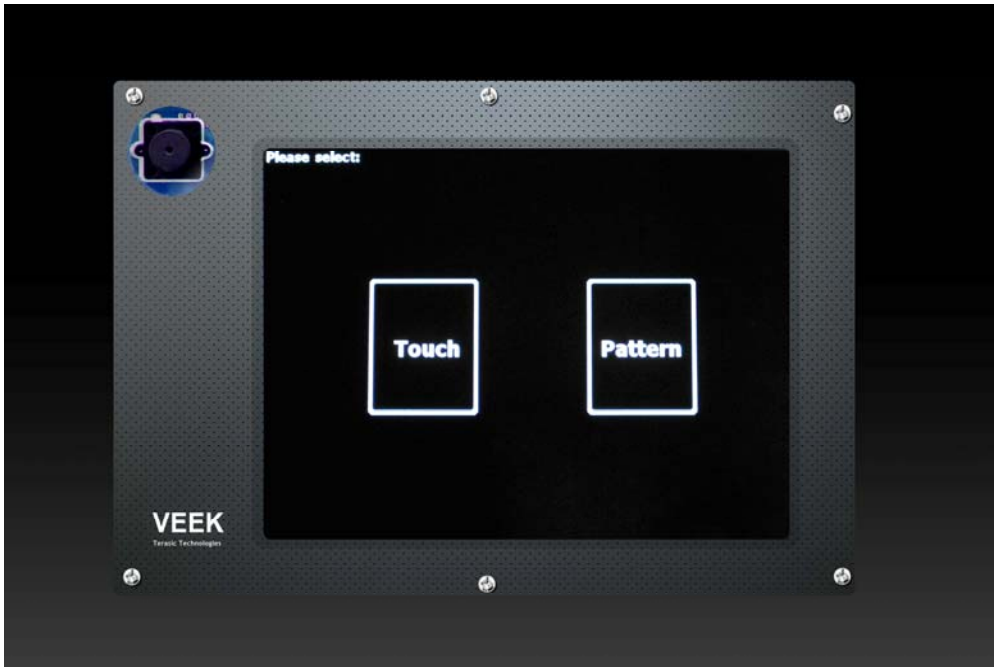

Figure 4-4 Main interface of the VEEK Starter demonstration

Figure 4-5 The VEEK Starter Touch sub item

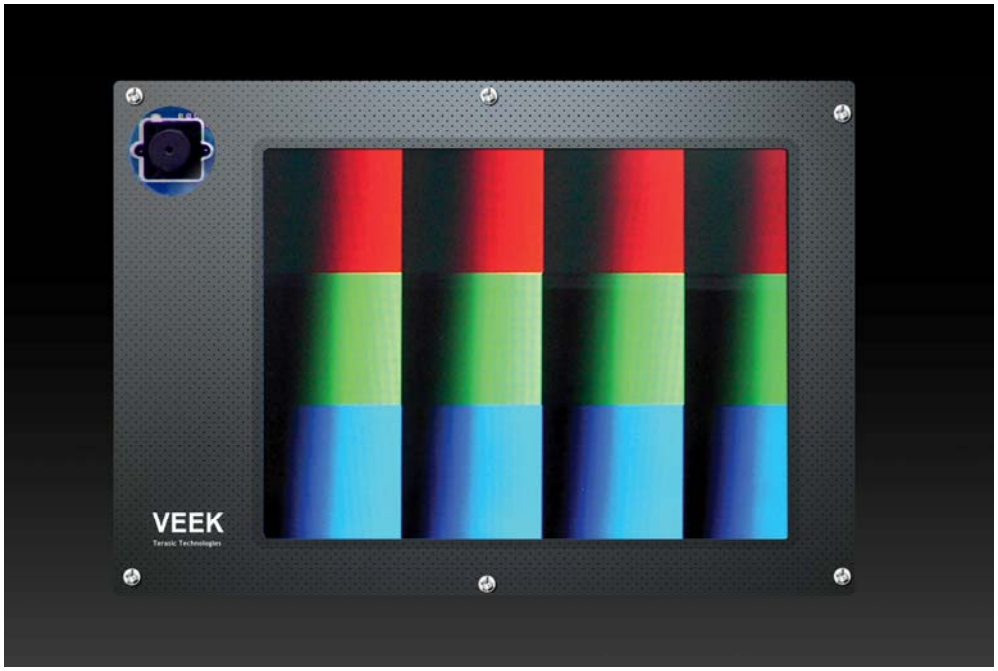

Figure 4-6 The VEEK Starter Pattern sub item

4.4 VEEK Picture Viewer

This demonstration shows a simple picture viewer implementation using Nios II based SOPC system. It reads JPEG images stored on SD Card and displays them on the LCD. The Nios II CPU decodes the images and fills the raw result data into frame buffers in SDRAM. The VEEK will show the image the buffer being displayed points to. When users touch the LCD Touch Panel, it will proceed to display the next buffered image or last buffered image. **Figure 4-7** shows the block diagram of this demonstration.

The Nios II CPU here takes a key roll in the demonstration. It is responsible of decoding the JPEG images and coordinates the works of all the peripherals. The touch panel handling program uses the timer as a regular interrupter and periodically updates the pen state and sampled coordinates.

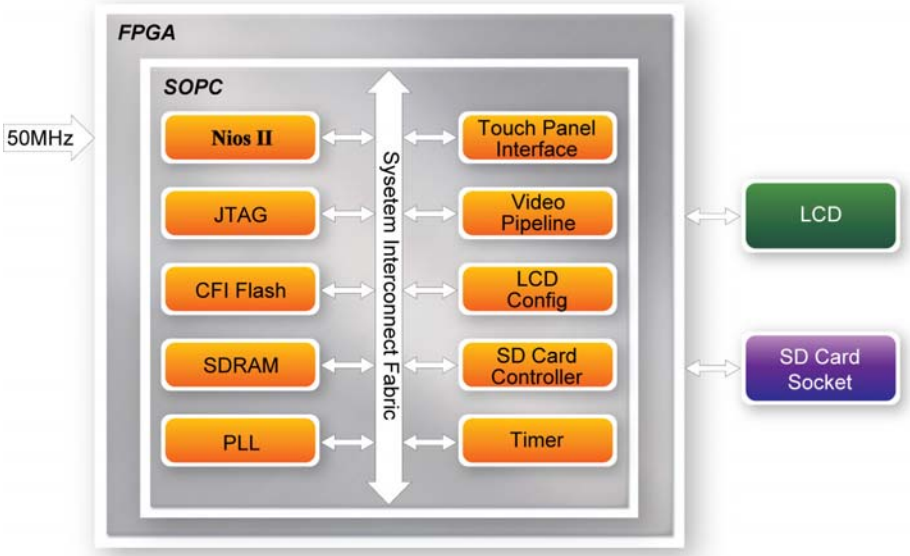

Figure 4-7 Block diagram of the picture viewer demonstration

■ Demonstration Source Code

- Project directory: VEEK_Picture_Viewer
- Bit stream used: VEEK_Picture_Viewer.sof
- Nios II Workspace: VEEK_Picture_Viewer\Software

■ Demonstration Batch File

Demo Batch File Folder: VEEK_Picture_Viewer\demo_batch

The demo batch file includes the following files:

- Batch File: VEEK_Picture_Viewer.bat, VEEK_Picture_Viewer _bashrc
- FPGA Configure File: VEEK_Picture_Viewer.sof
- Nios II Program: VEEK_Picture_Viewer.elf

■ Demonstration Setup

- Format your SD Card into FAT16 format
- Place the jpg image files to the \jpg subdirectory of the SD Card. For best display result, the image should have a resolution of 800x600 or the multiple of that
- Insert the SD Card to the SD Card slot on the VEEK
- Load the bitstream into the FPGA on the VEEK board