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# Video and Embedded Evaluation Kit – Multi-touch

## User Manual



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**ALTERA**

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## Chapter 1

# *Introduction*

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The Video and Embedded Evaluation Kit - Multi-touch (VEEK-MT) is a comprehensive design environment with everything embedded developers need to create processing-based systems. VEEK-MT delivers an integrated platform that includes hardware, design tools, intellectual property (IP) and reference designs for developing embedded software and hardware platform in a wide range of applications. The fully integrated kit allows developers to rapidly customize their processor and IP to best suit their specific application. The VEEK-MT features the DE2-115 development board targeting the Cyclone IV E FPGA, as well as a capacitive LCD multimedia color touch panel which natively supports multi-touch gestures. A 5-megapixel digital image sensor, ambient light sensor, and 3-axis accelerometer make up the rich feature-set.

The VEEK-MT is preconfigured with an FPGA hardware reference design including several ready-to-run demonstration applications stored on the provided SD card. Software developers can use these reference designs as their platform to quickly architect, develop and build complex embedded systems. By simply scrolling through the demos of your choice on the LCD touch panel, you can evaluate numerous processor system designs.

The all-in-one embedded solution offered on the VEEK-MT, in combination of the LCD touch panel and digital image module, provides embedded developers the ideal platform for multimedia applications with unparalleled processing performance. Developers can benefit from the use of FPGA-based embedded processing system such as mitigating design risk and obsolescence, design reuse, reducing bill of material (BOM) costs by integrating powerful graphics engines within the FPGA, and lower cost.

**Figure 1-1** shows a photograph of VEEK-MT.



**Figure 1-1 Video and Embedded Development Kit – Multi-touch**

The key features of the board are listed below:

## ■ DE2-115 Development Board

- Cyclone IV EP4CE115 FPGA
  - 114,480 LEs
  - 432 M9K memory blocks
  - 3,888 Kb embedded memory
  - 4 PLLs
- Configuration
  - On-board USB-Blaster circuitry
  - JTAG and AS mode configuration supported
  - EPCS64 serial configuration device
- Memory Devices
  - 128MB SDRAM
  - 2MB SRAM
  - 8MB Flash with 8-bit mode
  - 32Kb EEPROM
- Switches and Indicators
  - 18 switches and 4 push-buttons
  - 18 red and 9 green LEDs
  - Eight 7-segment displays
- Audio
  - 24-bit encoder/decoder (CODEC)
  - 3.5mm line-in, line-out, and microphone-in jacks

- Character Display
  - 16x2 LCD module
- On-board Clocking Circuitry
  - Three 50MHz oscillator clock inputs
  - SMA connectors (external clock input/output)
- SD Card Socket
  - Provides SPI and 4-bit SD mode for SD Card access
- Two Gigabit Ethernet Ports
  - Integrated 10/100/1000 Ethernet
- High Speed Mezzanine Card (HSMC)
  - Configurable I/O standards (voltage levels: 3.3/2.5/1.8/1.5V)
- USB Type A and B
  - Provides host and device controller compliant with USB 2.0
  - Supports data transfer at full-speed and low-speed
  - PC driver available
- 40-pin Expansion Port
  - Configurable I/O standards (voltage levels: 3.3/2.5/1.8/1.5V)
- VGA-out Connector
  - VGA DAC (high speed triple DACs)
- DB9 Serial Connector
  - RS232 port with flow control
- PS/2 Connector
  - PS/2 connector for connecting a PS2 mouse or keyboard
- TV-in Connector
  - TV decoder (NTSC/PAL/SECAM)
- Remote Control
  - Infrared receiver module
- Power
  - 12V DC input
  - Switching and step-down regulators LM3150MH

## ■ Capacitive LCD Touch Screen

- Equipped with an 7-inch amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module
- Module composed of LED backlight
- Supports 24-bit parallel RGB interface
- Converting the X/Y touch coordinates to corresponding digital data via Touch controller.

**Table 1-1** shows the general physical specifications of the touch screen (Note\*).

**Table 1-1 General Physical Specifications of the LCD**

<i>Item</i>	<i>Specification</i>	<i>Unit</i>
LCD size	7-inch (Diagonal)	-
Resolution	800 x3(RGB) x 480	dot
Dot pitch	0.1926(H) x0.1790 (V)	mm
Active area	154.08 (H) x 85.92 (V)	mm
Module size	164.9(H) x 100.0(V) x 5.7(D)	mm
Surface treatment	Glare	-
Color arrangement	RGB-stripe	-
Interface	Digital	-

## ■ 5-Megapixel Digital Image Sensor

- Superior low-light performance
- High frame rate
- Low dark current
- Global reset release, which starts the exposure of all rows simultaneously
- Bulb exposure mode, for arbitrary exposure times
- Snapshot-mode to take frames on demand
- Horizontal and vertical mirror image
- Column and row skip modes to reduce image size without reducing field-of-view
- Column and row binning modes to improve image quality when resizing
- Simple two-wire serial interface
- Programmable controls: gain, frame rate, frame size, exposure

**Table 1-2** shows the key parameters of the CMOS sensor (Note\*).

**Table 1-2 Key Performance Parameters of the CMOS sensor**

<i>Parameter</i>	<i>Value</i>	
Active Pixels	2592Hx1944V	
Pixel size	2.2umx2.2um	
Color filter array	RGB Bayer pattern	
Shutter type	Global reset release(GRR)	
Maximum data rate/master clock	96Mp/s at 96MHz	
Frame rate	Full resolution	Programmable up to 15 fps
	VGA mode	Programmable up to 70 fps
ADC resolution	12-bit	
Responsivity	1.4V/lux-sec(550nm)	

Pixel dynamic range		70.1dB
SNRMAX		38.1dB
Supply Voltage	Power	3.3V
	I/O	1.7V~3.1V

## ■ Digital Accelerometer

- Up to 13-bit resolution at +/- 16g
- SPI (3- and 4-wire) digital interface
- Flexible interrupts modes

## ■ Ambient Light Sensor

- Approximates human-eye response
- Precise luminance measurement under diverse lighting conditions
- Programmable interrupt function with user-defined upper and lower threshold settings
- 16-bit digital output with I<sup>2</sup>C fast-mode at 400 kHz
- Programmable analog gain and integration time
- 50/60-Hz lighting ripple rejection



*Note: for more detailed information of the LCD touch panel and CMOS sensor module, please refer to their datasheets respectively.*

## 1.1 About the Kit

The kit includes everything users need to run the demonstrations and develop custom designs, as shown in **Figure 1-2**.

The system CD contains technical documents of the VEEK-MT which includes component datasheets, demonstrations, schematic, and user manual.



Figure 1-2 VEEK-MT kit package contents

## 1.2 Setup License for Terasic Multi-Touch IP

To utilize the multi-touch panel in a Quartus II project, the Terasic Multi-Touch IP is required for operation. Error messages will be displayed if the license file for the Multi-Touch IP is not added before compiling projects. The license file is located at:

VEEK-MT System CD\License\license\_multi\_touch.dat

There are two ways to install the license. The first one is to add the license file (license\_multi\_touch.dat) to the “License file” listed in Quartus II, as shown in **Figure 1-3**. In order to reach this window, please navigate through to Quartus II → Tools → License Setup.

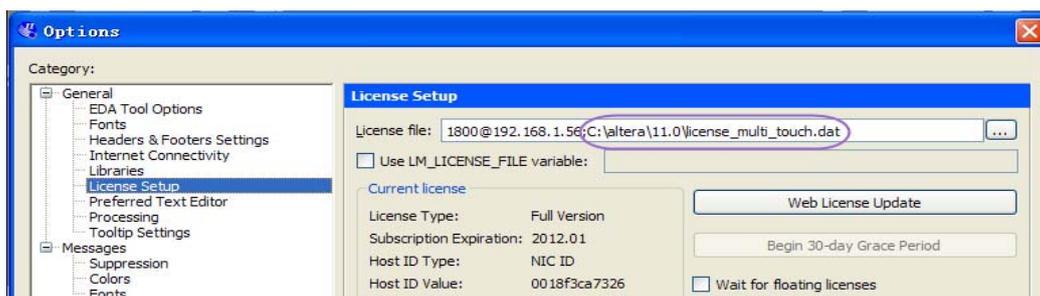


Figure 1-3 License Setup

The second way is to add license content to the existing license file. The procedures are listed below:

Use Notepad or other text editing software to open the file license\_multi\_touch.dat.

1. The license contains the FEATURE lines required to license the IP Cores as shown in **Figure 1-4**.

```

license_multi_touch.dat
0 10 20 30 40 50 60 70
1 FEATURE 535C 0018 alterad 9999.12 12-jan-9999 uncounted 3F15022F111E \
2  VENDOR_STRING="142c2k297gj7hoTVotLcny9Bti7hPsnSaeyATv8c8V5OsL3yQqoc1DdCIZ.
3  HOSTID=ANY TS_OK SIGN="1177 818B 8DA8 A068 5C33 BE57 9139 77D8 \
4  C855 3B4B 6582 721C 9B62 CD64 A358 0B19 40C2 15C8 B6C8 CA5B \
5  B5A9 C994 C296 D8FD E93C 9ADE 3D83 8952 EDCF 0843"

```

**Figure 1-4 Content of license\_multi\_touch.dat**

2. Open your Quartus II license.dat file in a text editor.
3. Copy everything under license\_multi\_touch.dat and paste it at the end of your Quartus II license file. (Note: Do not delete any FEATURE lines from the Quartus II license file. Doing so will result in an unusable license file.) .
4. Save the Quartus II license file.

## 1.3 Getting Help

Here is information of how to get help if you encounter any problem:

- Terasic Technologies
- Tel: +886-3-550-8800
- Email: [support@terasic.com](mailto:support@terasic.com)

## Chapter 2

# Architecture

This chapter describes the architecture of the Video and Embedded Evaluation Kit – Multi-touch (VEEK-MT) including block diagram and components.

### 2.1 Layout and Components

The picture of the VEEK-MT is shown in **Figure 2-1** and **Figure 2-2**. It depicts the layout of the board and indicates the locations of the connectors and key components.



**Figure 2-1 VEEK-MT PCB and Component Diagram (Top)**

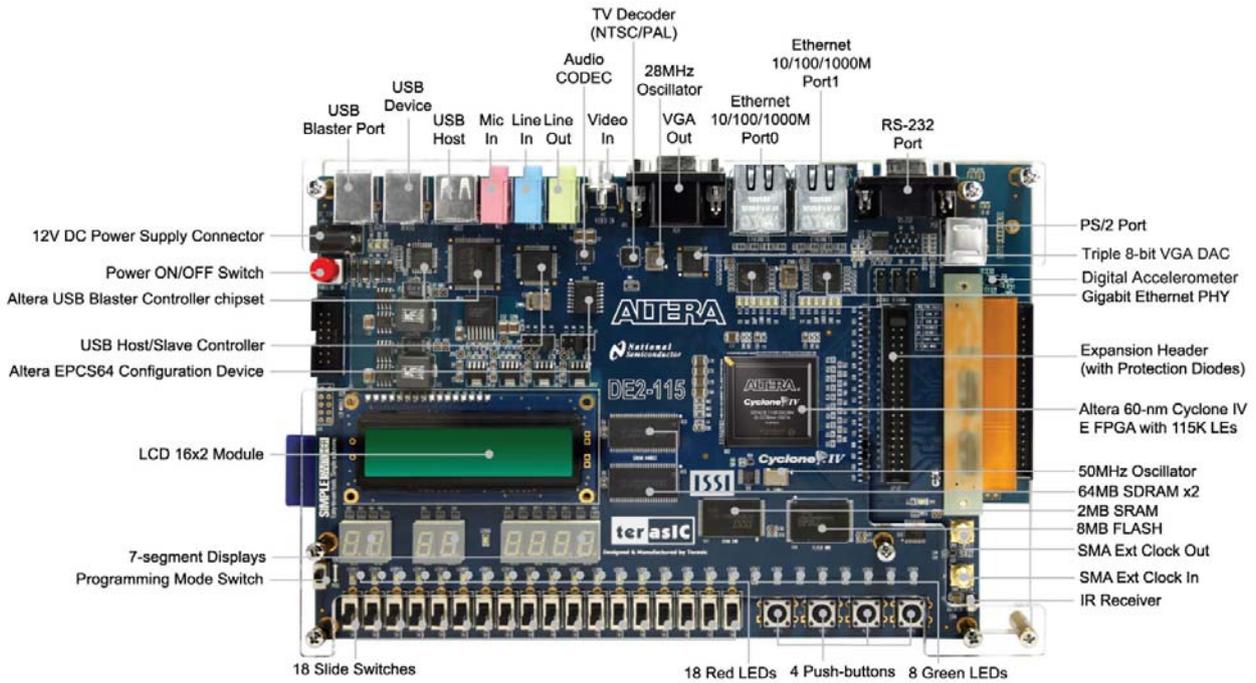


Figure 2-2 VEEK-MT PCB and Component Diagram (Bottom)

## 2.2 Block Diagram of the VEEK-MT

Figure 2-3 gives the block diagram of the VEEK-MT board. To provide maximum flexibility for the user, all connections are made through the Cyclone IV E FPGA device. Thus, the user can configure the FPGA to implement any system design.

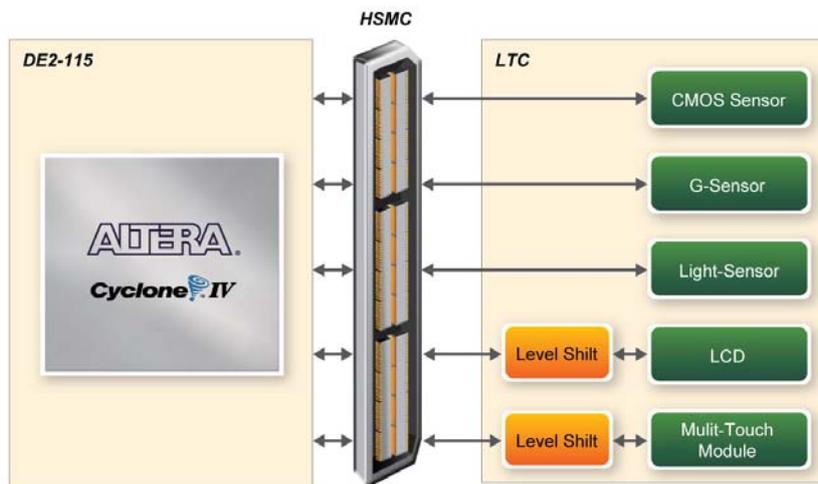


Figure 2-3 Block Diagram of VEEK-MT

## Chapter 3

# Using VEEK-MT

This section describes the detailed information of the components, connectors, and pin assignments of the VEEK-MT.

### 3.1 Configuring the Cyclone IV E FPGA

The Video and Embedded Evaluation Kit (VEEK-MT) contains a serial configuration device that stores configuration data for the Cyclone IV E FPGA. This configuration data is automatically loaded from the configuration device into the FPGA every time while power is applied to the board. Using the Quartus II software, it is possible to reconfigure the FPGA at any time, and it is also possible to change the non-volatile data that is stored in the serial configuration device. Both types of programming methods are described below.

1. **JTAG programming:** In this method of programming, named after the IEEE standards Joint Test Action Group, the configuration bit stream is downloaded directly into the Cyclone IV E FPGA. The FPGA will retain this configuration as long as power is applied to the board; the configuration information will be lost when the power is turned off.
2. **AS programming:** In this method, called Active Serial programming, the configuration bit stream is downloaded into the Altera EPCS64 serial configuration device. It provides non-volatile storage of the bit stream, so that the information is retained even when the power supply to the VEEK-MT is turned off. When the board's power is turned on, the configuration data in the EPCS64 device is automatically loaded into the Cyclone IV E FPGA.

#### ■ JTAG Chain on VEEK-MT

To use the JTAG interface for configuring FPGA device, the JTAG chain on the VEEK-MT must form a closed loop that allows Quartus II programmer to detect the FPGA device. **Figure 3-1** illustrates the JTAG chain on the VEEK-MT. Shorting pin1 and pin2 on JP3 can disable the JTAG signals on the HSMC connector that will form a close JTAG loopback on DE2-115 (See **Figure 3-2**). Thus, only the on-board FPGA device (Cyclone IV E) will be detected by Quartus II programmer. By default, a jumper is placed on pin1 and pin2 of JP3. To prevent any changes to the bus controller (Max II EPM240) described in later sections, users should not adjust the jumper on JP3.

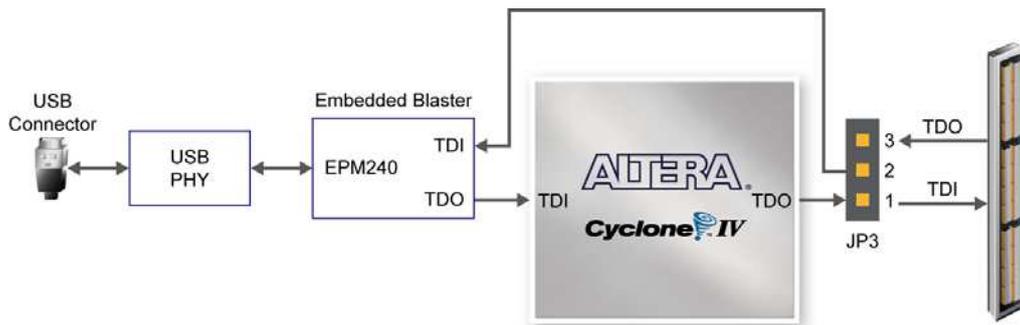


Figure 3-1 JTAG Chain

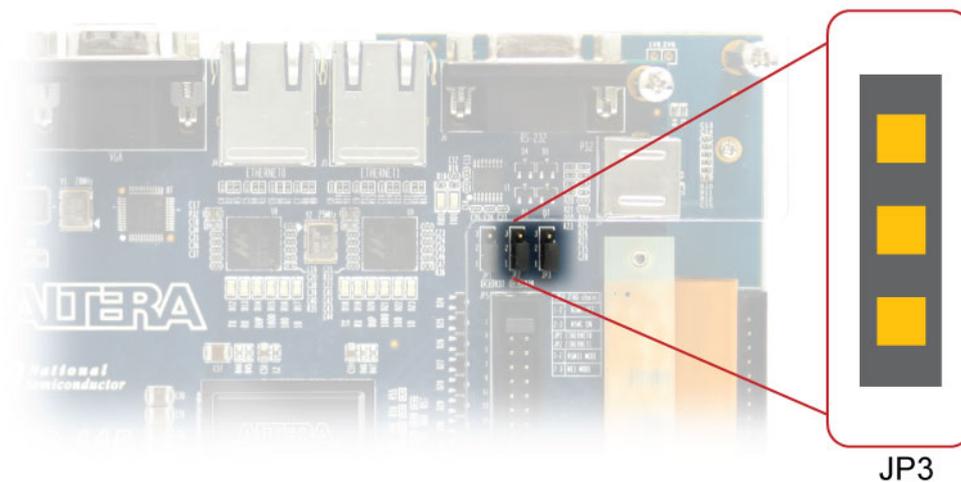
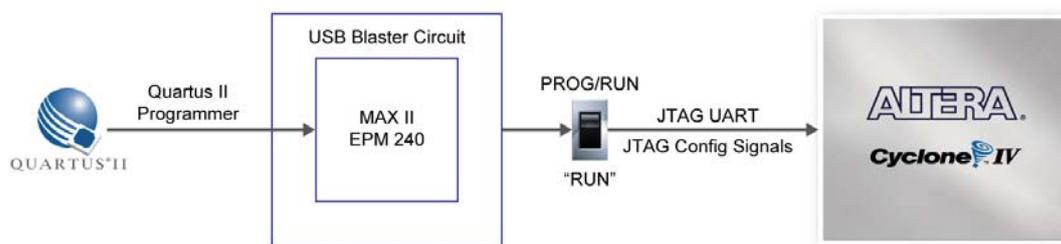


Figure 3-2 JTAG Chain Configuration Header

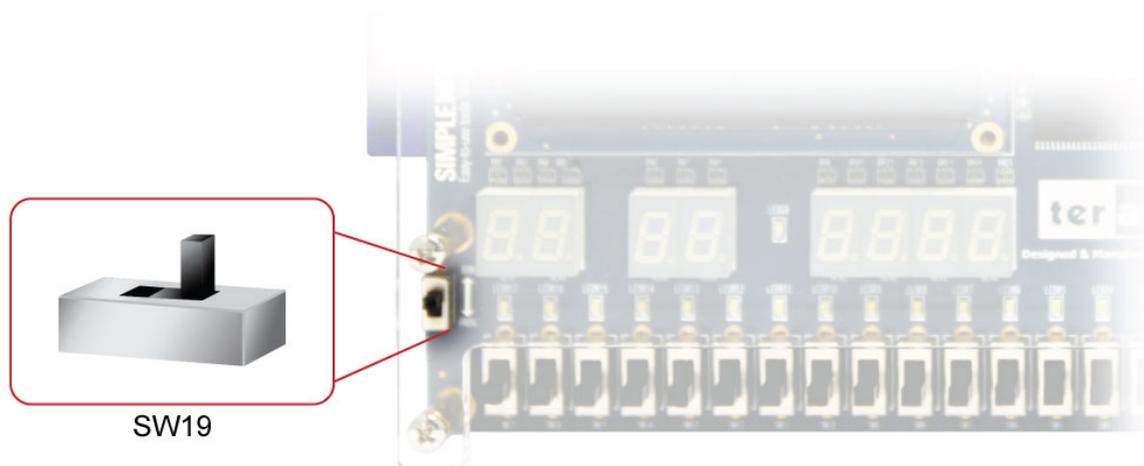
## ■ Configuring the FPGA in JTAG Mode

Figure 3-3 illustrates the JTAG configuration setup. To download a configuration bit stream into the Cyclone IV E FPGA, perform the following steps:

- Ensure that power is applied to the VEEK-MT
- Configure the JTAG programming circuit by setting the RUN/PROG slide switch (SW19) to the RUN position (See Figure 3-4)
- Connect the supplied USB cable to the USB-Blaster port on the VEEK-MT
- The FPGA can now be programmed by using the Quartus II Programmer module to select a configuration bit stream file with the .sof filename extension



**Figure 3-3 JTAG Chain Configuration Scheme**



**Figure 3-4 The RUN/PROG Switch (SW19) Set to JTAG Mode**

### ■ Configuring the EPCS64 in AS Mode

**Figure 3-5** illustrates the AS configuration set up. To download a configuration bit stream into the EPCS64 serial configuration device, perform the following steps:

- Ensure that power is applied to the VEEK-MT
- Connect the supplied USB cable to the USB-Blaster port on the VEEK-MT
- Configure the JTAG programming circuit by setting the RUN/PROG slide switch (SW19) to the PROG position
- The EPCS64 chip can now be programmed by using the Quartus II Programmer module to select a configuration bit stream file with the .pof filename extension
- Once the programming operation is finished, set the RUN/PROG slide switch back to the RUN position and then reset the board by turning the power switch off and back on; this action causes the new configuration data in the EPCS64 device to be loaded into the FPGA chip

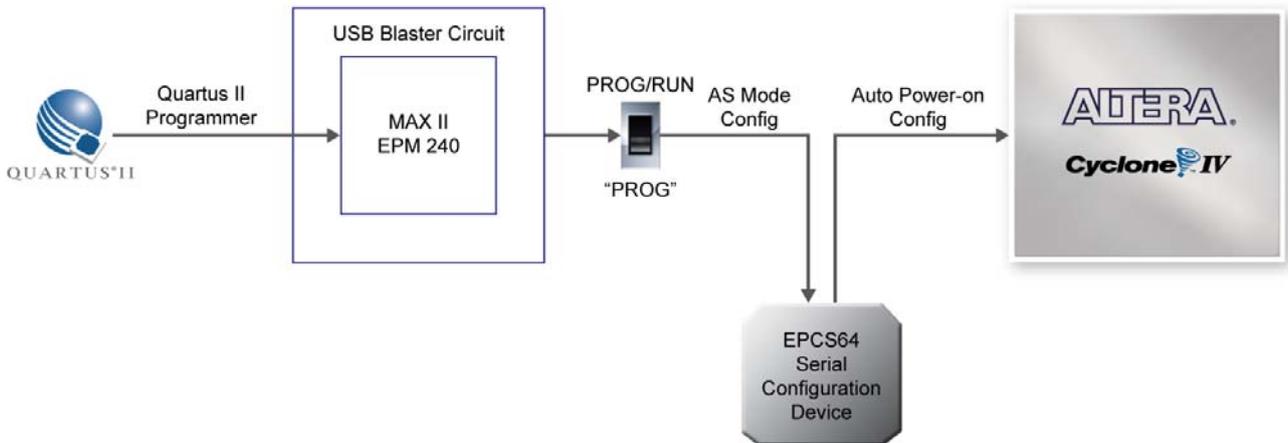


Figure 3-5 The AS Configuration Scheme

## 3.2 Bus Controller

The VEEK-MT comes with a bus controller using the Max II EPM240 that allows user to access the touch screen module through the HSMC connector. This section describes its structure in block diagram-form and its capabilities.

### ■ Bus Controller Introduction

The bus controller provides level shifting functionality from 2.5V (HSMC) to 3.3V domains.

### ■ Block Diagram of the Bus Controller

Figure 3-6 gives the block diagram of the connection setup from the HSMC connector to the bus controller on the Max II EPM240 to the touch screen module. To provide maximum flexibility for the user, all connections are established through the HSMC connector. Thus, the user can configure the Cyclone IV E FPGA on the VEEK-MT to implement any system design.



Figure 3-6 Block Diagram of the Bus Controller

### 3.3 Using the 7” LCD Capacitive Touch Screen

The VEEK-MT features a 7-inch capacitive amorphous TFT-LCD panel. The LCD touch screen offers resolution of (800x480) to provide users the best display quality for developing applications. The LCD panel supports 24-bit parallel RGB data interface.

The VEEK-MT is also equipped with a Touch controller, which can read the coordinates of the touch points through a serial port interface.

To display images on the LCD panel correctly, the RGB color data along with the data enable and clock signals must act according to the timing specification of the LCD touch panel as shown in **Table 3-1**.

**Table 3-2** gives the pin assignment information of the LCD touch panel.

**Table 3-1 LCD timing specifications**

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
DCLK	Dot Clock	1/tCLK		33		MHZ	
	DCLK pulse duty	Tcwh	40	50	60	%	
DE	Setup time	Tesu	8			ns	
	Hold time	Tehd	8			ns	
	Horizontal period	tH		1056		tCLK	
	Horizontal Valid	tHA		800		tCLK	
	Horizontal Blank	tHB		256		tCLK	
	Vertical Period	tV		525		tH	
	Vertical Valid	tVA		480		tH	
	Vertical Blank	tVB		45		tH	
	SYNC	HSYNC setup time	Thst	8			ns
HSYNC hold time		Thhd	8			ns	
VSYNC Setup Time		Tvst	8			ns	
VSYNC Hold Time		Tvhd	8			ns	
Horizontal Period		th		1056		tCLK	
Horizontal Pulse Width		thpw		30		tCLK	thb+thpw=46DCLK is fixed
Horizontal Back Porch		thb		16		tCLK	
Horizontal Front Porch		thfp		210		tCLK	
Horizontal Valid		thd		800		tCLK	
Vertical Period		tv		525		th	
Vertical Pulse Width		tpw		13		th	tpw + tvb = 23th is fixed
Vertical Back Porch		tvb		10		th	
Vertical Front Porch		tvfp		22		th	

	Vertical Valid	tvd	480			th	
DATA	Setup time	Tdsu	8			ns	
	Hold time	Tdsu	8			ns	

**Table 3-2 Pin assignment of the LCD touch panel**

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>
LCD_B0	P28	LCD blue data bus bit 0	2.5V
LCD_B1	P27	LCD blue data bus bit 1	2.5V
LCD_B2	J24	LCD blue data bus bit 2	2.5V
LCD_B3	J23	LCD blue data bus bit 3	2.5V
LCD_B4	T26	LCD blue data bus bit 4	2.5V
LCD_B5	T25	LCD blue data bus bit 5	2.5V
LCD_B6	R26	LCD blue data bus bit 6	2.5V
LCD_B7	R25	LCD blue data bus bit 7	2.5V
LCD_DCLK	V24	LCD Clock	2.5V
LCD_DE	H23	Data Enable signal	2.5V
LCD_DIM	P21	LCD backlight enable	2.5V
LCD_DITH	L23	Dithering setting	2.5V
LCD_G0	P26	LCD green data bus bit 0	2.5V
LCD_G1	P25	LCD green data bus bit 1	2.5V
LCD_G2	N26	LCD green data bus bit 2	2.5V
LCD_G3	N25	LCD green data bus bit 3	2.5V
LCD_G4	L22	LCD green data bus bit 4	2.5V
LCD_G5	L21	LCD green data bus bit 5	2.5V
LCD_G6	U26	LCD green data bus bit 6	2.5V
LCD_G7	U25	LCD green data bus bit 7	2.5V
LCD_HSD	U22	Horizontal sync input.	2.5V
LCD_MODE	L24	DE/SYNC mode select	2.5V
LCD_POWER_CTL	M25	LCD power control	2.5V
LCD_R0	V28	LCD red data bus bit 0	2.5V
LCD_R1	V27	LCD red data bus bit 1	2.5V
LCD_R2	U28	LCD red data bus bit 2	2.5V
LCD_R3	U27	LCD red data bus bit 3	2.5V
LCD_R4	R28	LCD red data bus bit 4	2.5V
LCD_R5	R27	LCD red data bus bit 5	2.5V
LCD_R6	V26	LCD red data bus bit 6	2.5V
LCD_R7	V25	LCD red data bus bit 7	2.5V
LCD_RSTB	K22	Global reset pin	2.5V
LCD_SHLR	H24	Left or Right Display Control	2.5V

LCD_UPDN	K21	Up / Down Display Control	2.5V
LCD_VSD	V22	Vertical sync input.	2.5V
TOUCH_I2C_SCL	T22	touch I2C clock	2.5V
TOUCH_I2C_SDA	T21	touch I2C data	2.5V
TOUCH_INT_n	R23	touch interrupt	2.5V

### 3.4 Using 5 Megapixel Digital Image Sensor

The VEEK-MT is equipped with a 5 megapixel digital image sensor that provides an active imaging array of 2,592H x 1,944V. It features low-noise CMOS imaging technology that achieves CCD image quality. In addition, it incorporates sophisticated camera functions on-chip such as windowing, column and row skip mode, and snapshot mode.

The sensor can be operated in its default mode or programmed by the user through a simple two-wire serial interface for frame size, exposure, gain settings, and other parameters. **Table 3-3** contains the pin names and descriptions of the image sensor module.

**Table 3-3 Pin Assignment of the CMOS Sensor**

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>
CAMERA_PIXCLK	J27	Pixel clock	2.5V
CAMERA_D0	F24	Pixel data bit 0	2.5V
CAMERA_D1	F25	Pixel data bit 1	2.5V
CAMERA_D2	D26	Pixel data bit 2	2.5V
CAMERA_D3	C27	Pixel data bit 3	2.5V
CAMERA_D4	F26	Pixel data bit 4	2.5V
CAMERA_D5	E26	Pixel data bit 5	2.5V
CAMERA_D6	G25	Pixel data bit 6	2.5V
CAMERA_D7	G26	Pixel data bit 7	2.5V
CAMERA_D8	H25	Pixel data bit 8	2.5V
CAMERA_D9	H26	Pixel data bit 9	2.5V
CAMERA_D10	K25	Pixel data bit 10	2.5V
CAMERA_D11	K26	Pixel data bit 11	2.5V
CAMERA_STROBE	E27	Snapshot strobe	2.5V
CAMERA_LVAL	D28	Line valid	2.5V
CAMERA_FVAL	D27	Frame valid	2.5V
CAMERA_RESET_n	F27	Image sensor reset	2.5V
CAMERA_SCLK	AE26	Serial clock	2.5V
CAMERA_TRIGGER	E28	Snapshot trigger	2.5V
CAMERA_SDATA	AE27	Serial data	2.5V
CAMERA_XCLKIN	G23	External input clock	2.5V

### 3.5 Using the Digital Accelerometer

The VEEK-MT is equipped with a digital accelerometer sensor module. The ADXL345 is a small, thin, ultralow power assumption 3-axis accelerometer with high resolution measurement. Digitalized output is formatted as 16-bit twos complement and can be accessed either using SPI interface or I2C interface. This chip uses the 3.3V CMOS signaling standard. Main applications include medical instrumentation, industrial instrumentation, personal electronic aid and hard disk drive protection etc. Some of the key features of this device are listed below. For more detailed information of better using this chip, please refer to its datasheet which is available on manufacturer's website or under the /datasheet folder of the system CD.

**Table 3-4 Pin Names and Descriptions of the GSENSOR Module**

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>
GSENSOR_INT1	G27	Interrupt 1 output	2.5V
GSENSOR_INT2	G28	Interrupt 2 output	2.5V
GSENSOR_CS_n	F28	Chip Select	2.5V
GSENSOR_ALT_ADDR	K27	I2C Address Select	2.5V
GSENSOR_SDA_SDI_SDIO	K28	Serial Data	2.5V
GSENSOR_SCL_SCLK	M27	Serial Communications Clock	2.5V

### 3.6 Using the Ambient Light Sensor

The APDS-9300 is a low-voltage digital ambient light sensor that converts light intensity to digital signal output capable of direct I2C communication. Each device consists of one broadband photodiode (visible plus infrared) and one infrared photodiode. Two integrating ADCs convert the photodiode currents to a digital output that represents the irradiance measured on each channel. This digital output can be input to a microprocessor where illuminance (ambient light level) in lux is derived using an empirical formula to approximate the human-eye response. For more detailed information of better using this chip, please refer to its datasheet which is available on manufacturer's website or under the /datasheet folder of the system CD.

**Table 3-5 Pin names and Descriptions of Ambient Light Sensor Module**

<i>Signal Name</i>	<i>FPGA Pin No.</i>	<i>Description</i>	<i>I/O Standard</i>
LSENSOR_ADDR_SEL	J25	Chip select	2.5V
LSENSOR_INT	L28	Interrupt output	2.5V
LSENSOR_SCL	J26	Serial Communications Clock	2.5V
LSENSOR_SDA	L27	Serial Data	2.5V

### 3.7 Using Terasic Multi-Touch IP

Terasic Multi-Touch IP is provided for developers to retrieve user inputs, including multi-touch gestures and single-touch. The file name of this IP is **i2c\_touch\_config** and it is encrypted. To compile projects with the IP, users need to install the IP license first. For license installation, please refer to section **1.2 Setup License for Terasic Multi-Touch IP** in this document. The license file is located at:

VEEK-MT System CD\License\license\_multi\_touch.dat

The IP decodes I2C information and outputs coordinate and gesture information. The IP interface is shown below:

```

module i2c_touch_config (
    // Host Side
    iCLK,
    iRSTN,
    iTRIG,
    oREADY,
    oREG_X1,
    oREG_Y1,
    oREG_X2,
    oREG_Y2,
    oREG_TOUCH_COUNT,
    oREG_GESTURE,
    // I2C Side
    I2C_SCLK,
    I2C_SDAT
);

```

The signal purpose of the IP is described in **Table 3-6**. The IP requires a 50MHz signal as a reference clock to the **iCLK** pin and system reset signal to **iRSTN**. **iTRIG**, **I2C\_SCLK**, and **IC2\_SDAT** pins should be connected of the TOUCH\_INT\_n, TOUCH\_I2C\_SCL, and TOUCH\_I2C\_SDA signals in the 2x20 GPIO header respectively. When **oREADY** rises, it means there is touch activity, and associated information is given in the **oREG\_X1**, **oREG\_Y1**, **oREG\_X2**, **oREG\_Y2**, **oREG\_TOUCH\_COUNT**, and **oREG\_GESTURE** pins.

For the control application, when touch activity occurs, it should check whether the value of **oREG\_GESTURE** matched a pre-defined gesture ID defined in **Table 3-7**. If it is not a gesture, it means a single-touch has occurred and the relative X/Y coordinates can be derived from **oREG\_X1** and **oREG\_Y1**.

**Table 3-6 Interface Definitions of Terasic Multi-touch IP**

<i>Pin Name</i>	<i>Direction</i>	<i>Description</i>
<b>iCLK</b>	<b>Input</b>	<b>Connect to 50MHz Clock</b>
<b>iRSTN</b>	<b>Input</b>	<b>Connect to system reset signal</b>
<b>iTRIG</b>	<b>Input</b>	<b>Connect to Interrupt Pin of Touch IC</b>
<b>oREADY</b>	<b>Output</b>	<b>Rising Trigger when following six output data is valid</b>
<b>oREG_X1</b>	<b>Output</b>	<b>10-bits X coordinate of first touch point</b>
<b>oREG_Y1</b>	<b>Output</b>	<b>9-bits Y coordinate of first touch point</b>
<b>oREG_X2</b>	<b>Output</b>	<b>10-bits X coordinate of second touch point</b>

<b>oREG_Y2</b>	<b>Output</b>	<b>9-bits Y coordinate of second touch point</b>
<b>oREG_TOUCH_COUNT</b>	<b>Output</b>	<b>2-bits touch count. Valid value is 0, 1, or 2.</b>
<b>oREG_GESTURE</b>	<b>Output</b>	<b>8-bits gesture ID (See <a href="#">Table 3-7</a>)</b>
<b>I2C_SCLK</b>	<b>Output</b>	<b>Connect to I2C Clock Pin of Touch IC</b>
<b>I2C_SDAT</b>	<b>Inout</b>	<b>Connect to I2C Data Pin of Touch IC</b>

The supported gestures and IDs are shown in [Table 3-7](#).

**Table 3-7 Gestures**

<i><b>Gesture</b></i>	<i><b>ID (hex)</b></i>
<b>One Point Gesture</b>	
<b>North</b>	<b>0x10</b>
<b>North-East</b>	<b>0x12</b>
<b>East</b>	<b>0x14</b>
<b>South-East</b>	<b>0x16</b>
<b>South</b>	<b>0x18</b>
<b>South-West</b>	<b>0x1A</b>
<b>West</b>	<b>0x1C</b>
<b>North-West</b>	<b>0x1E</b>
<b>Rotate Clockwise</b>	<b>0x28</b>
<b>Rotate Anti-clockwise</b>	<b>0x29</b>
<b>Click</b>	<b>0x20</b>
<b>Double Click</b>	<b>0x22</b>
<b>Two Point Gesture</b>	
<b>North</b>	<b>0x30</b>
<b>North-East</b>	<b>0x32</b>
<b>East</b>	<b>0x34</b>
<b>South-East</b>	<b>0x36</b>
<b>South</b>	<b>0x38</b>
<b>South-West</b>	<b>0x3A</b>
<b>West</b>	<b>0x3C</b>
<b>North-West</b>	<b>0x3E</b>
<b>Click</b>	<b>0x40</b>
<b>Zoom In</b>	<b>0x48</b>
<b>Zoom Out</b>	<b>0x49</b>

Note: The Terasic Multi-Touch IP can also be found under the \IP folder in the system CD as well as the \IP folder in the reference designs.

## Chapter 4

# *VEEK-MT Demonstrations*

This chapter gives detailed description of the provided bundles of exclusive demonstrations implemented on VEEK-MT. These demonstrations are particularly designed (or ported) for VEEK-MT, with the goal of showing the potential capabilities of the kit and showcase the unique benefits of FPGA-based SOPC systems such as reducing BOM costs by integrating powerful graphics and video processing circuits within the FPGA.

### 4.1 System Requirements

To run and recompile the demonstrations, you should:

- Install Altera Quartus II 11.0 and NIOS II EDS 11.0 or later edition on the host computer
- Install the USB-Blaster driver software. You can find instructions in the tutorial “Getting Started with Altera’s DE2-115 Board” (tut\_initialDE2-115.pdf) which is available on the DE2-115 system CD
- Copy the entire demonstrations folder from the VEEK-MT system CD to your host computer

### 4.2 Factory Configuration

The VEEK-MT development kit comes preconfigured with a default utility that boots up on power on and allows users to quickly select, load, and run different Ready-to-Run demonstrations stored on an SD card using the VEEK-MT touch panel. **Figure 4-1** gives a snapshot of the default application selector interface (Note\*). Every demonstration consists of an FPGA hardware image and an application software image. When you select a demonstration the application selector copies the hardware image to EPCS device and software image to flash memory and reconfigures the FPGA with your selection. For more comprehensive information of the application selector factory configuration, please refer to chapter 5.



Figure 4-1 Application Selector Interface



*Note: Please insert the supplied SD card from this demonstration.*

## 4.3 Painter Demonstration

This chapter shows how to control LCD and touch controller to establish a paint demo based on SOPC Builder and Altera VIP Suite. The demonstration shows how multi-touch gestures and single-touch coordinates operate.

**Figure 4-2** shows the hardware system block diagram of this demonstration. For LCD display processing, the reference design is developed based on the Altera Video and Image Processing Suite (VIP). The Frame Reader VIP is used for reading display content from the associated video memory, and VIP Video Out is used to display the display content. The display content is filled by NIOS II processor according to users' input.

For multi-touch processing, a Terasic Memory-Mapped IP is used to retrieve the user input, including multi-touch gesture and single-touch coordinates. Note, the IP is encrypted, so the license should be installed before compiling the Quartus II project. For IP--usage details please refer to the section **3.7 Using Terasic Multi-Touch IP** in this document.

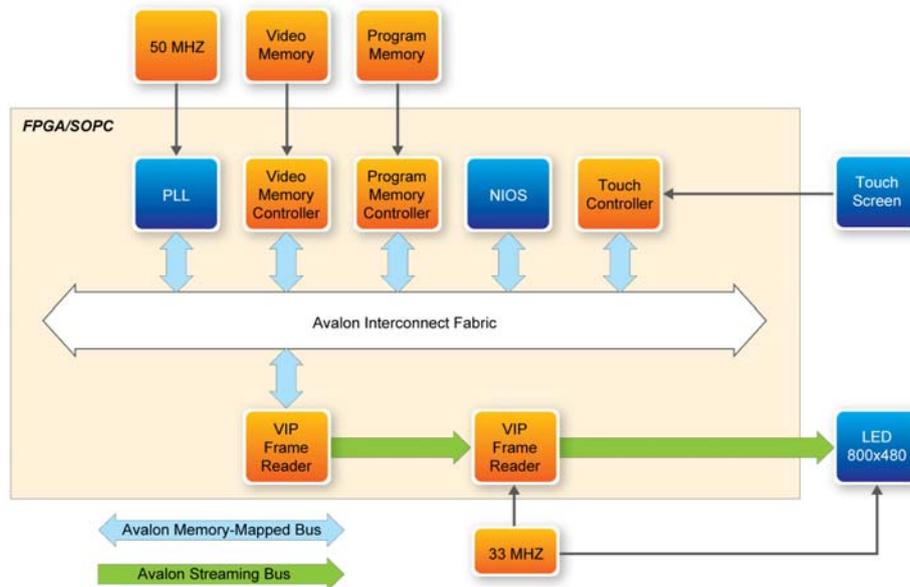


Figure 4-2 Block Diagram of the Painter Demonstration

## ■ Demonstration Source Code

- Project directory: Painter
- Bit stream used: Painter.sof
- Nios II Workspace: Painter \Software

## ■ Demonstration Batch File

Demo Batch File Folder: Painter \demo\_batch

The demo batch file includes the following files:

- Batch File: test.bat, test\_bashrc
- FPGA Configuration File: Painter.sof
- Nios II Program: Painter.elf

## ■ Demonstration Setup

1. Make sure Quartus II and Nios II are installed on your PC
  2. Power on the DE2-115 board
  3. Connect USB-Blaster to the DE2-115 board and install USB-Blaster driver if necessary
  4. Execute the demo batch file “test.bat” under the batch file folder, Painter \demo\_batch
  5. After Nios II program is downloaded and executed successfully, you will see a painter GUI in the LCD. **Figure 4-3** shows the GUI of the Painter Demo.
- The GUI is classified into three areas: Palette, Canvas, and Gesture. Users can select pen color from the color palette and start painting in the Canvas area. If gesture is detected, the associated gesture symbol is shown in the gesture area. To clear canvas content, press the “Clear” button.