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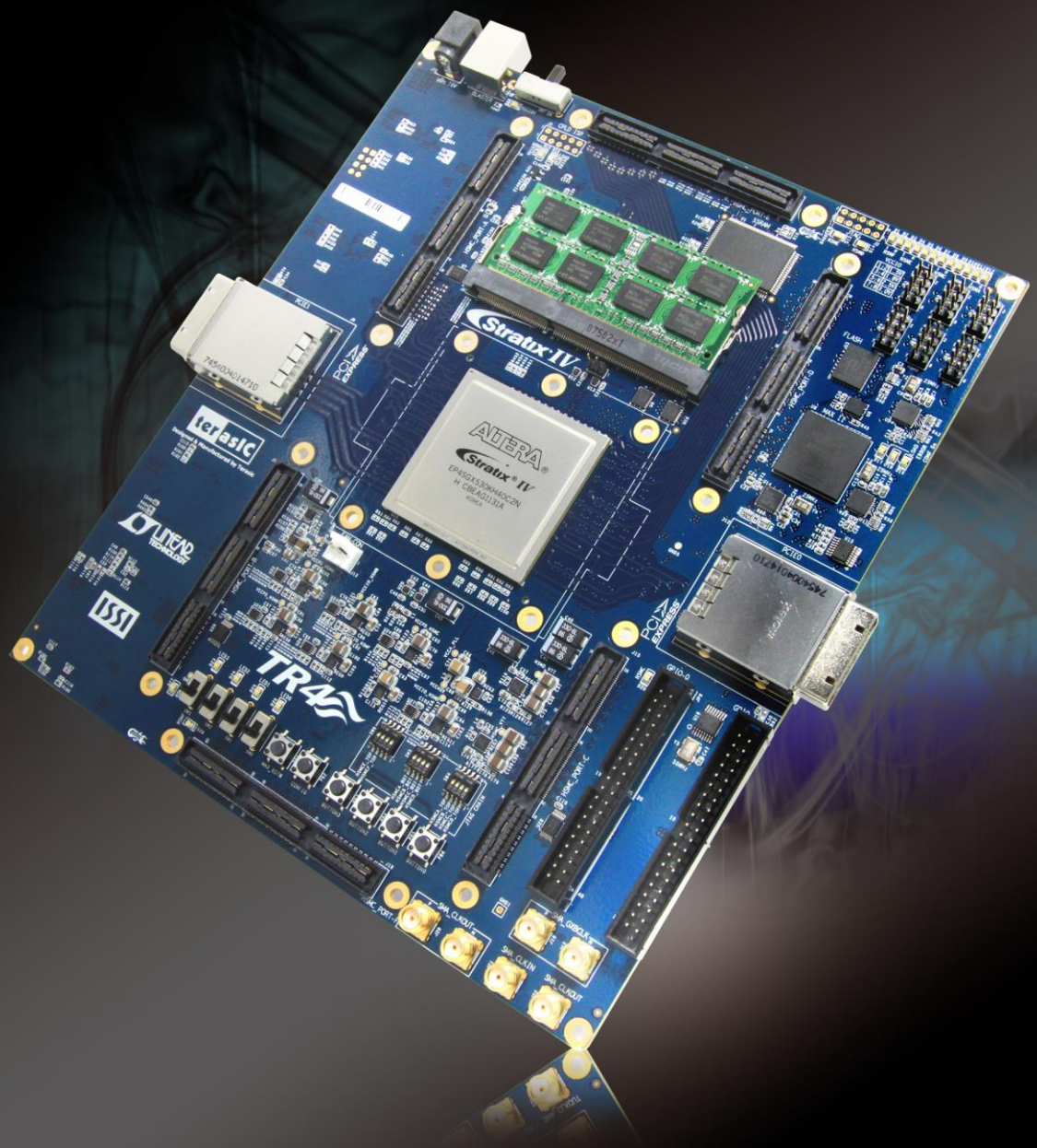
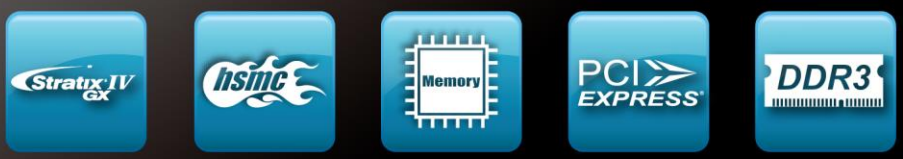
TR4

FPGA Development Kit

User Manual





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CONTENTS

Chapter 1

Overview

This chapter provides an overview of the TR4 Development Board and details the components and features of the board.

1.1 General Description

The TR4 Development Board provides the ideal hardware platform for system designs that demand high-performance, serial connectivity, and advanced memory interfacing. Developed specifically to address the rapidly evolving requirements in many end markets for greater bandwidth, improved jitter performance, and lower power consumption, the TR4 is powered by the Stratix® IV GX device and supported by industry-standard peripherals, connectors and interfaces that offer a rich set of features that is suitable for a wide range of compute-intensive applications.

The advantages of the Stratix® IV GX FPGA platform with integrated transceivers have allowed the TR4 to be fully compliant with version 2.0 of the PCI Express standard. This will accelerate mainstream development of PCI Express-based applications and enable customers to deploy designs for a broad range of high-speed connectivity applications.

The TR4 is supported by multiple reference designs and six High-Speed Mezzanine Card (HSMC) connectors that allow scaling and customization with mezzanine daughter cards. For large-scale ASIC prototype development, multiple TR4s can be stacked together to create an easily-customizable multi-FPGA system.

1.2 Key Features

Featured Device

- Altera Stratix® IV GX FPGA (EP4SGX230C2/EP4SGX530C2)

Configuration and Set-up Elements

- Built-in USB Blaster circuit for programming
- Fast passive parallel (FPP) configuration via MAX II CPLD and FLASH

Components and Interfaces

- Six HSMC connectors (two with transceiver support)
- Two 40-pin GPIO expansion headers (shares pins with HSMC Port C)
- Two external PCI Express 2.0 (x4 lane) connectors

Memory

- DDR3 SO-DIMM socket (8GB Max)
- 64MB FLASH
- 2MB SSRAM

General User Input/Output:

- Four LEDs
- Four push-buttons
- Four slide switches

Clock system

- On-board 50MHz oscillator
- Three on-board programmable PLL timing chips
- SMA connector pair for differential clock input
- SMA connector pair for differential clock output
- SMA connector for external clock input
- SMA connector for clock output

Other

- Temperature sensor
- FPGA cooling fan

1.3 Board Overview

Figure 1-1 and Figure 1-2 show the top and bottom view of the TR4 board. It depicts the layout of the board and indicates the location of the connectors and key components. Users can refer to these figures for relative location when the connectors and key components are introduced in the following chapters.

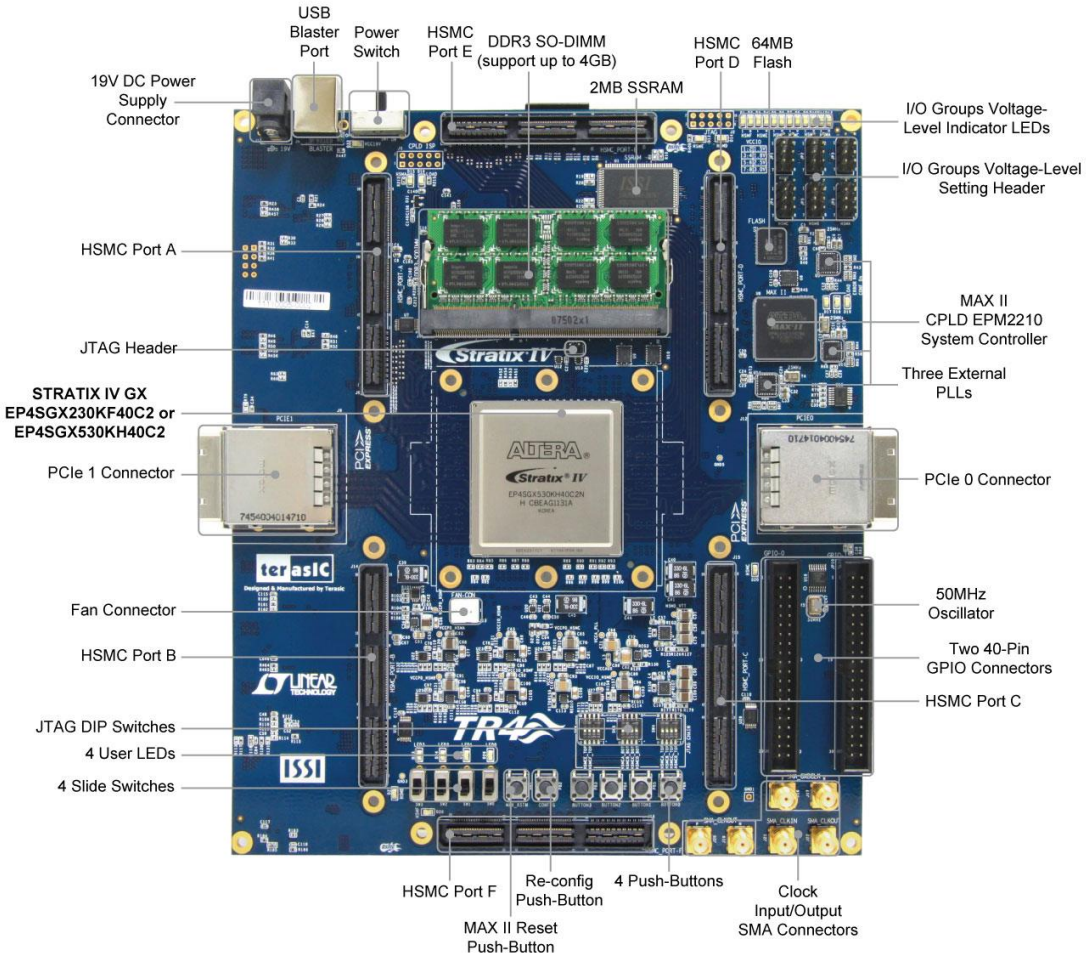

Figure 1-1 TR4 Board View (Top)

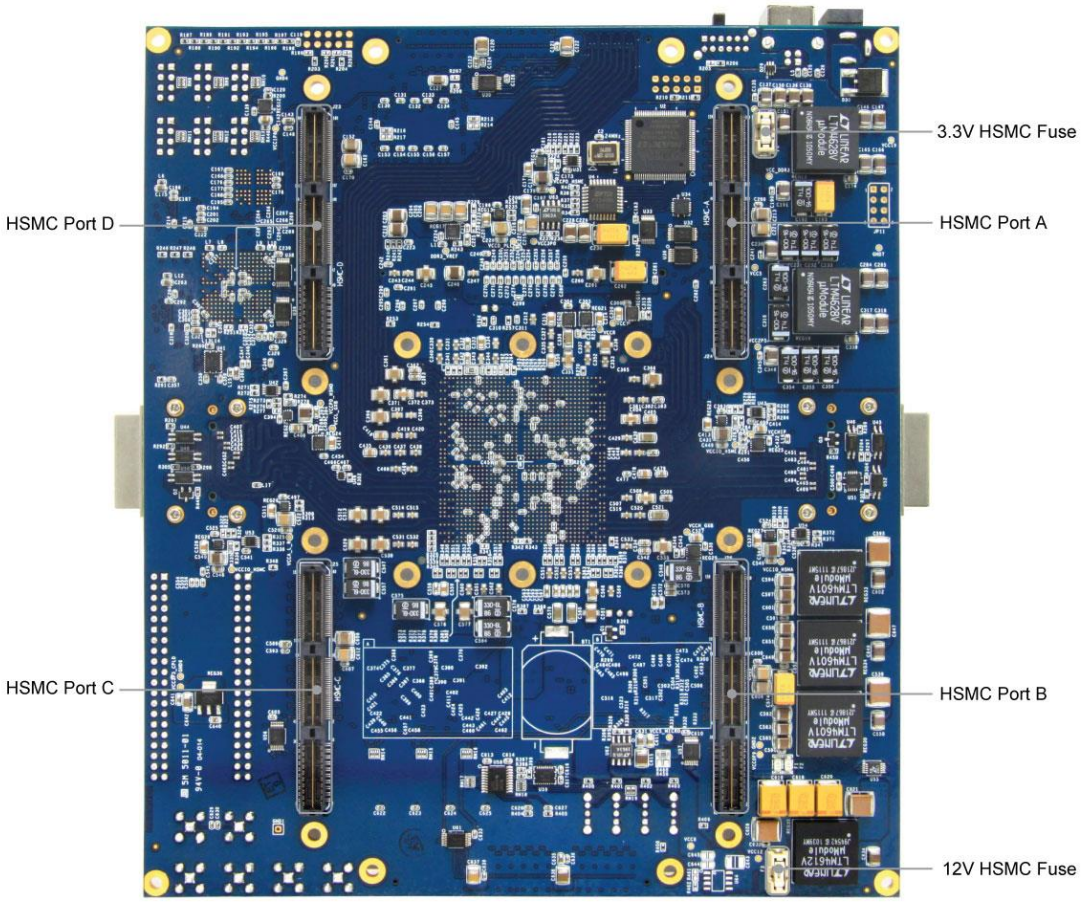

Figure 1-2 TR4 Board View (Bottom)

1.4 Block Diagram

Figure 1-3 shows the block diagram of the TR4 board. To provide maximum flexibility for the users, all key components are connected with the Stratix IV GX FPGA device, allowing the users to implement any system design.

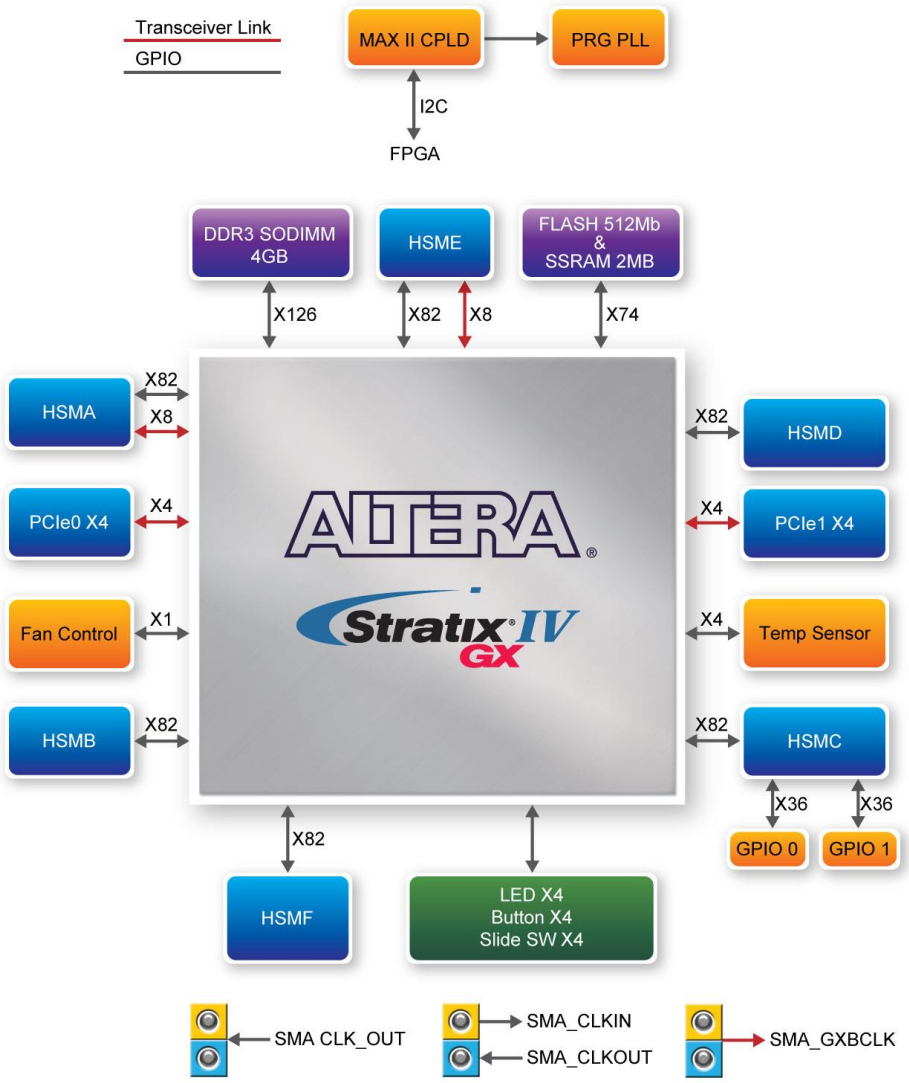

Figure 1-3 TR4 Block Diagram

Below is more detailed information regarding the blocks in Figure 1-3.

Stratix IV GX FPGA

EP4SGX230C2

- 228,000 logic elements (LEs)
- 17,133 total memory Kb
- 1,288 18x18-bit multipliers blocks
- 2 PCI Express hard IP blocks

- 744 user I/Os
- 8 phase locked loops (PLLs)

EP4SGX530C2

- 531,200 logic elements (LEs)
- 27,376K total memory Kb
- 1,024 18x18-bit multipliers blocks
- 4 PCI Express hard IP blocks
- 744 user I/Os
- 8 phase locked loops (PLLs)

Configuration Device and USB Blaster Circuit

- MAXII CPLD EPM2210 System Controller and Fast Passive Parallel (FPP) configuration
- On-board USB Blaster for use with the Quartus II Programmer
- Programmable PLL timing chip configured via MAX II CPLD
- Supports JTAG mode

Memory Devices

- 64MB Flash (32M x16) with a 16-bit data bus
- 2MB SSRAM (512K x 32)

DDR3 SO-DIMM Socket

- Up to 8GB capacity
- Maximum memory clock rate at 533MHz
- Theoretical bandwidth up to 68Gbps

LEDs

- 4 user-controllable LEDs
- Active-low

Push-buttons

- 4 user-defined inputs
- Active-low

Slide Switches

- 4 slide switches for user-defined inputs
- Logic low for DOWN position; Logic high for UP position

On-Board Clocking Circuitry

- 50MHz oscillator
- SMA connector pair for differential clock inputs
- SMA connector pair for differential clock outputs
- SMA connector for external clock input
- SMA connector for clock output

Two PCI Express x4 Edge Connectors

- Support connection speed of Gen1 at 2.5Gbps/lane to Gen2 at 5.0Gbps/lane
- Support downstream mode

Six High Speed Mezzanine Card (HSMC) Connectors

- Two HSMC ports include 16 pairs of CDR-based transceivers at data rates of up to 6.5Gbps
- Among HSMC Port A to D, there are 55 true LVDS TX channels to 1.6Gbps and 17 emulated LVDS TX channels up to 1.1Gbps whereas there are 9 additional TX channels from HSMC Port E.
- Configurable I/O standards - 1.5V, 1.8V, 2.5V, 3.0V

Two 40-pin GPIO Expansion Headers

- 72 FPGA I/O pins; 4 power and ground lines
- Shares pins with HSMC Port C
- Configurable I/O standards: 1.5V, 1.8V, 2.5V, 3.0V

Power

- Standalone DC 19V input

Other

- Temperature Sensor
- Cooling Fan

1.5 Assembly

Attach the included rubber (silicon) foot stands, as shown in **Figure 1-4**, to each of the four copper stands on the TR4 board.

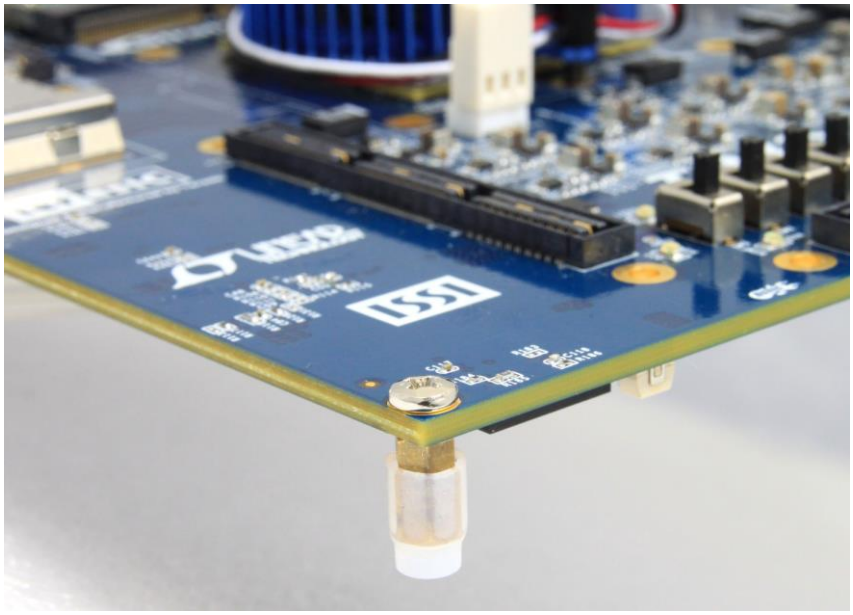

Figure 1-4 Mount Silicon Foot Stands

Chapter 2

Using the TR4 Board

This chapter gives instructions for using the TR4 board and its components.

It is strongly recommended that users read the *TR4 Getting Started Guide.pdf* before operating the TR4 board. The document is located in the *Usermanual* folder on the **TR4 System CD**. The contents of the document include the following:

- Introduction to the TR4 Development Board
- TR4 Development Kit Contents
- Key Features
- Before You Begin
- Software Installation
- Development Board Setup
- Programming the Stratix IV GX Device
- Programming through Flash

2.1 Configuration Options

■ JTAG FPGA Programming with USB-Blaster

The USB-blaster is implemented on the TR4 board to provide a JTAG configuration through the on-board USB-to-JTAG configuration logic through the type-B USB connector, an FTDI USB 2.0 PHY device, and an Altera MAX II CPLD. For this programming mode, configuration data will be lost when the power is turned off.

To download a configuration bit stream into the Stratix IV GX FPGA, perform the following steps:

- Make sure that power is provided to the TR4 board.
- Open JP7 to bypass the JTAG interface of the HSMC if it won't be used.
- Connect the USB cable supplied directly to the USB Blaster port of the TR4 board (see Figure 2-1).
- The FPGA can now be programmed in the Quartus II Programmer by selecting a configuration bit stream file with the .sof filename extension.
- If users need to use the JTAG interface on HSMC, please refer to Section 2.2 for detailed HSMC JTAG switch settings.

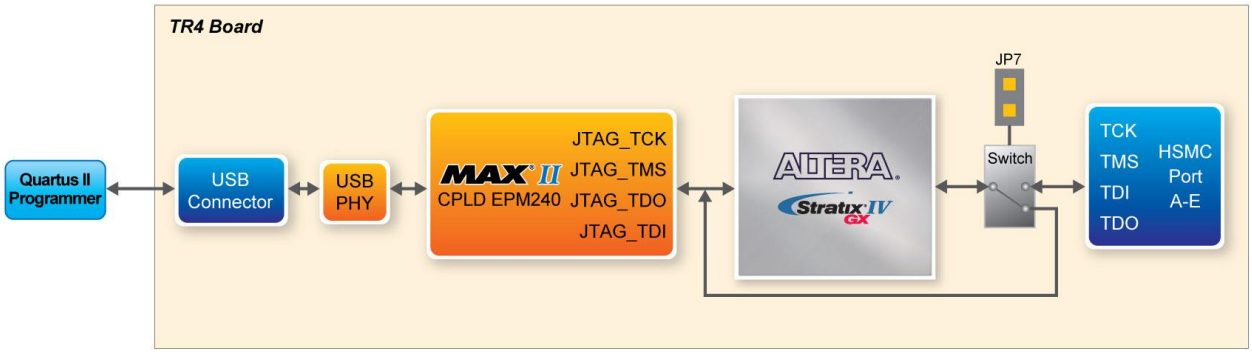

Figure 2-1 JTAG Configuration Scheme

■ JTAG FPGA Programming with External Blaster

The TR4 board supports JTAG programming over external blaster via J2. To use this interface, users need to solder a 2x5 pin connector (2.54mm pitch) to J2. Make sure JP7 is open to bypass the JTAG interface of HSMC.

■ Flash Programming

The TR4 development board contains a common Flash interface (CFI) memory to meet the demands for larger FPGA configurations. The Parallel Flash Loader (PFL) feature in MAX II devices provides an efficient method to program CFI flash memory devices through the JTAG interface and the logic to control configuration from the flash memory device to the Stratix IV GX FPGA. Figure 2-2 depicts the connection setup between the CFI flash memory, Max II CPLD, and Stratix IV GX.

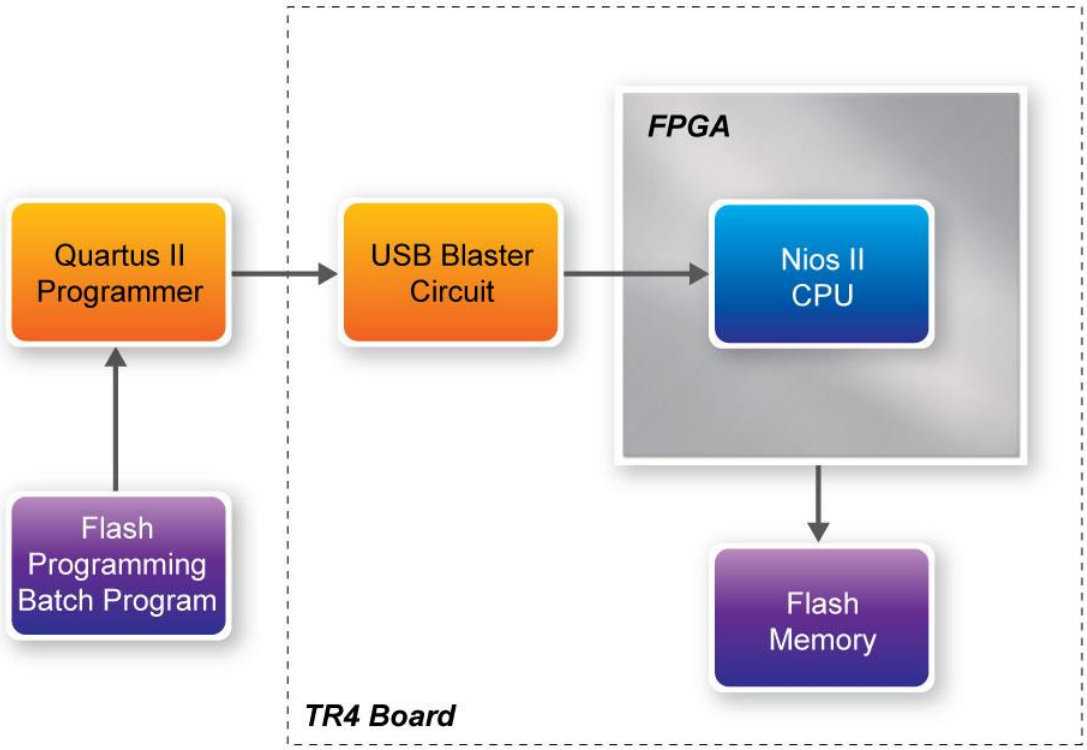

Figure 2-2 Flash Programming Scheme

■ Programming Flash Memory using Batch File

The TR4 provides a batch file (program_Flash.bat) to limit the steps that are taken when users program the flash memory on the TR4.

■ Software Requirements:

- Quartus II 11.1 or later
- Nios II IDE 11.1 or later
- Program_Flash folder contents:
- Program_Flash.bat
- Program_Flash.pl
- Program_Flash.sh
- tr4_default_flash_loader.sof
- boot_loader_cfi.srec

Before you use the program_Flash.bat batch file to program the flash memory, make sure the TR4 is

turned on and USB cable is connected to the USB blaster port (J4). In addition, place the .sof and .elf file you wish to program/convert in the *Program_Flash* directory.

Programming Flash Memory with .sof using Program_Flash.bat

1. Launch the program_Flash.bat batch file from the directory (*demonstrations\TR4_<Stratix device>\ TR4_Default_Flash_Loaderr\Program_Flash*) of the **TR4 system CD-ROM**.

2. The Flash program tool shows the menu options.

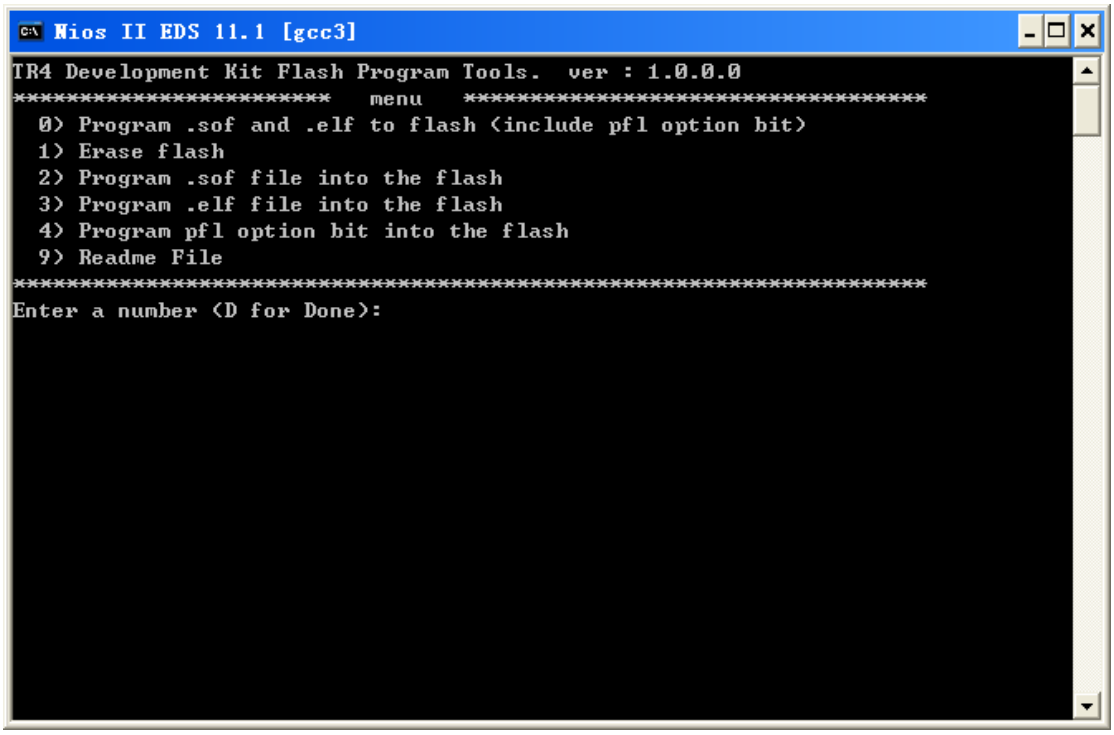

Figure 2-3 Flash Program Tools

3. Select option 2.

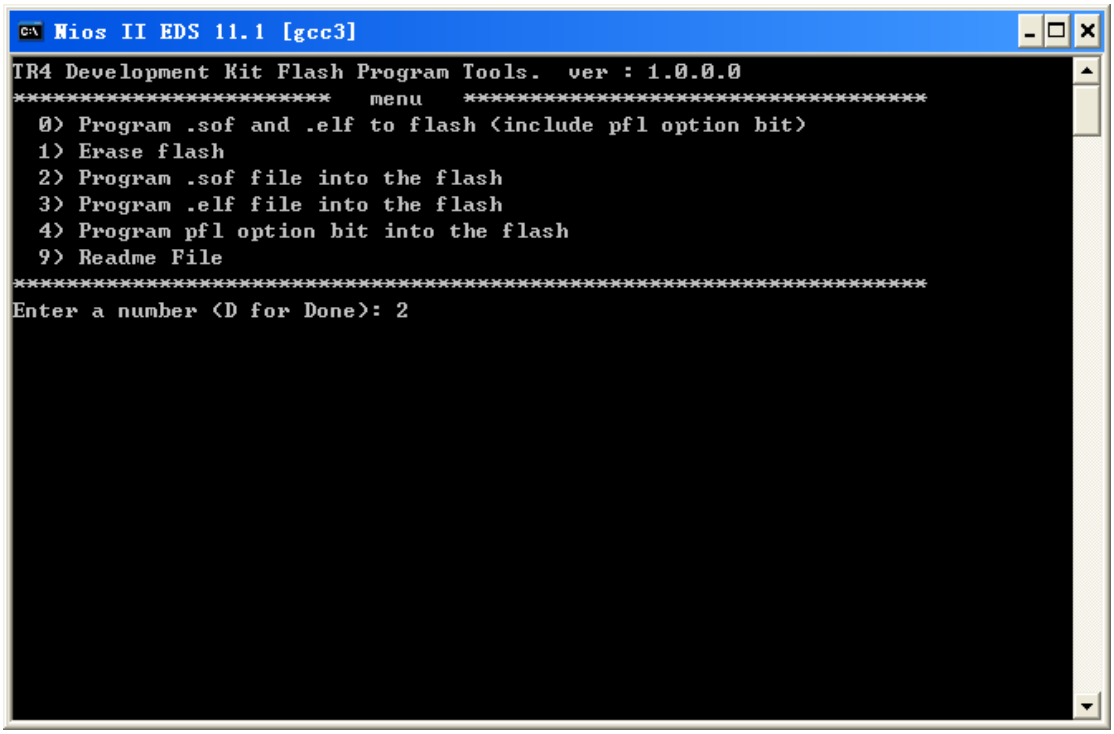

Figure 2-4 Option 2

4. Enter the .sof file name to be programmed onto the flash memory.

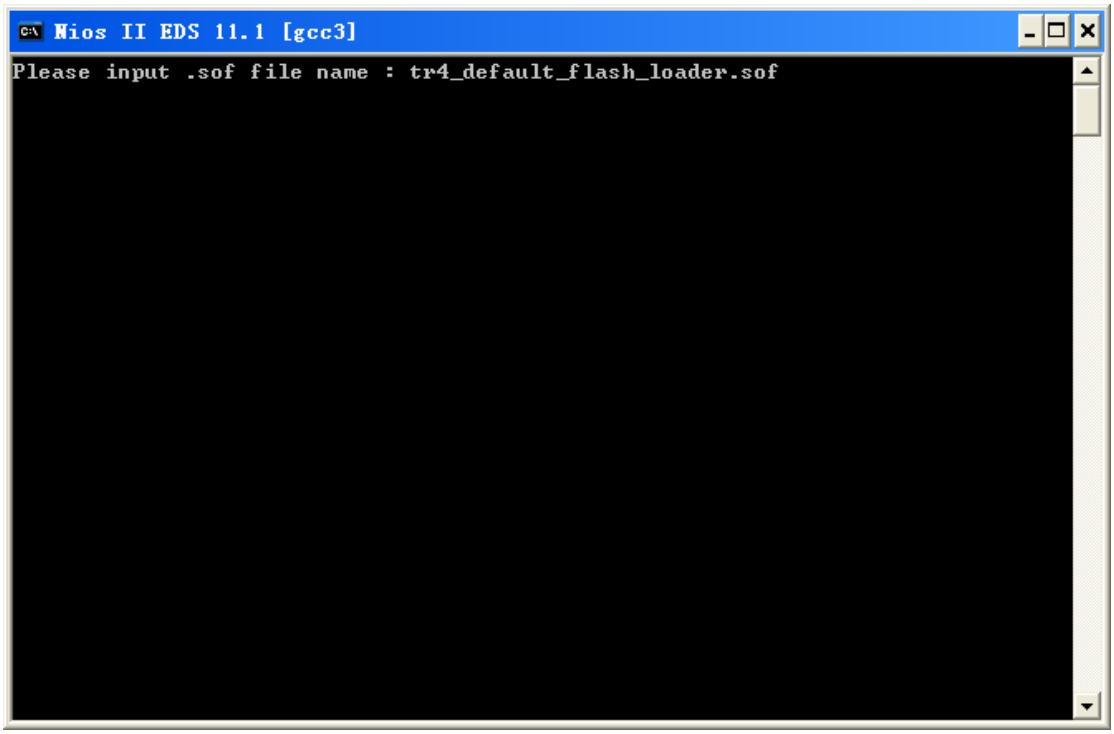

Figure 2-5 Enter .sof Name to Program

5. The following lines will appear during Flash programming: ‘Extracting Option bits SREC’, ‘Extracting FPGA Image SREC’, and ‘Deleting intermediate files’. If these lines don’t appear on the windows command, programming on the flash memory is not successfully set up. Please make sure Quartus II 11.1 and Nios II 11.1 IDE or later is used.

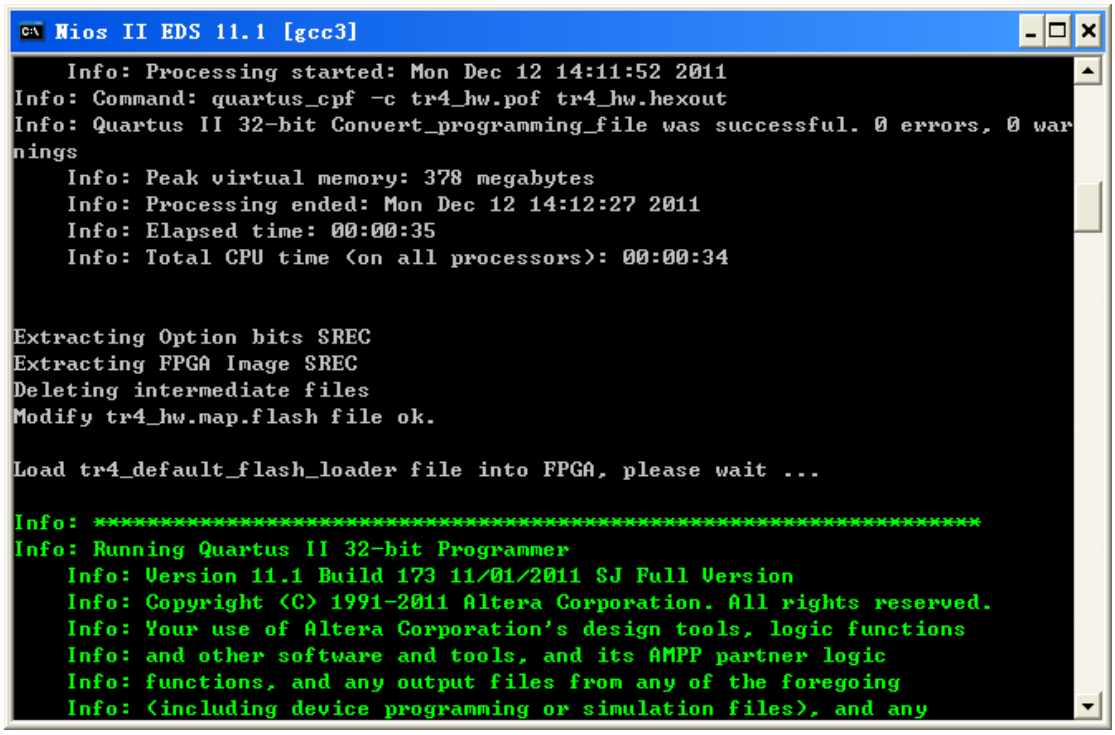

Figure 2-6 Loading .sof File

6. Erasing Flash.

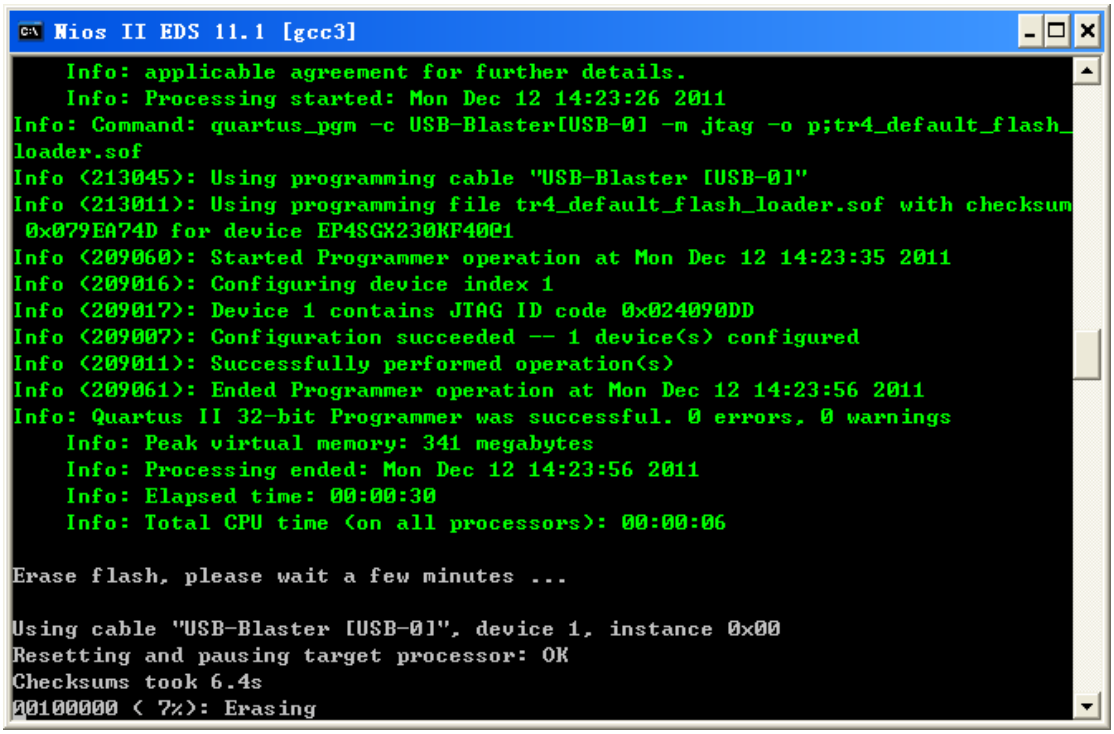

Figure 2-7 Erasing Flash

7. Programming Flash.

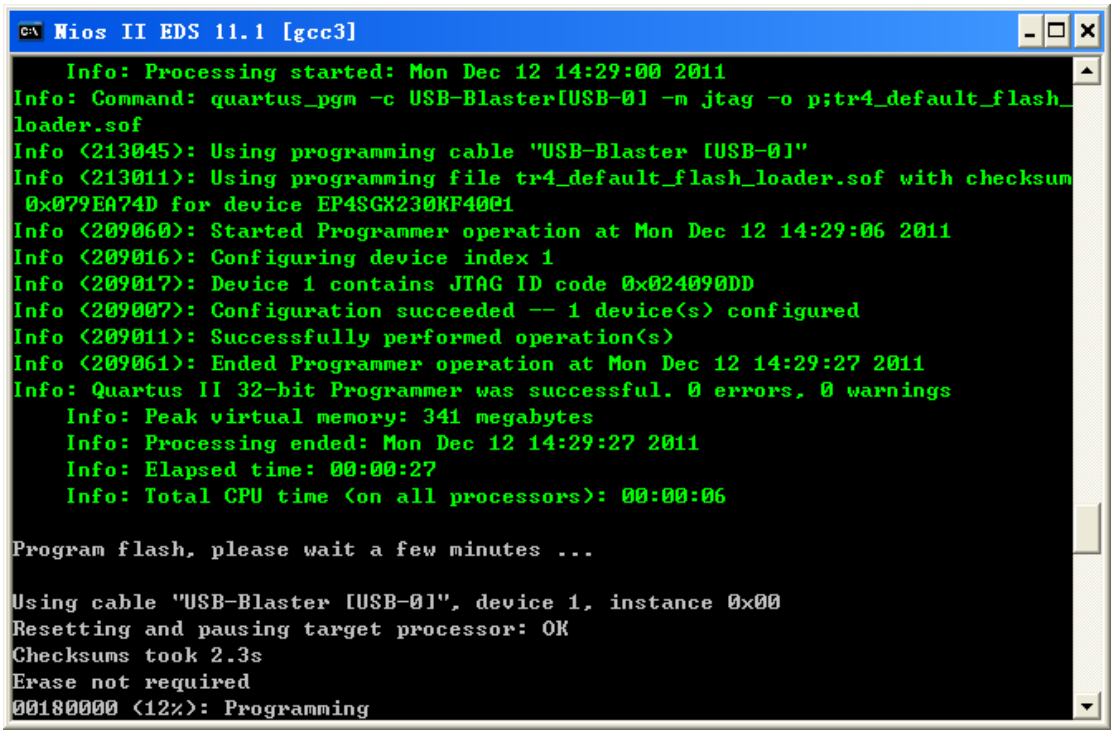

Figure 2-8 Programming Flash

8. Programming complete.

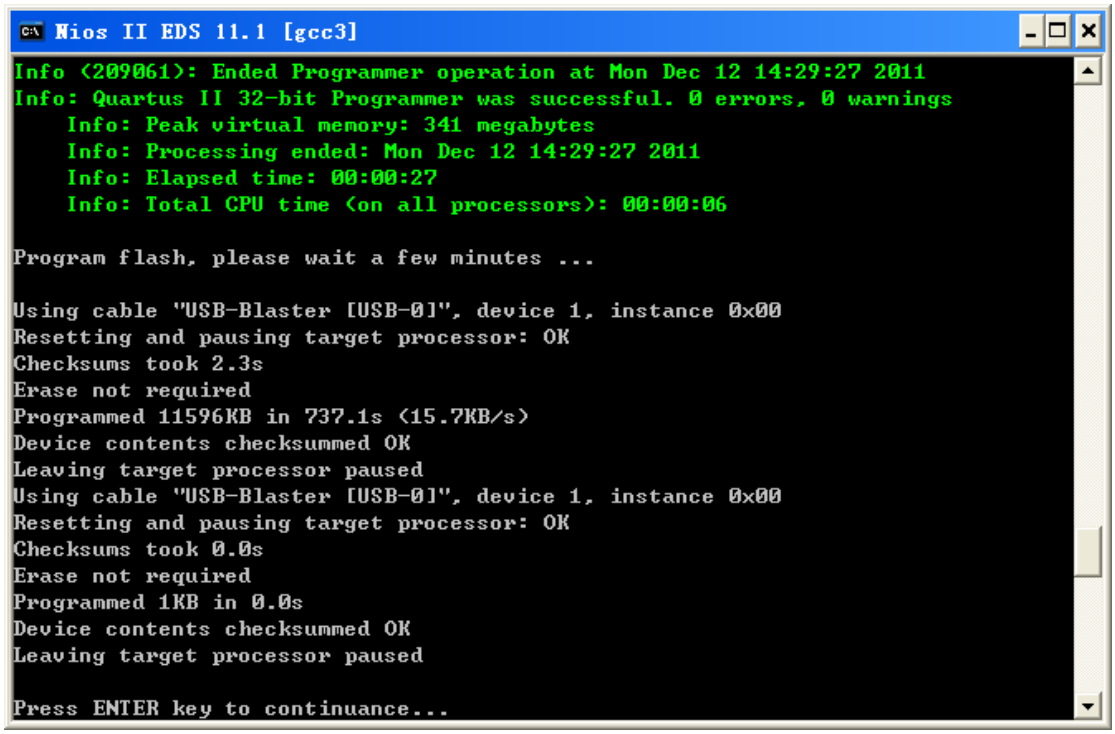

Figure 2-9 Programming Flash complete

2.2 Setup Elements

■ JTAG Control DIP Switch

The TR4 supports individual JTAG interfaces on each HSMC connector. This feature allows users to extend the JTAG chain to daughter cards or additional TR4s. **Before using this interface, JP7 needs to be shorted to enable the JTAG interface on all the HSMC connectors.**

The JTAG signals on each HSMC connector can be removed or included in the active JTAG chain via DIP switches. Table 2-1 lists the position of the DIP switches and their associated interfaces.

Note that if the JTAG interface on HSMC connector is enabled, make sure that the active JTAG chain must be a closed loop or the FPGA may not be detected. Section 2.5 will give an example on how to extend the JTAG interface to a daughter card. Also, a document named *Using_Mult-TR4_system.pdf* in TR4 system CD shows how to connect the JTAG interface on two stacked TR4 boards.

Table 2-1 JTAG Control

Components		Name	Description	Default
SW4	position 1	HSMCA_TOP	ON: HSMA TOP in-chain OFF: Bypass HSMA TOP	OFF
	position 2	HSMCB_TOP	ON: HSMB TOP in-chain OFF: Bypass HSMB TOP	OFF
	position 3	HSMCC_TOP	ON: HSMC TOP in-chain OFF: Bypass HSMC TOP	OFF
	position 4	HSMCD_TOP	ON: HSMD TOP in-chain OFF: Bypass HSMD TOP	OFF
SW5	position 1	HSMCA_BOT	ON: HSMA BOT in-chain OFF: Bypass HSMA BOT	OFF
	position 2	HSMCB_BOT	ON: HSMB BOT in-chain OFF: Bypass HSMB BOT	OFF
	position 3	HSMCC_BOT	ON: HSMC BOT in-chain OFF: Bypass HSMC BOT	OFF
	position 4	HSMCD_BOT	ON: HSMD BOT in-chain OFF: Bypass HSMD BOT	OFF
SW6	position 1	HSMCE_TOP	ON: HSME TOP in-chain OFF: Bypass HSME TOP	OFF
	position 2	HSMCF_TOP	ON: HSMF TOP in-chain OFF: Bypass HSMF TOP	OFF

2.3 Status Elements

The TR4 includes status LEDs. Please refer Table 2-2 for the status of the LED indicator.

Table 2-2 LED Indicators

Board Reference	LED name	Description
D13	HSMC Port E present	These LEDs are lit when HSMC Port A/B/C/D/E/F have a board or cable plugged-in such that pin 160 becomes grounded.
D14	HSMC Port D present	
D15	HSMC Port A present	
D20	HSMC Port C Present	
D27	HSMC Port B Present	
D28	HSMC Port F Present	
D16	USB Blaster Circuit	This LED is lit when the USB blaster circuit transmits or receives data.
D17	MAX_LOAD	This LED is lit when the FPGA is being actively configured.

D18	MAX_ERROR	This LED is lit when the MAX II CPLD EPM2210 System Controller fails to configure the FPGA.
D19	MAX_CONF_DONEn	This LED is lit when the FPGA is successfully configured.
D33	19V POWER	This LED is lit after the 19V adapter is plugged in
D1~D12	HSMC VCCIO_LED	These LEDs indicate the I/O standard of the HSMC ports (see Table 2-12)

2.4 General User Input/Output

■ Push-buttons

The TR4 includes six push-buttons that allow you to interact with the Stratix IV GX FPGA. Each of these buttons is debounced using a Schmitt Trigger circuit, as indicated in Figure 2-10. Each push-button provides a high logic level or a low logic level when it is not pressed or pressed, respectively (active-low).Table 2-3 lists the board references, signal names and their corresponding Stratix IV GX device pin numbers.

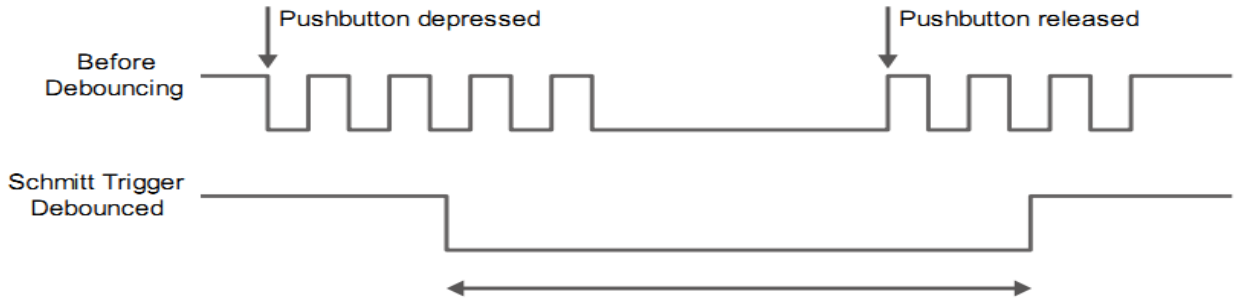

Figure 2-10 Push-button Debouncing

Table 2-3 Push-button Pin Assignments, Schematic Signal Names, and Functions

Name	*Locate*	*Description*	*I/O Standard*	*Stratix IV GX Pin Number*
PB3	BUTTON3	Low when pushed (Active-low)	1.5V	PIN_P20
PB4	BUTTON2		1.5V	PIN_A19
PB5	BUTTON1		1.5V	PIN_M19
PB6	BUTTON0		1.5V	PIN_L19

The **MAX_RSTN** push-button is used to reset the MAX II EPM2210 CPLD. The **Config** push-button can configure default code to FPGA. Table 2-4 lists the board references, signal names and their corresponding Stratix IV GX device pin numbers.

Table 2-4 Push-button Pin Assignments, Schematic Signal Names, and Functions

Name	*Locate*	*Description*	*I/O Standard*	*EPM2210 Pin Number*
PB1	MAX_RSTn	MAX II reset	3.3V-VTTL	PIN_M9
PB2	CONFIG	FPGA reconfig	3.3V-VTTL	PIN_D12

■ Slide Switches

There are four slide switches on the TR4 to provide additional FPGA input control. Each switch is connected directly to a pin of the Stratix IV GX FPGA. When a slide switch is in the DOWN position or the UP position, it provides a low logic level or a high logic level (**VCCIO_HSMF** or **VCCIO_HSMA**) to the FPGA, respectively. Table 2-5 lists the board references, signal names and their corresponding Stratix IV GX device pin numbers.

Table 2-5 Slide Switches Pin Assignments, Schematic Signal Names, and Functions

Name	*Locate*	*Description*	*I/O Standard*	*Stratix IV GX Pin Number*
SW0	SLIDE SW	Provides high logic level when in the UP position	VCCIO_HSMF	PIN_AH18
SW1	SLIDE SW		VCCIO_HSMF	PIN_AH19
SW2	SLIDE SW		VCCIO_HSMA	PIN_D6
SW3	SLIDE SW		VCCIO_HSMA	PIN_C6

■ LEDs

The TR4 consists of 4 user-controllable LEDs to allow status and debugging signals to be driven to the LEDs from the designs loaded into the Stratix IV GX device. Each LED is driven directly by the Stratix IV GX FPGA. The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively (active-low). A list of the pin names on the FPGA that are connected to the LEDs is given in Table 2-6.

Table 2-6 User LEDs Pin Assignments, Schematic Signal Names, and Functions

Name	*Description*	*Description*	*I/O Standard*	*Stratix IV GX Pin Number*

D27	LED0	LEDs turn on when output is logic low (Active-low)	1.5V	PIN_B19
D28	LED1		1.5V	PIN_A18
D29	LED2		1.5V	PIN_D19
D30	LED3		1.5V	PIN_C19

2.5 High-Speed Mezzanine Cards

The High Speed Mezzanine Card (HSMC) interface provides a mechanism to extend the peripheral-set of an FPGA host board by means of add-on daughter cards, which can address today's high speed signaling requirements as well as low-speed device interface support. The HSMC interfaces support JTAG, clock outputs and inputs, high-speed serial I/O (transceivers), and single-ended or differential signaling. The detailed specifications of the HSMC connectors are described below:

■ 6 HSMC Connector Groups

There are ten HSMC connectors on the TR4 board are divided into 6 groups: HSMC A, HSMC B, HSMC C, HSMC D, HSMC E, and HSMC F. Each group has a male and female HSMC port on the top and bottom side of the TR4 board **except HSMC E and HSMC F.** In addition, both the male and female HSMC connector share the same I/O pins besides JTAG interface and high-speed serial I/O (transceivers).

Caution: DO NOT connect HSMC daughter cards to the backside HSMC (male) connectors. Doing so will permanently damage the on-board FPGA.

■ I/O Distribution

The HSMC connector on the TR4 includes a total of 172 pins, including 121 signal pins (120 signal pins +1 PSNTn pin), 39 power pins, and 12 ground pins. **Figure 2-11** shows the signal bank diagram of HSMC connector. Bank 1 also has dedicated JTAG, I2C bus, and clock signals. The main CMOS/LVDS interface signals, including LVDS/CMOS clocks, are found in banks 2 and 3. Both 12V and 3.3V power pins are also found in banks 2 and 3.

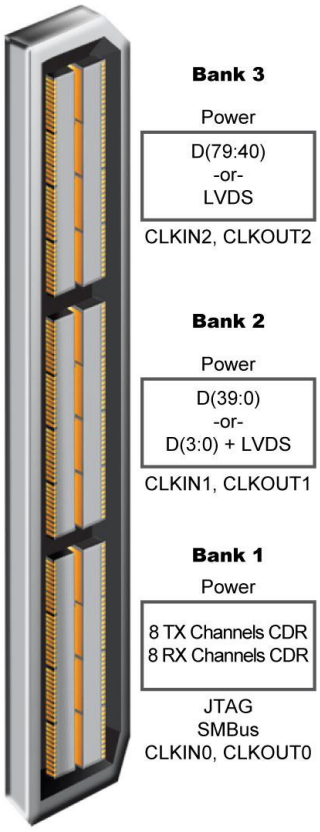

Figure 2-11 HSMC Signal Bank Diagram

Due to the limitation of FPGA bank I/O distribution and dedicated clock in/out pin numbers, there are some differences between individual HSMC connectors, listed below:

■ LVDS Interface

On the TR4 board, only HSMC ports A, B, C and D support LVDS. Each HSMC port provides 18*(1)* LVDS channel transceivers.

For LVDS transmitters, HSMC ports A and D support 18 true LVDS channels which can run up to 1.6Gbps. The LVDS transmitter on HSMC Port B and C contain true and emulated LVDS channels.

The emulated LVDS channels use two single-ended output buffers and external resistors as shown in **Figure 2-12**. The associated I/O standard of these differential FPGA I/O pins in the Quartus II project should be set to LVDS_E_3R. Emulated LVDS I/O data rates can reach speeds up to 1.1Gbps. The factory default setting for the Rs resistor will be 0 ohm and the Rp resistor will not be assembled for single-ended I/O standard applications. For emulated LVDS transmitters, please solder 120 and 170 ohm resistors onto the Rs and Rp positions, respectively.

For the LVDS receivers, HSMC Port A/B/D support true LVDS receivers which can run at 1.6Gbps. Unlike HSMC ports A/D, not all the LVDS receivers in HSMC ports B/C support On-Chip termination (OCT). To use these I/Os as LVDS receivers, the user needs to solder a 100 ohm resistor for input termination as show in **Figure 2-12**.

Table 2-7 gives the detailed numbers of true and emulated LVDS interfaces of each HSMC port. Also, it lists the numbers of LVDS receivers needed to assemble external input termination resistors on each HSMC ports.

Table 2-8 shows all the external input differential resistors for LVDS receivers on HSMC Port B and C. The factory default setting is not installed.

Finally, because HSMC Port C shares FPGA I/O pins with GPIO headers, so the LVDS performance can only support a data rate of up to 500Mbps.

(1) Although the specifications of the HSMC connector defines signals D0~D3 as single-ended I/Os, D0 and D2 can be used as LVDS transmitters and D1 and D3 can be used as LVDS receivers on the TR4.

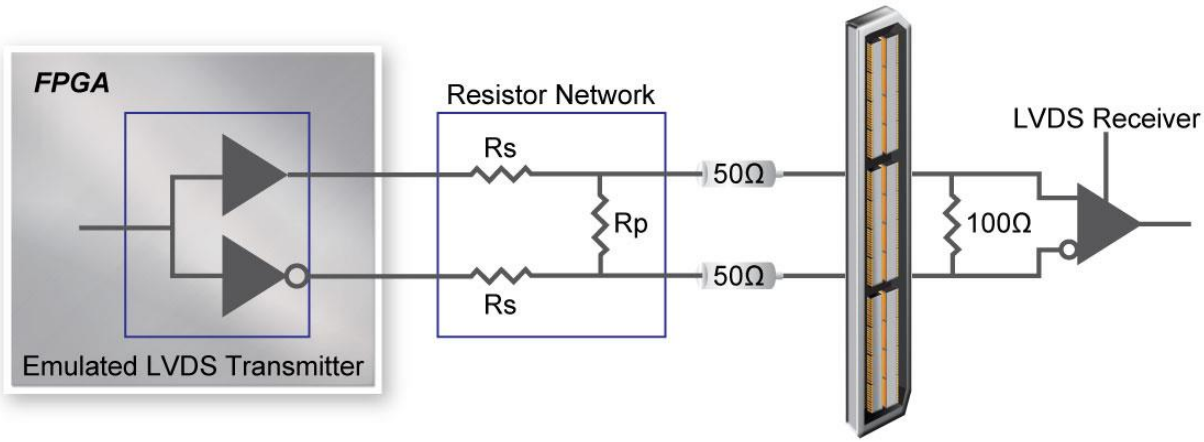

Figure 2-12 Emulated LVDS Resistor Network between FPGA and HSMC Port