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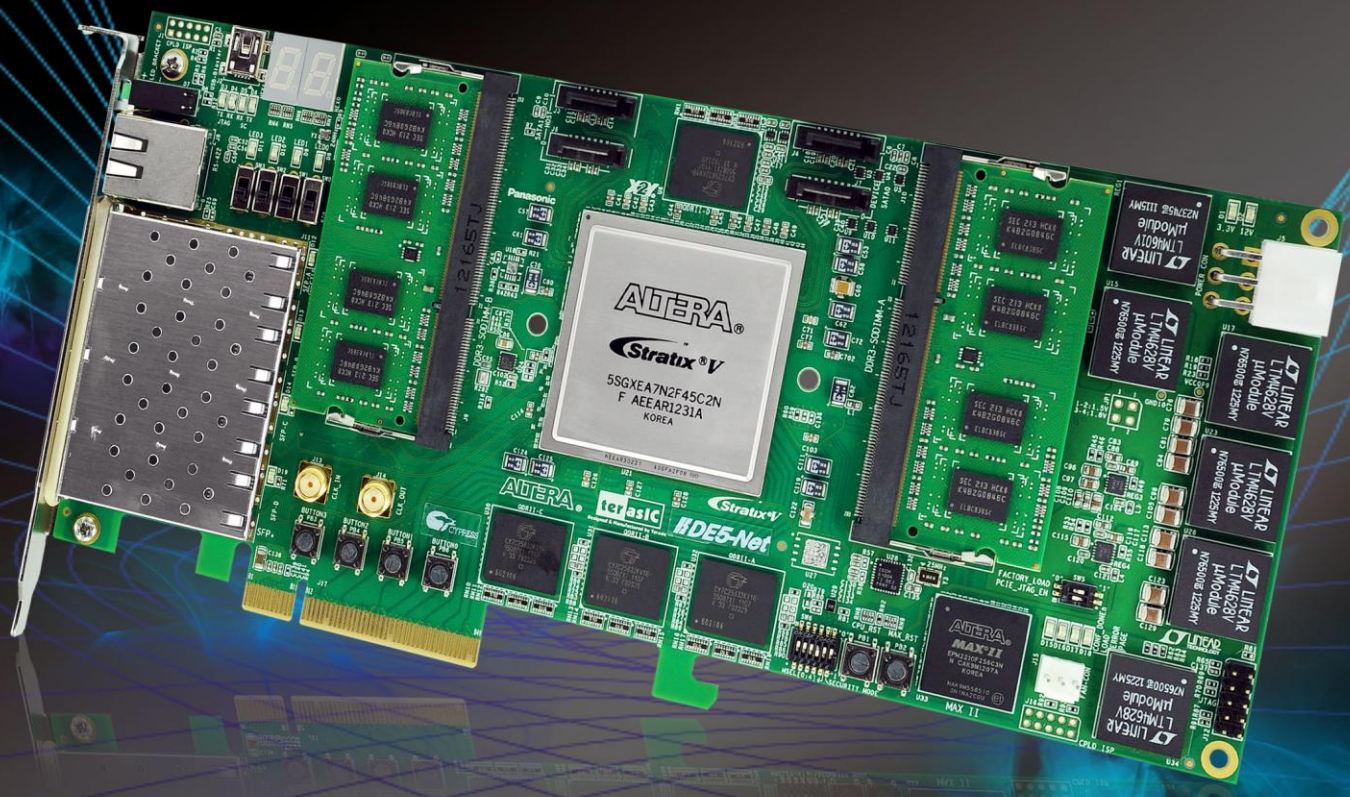
DE5-Net

FPGA Development Kit

User Manual



CONTENTS

Chapter 1

Overview

This chapter provides an overview of the DE5-Net Development Board and installation guide.

1.1 General Description

The Terasic DE5-Net Stratix V GX FPGA Development Kit provides the ideal hardware solution for designs that demand high capacity and bandwidth memory interfacing, ultra-low latency communication, and power efficiency. With a full-height, 3/4-length form-factor package, the DE5-Net is designed for the most demanding high-end applications, empowered with the top-of-the-line Altera Stratix V GX, delivering the best system-level integration and flexibility in the industry.

The Stratix® V GX FPGA features integrated transceivers that transfer at a maximum of 12.5 Gbps, allowing the DE5-Net to be fully compliant with version 3.0 of the PCI Express standard, as well as allowing an ultra low-latency, straight connections to four external 10G SFP+ modules. Not relying on an external PHY will accelerate mainstream development of network applications enabling customers to deploy designs for a broad range of high-speed connectivity applications. For designs that demand high capacity and high speed for memory and storage, the DE5-Net delivers with two independent banks of DDR3 SO-DIMM RAM, four independent banks of QDRII+ SRAM, high-speed parallel flash memory, and four SATA ports. The feature-set of the DE5-Net fully supports all high-intensity applications such as low-latency trading, cloud computing, high-performance computing, data acquisition, network processing, and signal processing.

1.2 Key Features

The following hardware is implemented on the DE5-Net board:

■ FPGA

- Altera Stratix® V GX FPGA (5SGXEA7N2F45C2)

■ FPGA Configuration

- On-Board USB Blaster II or JTAG header for FPGA programming
- Fast passive parallel (FPPx32) configuration via MAX II CPLD and flash memory

■ General user input/output:

- 10 LEDs
- 4 push-buttons
- 4 slide switches
- 2 seven-segment displays

■ Clock System

- 50MHz Oscillator
- Programmable oscillators Si570, CDCM61001 and CDCM61004
- One SMA connector for external clock input
- One SMA connector for clock output

■ Memory

- DDR3 SO-DIMM SDRAM
- QDRII+ SRAM
- FLASH

■ Communication Ports

- Four SFP+ connectors
- Two Serial ATA host ports
- Two Serial ATA device ports
- PCI Express (PCIe) x8 edge connector
- One RS422 transceiver with RJ45 connector

■ System Monitor and Control

- Temperature sensor
- Fan control

■ Power

- PCI Express 6-pin power connector, 12V DC Input
- PCI Express edge connector power

■ Mechanical Specification

- PCI Express full-height and 3/4-length

1.3 Block Diagram

Figure 1-1 shows the block diagram of the DE5-Net board. To provide maximum flexibility for the users, all key components are connected with the Stratix V GX FPGA device. Thus, users can configure the FPGA to implement any system design.

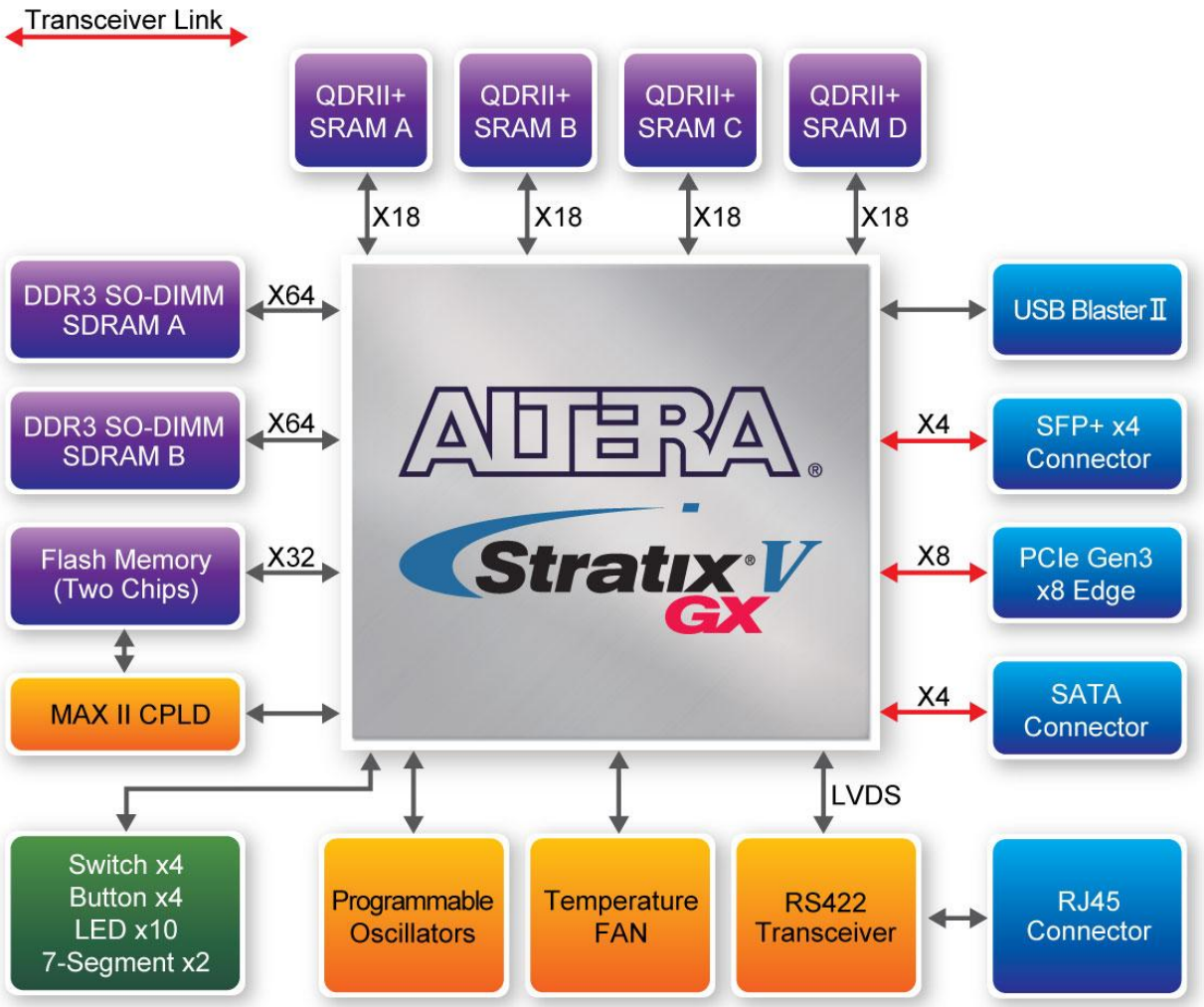


Figure 1-1 Block diagram of the DE5-Net board

Below is more detailed information regarding the blocks in Figure 1-1.

Stratix V GX FPGA

- 5SGXEA7N2F45C2
- 622,000 logic elements (LEs)
- 50-Mbits embedded memory
- 48 transceivers (12.5Gbps)
- 512 18-bit x 18-bit multipliers
- 256 27-bit x 27-bit DSP blocks

- 2 PCI Express hard IP blocks
- 840 user I/Os
- 210 full-duplex LVDS channels
- 28 phase locked loops (PLLs)

JTAG Header and FPGA Configuration

- On-board USB Blaster II or JTAG header for use with the Quartus Prime Programmer
- MAXII CPLD EPM2210 System Controller and Fast Passive Parallel (FPP) configuration

Memory devices

- 32MB QDRII+ SRAM
- Up to 8GB DDR3 SO-DIMM SDRAM
- 256MB FLASH

General user I/O

- 10 user controllable LEDs
- 4 user push buttons
- 4 user slide switches
- 2 seven-segment displays

On-Board Clock

- 50MHz oscillator
- Programming PLL providing clock for 10G SFP+ transceiver
- Programming PLL providing clock for SATA or 1G SFP+ transceiver

Four Serial ATA ports

- SATA 3.0 standard at 6Gbps signaling rate

Four SFP+ ports

- Four SFP+ connector (10 Gbps+)

PCI Express x8 edge connector

- Support for PCIe Gen1/2/3
- Edge connector for PC motherboard with x8 or x16 PCI Express slot

Power Source

- PCI Express 6-pin DC 12V power
- PCI Express edge connector power

Chapter 2

Board Components

This chapter introduces all the important components on the DE5-Net.

2.1 Board Overview

Figure 2-1 is the top and bottom view of the DE5-Net development board. It depicts the layout of the board and indicates the location of the connectors and key components. Users can refer to this figure for relative location of the connectors and key components.

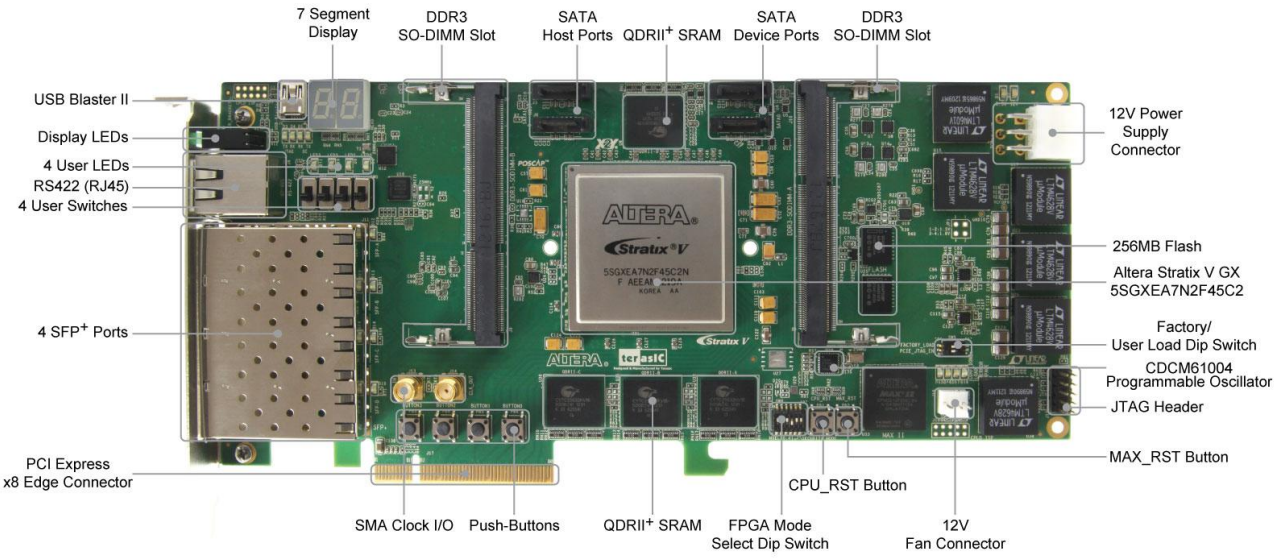


Figure 2-1 FPGA Board (Top)

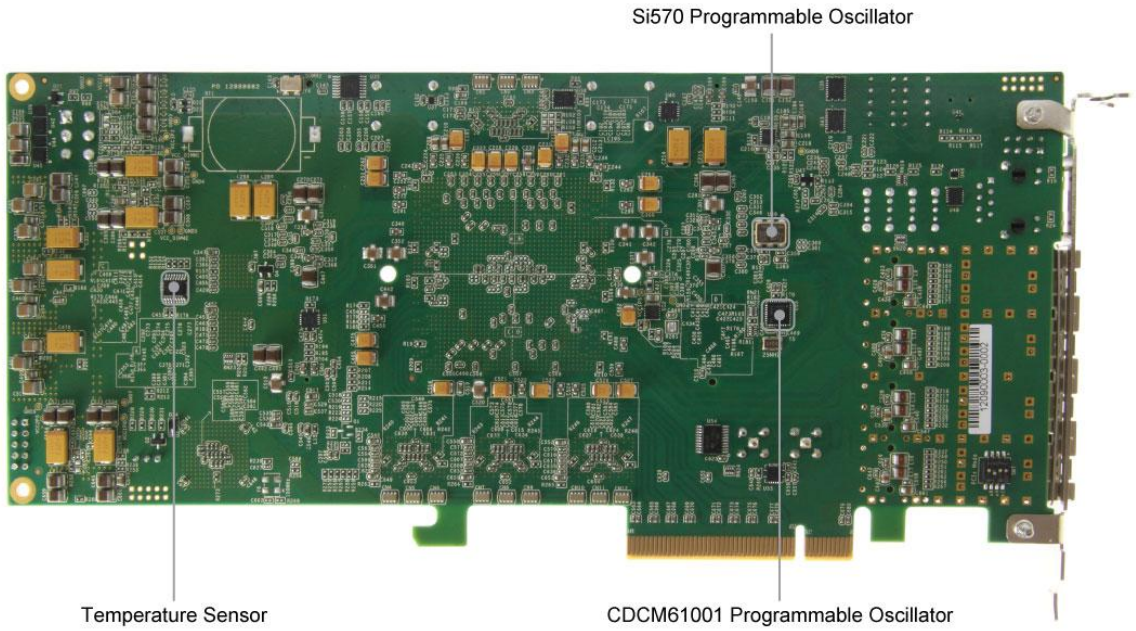


Figure 2-2 FPGA Board (Bottom)

2.2 Configuration, Status and Setup

■ Configure

The FPGA board supports two configuration methods for the Stratix V FPGA:

- Configure the FPGA using the on-board USB-Blaster II.
- Flash memory configuration of the FPGA using stored images from the flash memory on power-up.

For programming by on-board USB-Blaster II, the following procedures show how to download a configuration bit stream into the Stratix V GX FPGA:

- Make sure that power is provided to the FPGA board
- Connect your PC to the FPGA board using a mini-USB cable and make sure the USB-Blaster II driver is installed on PC.
- Launch Quartus Prime programmer and make sure the USB-Blaster II is detected.
- In Quartus Prime Programmer, add the configuration bit stream file (.sof), check the associated "Program/Configure" item, and click "Start" to start FPGA programming.

■ Status LED

The FPGA Board development board includes board-specific status LEDs to indicate board status. Please refer to Table 2-1 for the description of the LED indicator.

Table 2-1 Status LED

Board Reference	*LED Name*	*Description*
D2	12-V Power	Illuminates when 12-V power is active.
D1	3.3-V Power	Illuminates when 3.3-V power is active.
D15	CONF DONE	Illuminates when the FPGA is successfully configured. Driven by the MAX II CPLD EPM2210 System Controller.
D16	Loading	Illuminates when the MAX II CPLD EPM2210 System Controller is actively configuring the FPGA. Driven by the MAX II CPLD EPM2210 System Controller with the Embedded Blaster CPLD.
D17	Error	Illuminates when the MAX II CPLD EPM2210 System Controller fails to configure the FPGA. Driven by the MAX II CPLD EPM2210 System Controller.
D18	PAGE	Illuminates when FPGA is configured by the factory configuration bit stream.

■ Setup PCI Express Control DIP switch

The PCI Express Control DIP switch (SW7) is provided to enable or disable different configurations of the PCIe Connector. Table 2-2 lists the switch controls and description.

Table 2-2 SW3 PCIe Control DIP Switch

Board Reference	*Signal Name*	*Description*	*Default*
SW7.1	PCIE_PRSNT2n_x1	On : Enable x1 presence detect Off: Disable x1 presence detect	Off
SW7.2	PCIE_PRSNT2n_x4	On : Enable x4 presence detect Off: Disable x4 presence detect	Off
SW7.3	PCIE_PRSNT2n_x8	On : Enable x8 presence detect Off: Disable x8 presence detect	On

■ Setup Configure Mode Control DIP switch

The Configure Mode Control DIP switch (SW6) is provided to specify the configuration mode of the FPGA. As currently only one mode is supported, please set all positions as shown in **Figure 2-3**.

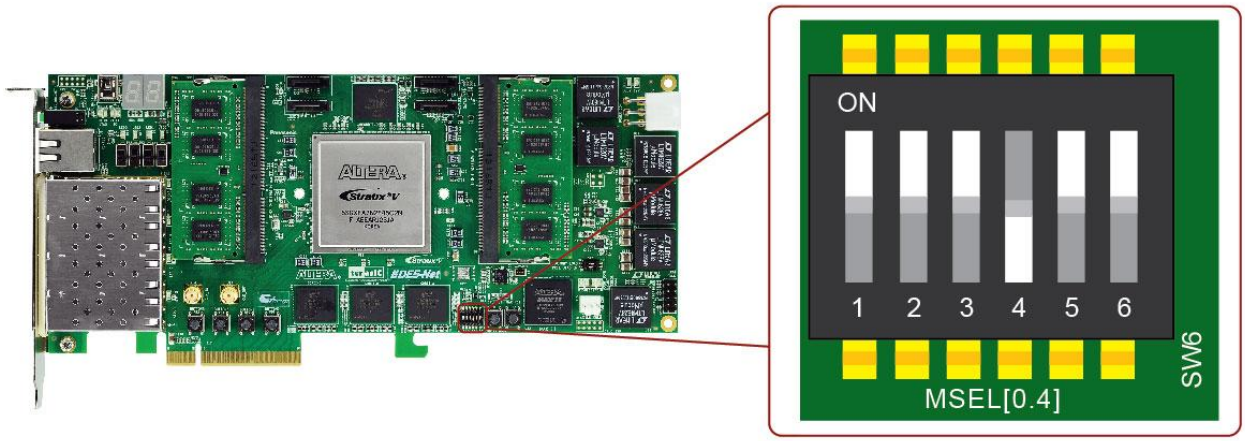


Figure 2-3 6-Position DIP switch for Configure Mode

■ Select Flash Image for Configuration

The Image Select DIP switch (SW5) is provided to specify the image for configuration of the FPGA. Setting Position 2 of SW5 to high (right) specifies the default factory image to be loaded, as shown in **Figure 2-4**. Setting Position 2 of SW5 to low (left) specifies the DE5-Net to load a user-defined image, as shown in **Figure 2-5**.

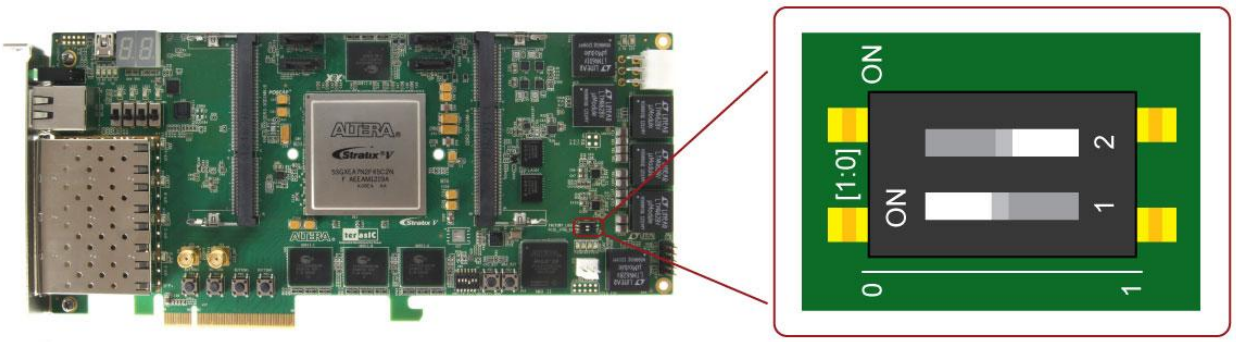


Figure 2-4 2-position DIP switch for Image Select – Factory Image Load

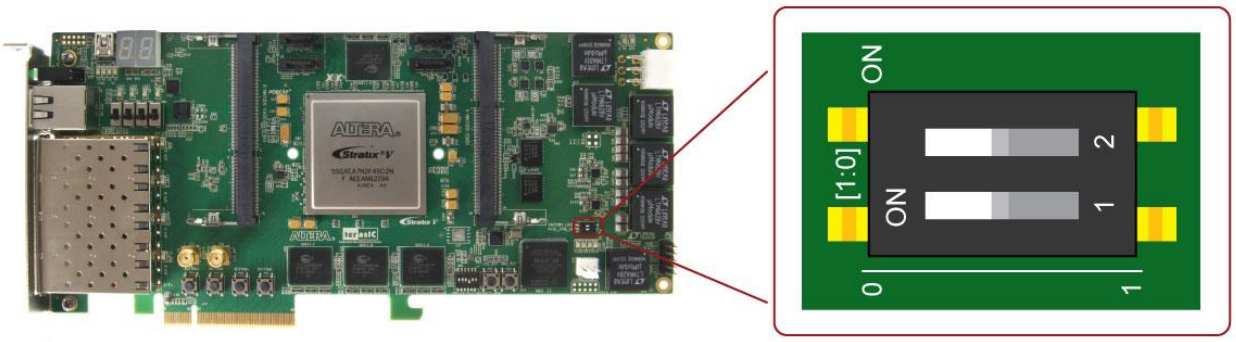


Figure 2-5 2-position DIP switch for Image Select – User Image Load

2.3 General User Input/Output

This section describes the user I/O interface to the FPGA.

■ User Defined Push-buttons

The FPGA board includes four user defined push-buttons that allow users to interact with the Stratix V GX device. Each push-button provides a high logic level or a low logic level when it is not pressed or pressed, respectively. Table 2-3 lists the board references, signal names and their corresponding Stratix V GX device pin numbers.

Table 2-3 Push-button Pin Assignments, Schematic Signal Names, and Functions

Board Reference	*Schematic Signal Name*	*Description*	*I/O Standard*	*Stratix V GX Pin Number*

PB6	BUTTON0	High Logic Level when the button is not pressed	2.5-V	PIN_AK15
PB5	BUTTON1		2.5-V	PIN_AK14
PB4	BUTTON2		2.5-V	PIN_AL14
PB3	BUTTON3		2.5-V	PIN_AL15

■ User-Defined Slide Switch

There are four slide switches on the FPGA board to provide additional FPGA input control. When a slide switch is in the DOWN position or the UPPER position, it provides a low logic level or a high logic level to the Stratix V GX FPGA, respectively, as shown in Figure 2-6.

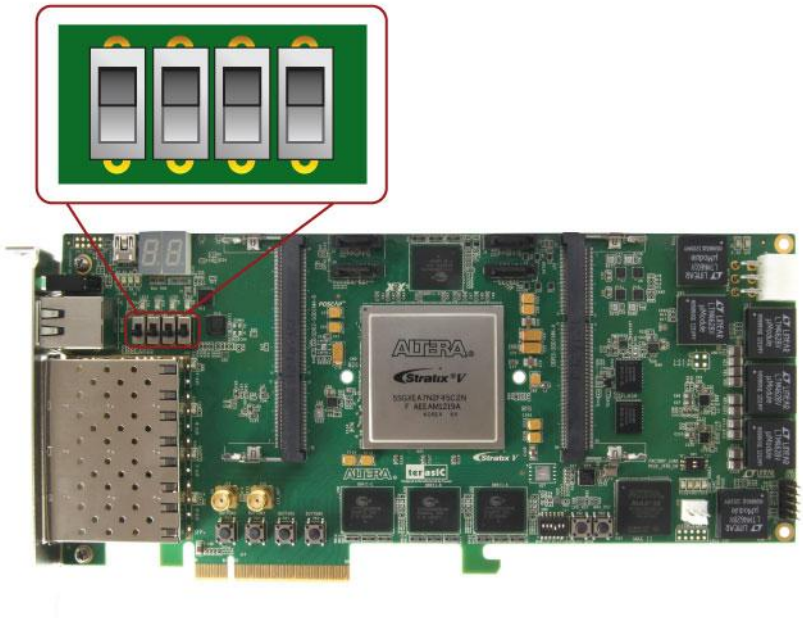


Figure 2-6 4 Slide switches

Table 2-4 lists the signal names and their corresponding Stratix V GX device pin numbers.

Table 2-4 Slide Switch Pin Assignments, Schematic Signal Names, and Functions

Board Reference	*Schematic Signal Name*	*Description*	*I/O Standard*	*Stratix V GX Pin Number*
SW0	SW0	High logic level when SW in the UPPER position.	1.8-V	PIN_B25
SW1	SW1		1.8-V	PIN_A25
SW2	SW2		1.8-V	PIN_B23

SW3	SW3		1.8-V	PIN_A23

■ User-Defined LEDs

The FPGA board consists of 10 user-controllable LEDs to allow status and debugging signals to be driven to the LEDs from the designs loaded into the Stratix V GX device. Each LED is driven directly by the Stratix V GX FPGA. The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin names on the FPGA that are connected to the LEDs is given in Table 2-5.

Table 2-5 User LEDs Pin Assignments, Schematic Signal Names, and Functions

Board Reference	*Schematic Signal Name*	*Description*	*I/O Standard*	*Stratix V GX Pin Number*
D8	LED0	Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	2.5-V	PIN_AW37
D9	LED1		2.5-V	PIN_AV37
D10	LED2		2.5-V	PIN_BB36
D11	LED3		2.5-V	PIN_BB39
D7-1	LED_BRACKET0		2.5-V	PIN_AH15
D7-3	LED_BRACKET1		2.5-V	PIN_AH13
D7-5	LED_BRACKET2		2.5-V	PIN_AJ13
D7-7	LED_BRACKET3		2.5-V	PIN_AJ14
J8-10	LED_RJ45_L		2.5-V	PIN_AG15
J8-12	LED_RJ45_R		2.5-V	PIN_AG16

■ 7-Segment Displays

The FPGA board has two 7-segment displays. As indicated in the schematic in Figure 2-7, the seven segments are connected to pins of the Stratix V GX FPGA. Applying a low or high logic level to a segment will turn it on or turn it off, respectively.

Each segment in a display is identified by an index listed from 0 to 6 with the positions given in Figure 2-8. In addition, the decimal point is identified as DP. Table 2-6 shows the mapping of the FPGA pin assignments to the 7-segment displays.

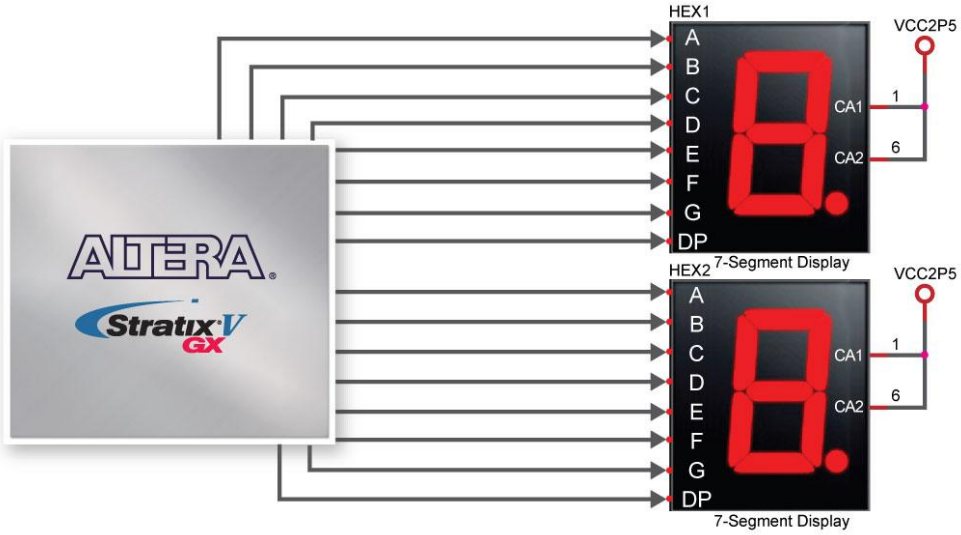


Figure 2-7 Connection between 7-segment displays and Stratix V GX FPGA

Figure 2-8 Position and index of each segment in a 7-segment display

Table 2-6 User LEDs Pin Assignments, Schematic Signal Names, and Functions

Board Reference	*Schematic Signal Name*	*Description*	*I/O Standard*	*Stratix V GX Pin Number*
HEX1	HEX1_D0	User-Defined 7-Segment Display. Driving logic 0 on the I/O port turns the 7-segment signal ON. Driving logic 1 on the I/O port turns the 7-segment signal OFF.	1.5-V	PIN_H18
HEX1	HEX1_D1		1.5-V	PIN_G16
HEX1	HEX1_D2		1.5-V	PIN_F16
HEX1	HEX1_D3		1.5-V	PIN_A7
HEX1	HEX1_D4		1.5-V	PIN_B7
HEX1	HEX1_D5		1.5-V	PIN_C9
HEX1	HEX1_D6		1.5-V	PIN_D10

HEX1	HEX1_DP		1.5-V	PIN_E9
HEX0	HEX0_D0		1.5-V	PIN_G8
HEX0	HEX0_D1		1.5-V	PIN_H8
HEX0	HEX0_D2		1.5-V	PIN_J9
HEX0	HEX0_D3		1.5-V	PIN_K10
HEX0	HEX0_D4		1.5-V	PIN_K8
HEX0	HEX0_D5		1.5-V	PIN_K9
HEX0	HEX0_D6		1.5-V	PIN_N8
HEX0	HEX0_DP		1.5-V	PIN_P8

2.4 Temperature Sensor and Fan Control

The FPGA board is equipped with a temperature sensor, MAX1619, which provides temperature sensing and over-temperature alert. These functions are accomplished by connecting the temperature sensor to the internal temperature sensing diode of the Stratix V GX device. The temperature status and alarm threshold registers of the temperature sensor can be programmed by a two-wire SMBus, which is connected to the Stratix V GX FPGA. In addition, the 7-bit POR slave address for this sensor is set to '0011000b'.

An optional 3-pin +12V fan located on J15 of the FPGA board is intended to reduce the temperature of the FPGA. Users can control the fan to turn on/off depending on the measured system temperature. The FAN is turned on when the FAN_CTRL pin is driven to a high logic level.

The pin assignments for the associated interface are listed in Table 2-7.

Table 2-7 Temperature Sensor Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	*Description*	*I/O Standard*	*Stratix V GX Pin Number*
TEMPDIODEp	Positive pin of temperature diode in Stratix V	1.8-V	PIN_P6
TEMPDIODEn	Negative pin of temperature diode in Stratix V	1.8-V	PIN_P7
TEMP_CLK	SMBus clock	2.5-V	PIN_D21
TEMP_DATAT	SMBus data	2.5-V	PIN_D20
TEMP_OVERT_n	SMBus alert (interrupt)	2.5-V	PIN_C22
TEMP_INT_n	SMBus alert (interrupt)	2.5-V	PIN_C21
FAN_CTRL	Fan control	2.5-V	PIN_AR32

2.5 Clock Circuit

The development board includes one 50 MHz and three programmable oscillators. **Figure 2-9** shows the default frequencies of on-board all external clocks going to the Stratix V GX FPGA. The figures also show an off-board external clock from PCI Express Host to the FPGA.

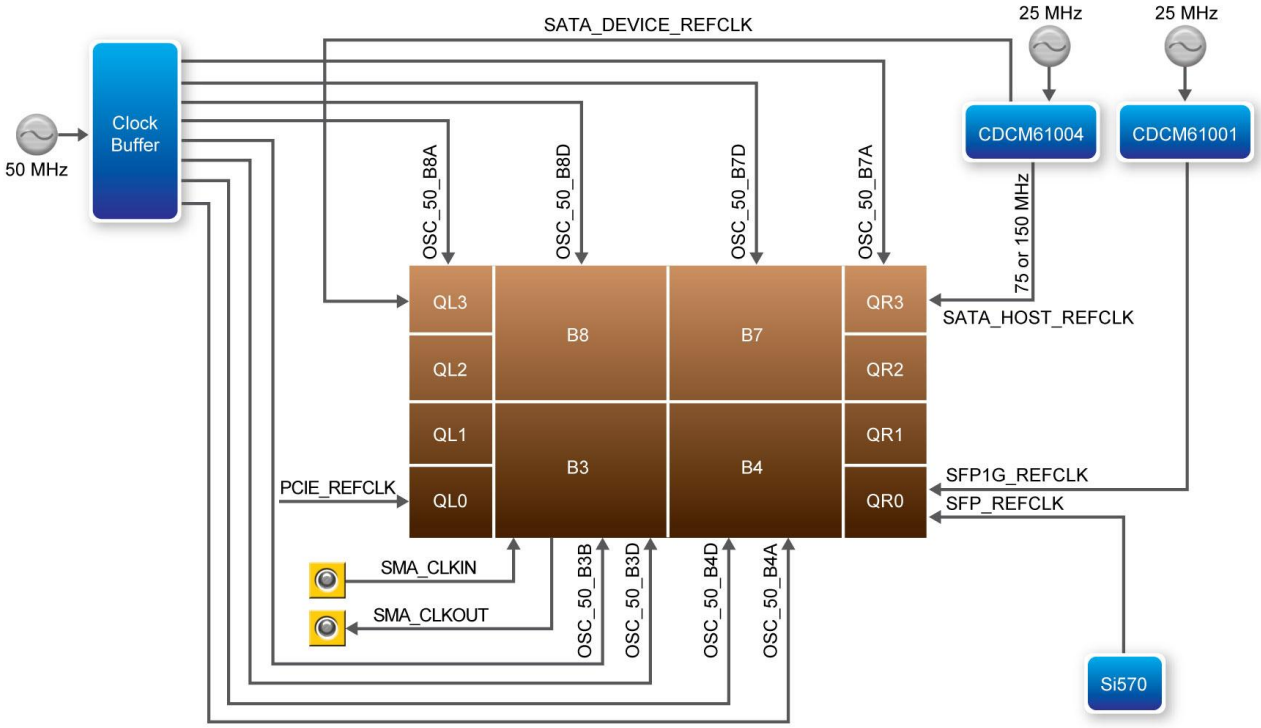


Figure 2-9 Clock circuit of the FPGA Board

A clock buffer is used to duplicate the 50 MHz oscillator, so each bank of FPGA I/O bank 3/4/7/8 has two clock inputs. The three programming oscillators are low-jitter oscillators which are used to provide special and high quality clock signals for high-speed transceivers. **Figure 2-10** shows the control circuits of programmable oscillators. The clock generator controller in the MAX II CPLD can be used to program the CDCM61001 and CDCM61004 to generate 1G Ethernet SFP+ and SATA reference clocks respectively. The Si570 programmable clock generator is programmed via an I2C serial interface to generate the 10G Ethernet SFP+ reference clock. Two SMA connectors provide external clock input and clock output respectively.

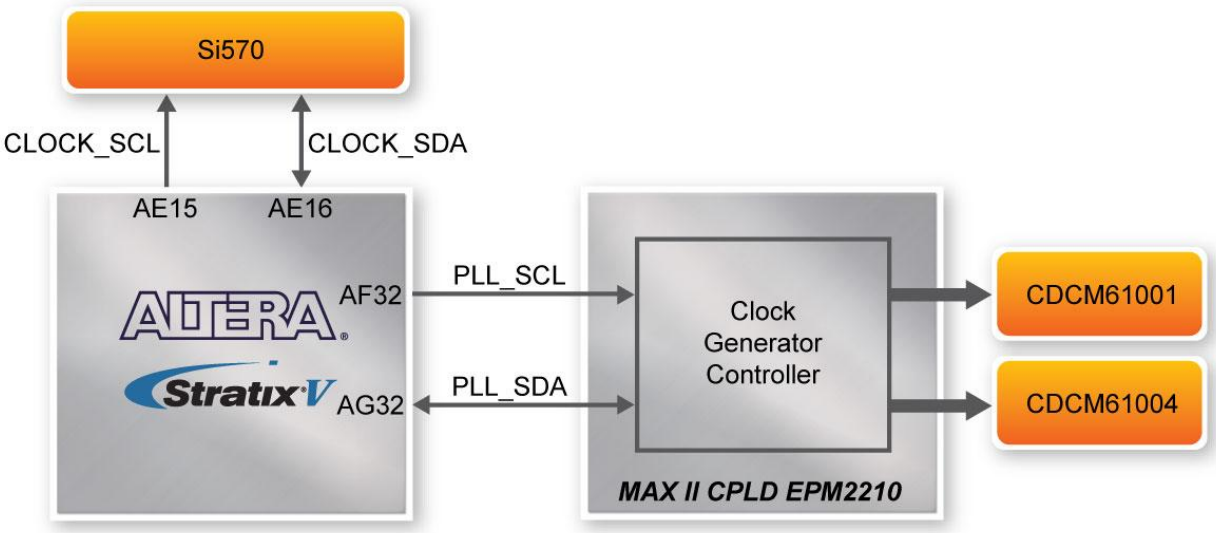


Figure 2-10 Control circuits of Programmable Oscillators

Table 2-8 lists the clock source, signal names, default frequency and their corresponding Stratix V GX device pin numbers.

Table 2-8 Clock Source, Signal Name, Default Frequency, Pin Assignments and Functions

Source	*Schematic Signal Name*	*Default Frequency*	*I/O Standard*	*Stratix V GX Pin Number*	*Application*
Y4	OSC_50_B3B	50.0 MHz	2.5-V	PIN_AW35	
	OSC_50_B3D		1.8-V	PIN_BC28	
	OSC_50_B4A		1.8-V	PIN_AP10	
	OSC_50_B4D		1.8-V	PIN_AY18	
	OSC_50_B7A		1.5-V	PIN_M8	
	OSC_50_B7D		1.5-V	PIN_J18	
	OSC_50_B8A		1.5-V	PIN_R36	
	OSC_50_B8D		1.8-V	PIN_R25	
J13	SMA_CLKIN	User Defined	2.5V	PIN_BB33	External Clock Input
J14	SMA_CLKOUT	User Defined	2.5V	PIN_AV34	Clock Output
U49	SFP_REFCLK _p	100.0 MHz	LVDS	PIN_AK7	10G SFP+
U53	SFP1G_REFCLK_p	125.0 MHz	LVDS	PIN_AH6	1G SFP+
U28	SATA_HOST_REFCLK_p	125.0 MHz	LVDS	PIN_V6	SATA HOST
U28	SATA_DEVICE_REFCLK_p	125.0 MHz	LVDS	PIN_V39	SATA DEVICE

J17	PCIE_REFCLK_p	From Host	LVDS	PIN_AK38	PCI Express

Table 2-9 lists the programmable oscillator control pins, signal names, I/O standard and their corresponding Stratix V GX device pin numbers.

Table 2-9 Programmable oscillator control pin, Signal Name, I/O standard, Pin Assignments and Descriptions

Programmable Oscillator	*Schematic Signal Name*	*I/O Standard*	*Stratix V GX Pin Number*	*Description*
Si570 (U49)	CLOCK_SCL	2.5-V	PIN_AE15	I2C bus, direct connected with Si570
	CLOCK_SDA	2.5-V	PIN_AE16	
CDCM61001 (U53)	PLL_SCL	2.5-V	PIN_AF32	I2C bus, connected with MAX II CPLD
	PLL_SDA	2.5-V	PIN_AG32	
CDCM61004 (U28)	PLL_SCL	2.5-V	PIN_AF32	I2C bus, connected with MAX II CPLD
	PLL_SDA	2.5-V	PIN_AG32	

2.6 RS-422 Serial Port

The RS-422 is designed to perform communication between boards, allowing a transmission speed of up to 20 Mbps. Figure 2-11 shows the RS-422 block diagram of the development board. The full-duplex LTC2855 is used to translate the RS-422 signal, and the RJ45 is used as an external connector for the RS-422 signal.

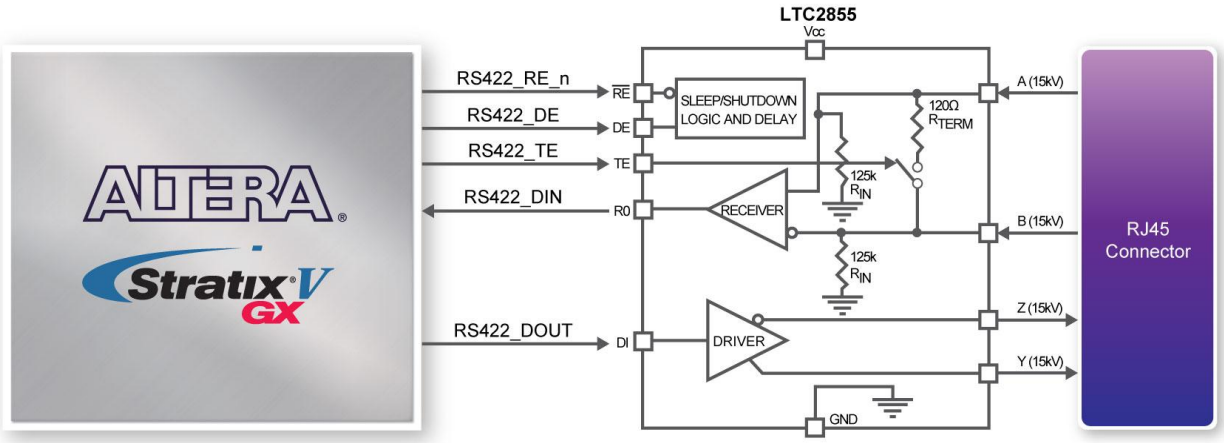


Figure 2-11 Block Diagram of RS-422

Table 2-10 lists the RS-422 pin assignments, signal names and functions.

Table 2-10 RS-422 Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	*Description*	*I/O Standard*	*Stratix V GX Pin Number*
RS422_DE	Driver Enable. A high on DE enables the driver. A low input will force the driver outputs into a high impedance state.	2.5-V	PIN_AG14
RS422_DIN	Receiver Output. The data is send to FPGA.		PIN_AE18
RS422_DOUT	Driver Input. The data is sent from FPGA.		PIN_AE17
RS422_RE_n	Receiver Enable. A low enables the receiver. A high input forces the receiver output into a high impedance state.		PIN_AF17
RS422_TE	Internal Termination Resistance Enable. A high input will connect a termination resistor (120Ω typical) between pins A and B.		PIN_AF16

2.7 FLASH Memory

The development board has two 1Gb CFI-compatible synchronous flash devices for non-volatile

storage of FPGA configuration data, user application data, and user code space.

Each interface has a 16-bit data bus and the two devices combined allow for FPP x32 configuration. This device is part of the shared flash and MAX (FM) bus, which connects to the flash memory and MAX II CPLD (EPM2210) System Controller. Figure 2-12 shows the connections between the Flash, MAX and Stratix V GX FPGA.

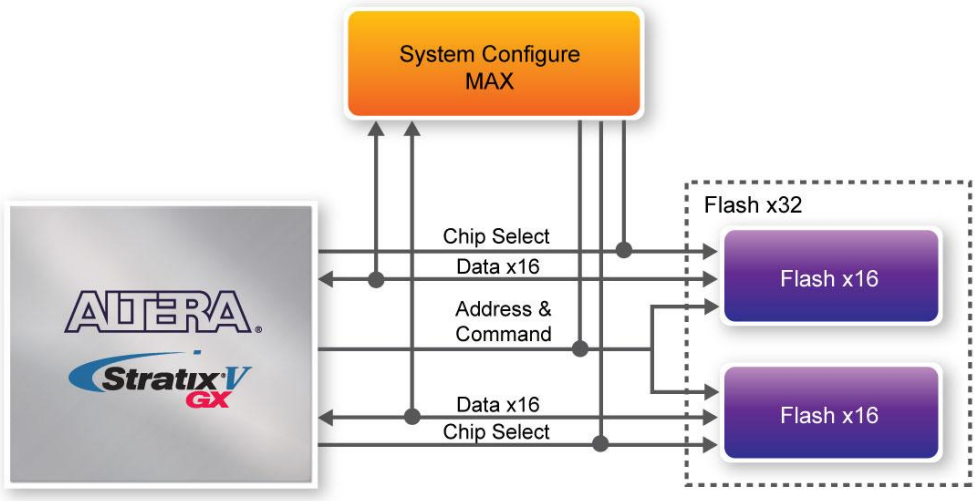


Figure 2-12 Connection between the Flash, Max and Stratix V GX FPGA

Table 2-11 lists the flash pin assignments, signal names, and functions.

Table 2-11 Flash Memory Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	*Description*	*I/O Standard*	*Stratix V GX Pin Number*
FSM_A0	Address bus	2.5-V	PIN_AU32
FSM_A1	Address bus	2.5-V	PIN_AH30
FSM_A2	Address bus	2.5-V	PIN_AJ30
FSM_A3	Address bus	2.5-V	PIN_AH31
FSM_A4	Address bus	2.5-V	PIN_AK30
FSM_A5	Address bus	2.5-V	PIN_AJ32
FSM_A6	Address bus	2.5-V	PIN_AG33
FSM_A7	Address bus	2.5-V	PIN_AL30
FSM_A8	Address bus	2.5-V	PIN_AK33
FSM_A9	Address bus	2.5-V	PIN_AJ33
FSM_A10	Address bus	2.5-V	PIN_AN30
FSM_A11	Address bus	2.5-V	PIN_AH33

FSM_A12	Address bus	2.5-V	PIN_AK32
FSM_A13	Address bus	2.5-V	PIN_AM32
FSM_A14	Address bus	2.5-V	PIN_AM31
FSM_A15	Address bus	2.5-V	PIN_AL31
FSM_A16	Address bus	2.5-V	PIN_AN33
FSM_A17	Address bus	2.5-V	PIN_AP33
FSM_A18	Address bus	2.5-V	PIN_AT32
FSM_A19	Address bus	2.5-V	PIN_AT29
FSM_A20	Address bus	2.5-V	PIN_AP31
FSM_A21	Address bus	2.5-V	PIN_AR30
FSM_A22	Address bus	2.5-V	PIN_AU30
FSM_A23	Address bus	2.5-V	PIN_AJ31
FSM_A24	Address bus	2.5-V	PIN_AP30
FSM_A25	Address bus	2.5-V	PIN_AN31
FSM_A26	Address bus	2.5-V	PIN_AT30
FSM_D0	Data bus	2.5-V	PIN_AG26
FSM_D1	Data bus	2.5-V	PIN_AD33
FSM_D2	Data bus	2.5-V	PIN_AE34
FSM_D3	Data bus	2.5-V	PIN_AF31
FSM_D4	Data bus	2.5-V	PIN_AG28
FSM_D5	Data bus	2.5-V	PIN_AG30
FSM_D6	Data bus	2.5-V	PIN_AF29
FSM_D7	Data bus	2.5-V	PIN_AE29
FSM_D8	Data bus	2.5-V	PIN_AG25
FSM_D9	Data bus	2.5-V	PIN_AF34
FSM_D10	Data bus	2.5-V	PIN_AE33
FSM_D11	Data bus	2.5-V	PIN_AE31
FSM_D12	Data bus	2.5-V	PIN_AF28
FSM_D13	Data bus	2.5-V	PIN_AE30
FSM_D14	Data bus	2.5-V	PIN_AG29
FSM_D15	Data bus	2.5-V	PIN_AG27
FSM_D16	Data bus	2.5-V	PIN_AP28
FSM_D17	Data bus	2.5-V	PIN_AN28
FSM_D18	Data bus	2.5-V	PIN_AU31
FSM_D19	Data bus	2.5-V	PIN_AW32
FSM_D20	Data bus	2.5-V	PIN_BD32
FSM_D21	Data bus	2.5-V	PIN_AY31
FSM_D22	Data bus	2.5-V	PIN_BA30
FSM_D23	Data bus	2.5-V	PIN_BB30
FSM_D24	Data bus	2.5-V	PIN_AM29
FSM_D25	Data bus	2.5-V	PIN_AR29

FSM_D26	Data bus	2.5-V	PIN_AV31
FSM_D27	Data bus	2.5-V	PIN_AV32
FSM_D28	Data bus	2.5-V	PIN_BC31
FSM_D29	Data bus	2.5-V	PIN_AW30
FSM_D30	Data bus	2.5-V	PIN_BC32
FSM_D31	Data bus	2.5-V	PIN_BD31
FLASH_CLK	Clock	2.5-V	PIN_AL29
FLASH_RESET_n	Reset	2.5-V	PIN_AE28
FLASH_CE_n[0]	Chip enable of of flash-0	2.5-V	PIN_AE27
FLASH_CE_n[1]	Chip enable of of flash-1	2.5-V	PIN_BA31
FLASH_OE_n	Output enable	2.5-V	PIN_AY30
FLASH_WE_n	Write enable	2.5-V	PIN_AR31
FLASH_ADV_n	Address valid	2.5-V	PIN_AK29
FLASH_RDY_BSY_n[0]	Ready of flash-0	2.5-V	PIN_BA29
FLASH_RDY_BSY_n[1]	Ready of flash-1	2.5-V	PIN_BB32

2.8 DDR3 SO-DIMM

The development board supports two independent banks of DDR3 SDRAM SO-DIMM. Each DDR3 SODIMM socket is wired to support a maximum capacity of 8GB with a 64-bit data bus. Using differential DQS signaling for the DDR3 SDRAM interfaces, it is capable of running at up to 800MHz memory clock for a maximum theoretical bandwidth up to 95.4Gbps. **Figure 2-13** shows the connections between the DDR3 SDRAM SO-DIMMs and Stratix V GX FPGA.