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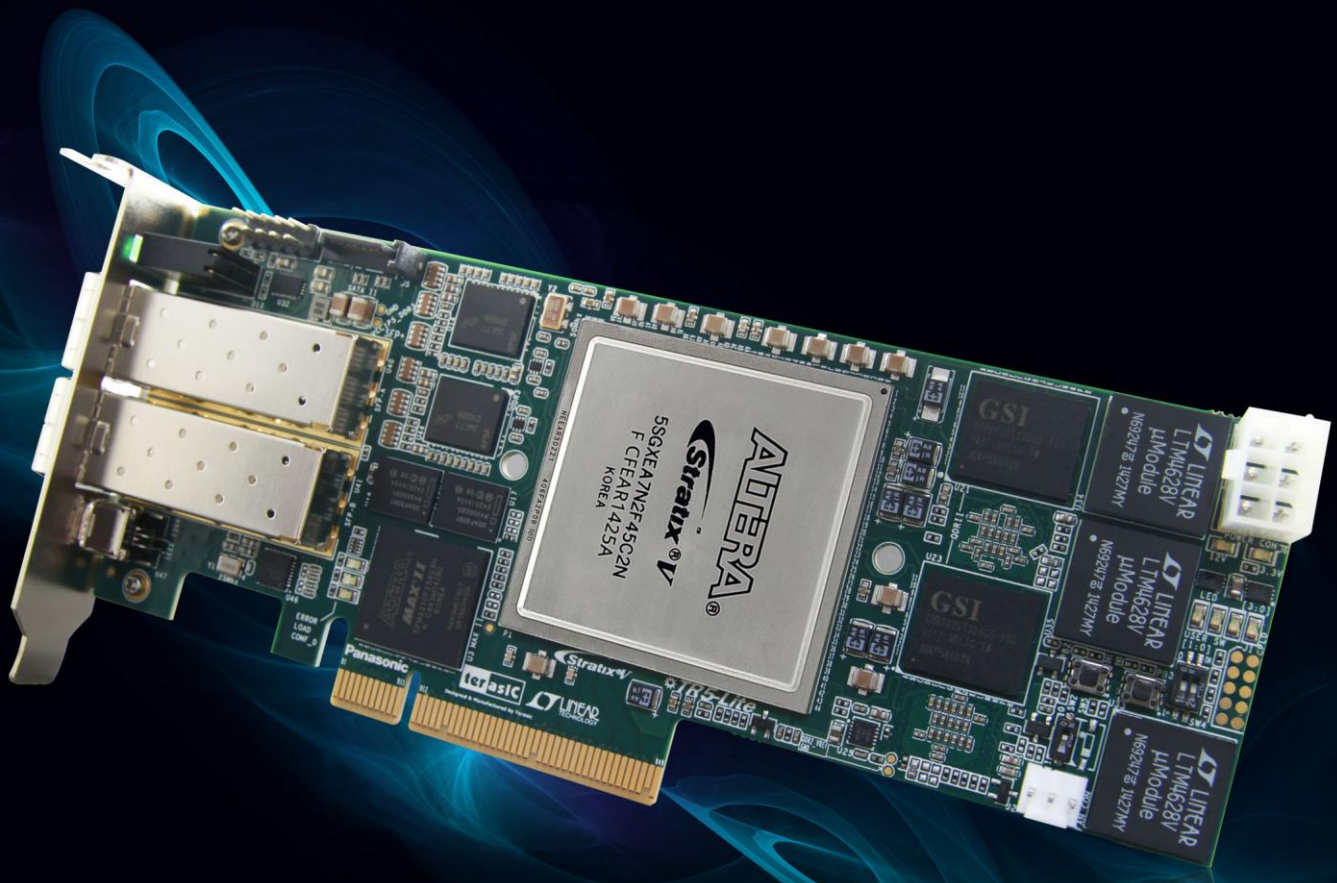
TR5-Lite

FPGA Development Kit

User Manual



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Chapter 1

Overview

This chapter provides an overview of the TR5-Lite Development Board and installation guide.

1.1 General Description

The Terasic TR5-Lite Stratix V GX FPGA Development Kit provides the ideal hardware solution for designs that demand high bandwidth, advanced memory interfacing, and power efficiency in a convenient half-height, half-length form-factor package. Designed for the most demanding high-end applications, the TR5-Lite is empowered with the top-of-the-line Altera Stratix V GX, delivering the best system-level integration and flexibility in the industry.

The Stratix® V GX FPGA features integrated transceivers that transfer at a maximum of 12.5 Gbps, allowing the TR5-Lite to be fully compliant with version 3.0 of the PCI Express standard, as well as allowing an ultra low-latency, straight connections to dual external 10G SFP+ modules. Not relying on an external PHY will accelerate mainstream development of network applications enabling customers to deploy designs for a broad range of high-speed connectivity applications. Matched with two independent banks of DDR3 RAM, four independent banks of QDRII, and flash memory, the TR5-Lite fully delivers in all high-bandwidth applications such as high frequency trading, data acquisition, network processing, and signal processing.

It is highly recommended that users read the *TR5-Lite Getting Started Guide.pdf* before using the TR5-Lite board.

1.2 Key Features

The following hardware is implemented on the TR5-Lite board:

- FPGA
  - Altera Stratix® V GX FPGA (5SGXEA7N2F45C2)

- FPGA Configuration
  - JTAG header for FPGA programming
  - Fast passive parallel (FPPx32) configuration via MAX II CPLD and flash memory

- General user input/output:
  - 4 LEDs
  - 2 push-buttons
  - 2-position DIP switch

- On-Board Clock
  - 50MHz Oscillator
  - Programmable oscillators Si570 and CDCM61004

- Memory
  - DDR3 SDRAM
  - QDRII+ SRAM
  - FLASH

- Communication Ports
  - Two SFP+ connectors
  - One Serial ATA (SATA II) host port
  - PCI Express (PCIe) x8 edge connector
  - One RS422 transevier with 1394 connector

- System Monitor and Control
  - Temperature sensor
  - Fan control

- Power
  - PCI Express 6-pin power connector, 12V DC Input
  - PCI Express edge connector power

- Mechanical Specification
  - PCI Express half-height and half-length

1.3 Block Diagram

Figure 1-1 shows the block diagram of the TR5-Lite board. To provide maximum flexibility for the users, all key components are connected with the Stratix V GX FPGA device. Thus, users can configure the FPGA to implement any system design.

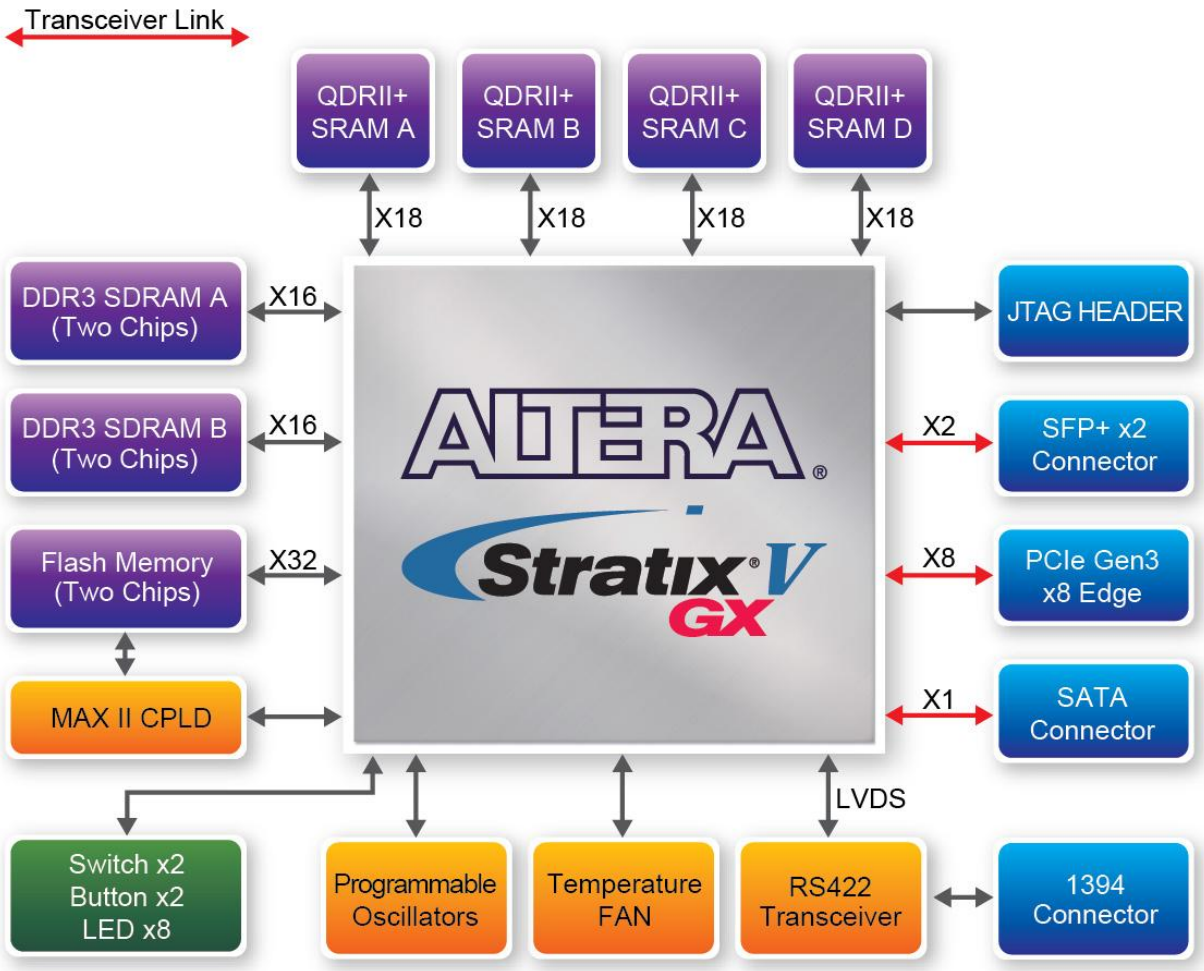

Figure 1-1 Block diagram of the TR5-Lite board

Below is more detailed information regarding the blocks in Figure 1-1.

Stratix V GX FPGA

- 5SGXEA7N2F45C2
- 622,000 logic elements (LEs)
- 50-Mbits embedded memory
- 48 transceivers (12.5Gbps)
- 512 18-bit x 18-bit multipliers
- 256 27-bit x 27-bit DSP blocks
- 2 PCI Express hard IP blocks
- 840 user I/Os
- 210 full-duplex LVDS channels
- 28 phase locked loops (PLLs)

JTAG Header and FPGA Configuration

- On-board JTAG header for use with the Quartus II Programmer
- MAXII CPLD EPM2210 System Controller and Fast Passive Parallel (FPP) configuration

Memory devices

- 32MB QDRII+ SRAM
- 2GB DDR3 SDRAM
- 256MB FLASH

General user I/O

- 4 user controllable LEDs
- 2 user push buttons
- 2 user DIP switches

On-Board Clock

- 50MHz oscillator
- Programming PLL providing clock for 10G SFP+ transceiver
- Programming PLL providing clock for SATA or 1G SFP+ transceiver

One Serial ATA ports

- SATA 3.0 standard 6Gbps signaling rate

Two SFP+ ports

- Two SFP+ connector (10 Gbps+)

PCI Express x8 edge connector

- Support PCIe Gen1/2/3
- Connection established with PC motherboard with x8 or x16 PCI Express slot

Power Source

- PCI Express 6-pin DC 12V power
- PCI Express edge connector power

1.4 Installation Setup

The TR5-Lite board can be functional standalone or installed on a host PC. External USB-Blaster is required to configure the board through the on-board JTAG Header.

Switch Setup

The MSEL[0:4] switches should be in the ON position(MSEL[0:4]=00010), as shown in **Figure 1-2.**

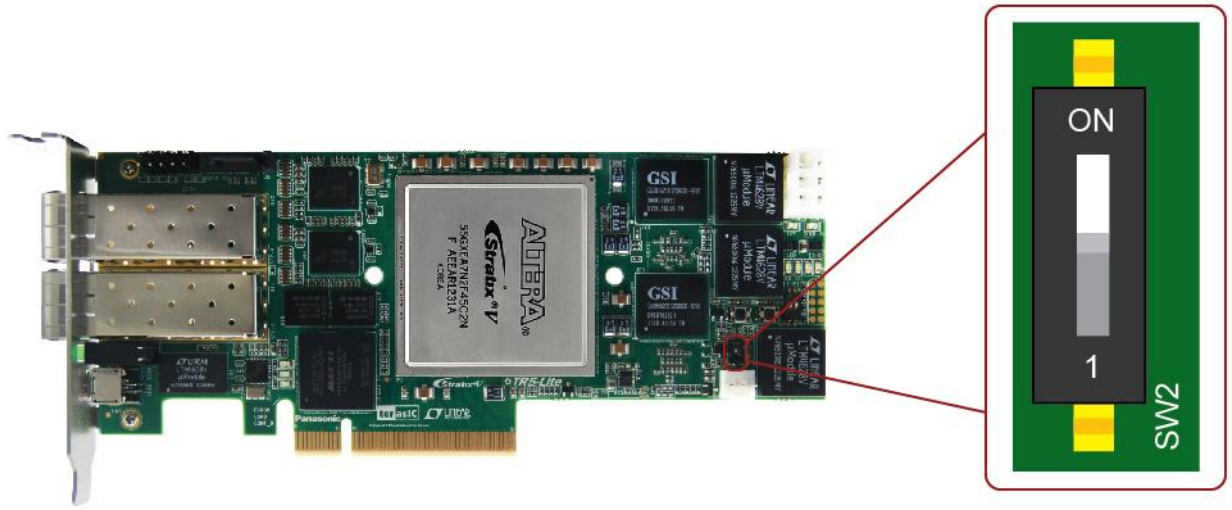

Figure 1-2 MSEL Default Configuration

SW1 is set to low for loading the default factory FPGA configuration. For more details, please see **Figure 1-3**.

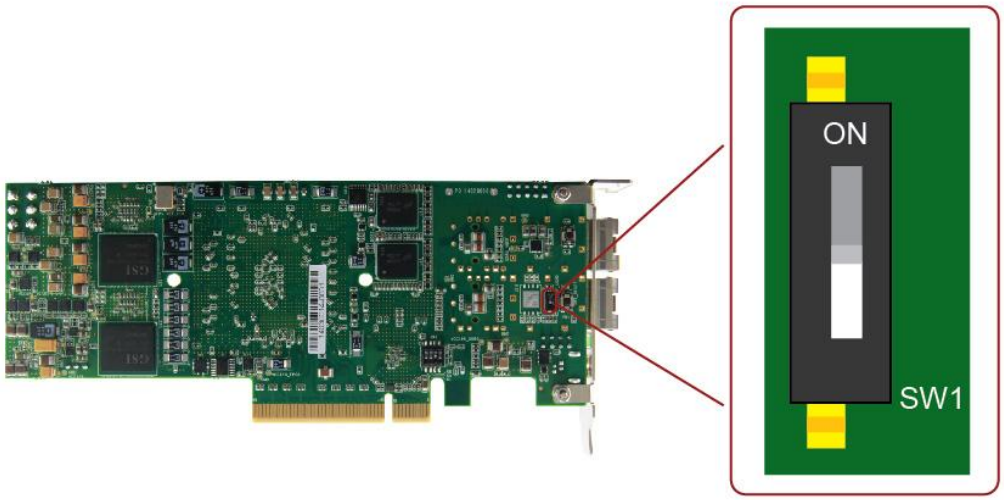

Figure 1-3 Factory Default Configuration Setting

USB-Blaster Setup

An external USB-Blaster (or USB-Blaster II) is required to configure the TR5-Lite board. **Figure 1-4** shows how connect Terasic USB-Blaster II to the JTAG header (J3) on the TR5-Lite. Terasic USB-Blaster II is recommended because it provides a faster downloading speed than the traditional USB-Blaster. Please note the red edge in the flat cable should be connected to the first pin in JTAG header.

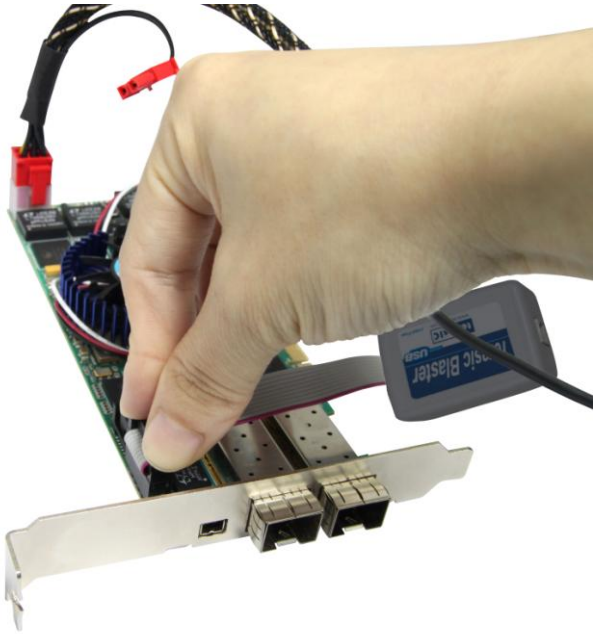

Figure 1-4 Connect the Terasic USB-Blaster II to the JTAG header (J3)

Power Setup

The TR5-Lite power is provided from both the 6-pin DC 12V power connector and PCI Express edge connector. In standalone-mode, only the 6-pin DC 12V power input is required. **Figure 1-5** shows the installation of connecting PCIe 12V DC power source to the 6-pin PCIe power connector on the TR5-Lite board.

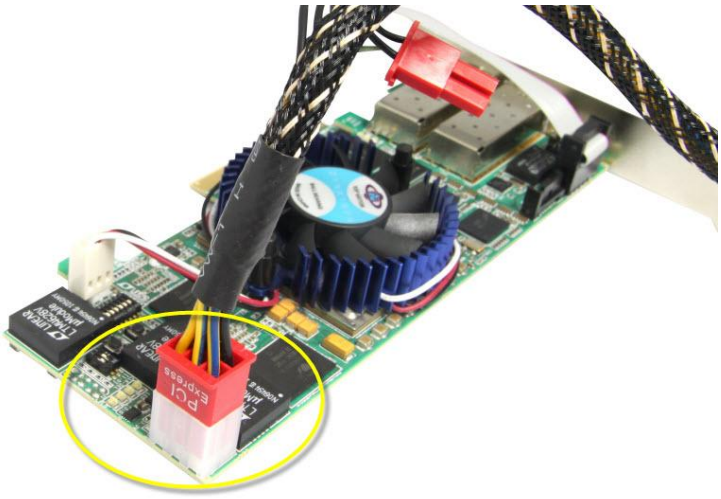

Figure 1-5 Installation of 12V DC for TR5-Lite through the 6-Pin PCIe Power Connector

When TR5-Lite is installed on a PC, the 6-pin DC 12 V power input also is **required** even if there is a power provided through the PCI Express edge connector, as shown in **Figure 1-6**. The 12V DC input can come from the PC power supply if it supports 6-pin PCIe power source. Without the 12V DC power from the 6-pin power connector, the TR5-Lite may be damaged due to insufficient power from the PCIe edge connector when many FPGA resources are used.

Figure 1-6 TR5-Lite Installed on PC

Quartus II Setup

64-bit Quartus 11.1 SP1 or later is strongly recommended. When compiling with Stratix V FPGA with 32-bit Quartus, an out of memory error may occur due to the memory limitation of operating system on the host computer.

The Quartus II golden top project for TR5-Lite is available on the TR5-Lite System CD location **Demonstrations/TR5_Lite_Golden_Top**. The project includes complete pin assignments, so users can develop their projects based on this golden top project regardless of the assignment details.

Chapter 2

Board Components

This chapter introduces all the important components on the TR5-Lite.

2.1 Board Overview

Figure 2-1 and Figure 2-2 is the top and bottom view of the TR5-Lite development board. It depicts the layout of the board and indicates the location of the connectors and key components. Users can refer to this figure for relative location of the connectors and key components.

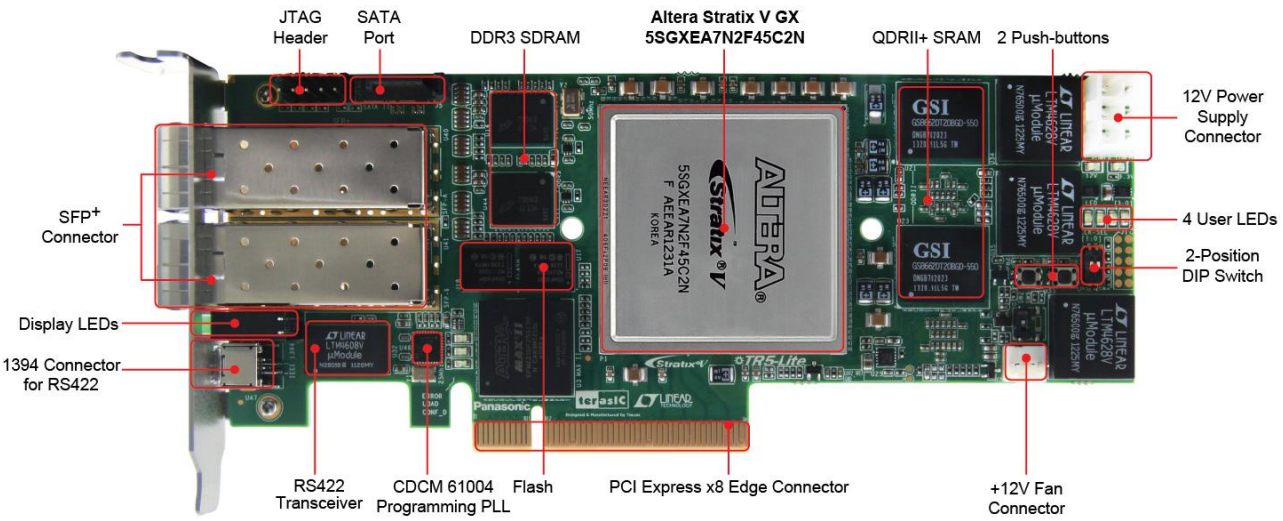

Figure 2-1 The TR5-Lite Board (Top)

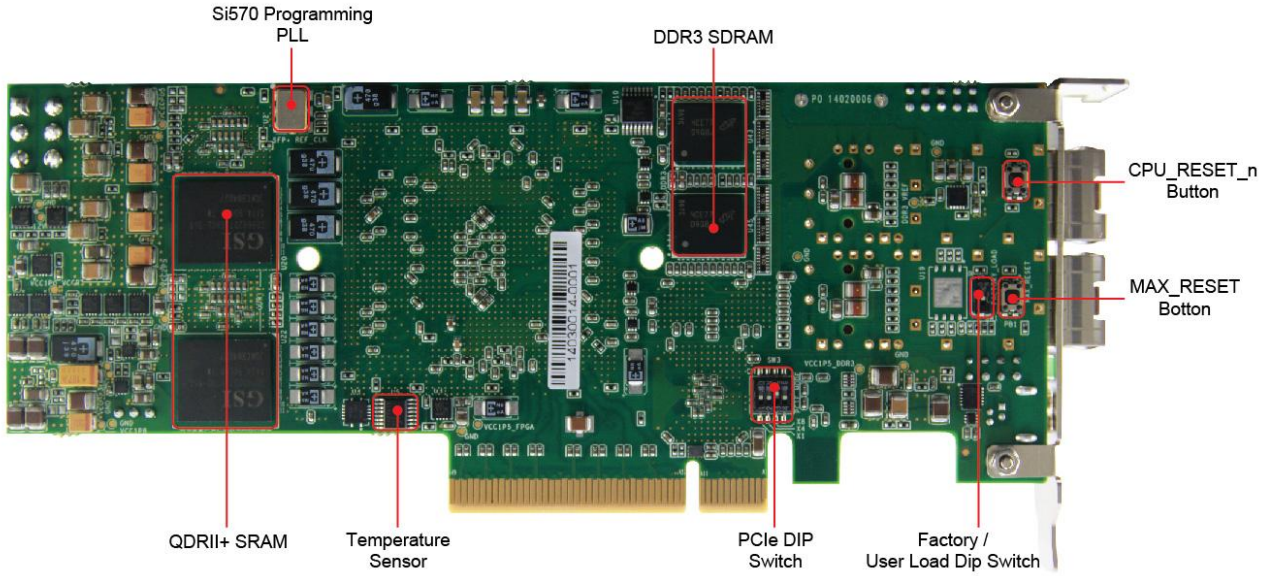

Figure 2-2 The TR5-Lite Board (Bottom)

2.2 Configuration, Status and Setup

■ Configure

The TR5-Lite board supports two configuration methods for the Stratix V FPGA:

- External USB-Blaster for configuring the FPGA using the external USB-Blaster.
- Flash memory configuration of the FPGA using stored images from the flash memory on power-up.

For programming by USB-Blaster, the USB-Blaster should connect to the JTAG header (J3) on the TR5-Lite board. The following procedures show how to download a configuration bit stream into the Stratix V GX FPGA:

- Make sure that power is provided to the TR5-Lite board
- Connect your PC to the TR5-Lite board using a USB-Blaster (or USB-Blaster II) module and make sure the USB-Blaster driver is installed on PC.
- Launch Quartus II programmer and make sure the USB-Blaster (or USB-Blaster II) is detected.
- In Quartus II Programmer, add the configuration bit stream file (.sof), check the associated "Program/Configure" item, and click "Start" to start FPGA programming.

■ Status LED

The TR5-Lite development board includes board-specific status LEDs to indicate board status. Please refer to Table 2-1 for the description of the LED indicator.

Table 2-1 Status LED

Board Reference	*LED Name*	*Description*
D12	12-V Power	Illuminates when 12-V power is active.
D11	3.3-V Power	Illuminates when 3.3-V power is active.
D1	CONF DONE	Illuminates when the FPGA is successfully configured. Driven by the MAX II CPLD EPM2210 System Controller.
D2	Loading	Illuminates when the MAX II CPLD EPM2210 System Controller is actively configuring the FPGA. Driven by the MAX II CPLD EPM2210 System Controller with the Embedded Blaster CPLD.
D3	Error	Illuminates when the MAX II CPLD EPM2210 System Controller fails to configure the FPGA. Driven by the MAX II CPLD EPM2210 System Controller.

■ Setup PCI Express Control DIP switch

The PCI Express Control DIP switch (SW3) is provided to enable or disable different configurations of the PCIe Connector. Table 2-2 lists the switch controls and description.

Table 2-2 SW3 PCIe Control DIP Switch

Board Reference	*Signal Name*	*Description*	*Default*
SW3.1	PCIE_PRSNT2n_x1	On : Enable x1 presence detect Off: Disable x1 presence detect	Off
SW3.2	PCIE_PRSNT2n_x4	On : Enable x4 presence detect Off: Disable x4 presence detect	Off
SW3.3	PCIE_PRSNT2n_x8	On : Enable x8 presence detect Off: Disable x8 presence detect	On

■ Setup Configure Mode Control DIP switch

The Configure Mode Control DIP switch (SW2) is provided to specify the configuration mode of the FPGA. Because currently only one mode is supported, please set all positions to OFF as shown in Figure 2-3.

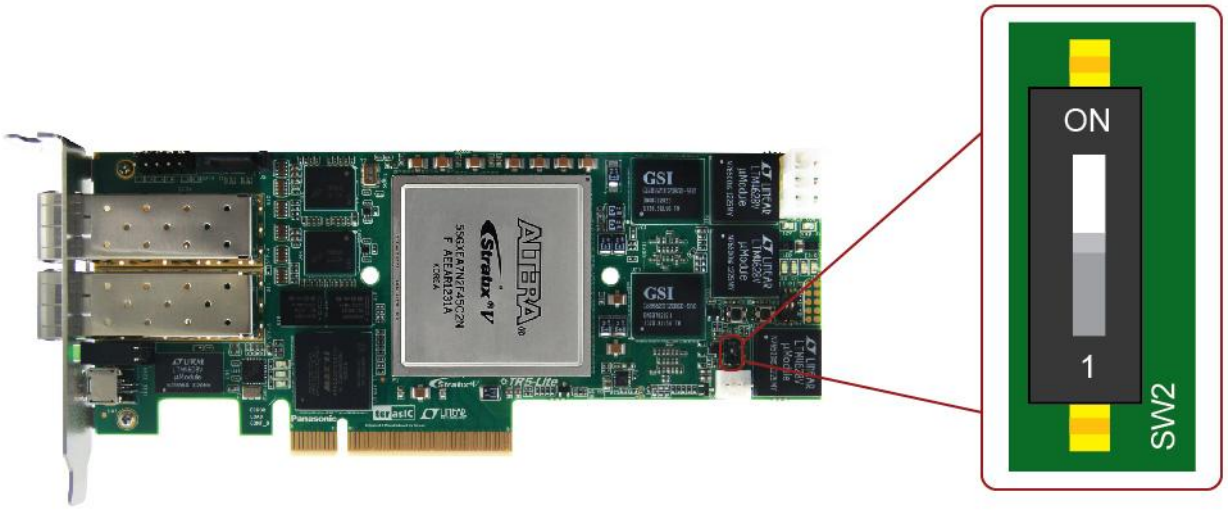

Figure 2-3 6-Position DIP switch for Configure Mode

■ Selecting Default Factory FPGA Configuration or User-defined Configuration

Users can select loading from default factory hardware or user-defined hardware through the use of SW1. The settings for the configurations are shown in Table 2-3.

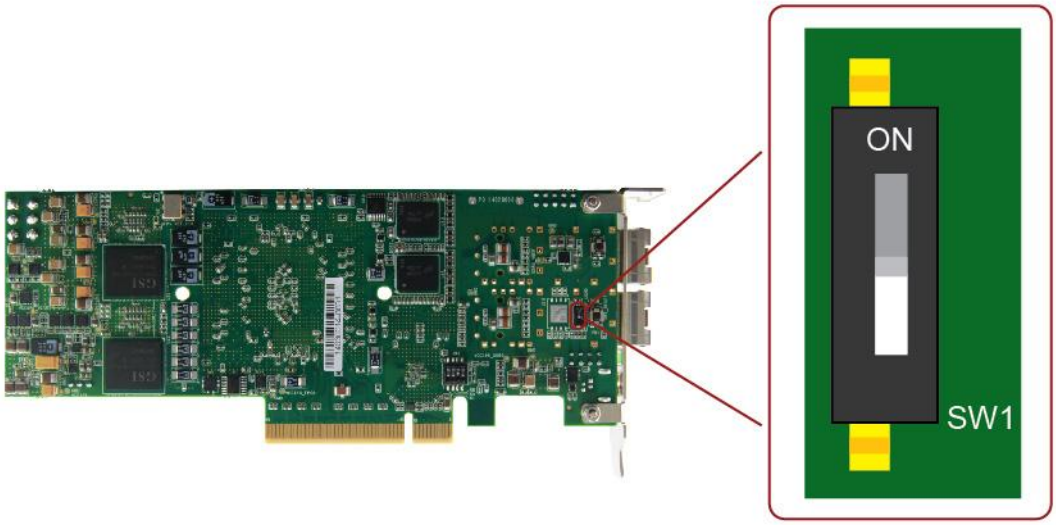

Figure 2-4 Position Dip Switch for FPGA Configuration

Table 2-3 SW1 FPGA Configuration Settings

Board Reference	*Description*	*Default*
SW1	On : User-defined Configuration Off: Factory Default Configuration	Off

2.3 General User Input/Output

This section describes the user I/O interface to the FPGA.

■ User Defined Push-buttons

The TR5-Lite board includes two user defined push-buttons that allow users to interact with the Stratix V GX device. Each push-button provides a high logic level or a low logic level when it is not pressed or pressed, respectively. Table 2-4 lists the board references, signal names and their corresponding Stratix V GX device pin numbers.

Table 2-4 Push-button Pin Assignments, Schematic Signal Names, and Functions

Board Reference	*Schematic Signal Name*	*Description*	*I/O Standard*	*Stratix V GX Pin Number*
PB2	BUTTON0	High Logic Level when the button is not pressed	2.5-V	PIN_A35
PB3	BUTTON1		2.5-V	PIN_A34

■ User-Defined DIP Switch

There is one 2-position DIP switch (SW4) on the TR5-Lite board to provide additional FPGA input control. Each switch is connected directly to a pin of the Stratix V GX FPGA. For 2-position DIP switch, when a switch is in the ON position, it provides a low logic level to the FPGA, as shown in Figure 2-5.

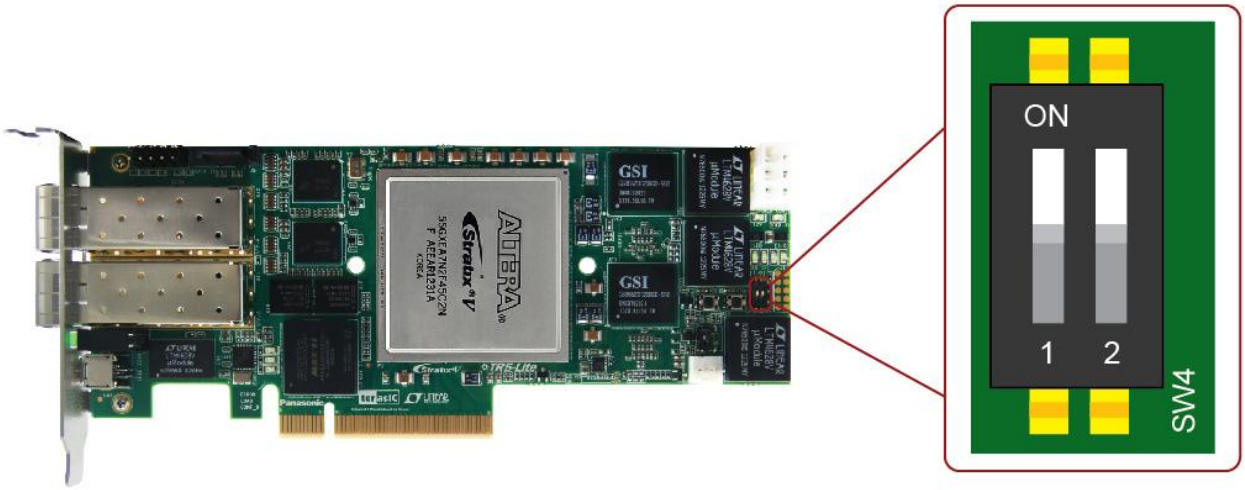

Figure 2-5 2-Position DIP switches

Table 2-5 lists the signal names and their corresponding Stratix V GX device pin numbers.

Table 2-5 DIP Switch Pin Assignments, Schematic Signal Names, and Functions

Board Reference	*Schematic Signal Name*	*Description*	*I/O Standard*	*Stratix IV GX Pin Number*
SW4	SLIDE_SW0	When the switch is in the ON position, a logic 0 is selected.	2.5-V	PIN_E33
SW4	SLIDE_SW1		2.5-V	PIN_D33

■ User-Defined LEDs

The TR5-Lite board consists of 4 user-controllable LEDs to allow status and debugging signals to be driven to the LEDs from the designs loaded into the Stratix V GX device. Each LED is driven directly by the Stratix V GX FPGA. The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin names on the FPGA that are connected to the LEDs is given in Table 2-6.

Table 2-6 User LEDs Pin Assignments, Schematic Signal Names, and Functions

Board Reference	*Schematic Signal Name*	*Description*	*I/O Standard*	*Stratix IV GX Pin Number*
D3	LED0	Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	2.5-V	PIN_C33
D4	LED1		2.5-V	PIN_B32
D5	LED2		2.5-V	PIN_C34
D6	LED3		2.5-V	PIN_B34

2.4 Temperature Sensor and Fan Control

The TR5-Lite is equipped with a temperature sensor, MAX1619, which provides temperature sensing and over-temperature alert. These functions are accomplished by connecting the temperature sensor to the internal temperature sensing diode of the Stratix V GX device. The temperature status and alarm threshold registers of the temperature sensor can be programmed by a two-wire SMBus, which is connected to the Stratix V GX FPGA. In addition, the 7-bit POR slave address for this sensor is set to '0011000b'.

An optional 3-pin +12V fan located on J2 of the TR5-Lite board is intended to reduce the temperature of the FPGA. Users can control the fan to turn on/off depending on the measured system temperature. The FAN is turned on when the FAN_CTRL pins are driven to a high logic level.

The pin assignments for the associated interface are listed in Table 2-7.

Table 2-7 Temperature Sensor Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	*Description*	*I/O Standard*	*Stratix IV GX Pin Number*
TEMPDIODEp	Positive pin of temperature diode in Stratix V	2.5-V	PIN_P6

TEMPDIODEn	Negative pin of temperature diode in Stratix V	2.5-V	PIN_EP7
TEMP_CLK	SMBus clock	2.5-V	PIN_F35
TEMP_DATAT	SMBus data	2.5-V	PIN_E35
TEMP_OVERT_n	SMBus alert (interrupt)	2.5-V	PIN_H35
TEMP_INT_n	SMBus alert (interrupt)	2.5-V	PIN_G34
FAN_CTRL	Fan control	2.5-V	PIN_F34

2.5 Clock Circuit

The development board includes one 50 MHz and two programmable oscillators. Figure 2-6 shows the default frequencies of on-board all external clocks going to the Stratix V GX FPGA. The figures also show an off-board external clock from PCI Express Host to the FPGA.

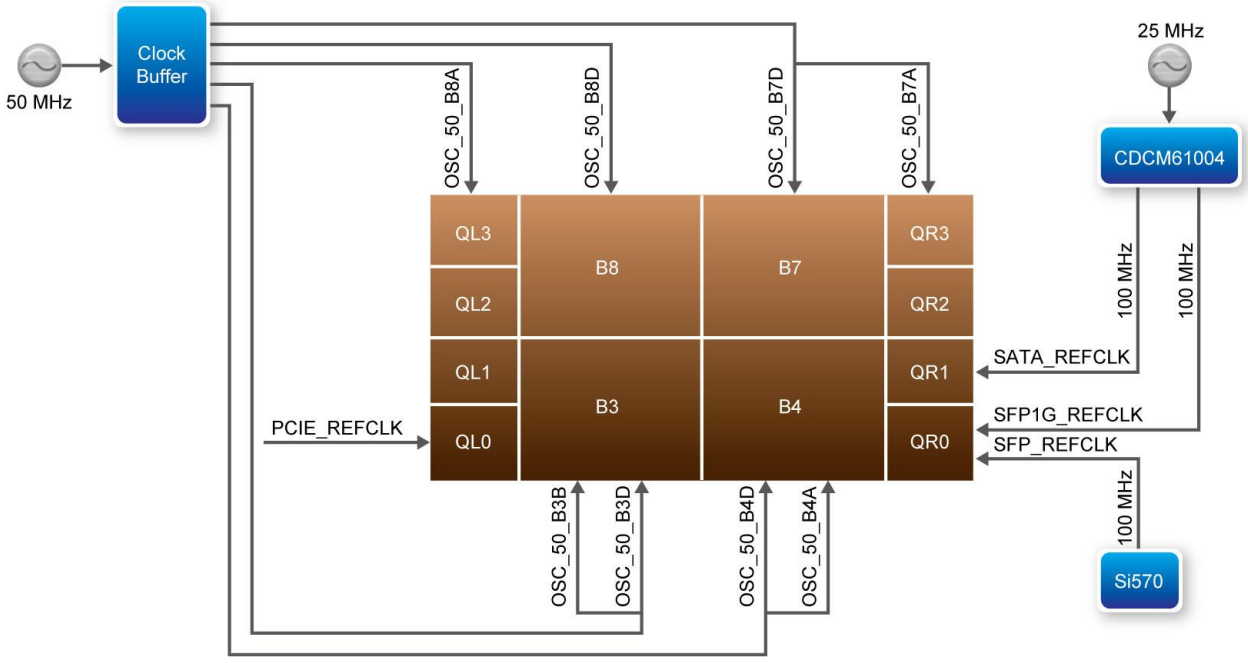

Figure 2-6 Clock circuit of the TR5-Lite

A clock buffer is used to duplicate the 50 MHz oscillator, so each bank of FPGA I/O bank 3/4/7/8 has two clock inputs. The two programming oscillators are low-jitter oscillators which are used to provide special and high quality clock signals for high-speed transceivers.

Table 2-8 lists the clock source, signal names, default frequency and their corresponding Stratix V GX device pin numbers.

Table 2-8 Clock Source, Signal Name, Default Frequency, Pin Assignments and Functions

Source	*Schematic Signal Name*	*Default Frequency*	*I/O Standard*	*Stratix V GX Pin Number*	*Application*
Y2	OSC_50_B3B	50.0 MHz	2.5-V	PIN_AW35	
	OSC_50_B3D		2.5-V	PIN_BC28	
	OSC_50_B4A		1.5-V	PIN_AP10	
	OSC_50_B4D		1.5-V	PIN_AY18	
	OSC_50_B7A		1.8-V	PIN_M9	
	OSC_50_B7D		1.8-V	PIN_J18	
	OSC_50_B8A		1.8-V	PIN_R36	
	OSC_50_B8D		1.8-V	PIN_R25	
U2	SFP_REFCLK _p	100.0 MHz	LVDS	PIN_AK7	10G SFP+
U46	SFP1G_REFCLK_p	100.0 MHz	LVDS	PIN_AH6	1G SFP+
U46	SATA_REFCLK_p	100.0 MHz	LVDS	PIN_AF7	SATA
J4	PCIE_REFCLK_p	From Host	LVDS	PIN_AK38	PCI Express

2.6 RS-422 Serial Port

The RS422 is designed to perform communication between boards, allowing a transmission speed of up to 20 Mbps. Figure 2-7 shows the RS-422 block diagram of the development board. The full-duplex LTC28255 is used to translate the RS-422 signal, and the 1394 is used as an external connector for the RS-422 signal.

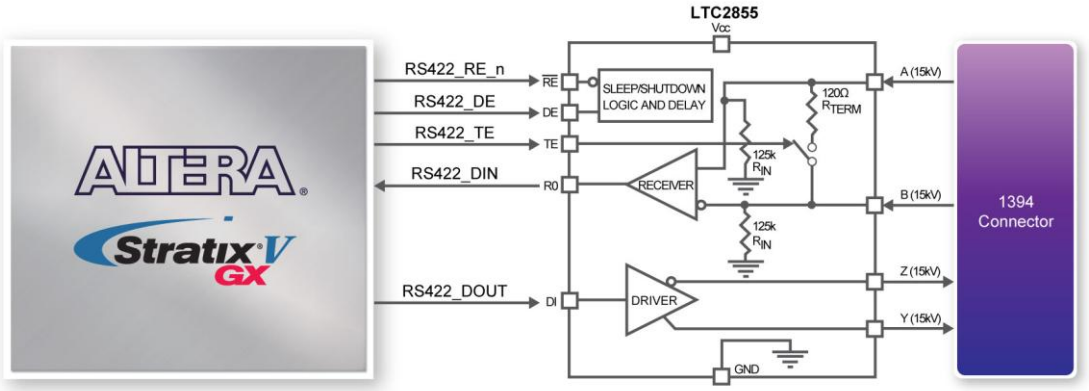

Figure 2-7 Block Diagram of RS-422

Table 2-9 lists the RS-422 pin assignments, signal names and functions.

Table 2-9 RS-422 Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	*Description*	*I/O Standard*	*Stratix V GX Pin Number*
RS422_DE	Driver Enable. A high on DE enables the driver. A low input will force the driver outputs into a high impedance state.	2.5-V	PIN_AU23
RS422_DIN	Receiver Output. The data is send to FPGA.		PIN_AR24
RS422_DOUT	Driver Input. The data is sent from FPGA.		PIN_AV23
RS422_RE_n	Receiver Enable. A low enables the receiver. A high input forces the receiver output into a high impedance state.		PIN_AL24
RS422_TE	Internal Termination Resistance Enable. A high input will connect a termination resistor (120Ω typical) between pins A and B.		PIN_AL23

2.7 FLASH Memory

The development board has two 1Gb CFI-compatible synchronous flash devices for non-volatile

storage of FPGA configuration data, user application data, and user code space.

Each interface has a 16-bit data bus and the two devices combined allow for x32 FPP configuration. This device is part of the shared flash and MAX (FM) bus, which connects to the flash memory and MAX II CPLD (EPM2210) System Controller. **Figure 2-8** shows the connections between the Flash, MAX and Stratix V GX FPGA.

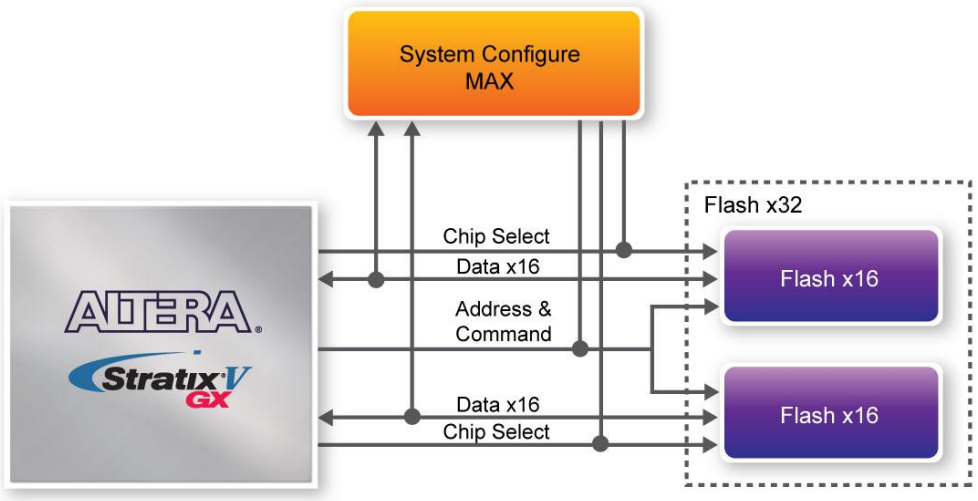

Figure 2-8 Connection between the Flash, Max and Stratix V GX FPG

Table 2-10 lists the flash pin assignments, signal names, and functions.

Table 2-10 Flash Memory Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	*Description*	*I/O Standard*	*Stratix IV GX Pin Number*
FSM_A0	Address bus	2.5-V	PIN_AG33
FSM_A1	Address bus	2.5-V	PIN_AN31
FSM_A2	Address bus	2.5-V	PIN_AP31
FSM_A3	Address bus	2.5-V	PIN_AH33
FSM_A4	Address bus	2.5-V	PIN_AG32
FSM_A5	Address bus	2.5-V	PIN_AF32
FSM_A6	Address bus	2.5-V	PIN_AV34
FSM_A7	Address bus	2.5-V	PIN_AM31
FSM_A8	Address bus	2.5-V	PIN_AP33
FSM_A9	Address bus	2.5-V	PIN_AF34
FSM_A10	Address bus	2.5-V	PIN_AR31

FSM_A11	Address bus	2.5-V	PIN_AE34
FSM_A12	Address bus	2.5-V	PIN_AW33
FSM_A13	Address bus	2.5-V	PIN_AN33
FSM_A14	Address bus	2.5-V	PIN_AJ32
FSM_A15	Address bus	2.5-V	PIN_AR32
FSM_A16	Address bus	2.5-V	PIN_AE30
FSM_A17	Address bus	2.5-V	PIN_AE29
FSM_A18	Address bus	2.5-V	PIN_AK32
FSM_A19	Address bus	2.5-V	PIN_AJ33
FSM_A20	Address bus	2.5-V	PIN_AE32
FSM_A21	Address bus	2.5-V	PIN_AE31
FSM_A22	Address bus	2.5-V	PIN_AK33
FSM_A23	Address bus	2.5-V	PIN_AD32
FSM_A24	Address bus	2.5-V	PIN_AD33
FSM_A25	Address bus	2.5-V	PIN_AM32
FSM_A26	Address bus	2.5-V	PIN_AF31
FSM_D0	Data bus	2.5-V	PIN_AF28
FSM_D1	Data bus	2.5-V	PIN_AG30
FSM_D2	Data bus	2.5-V	PIN_AG25
FSM_D3	Data bus	2.5-V	PIN_AK29
FSM_D4	Data bus	2.5-V	PIN_BA29
FSM_D5	Data bus	2.5-V	PIN_AG26
FSM_D6	Data bus	2.5-V	PIN_AG27
FSM_D7	Data bus	2.5-V	PIN_AE28
FSM_D8	Data bus	2.5-V	PIN_AG29
FSM_D9	Data bus	2.5-V	PIN_AK30
FSM_D10	Data bus	2.5-V	PIN_AG28
FSM_D11	Data bus	2.5-V	PIN_AF29
FSM_D12	Data bus	2.5-V	PIN_AJ29
FSM_D13	Data bus	2.5-V	PIN_AE27
FSM_D14	Data bus	2.5-V	PIN_AP28
FSM_D15	Data bus	2.5-V	PIN_BD31
FSM_D16	Data bus	2.5-V	PIN_BC31
FSM_D17	Data bus	2.5-V	PIN_BB32
FSM_D18	Data bus	2.5-V	PIN_BB30
FSM_D19	Data bus	2.5-V	PIN_BA31
FSM_D20	Data bus	2.5-V	PIN_AW30
FSM_D21	Data bus	2.5-V	PIN_BA30
FSM_D22	Data bus	2.5-V	PIN_AL29
FSM_D23	Data bus	2.5-V	PIN_AR29

FSM_D24	Data bus	2.5-V	PIN_BC32
FSM_D25	Data bus	2.5-V	PIN_AM29
FSM_D26	Data bus	2.5-V	PIN_BD32
FSM_D27	Data bus	2.5-V	PIN_AY30
FSM_D28	Data bus	2.5-V	PIN_AY31
FSM_D29	Data bus	2.5-V	PIN_AN28
FSM_D30	Data bus	2.5-V	PIN_AL30
FSM_D31	Data bus	2.5-V	PIN_AL31
FLASH_CLK	Clock	2.5-V	PIN_AU31
FLASH_RESET_n	Reset	2.5-V	PIN_AV31
FLASH_CE_n[0]	Chip enable of of flash-0	2.5-V	PIN_AJ31
FLASH_CE_n[1]	Chip enable of of flash-1	2.5-V	PIN_AW32
FLASH_OE_n	Output enable	2.5-V	PIN_AU30
FLASH_WE_n	Write enable	2.5-V	PIN_AH30
FLASH_ADV_n	Address valid	2.5-V	PIN_AT29
FLASH_RDY_BSY_n[0]	Ready of flash-0	2.5-V	PIN_AJ30
FLASH_RDY_BSY_n[0]	Ready of flash-1	2.5-V	PIN_AV32

2.8 DDR3 SDRAM

The development board supports two independent banks of DDR3 SDRAM which totals 2GB in memory. Each bank comprises of two x8 DDR3 devices. The DDR3 signals are connected to the vertical I/O banks on the bottom edge of the FPGA. The DDR3 devices shipped with this board are running at 667 MHz, for a total theoretical bandwidth of over 42.68 Gbps. **Figure 2-9** shows the connections between the DDR3 and Stratix V GX FPGA.