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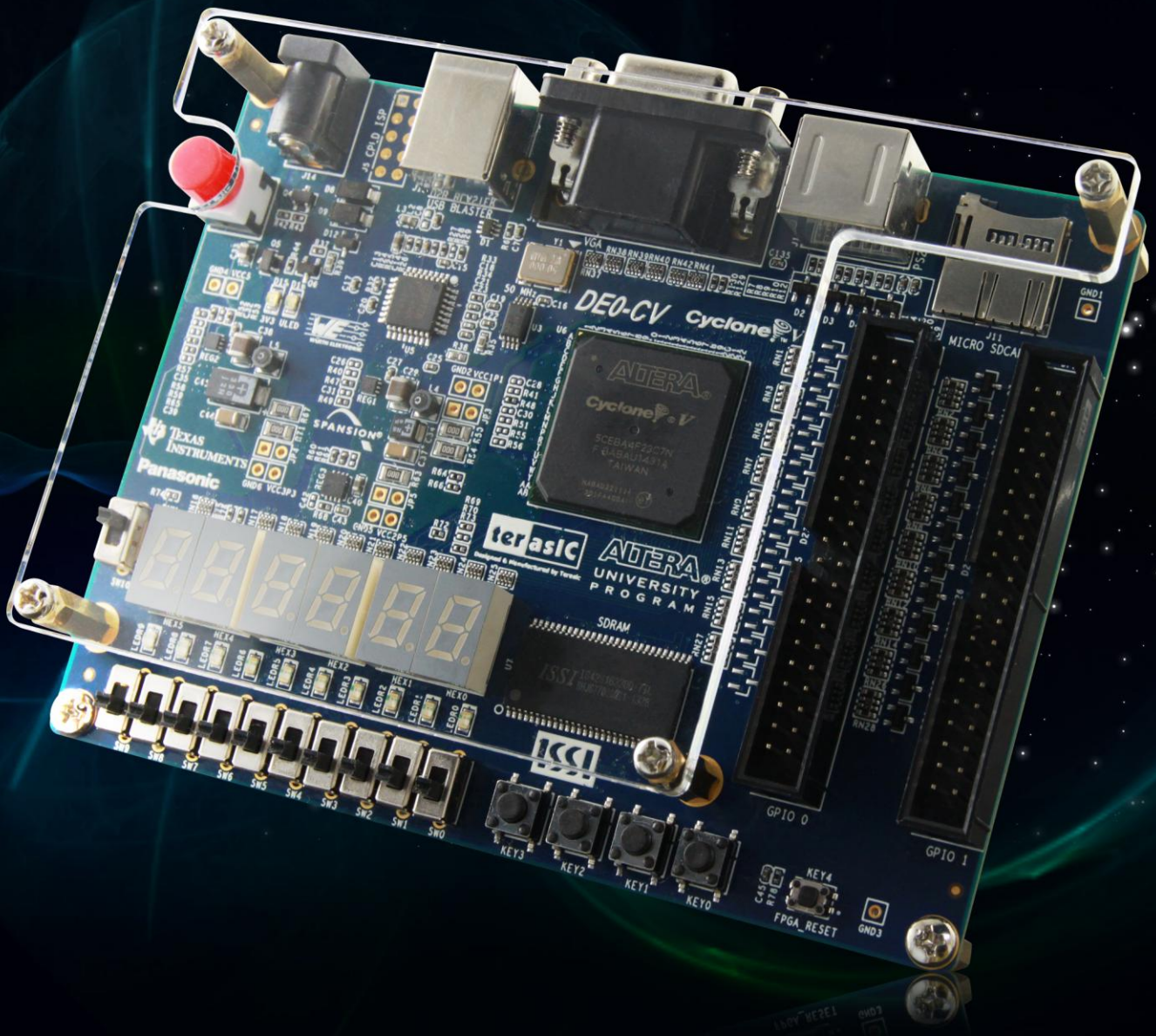
DE0-CV

User Manual



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Chapter 1

Introduction

The DE0-CV presents a robust hardware design platform built around the Altera Cyclone V FPGA, which is optimized for the lowest cost and power requirement for transceiver applications with industry-leading programmable logic for ultimate design flexibility. With Cyclone V FPGAs, you can get the power, cost, and performance levels you need for high-volume applications including protocol bridging, motor control drives and capture cards, and handheld devices. The DE0-CV development board includes hardware such as on-board USB Blaster, video capabilities and much more. By leveraging all of these capabilities, the DE0-CV is the perfect solution for showcasing, evaluating, and prototyping the true potential of the Altera Cyclone V FPGA.

The DE0-CV contains all components needed to use the board in conjunction with a computer that runs the Microsoft Windows XP or later.

1.1 Package Contents

Figure 1-1 shows a photograph of the DE0-CV package.

Figure 1-1 The DE0-CV package contents

The DE0-CV package includes:

- The DE0-CV board
- 5V DC Power Supply
- Type A Male to Type B Male USB Cable

1. 2 DE0-CV System CD

The DE0-CV System CD contains the documentation and supporting materials, including the User Manual, Control Panel, System Builder, reference designs and device datasheets. User can download this System CD from the web (http://cd-de0-cv.terasic.com).

1. 3 Layout and Components

This section presents the features and design characteristics of the board.

A photograph of the board is shown in **Figure 1-2** and **Figure 1-3.** It depicts the layout of the board and indicates the location of the connectors and key components.

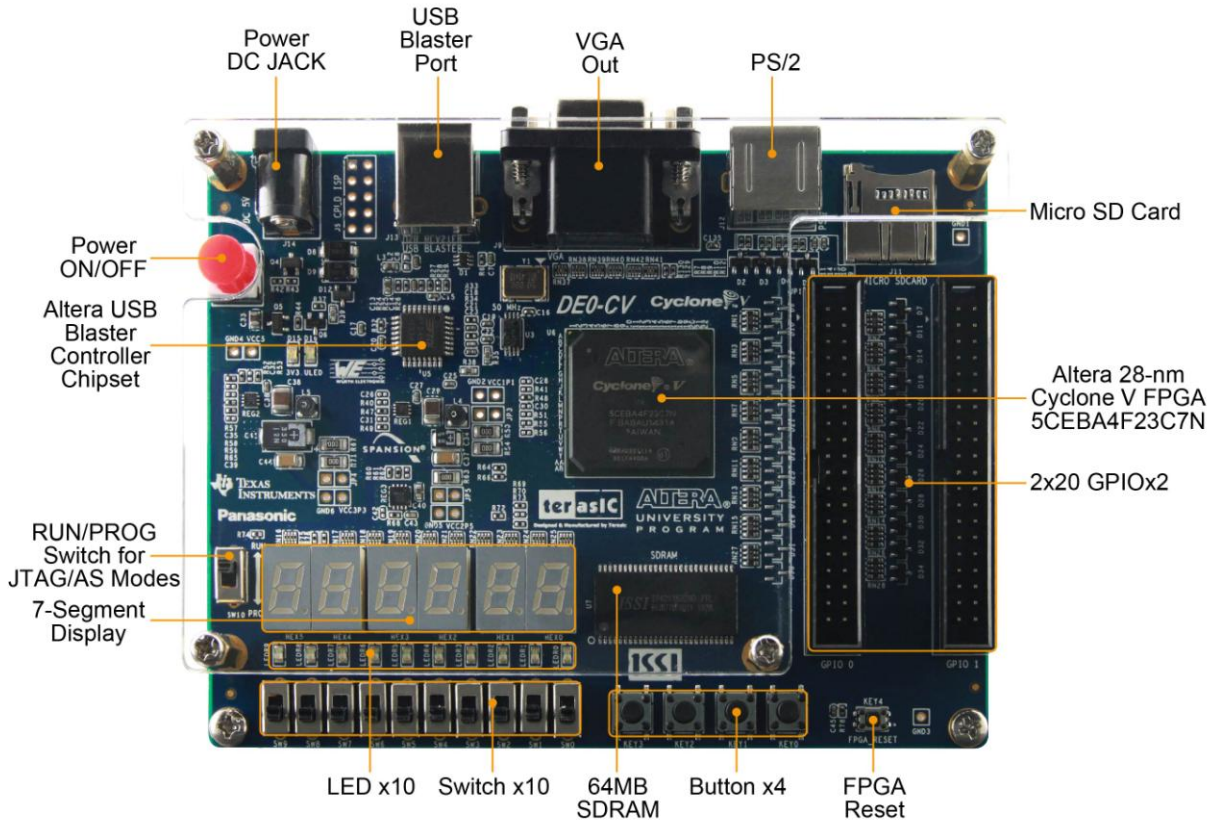

Figure 1-2 Development Board (top view)

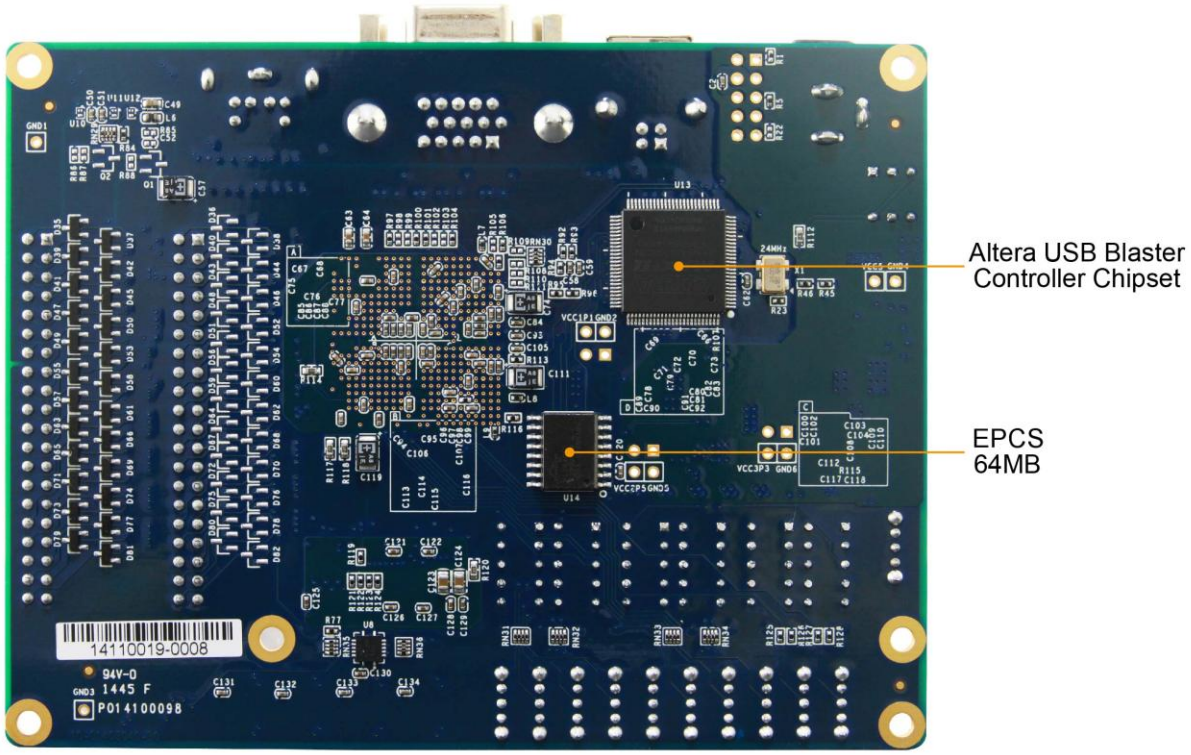

Figure 1-3 Development Board (bottom view)

This board has many features that allow users to implement a wide range of designed circuits, from simple circuits to various multimedia projects.

The following hardware is provided on the board:

FPGA Device

- Cyclone V 5CEBA4F23C7N Device
- 49K Programmable Logic Elements
- 3080 Kbits embedded memory
- 4 Fractional PLLs

Configuration and Debug

- Serial Configuration device – EPCS64 on FPGA
- On-Board USB Blaster (Normal type B USB connector)
- JTAG and AS mode configuration supported

Memory Device

- 64MB SDRAM, x16 bits data bus

Communication

- PS/2 mouse/keyboard

Connectors

- 2x20 GPIO Header

Display

- Uses a 4-bit resistor-network DAC
- With 15-pin high-density D-sub connector

Micro SD Card Socket

- Provides SPI and 4-bit SD mode for Micro SD Card access

Switches, Buttons and LEDs

- 10 LEDs
- 10 Slide Switches
- 4 Debounced Push Buttons
- 1 CPU reset Push Buttons
- Six 7-Segments

Power

- 5V DC input

1.4 Block Diagram of the Cyclone V Starter Board

Figure 1-4 gives the block diagram of the board. To provide maximum flexibility for the user, all connections are made through the Cyclone V FPGA device. Thus, the user can configure the FPGA to implement any system design.

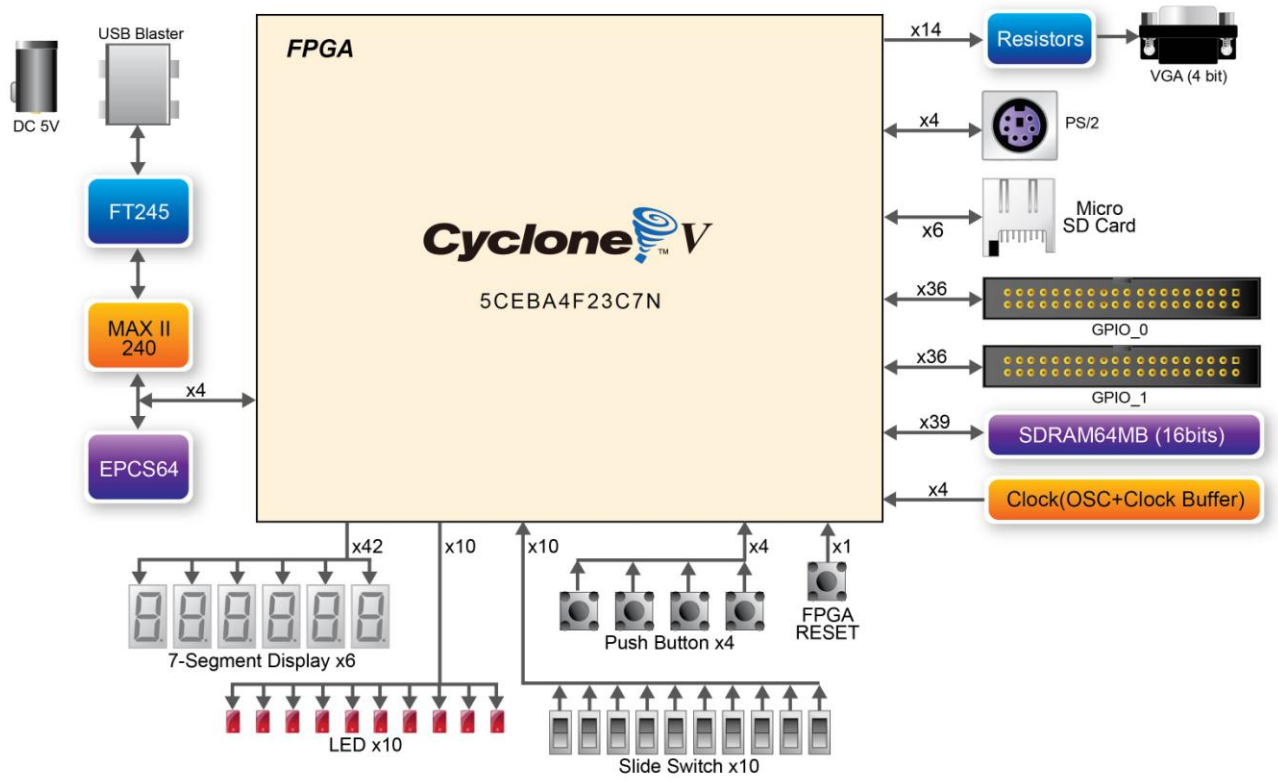

Figure 1-4 Board Block Diagram

1. 5 Getting Help

Here are the addresses where you can get help if you encounter any problem:

- Terasic Inc.

9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan

Email: support@terasic.com

Tel.: +886-3-5750-880

Web: http://www.DE0-CV.terasic.com

Chapter 2

Control Panel

The DE0-CV board comes with a Control Panel program that allows users to access various components on the board from a host computer. The host computer communicates with the board through a USB connection. The program can be used to verify the functionality of components on the board or be used as a debug tool while developing any RTL code.

This chapter first presents some basic functions of the Control Panel, then describes its structure in the block diagram form, and finally describes its capabilities.

2. 1 Control Panel Setup

The Control Panel Software Utility is located in the directory "Tools/ControlPanel" in the **DE0-CV System CD**. It's free of installation, just copy the whole folder to your host computer and launch the control panel by executing the "DE0CV_ControlPanel.exe".

Specific control circuits should be downloaded to your FPGA board before the control panel can request it to perform required tasks. The program will call Quartus II tools to download the control circuit to the FPGA board through the USB-Blaster[USB-0] connection.

To activate the Control Panel, perform the following steps:

1. Make sure Quartus II 14.0 or a later version is installed successfully on your PC.

2. Set the RUN/PROG switch to the RUN position.

3. Connect the USB cable provided to the USB Blaster port, connect the 5V power supply, and turn the power switch ON.

4. Start the executable *DE0CV_ControlPanel.exe* on the host computer. The Control Panel user interface shown in **Figure 2-1** will appear.

5. The DE0CV_ControlPanel.sof bit stream is loaded automatically as soon as the *DE0CV_ControlPanel.exe* is launched.

6. In case of a disconnect, click on CONNECT where the .sof will be re-loaded onto the board.

Please note that the Control Panel will occupy the USB port until you close that port; you cannot use Quartus II to download a configuration file into the FPGA until the USB port is closed.

7. The Control Panel is now ready to use; experience it by setting the ON/OFF status for some LEDs and observing the result on the DE0-CV board.

Figure 2-1 The DE0-CV Control Panel

The concept of the DE0-CV Control Panel is illustrated in **Figure 2-2.** The "Control Circuit" that performs the control functions is implemented in the FPGA board. It communicates with the Control Panel window, which is active on the host computer, via the USB Blaster link. The graphical interface is used to send commands to the control circuit. It handles all the requests and performs data transfers between the computer and the DE0-CV board.

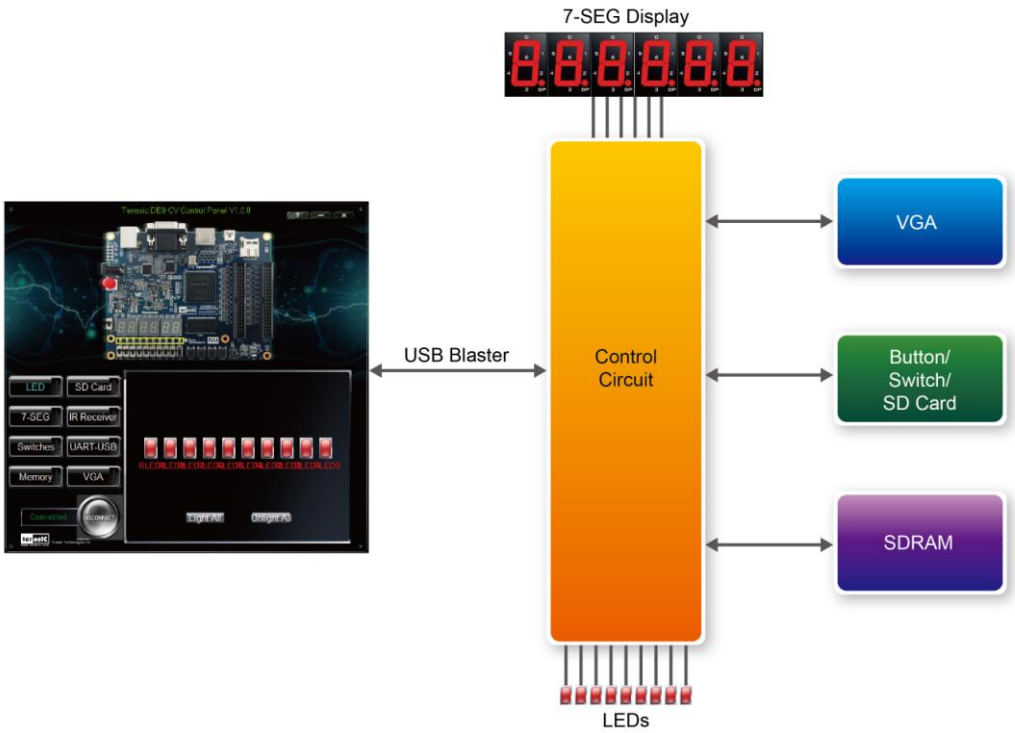

Figure 2-2 The DE0-CV Control Panel concept

The DE0-CV Control Panel can be used to light up LEDs, change the values displayed on the 7-segment, monitor buttons/switches status, read/write the SDRAM Memory, output VGA color pattern to VGA monitor, read SD Card specification information. The feature of reading/writing a word or an entire file from/to the Memory allows the user to develop multimedia applications without worrying about how to build a Memory Programmer.

2. 2 Controlling the LEDs, 7-segment Displays

A simple function of the Control Panel is to allow setting the values displayed on LEDs, 7-segment displays.

Choosing the **LED** tab leads to the window in **Figure 2-3.** Here, you can directly turn the LEDs on or off individually or by clicking “Light All” or “Unlight All”.

Figure 2-3 Controlling LEDs

Choosing the 7-SEG tab leads to the window shown in **Figure 2-4.** From the window, directly use the left-right arrows to control the 7-SEG patterns on the DE0-CV board which are updated immediately. Note that the dots of the 7-SEGs are not enabled on the DE0-CV board.

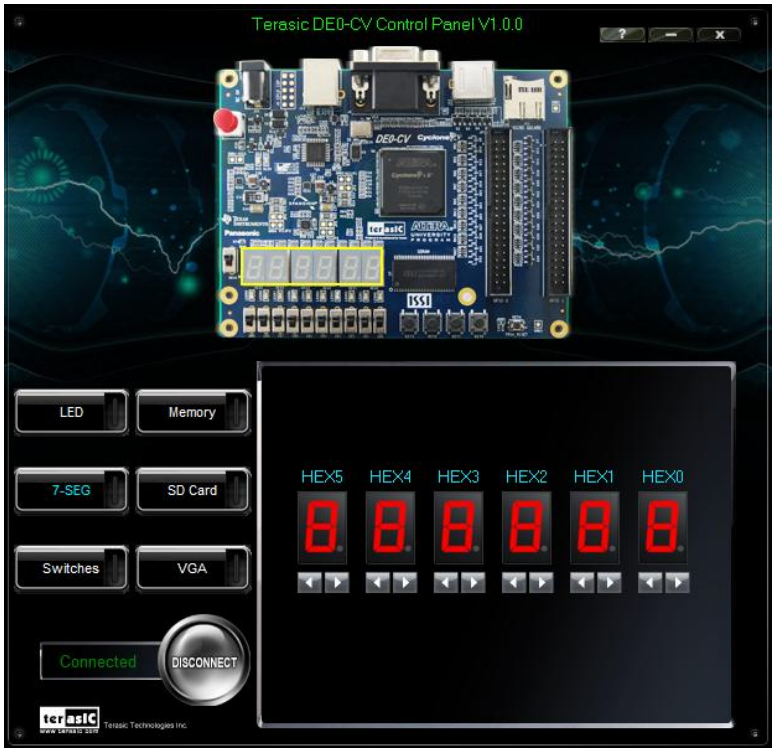

Figure 2-4 Controlling 7-SEG display

The ability to set arbitrary values into simple display devices is not needed in typical design activities. However, it gives users a simple mechanism for verifying that these devices are functioning correctly in case a malfunction is suspected. Thus, it can be used for troubleshooting purposes.

2. 3 Switches and Push-buttons

Choosing the Switches tab leads to the window in Figure 2-5. The function is designed to monitor the status of slide switches and push buttons in real time and show the status in a graphical user interface. It can be used to verify the functionality of the slide switches and push-buttons.

Figure 2-5 Monitoring switches and buttons

The ability to check the status of push-button and slide switch is not needed in typical design activities. However, it provides users a simple mechanism to verify if the buttons and switches are functioning correctly. Thus, it can be used for troubleshooting purposes.

2. 4 SDRAM Controller and Programmer

The Control Panel can be used to write/read data to/from the SDRAM chips on the DE0-CV board. As shown below, we will describe how the SDRAM may be accessed; Click on the Memory tab and select “SDRAM” to reach the window in Figure 2-6.

Figure 2-6 Accessing the SDRAM

A 16-bit word can be written into the SDRAM by entering the address of the desired location, specifying the data to be written, and pressing the Write button. Contents of the location can be read by pressing the Read button. **Figure 2-6** depicts the result of writing the hexadecimal value 06CA into offset address 200, followed by reading the same location.

The Sequential Write function of the Control Panel is used to write the contents of a file into the SDRAM as follows:

1. Specify the starting address in the Address box.
2. Specify the number of bytes to be written in the Length box. If the entire file is to be loaded, then a checkmark may be placed in the File Length box instead of giving the number of bytes.
3. To initiate the writing process, click on the Write a File to Memory button.
4. When the Control Panel responds with the standard Windows dialog box asking for the source file, specify the desired file location in the usual manner.

The Control Panel also supports loading files with a .hex extension. Files with a .hex extension are ASCII text files that specify memory values using ASCII characters to represent hexadecimal values. For example, a file containing the line

0123456789ABCDEF

defines eight 8-bit values: 01, 23, 45, 67, 89, AB, CD, EF. These values will be loaded consecutively into the memory.

The Sequential Read function is used to read the contents of the SDRAM and fill them into a file as follows:

1. Specify the starting address in the Address box.
2. Specify the number of bytes to be copied into the file in the Length box. If the entire contents of the SDRAM are to be copied (which involves all 64 Mbytes), then place a checkmark in the Entire Memory box.
3. Press Load Memory Content to a File button.
4. When the Control Panel responds with the standard Windows dialog box asking for the destination file, specify the desired file in the usual manner.

2. 5 SD Card

The function is designed to read the identification and specification information of the SD Card. The 4-bit SD MODE is used to access the SD Card. This function can be used to verify the functionality of the SD Card Interface. Follow the steps below to perform the SD Card exercise:

1. Choosing the SD Card tab leads to the window in **Figure 2-7.**

2. Insert an SD Card to the DE0-CV board, and then press the Read button to read the SD Card. The SD Card's identification, specification, and file format information will be displayed in the control window.

Figure 2-7 Reading the SD Card Identification and Specification

2. 6 VGA

DE0-CV Control Panel provides VGA pattern function that allows users to output color pattern to LCD/CRT monitor using the DE0-CV board. Follow the steps below to generate the VGA pattern function:

Choosing the VGA tab leads to the window in **Figure 2-8.**

Plug a D-sub cable to the VGA connector of the DE0-CV board and LCD /CRT monitor.

The LCD/CRT monitor will display the same color pattern on the control panel window.

Click the drop down menu shown in **Figure 2-8** where you can output the selected pattern individually.

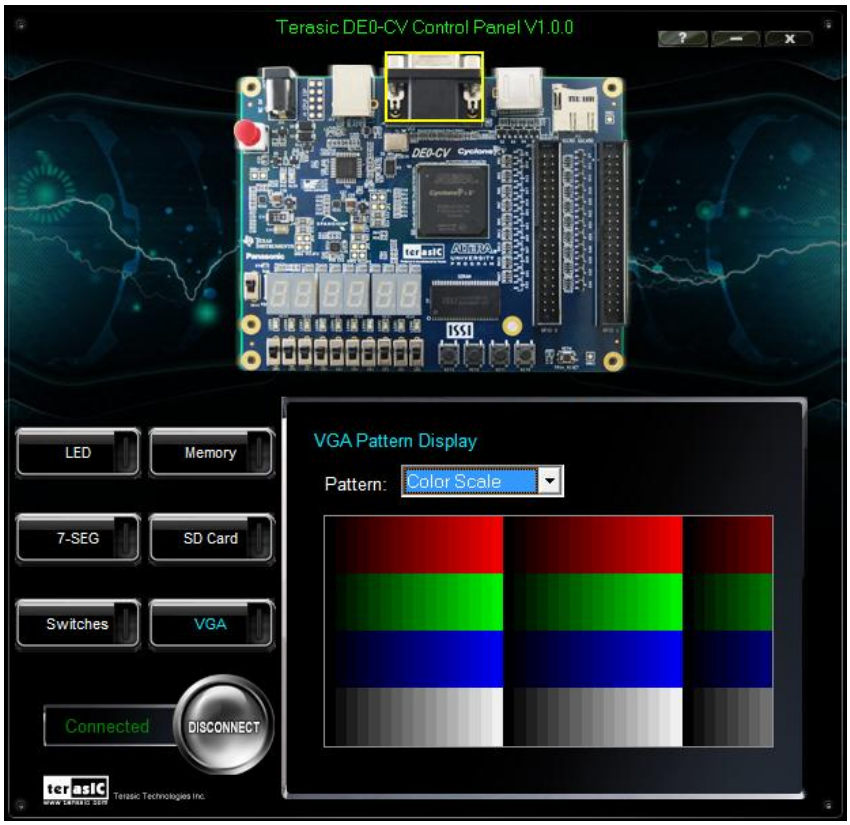

Figure 2-8 Controlling VGA display under Control Panel

2. 7 Overall Structure of the DE0-CV Control Panel

The DE0-CV Control Panel is based on a Nios II Qsys system instantiated in the Cyclone V FPGA with software running on the on-chip memory. The software part is implemented in C code; the hardware part is implemented in Verilog HDL code with Qsys builder. The source code is not available on the DE0-CV System CD.

To run the Control Panel, users should follow the configuration setting according to Section 3.1. Figure 2-9 depicts the structure of the Control Panel. Each input/output device is controlled by the Nios II Processor instantiated in the FPGA chip. The communication with the PC is done via the USB Blaster link. The Nios II interprets the commands sent from the PC and performs the corresponding actions.

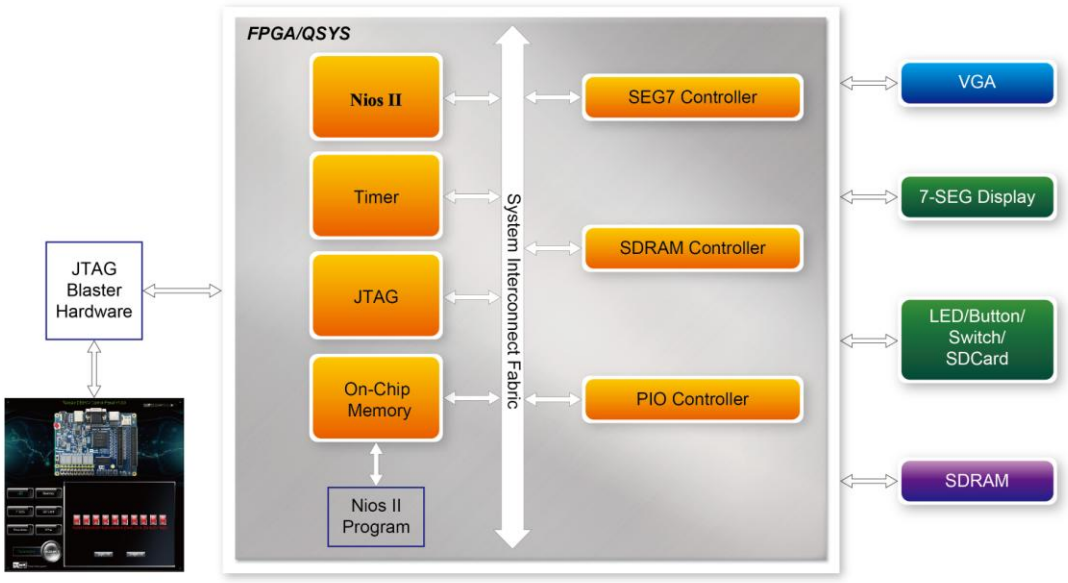

Figure 2-9 The block diagram of the DE0-CV control panel

Chapter 3

Using the Starter Kit

This chapter provides an instruction to use the board and describes the peripherals.

3. 1 Configuration of Cyclone V FPGA on DE0-CV

The DE0-CV board contains a serial configuration device that stores configuration data for the Cyclone V FPGA. This configuration data is automatically loaded from the configuration device into the FPGA when powered on. Using the Quartus II software, it is possible to reconfigure the FPGA at any time, and it is also possible to change the non-volatile data that is stored in the serial configuration device. Both types of programming methods are described below.

1. JTAG programming: In this method of programming, named after the IEEE standards Joint Test Action Group, the configuration bit stream is downloaded directly into the Cyclone V FPGA. The FPGA will retain this configuration as long as power is applied to the board; the configuration information will be lost when the power is turned off.

2. AS programming: In this method, called Active Serial programming, the configuration bit stream is downloaded into the Altera EPCS64 serial configuration device. It provides non-volatile storage of the bit stream, so that the information is retained even when the power supply to the DE0-CV board is turned off. When the board's power is turned on, the configuration data in the EPCS64 device is automatically loaded into the Cyclone V FPGA.

The sections below describe the steps to perform both JTAG and AS programming. For both methods the DE0-CV board is connected to a host computer via a USB cable. Using this connection, the board will be identified by the host computer as an Altera USB Blaster device.

■ Configuring the FPGA in JTAG Mode

Figure 3-1 illustrates the JTAG configuration setup. To download a configuration bit stream into the Cyclone V FPGA, you need to perform the following steps:

- Ensure that power is applied to the DE0-CV board
- Configure the JTAG programming circuit by setting the RUN/PROG slide switch (SW10) to the RUN position (See Figure 3-2)
- Connect the USB cable provided to the USB Blaster port on the DE0-CV board
- The FPGA can now be programmed by using the Quartus II Programmer to select a configuration bit stream file with the .sof filename extension

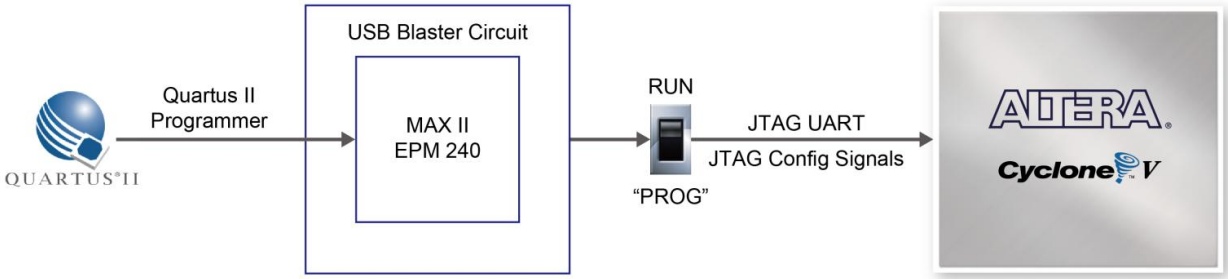

Figure 3-1 The JTAG configuration scheme

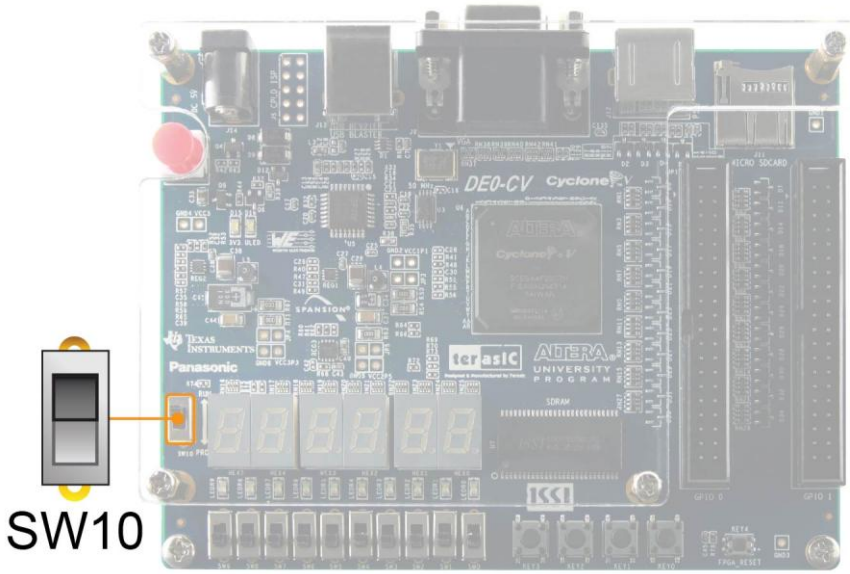

Figure 3-2 The RUN/PROG switch (SW10) is set in JTAG mode

■ Configuring the EPCS64 in AS Mode

Figure 3-3 illustrates the AS configuration setup. To download a configuration bit stream into the EPCS64 serial configuration device, you need to perform the following steps:

- Ensure that power is applied to the DE0-CV board.
- Connect the USB cable provided to the USB Blaster port on the DE0-CV board
- Configure the JTAG programming circuit by setting the RUN/PROG slide switch (SW10) to the PROG position.
- The EPCS64 chip can now be programmed by using the Quartus II Programmer to select a configuration bit stream file with the .pof filename extension.
- Once the programming operation is finished, set the RUN/PROG slide switch back to the RUN position and then reset the board by turning the power switch off and back on; this action causes the new configuration data in the EPCS64 device to be loaded into the FPGA chip.

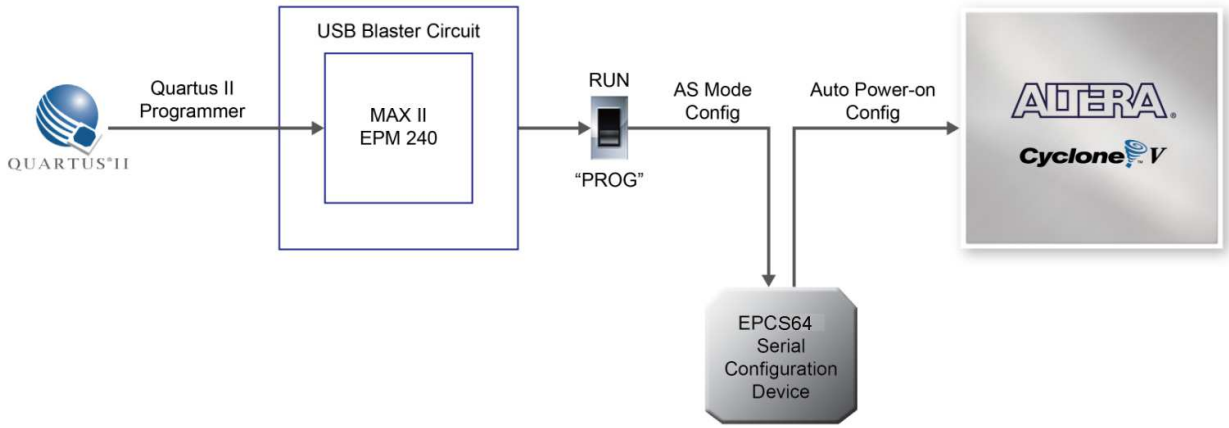

Figure 3-3 The AS configuration scheme

■ Status LED

- The FPGA development board includes board-specific status LEDs to indicate board status. Please refer to Table 3-1 for the description of the LED indicator. Please refer to Figure 3-4 for detailed LED location.

Table 3-1 Status LED

Board Reference	*LED Name*	*Description*
D15	3.3-V Power	Illuminates when 3.3-V power is active.
D16	ULED	Illuminates when the on-board USB-Blaster is working

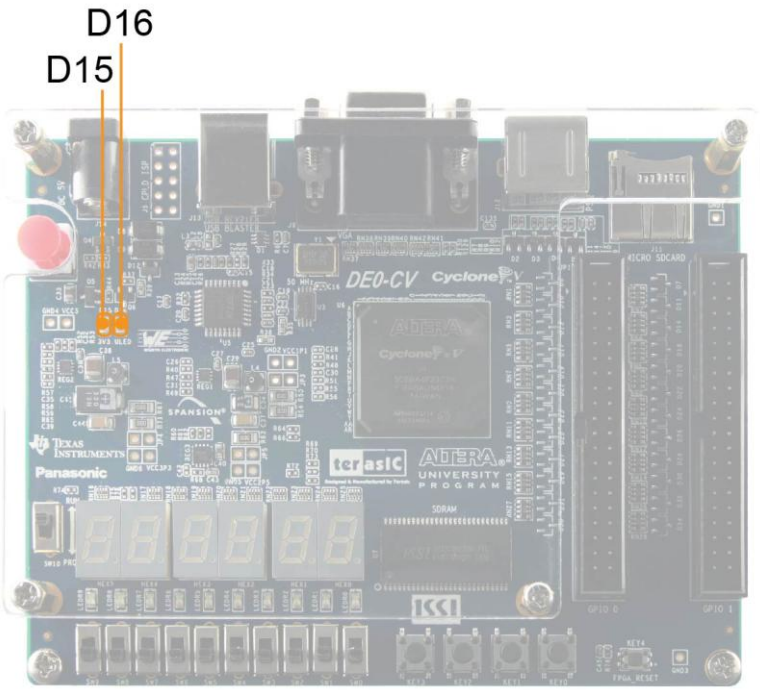

Figure 3-4 Status LED position

3. 2 Using the LEDs and Switches

■ User-Defined Push-buttons

The board includes four user defined push-buttons and one FPGA reset button that allow users to interact with the Cyclone V device as shown in Figure 3-5. Each of these switches is debounced using a Schmitt Trigger circuit, as indicated in Figure 3-6**.** The five outputs called KEY0, KEY1,

KEY2, KEY3 and RESET_N of the Schmitt Trigger devices are connected directly to the Cyclone V FPGA. Each push-button switch provides a high logic level when it is not pressed, and provides a low logic level when depressed. Since the push-button switches are debounced, they are appropriate for using as clocks or reset inputs in a circuit.

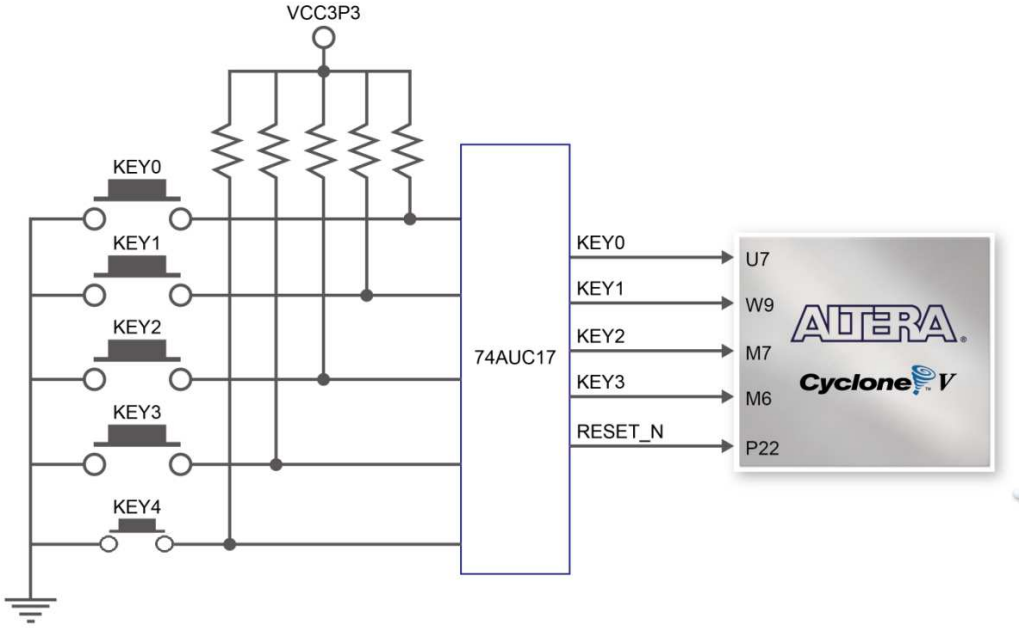

Figure 3-5 Connections between the push-button and Cyclone V FPGA

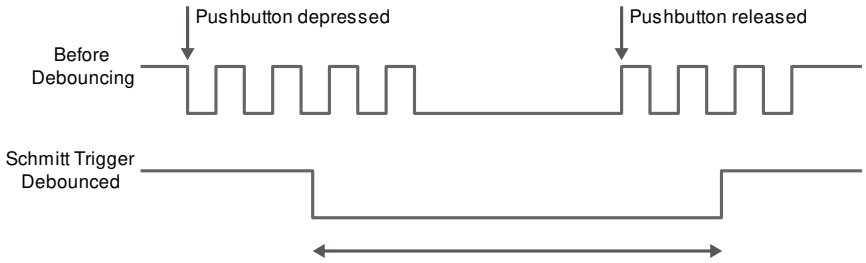

Figure 3-6 Switch debouncing

■ User-Defined Slide Switch

There are ten slide switches connected to FPGA on the board (See **Figure 3-7**). These switches are not debounced, and are assumed for use as level-sensitive data inputs to a circuit. Each switch is connected directly to a pin on the Cyclone V FPGA. When the switch is in the DOWN position (closest to the edge of the board), it provides a low logic level to the FPGA, and when the switch is in the UP position it provides a high logic level.

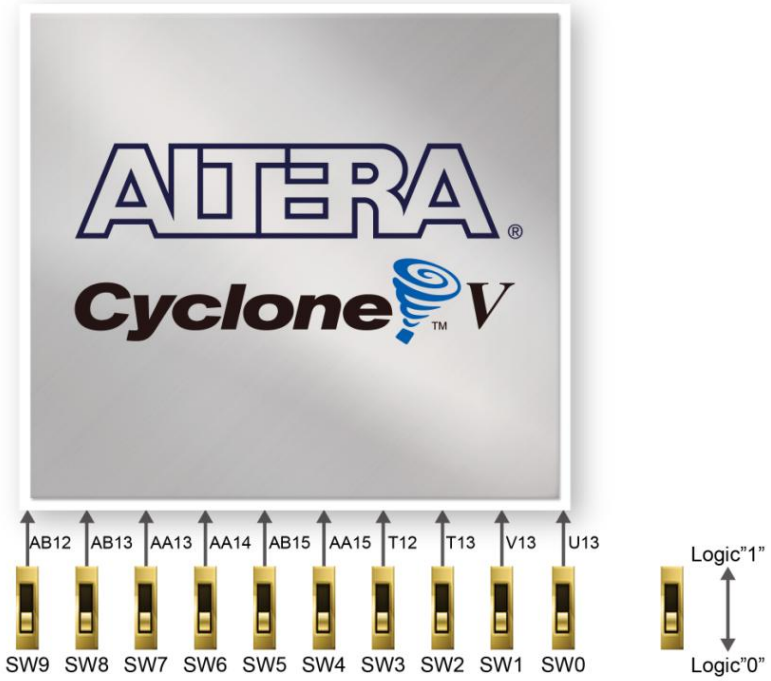

Figure 3-7 Connections between the slide switches and Cyclone V FPGA

■ User-Defined LEDs

There are also ten user-controllable LEDs connected to FPGA on the board. Each LED is driven directly by a pin on the Cyclone V FPGA; driving its associated pin to a high logic level turns the LED on, and driving the pin low turns it off. **Figure 3-8** shows the connections between LEDs and Cyclone V FPGA. **Table 3-2**, **Table 3-3** and **Table 3-4** list the pin assignment of user push-buttons, switches, and LEDs.

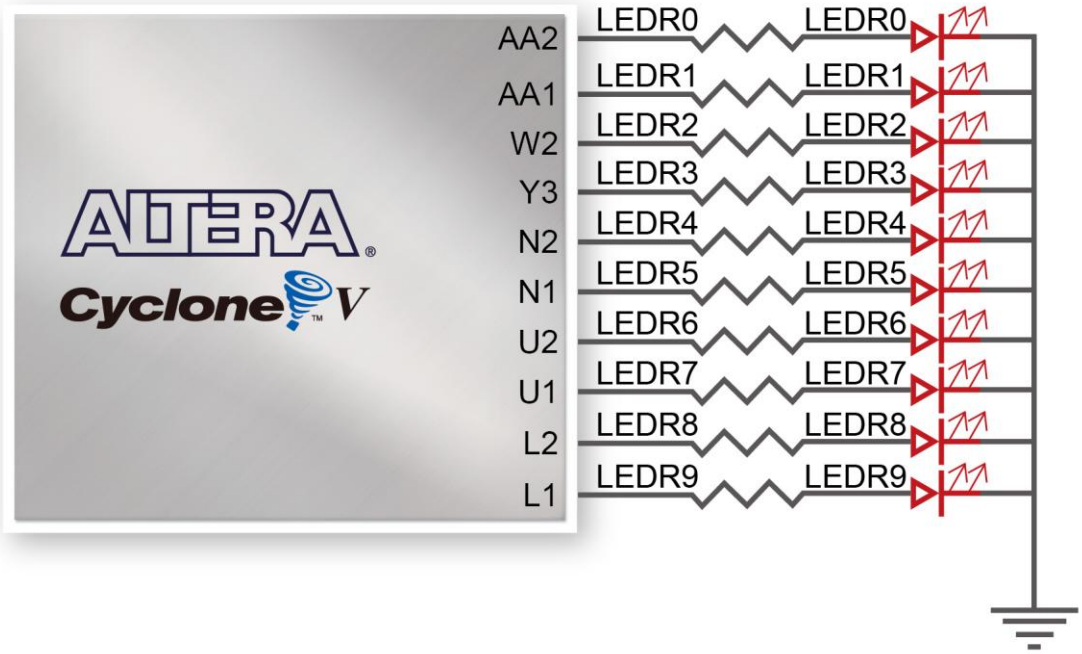

Figure 3-8 Connections between the LEDs and Cyclone V FPGA

Table 3-2 Pin Assignment of Push-buttons

Signal Name	*FPGA Pin No.*	*Description*
KEY0	PIN_U7	Push-button[0]
KEY1	PIN_W9	Push-button[1]
KEY2	PIN_M7	Push-button[2]
KEY3	PIN_M6	Push-button[3]
RESET_N	PIN_P22	Push-button which connected to DEV_CLRN Pin of FPGA

Table 3-3 Pin Assignment of Slide Switches

Signal Name	*FPGA Pin No.*	*Description*
SW0	PIN_U13	Slide Switch[0]
SW1	PIN_V13	Slide Switch[1]
SW2	PIN_T13	Slide Switch[2]
SW3	PIN_T12	Slide Switch[3]
SW4	PIN_AA15	Slide Switch[4]
SW5	PIN_AB15	Slide Switch[5]
SW6	PIN_AA14	Slide Switch[6]
SW7	PIN_AA13	Slide Switch[7]
SW8	PIN_AB13	Slide Switch[8]
SW9	PIN_AB12	Slide Switch[9]