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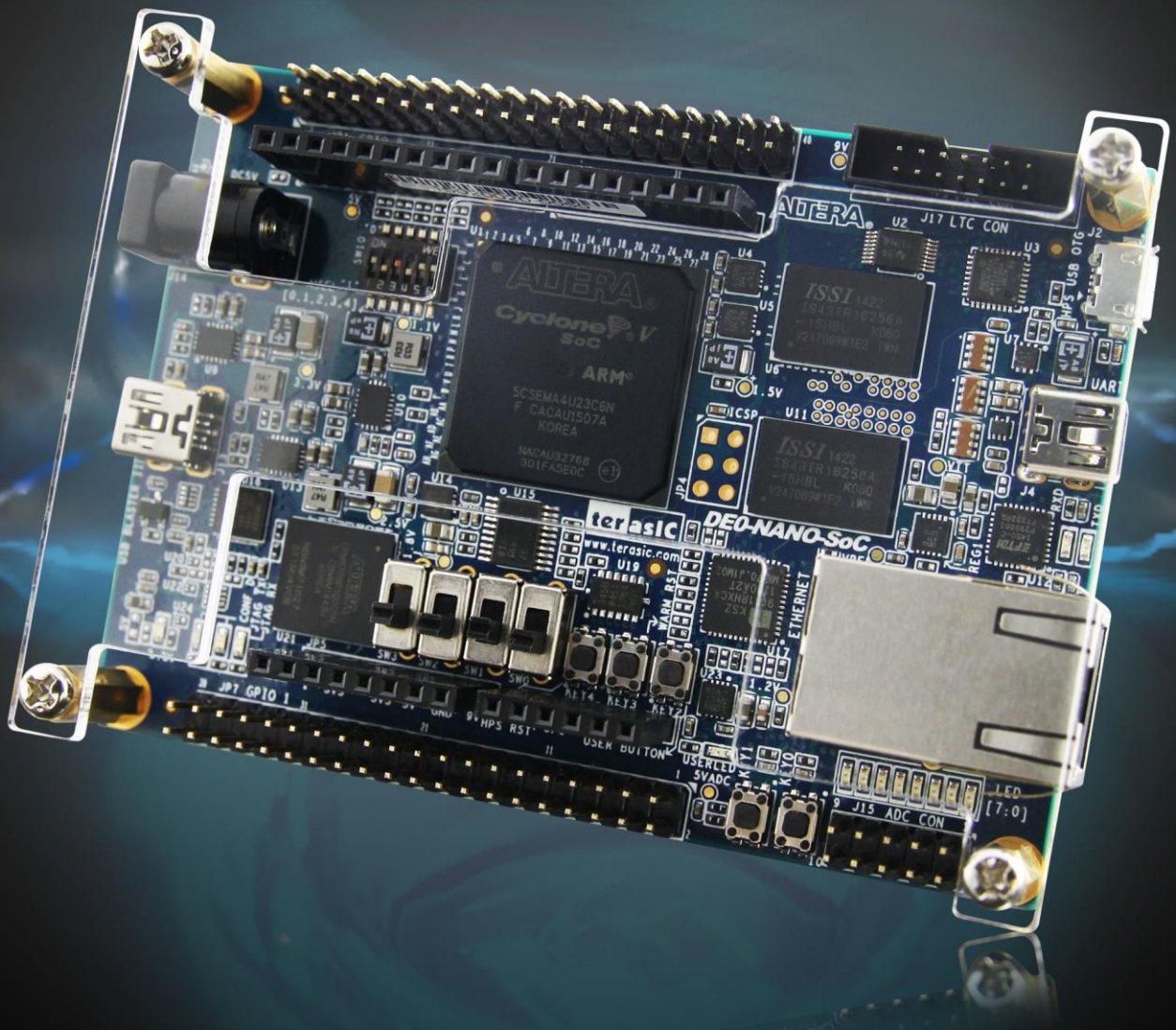
DE0-Nano-SoC

User Manual



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CONTENTS

Chapter 1

DE0-Nano-SoC Development Kit

The DE0-Nano-SoC Development Kit presents a robust hardware design platform built around the Altera System-on-Chip (SoC) FPGA, which combines the latest dual-core Cortex-A9 embedded cores with industry-leading programmable logic for ultimate design flexibility. Users can now leverage the power of tremendous re-configurability paired with a high-performance, low-power processor system. Altera's SoC integrates an ARM-based hard processor system (HPS) consisting of processor, peripherals and memory interfaces tied seamlessly with the FPGA fabric using a high-bandwidth interconnect backbone. The DE0-Nano-SoC development board is equipped with high-speed DDR3 memory, analog to digital capabilities, Ethernet networking, and much more that promise many exciting applications.

The DE0-Nano-SoC Development Kit contains all the tools needed to use the board in conjunction with a computer that runs the Microsoft Windows XP or later.

In addition, DE0-Nano-SoC Kit is also called Atlas-SoC Kit in Altera's Rockboard.org Linux community (http://www.rocketboards.org/atlas-soc). The hardware of DE0-Nano-SoC Kit and Atlas-SoC Kit are exactly the same, however, this community provides different development resource from DE0-Nano-SoC Kit. The details of kit contents can be found in the Appendix chapter.

1.1 Package Contents

Figure 1-1 shows a photograph of the DE0-Nano-SoC package.

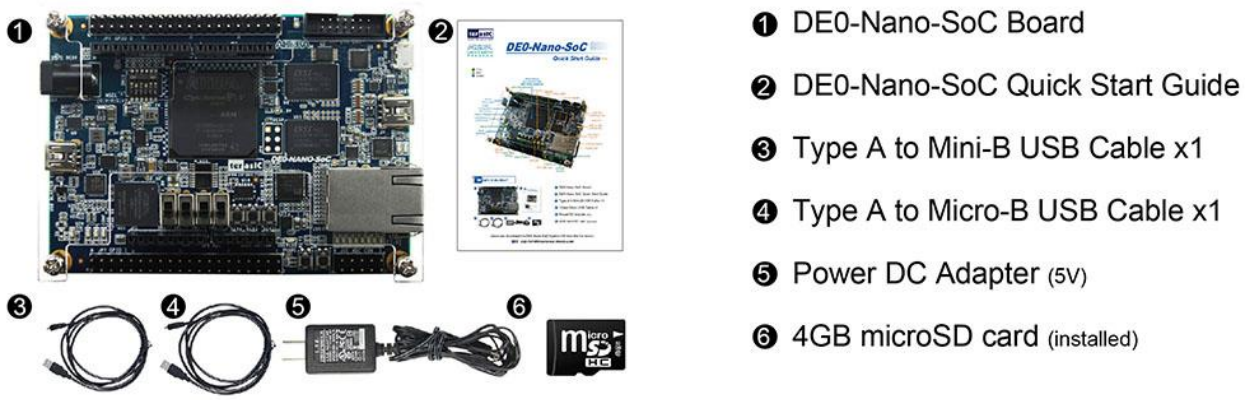

Figure 1-1 The DE0-Nano-SoC package contents

The DE0-Nano-SoC package includes:

- The DE0-Nano-SoC development board
- DE0-Nano-SoC Quick Start Guide
- USB cable Type A to Mini-B for FPGA programming or UART control
- USB cable Type A to Micro-B for USB OTG connect to PC
- 5V/2A DC power adapter
- 4GB microSD Card (Installed)

1.2 DE0-Nano-SoC System CD

The DE0-Nano-SoC System CD contains all the documents and supporting materials associated with DE0-Nano-SoC, including the user manual, system builder, reference designs, and device datasheets. Users can download this system CD from the link: http://cd-de0-nano-soc.terasic.com.

1.3 Getting Help

Here are the addresses where you can get help if you encounter any problems:

Altera Corporation

101 Innovation Drive San Jose, California, 95134 USA

Email: university@altera.com

Terasic Technologies

9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan

Email: support@terasic.com

Tel.: +886-3-575-0880

Website: de0-nano-soc.terasic.com

Chapter 2

Introduction of the DE0-Nano-SoC Board

This chapter provides an introduction to the features and design characteristics of the board.

2.1 Layout and Components

Figure 2-1 and Figure 2-2 shows a photograph of the board. It depicts the layout of the board and indicates the location of the connectors and key components.

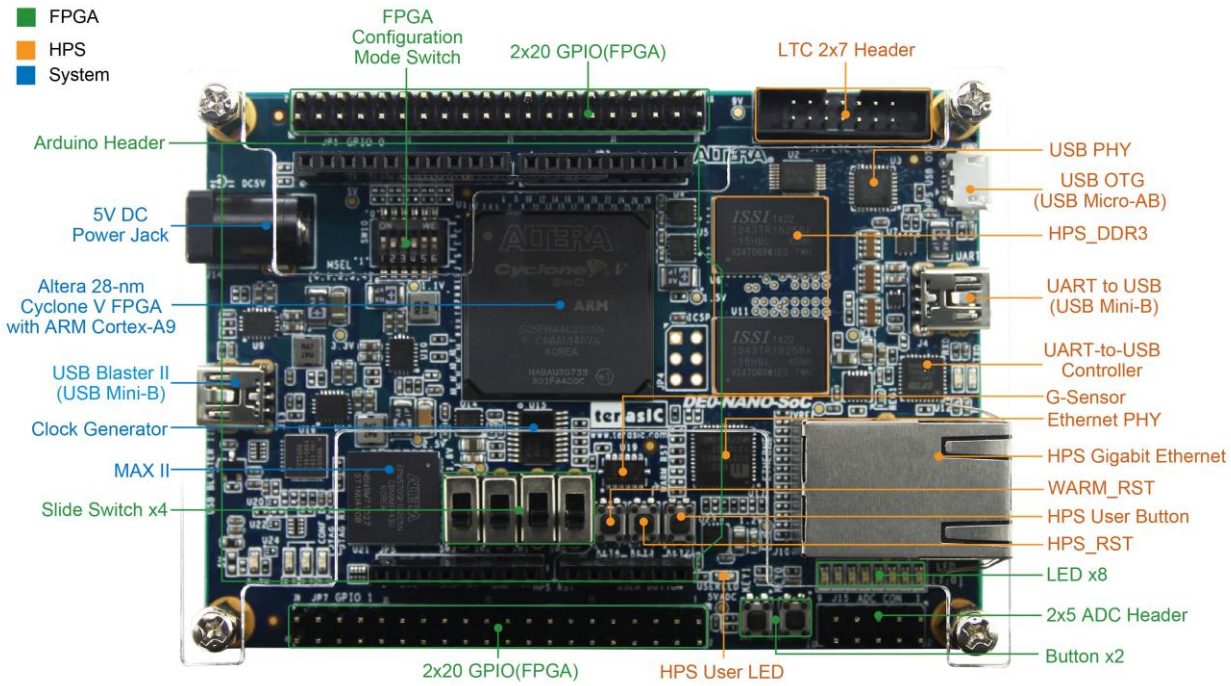

Figure 2-1 DE0-Nano-SoC development board (top view)

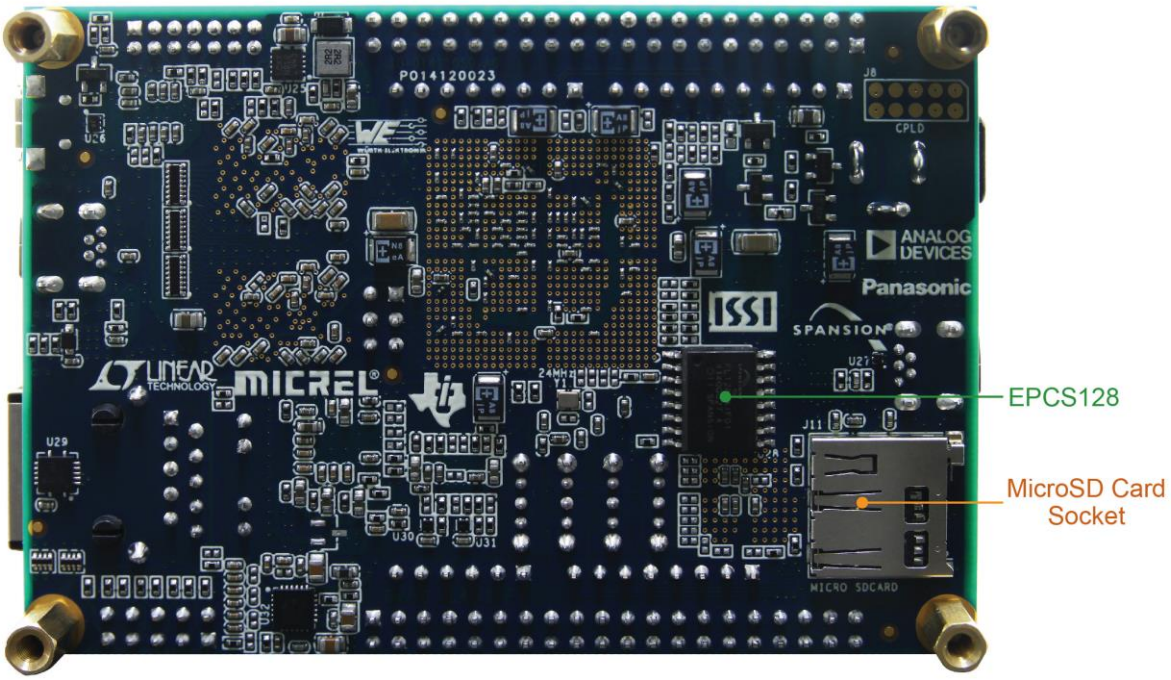

Figure 2-2 DE0-Nano-SoC development board (bottom view)

The DE0-Nano-SoC board has many features that allow users to implement a wide range of designed circuits, from simple circuits to various multimedia projects.

The following hardware is provided on the board:

■ FPGA

- Altera Cyclone® V SE 5CSEMA4U23C6N device
- Serial configuration device – EPCS128
- USB-Blaster II onboard for programming; JTAG Mode
- 2 push-buttons
- 4 slide switches
- 8 green user LEDs
- Three 50MHz clock sources from the clock generator
- Two 40-pin expansion header
- One Arduino expansion header (Uno R3 compatibility), can connect with Arduino shields.
- One 10-pin Analog input expansion header. (shared with Arduino Analog input)
- A/D converter, 4-wire SPI interface with FPGA

■ HPS (Hard Processor System)

- 925MHz Dual-core ARM Cortex-A9 processor
- 1GB DDR3 SDRAM (32-bit data bus)
- 1 Gigabit Ethernet PHY with RJ45 connector
- port USB OTG, USB Micro-AB connector
- Micro SD card socket
- Accelerometer (I2C interface + interrupt)
- UART to USB, USB Mini-B connector
- Warm reset button and cold reset button
- One user button and one user LED
- LTC 2x7 expansion header

2.2 Block Diagram of the DE0-Nano-SoC Board

Figure 2-3 is the block diagram of the board. All the connections are established through the Cyclone V SoC FPGA device to provide maximum flexibility for users. Users can configure the FPGA to implement any system design.

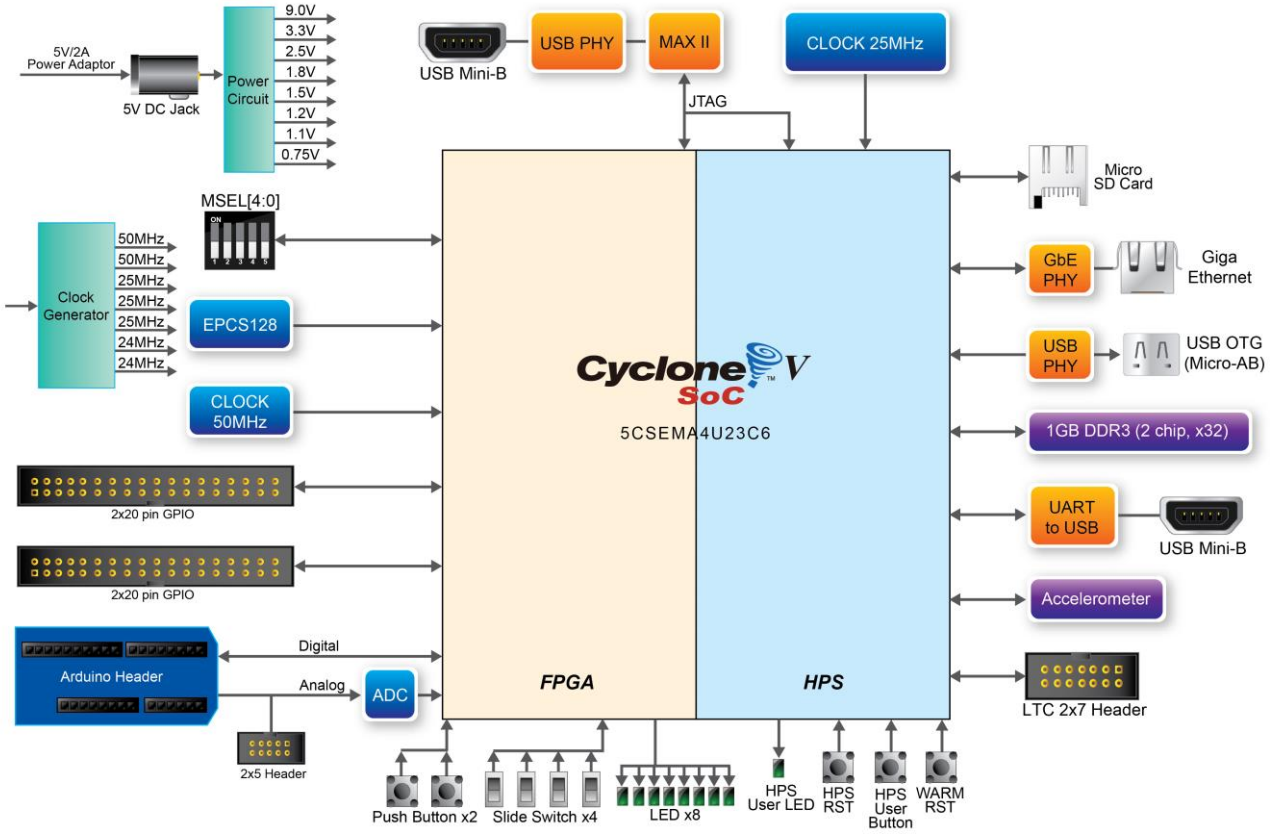

Figure 2-3 Block diagram of DE0-Nano-SoC

Detailed information about **Figure 2-3** are listed below.

FPGA Device

- Cyclone V SoC 5CSEMA4U23C6N Device
- Dual-core ARM Cortex-A9 (HPS)
- 40K programmable logic elements
- 2,460 Kbits embedded memory
- 5 fractional PLLs
- 2 hard memory controllers

Configuration and Debug

- Serial configuration device – EPCS128 on FPGA
- Onboard USB-Blaster II (Mini-B USB connector)

Memory Device

- 1GB (2x256Mx16) DDR3 SDRAM on HPS
- Micro SD card socket on HPS

Communication

- One USB 2.0 OTG (ULPI interface with USB Micro-AB connector)
- UART to USB (USB Mini-B connector)
- 10/100/1000 Ethernet

Connectors

- Two 40-pin expansion headers
- Arduino expansion header
- One 10-pin ADC input header
- One LTC connector (one Serial Peripheral Interface (SPI) Master ,one I2C and one GPIO interface)

ADC

- 12-Bit Resolution, 500Ksps Sampling Rate. SPI Interface.
- 8-Channel Analog Input. Input Range : 0V ~ 4.096V.

Switches, Buttons, and Indicators

- 3 user Keys (FPGA x2, HPS x1)
- 4 user switches (FPGA x4)
- 9 user LEDs (FPGA x8, HPS x 1)
- 2 HPS reset buttons (HPS_RESET_n and HPS_WARM_RST_n)

Sensors

- G-Sensor on HPS

Power

- 5V DC input

Chapter 3

Using the DE0-Nano-SoC Board

This chapter provides an instruction to use the board and describes the peripherals.

3.1 Settings of FPGA Configuration Mode

When the DE0-Nano-SoC board is powered on, the FPGA can be configured from EPCS or HPS.

The MSEL[4:0] pins are used to select the configuration scheme. It is implemented as a 6-pin DIP switch **SW10** on the DE0-Nano-SoC board, as shown in Figure 3-1.

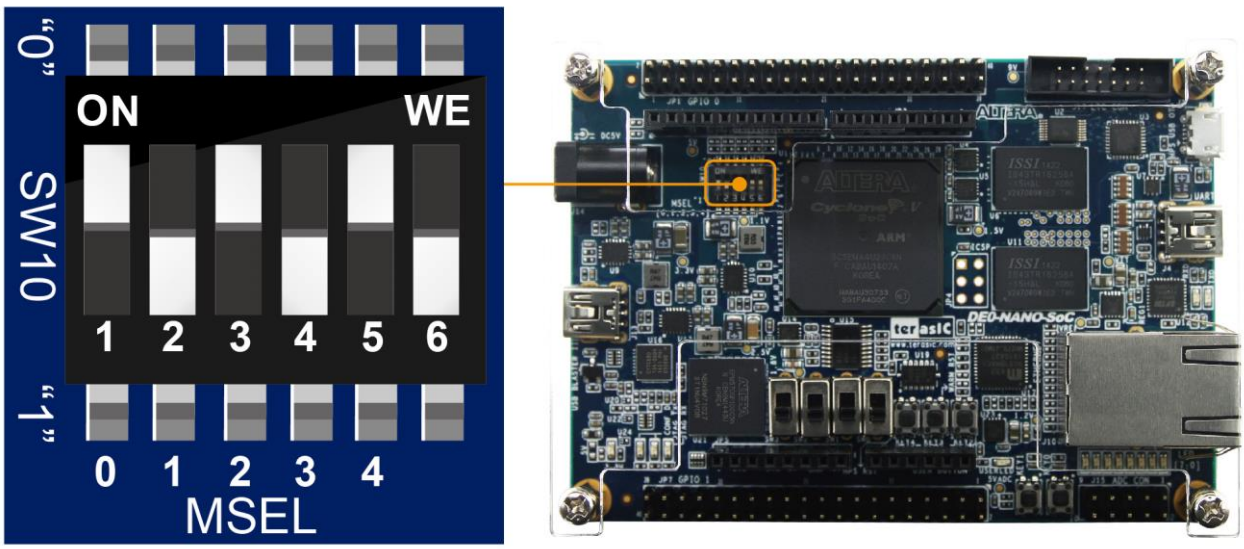

Figure 3-1 DIP switch (SW10) setting of FPP x32 mode

Table 3-1 shows the relation between MSEL[4:0] and DIP switch (SW10).

Table 3-1 FPGA Configuration Mode Switch (SW10)

Board Reference	*Signal Name*	*Description*	*Default*
SW10.1	MSEL0	Use these pins to set the FPGA Configuration scheme	ON (“0”)
SW10.2	MSEL1		OFF (“1”)
SW10.3	MSEL2		ON (“0”)
SW10.4	MSEL3		OFF (“1”)
SW10.5	MSEL4		ON (“0”)
SW10.6	N/A	N/A	N/A

Table 3-2 shows MSEL[4:0] setting for FPGA configure, and default setting is FPPx32 mode on DE0-Nano-SoC.

When the board is powered on and MSEL[4:0] set to “10010”, the FPGA is configured from EPCS, which is pre-programmed with the default code. If developers wish to configure FPGA from an application software running on Linux, the MSEL[4:0] needs to be set to “01010” before the programming process begins. If developers using the "Linux Console with frame buffer" or "Linux LXDE Desktop" SD Card image, the MSEL[4:0] needs to be set to “00000” before the board is powered on.

Table 3-2 MSEL Pin Settings for FPGA Configure of DE0-Nano-SoC

Configuration	*SW10.1 MSEL0*	*SW10.2 MSEL1*	*SW10.3 MSEL2*	*SW10.4 MSEL3*	*SW10.5 MSEL4*	*SW10.6*	*Description*
AS	ON	OFF	ON	ON	OFF	N/A	FPGA configured from EPCS
FPPx32 (Default)	ON	OFF	ON	OFF	ON	N/A	FPGA configured from HPS software: Linux (default)
FPPx16	ON	ON	ON	ON	ON	N/A	FPGA configured from HPS software: U-Boot, with image stored on the SD card, like LXDE Desktop or console Linux with frame buffer edition.

3.2 Configuration of Cyclone V SoC FPGA on DE0-Nano-SoC

There are two types of programming method supported by DE0-Nano-SoC:

1. JTAG programming: It is named after the IEEE standards Joint Test Action Group.

The configuration bit stream is downloaded directly into the Cyclone V SoC FPGA. The FPGA will retain its current status as long as the power keeps applying to the board; the configuration information will be lost when the power is off.

2. AS programming: The other programming method is Active Serial configuration.

The configuration bit stream is downloaded into the serial configuration device (EPCS128), which provides non-volatile storage for the bit stream. The information is retained within EPCS128 even if the DE0-Nano-SoC board is turned off. When the board is powered on, the configuration data in the EPCS128 device is automatically loaded into the Cyclone V SoC FPGA.

■ JTAG Chain on DE0-Nano-SoC Board

The FPGA device can be configured through JTAG interface on DE0-Nano-SoC board, but the JTAG chain must form a closed loop, which allows Quartus II programmer to the detect FPGA device. Figure 3-2 illustrates the JTAG chain on DE0-Nano-SoC board.

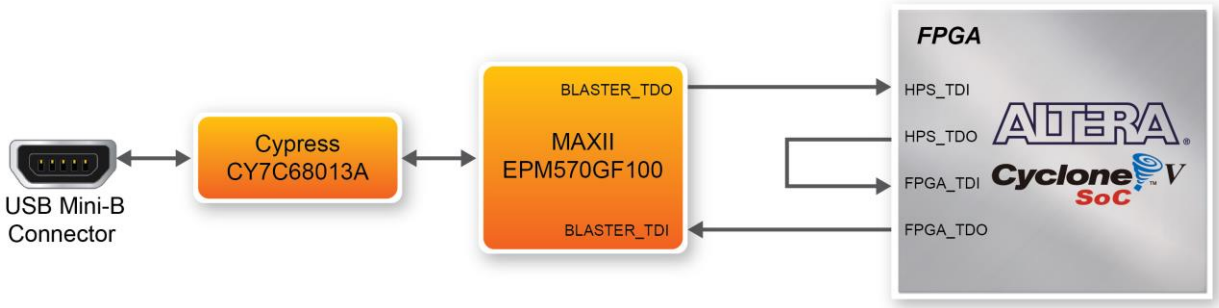

Figure 3-2 Path of the JTAG chain

■ Configure the FPGA in JTAG Mode

There are two devices (FPGA and HPS) on the JTAG chain. The following shows how the FPGA is programmed in JTAG mode step by step.

Open the Quartus II programmer and click “Auto Detect”, as circled in Figure 3-3

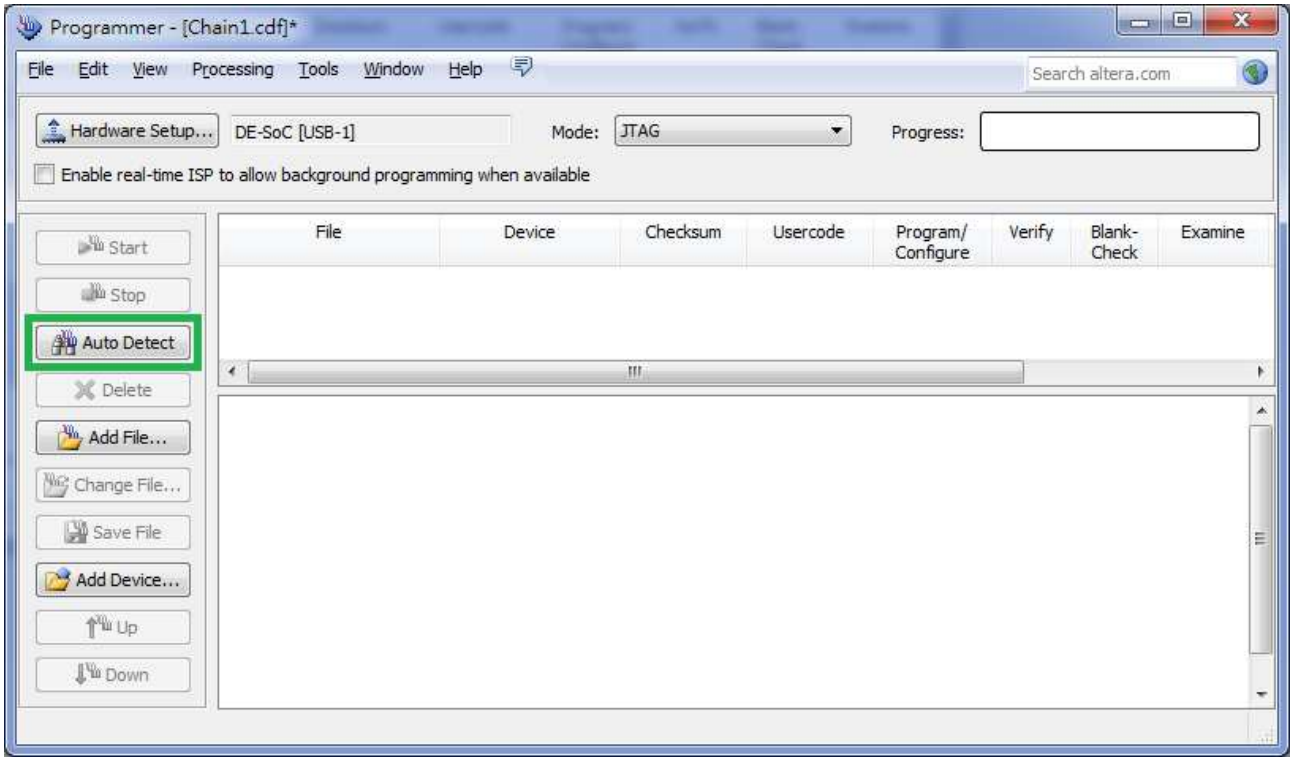

Figure 3-3 Detect FPGA device in JTAG mode

Select detected device associated with the board, as circled in Figure 3-4.

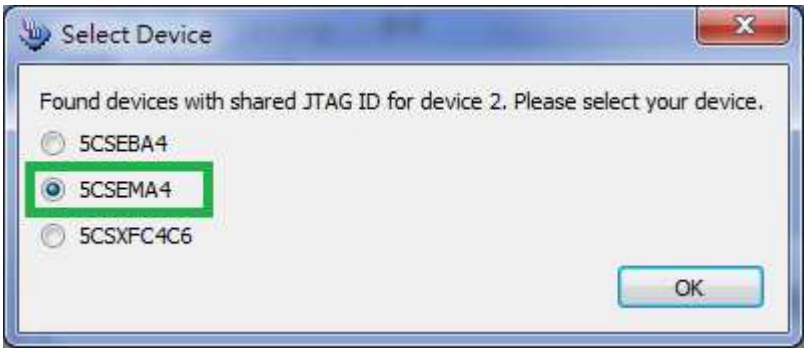

Figure 3-4 Select 5CSEMA4 device

Both FPGA and HPS are detected, as shown in Figure 3-5.

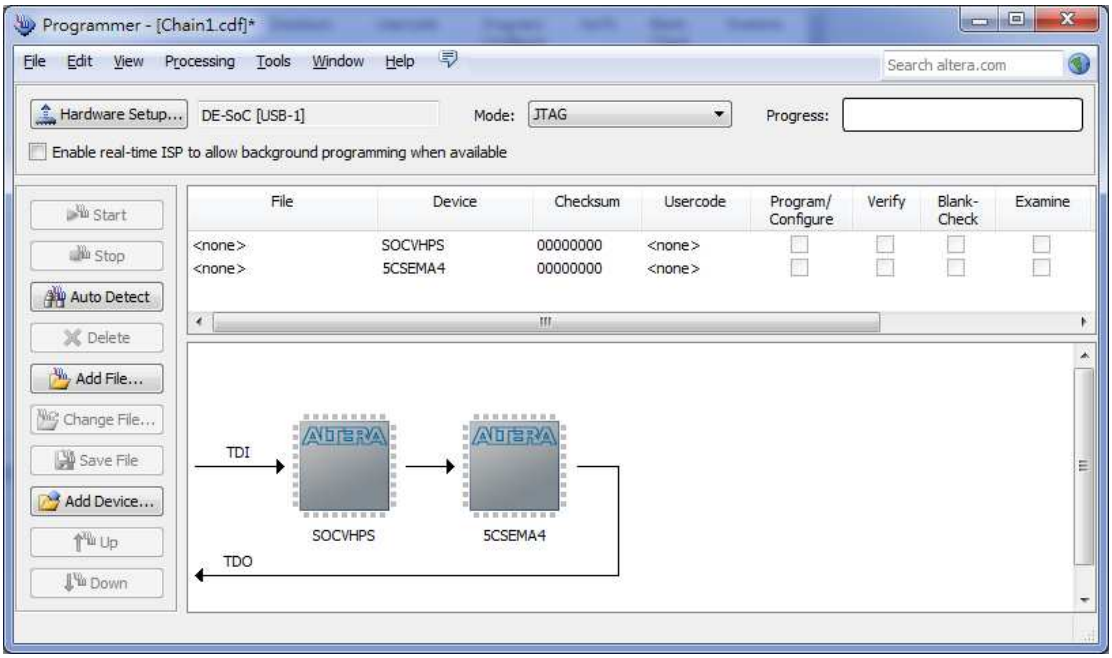

Figure 3-5 FPGA and HPS detected in Quartus programmer

Right click on the FPGA device and open the .sof file to be programmed, as highlighted in Figure 3-6.

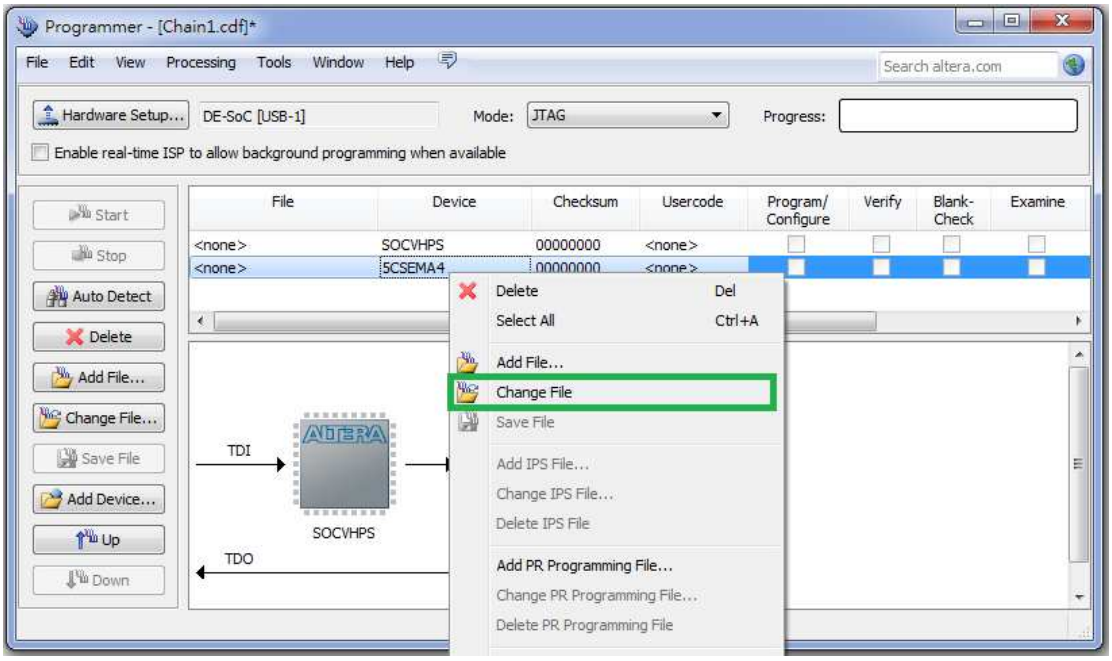

Figure 3-6 Open the .sof file to be programmed into the FPGA device

Select the .sof file to be programmed, as shown in Figure 3-7.

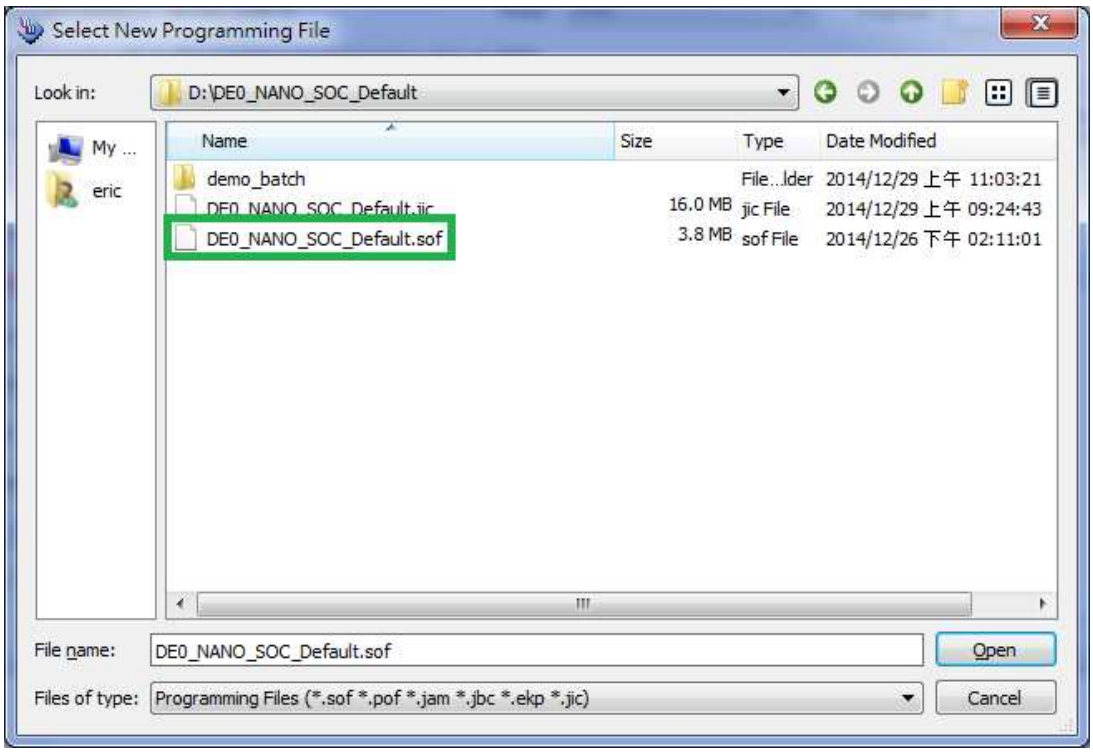

Figure 3-7 Select the .sof file to be programmed into the FPGA device

Click "Program/Configure" check box and then click "Start" button to download the .sof file into the FPGA device, as shown in Figure 3-8.

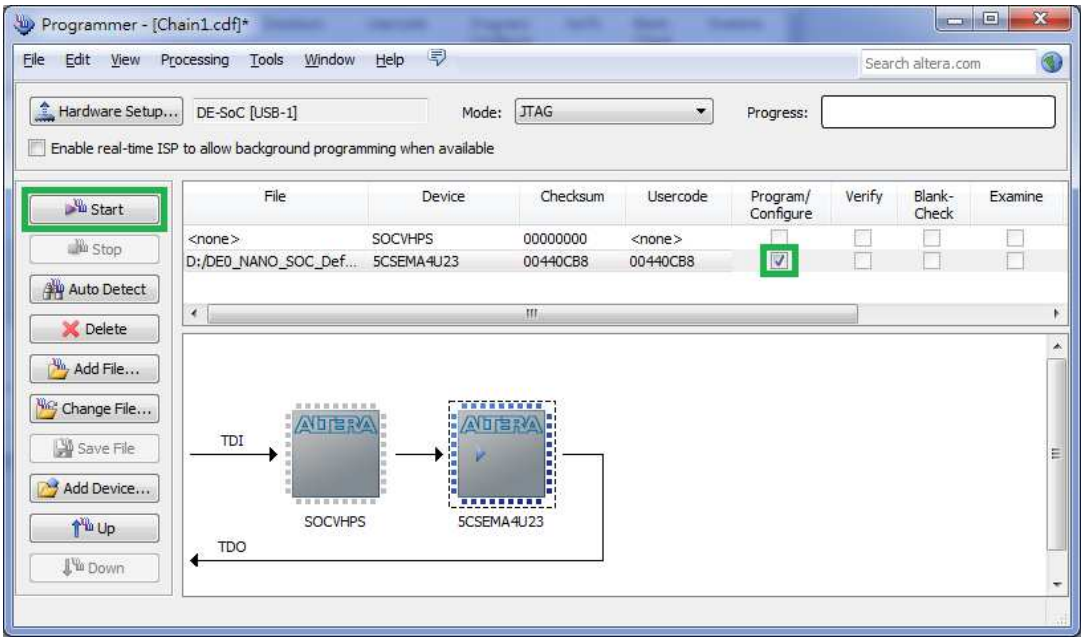

Figure 3-8 Program .sof file into the FPGA device

■ Configure the FPGA in AS Mode

The DE0-Nano-SoC board uses a serial configuration device (EPCS128) to store configuration data for the Cyclone V SoC FPGA. This configuration data is automatically loaded from the serial configuration device chip into the FPGA when the board is powered up.

Users need to use Serial Flash Loader (SFL) to program the serial configuration device via JTAG interface. The FPGA-based SFL is a soft intellectual property (IP) core within the FPGA that bridge the JTAG and Flash interfaces. The SFL Megafunction is available in Quartus II. **Figure 3-9** shows the programming method when adopting SFL solution.

Please refer to Chapter 8: Steps of Programming the Serial Configuration Device for the basic programming instruction on the serial configuration device.

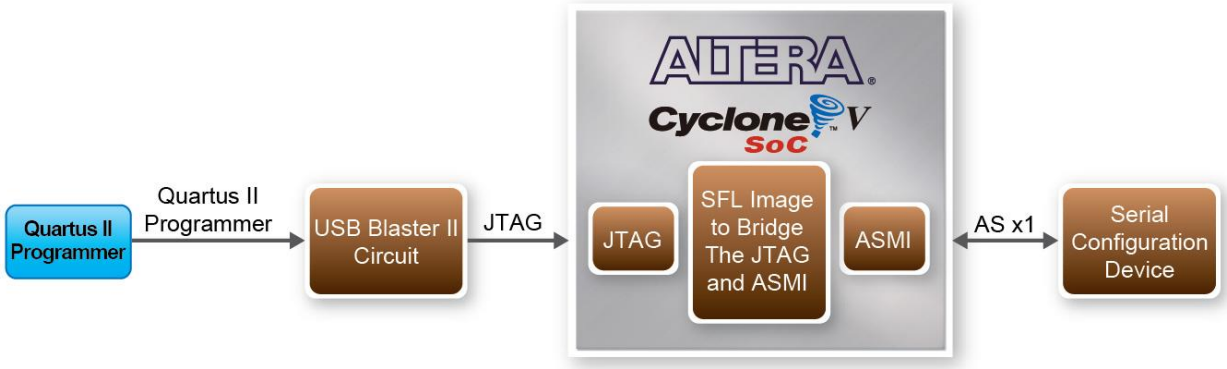

Figure 3-9 Programming a serial configuration device with SFL solution

3.3 Board Status Elements

In addition to the 9 LEDs that FPGA/HPS device can control, there are 6 indicators which can indicate the board status (See Figure 3-10), please refer the details in Table 3-3

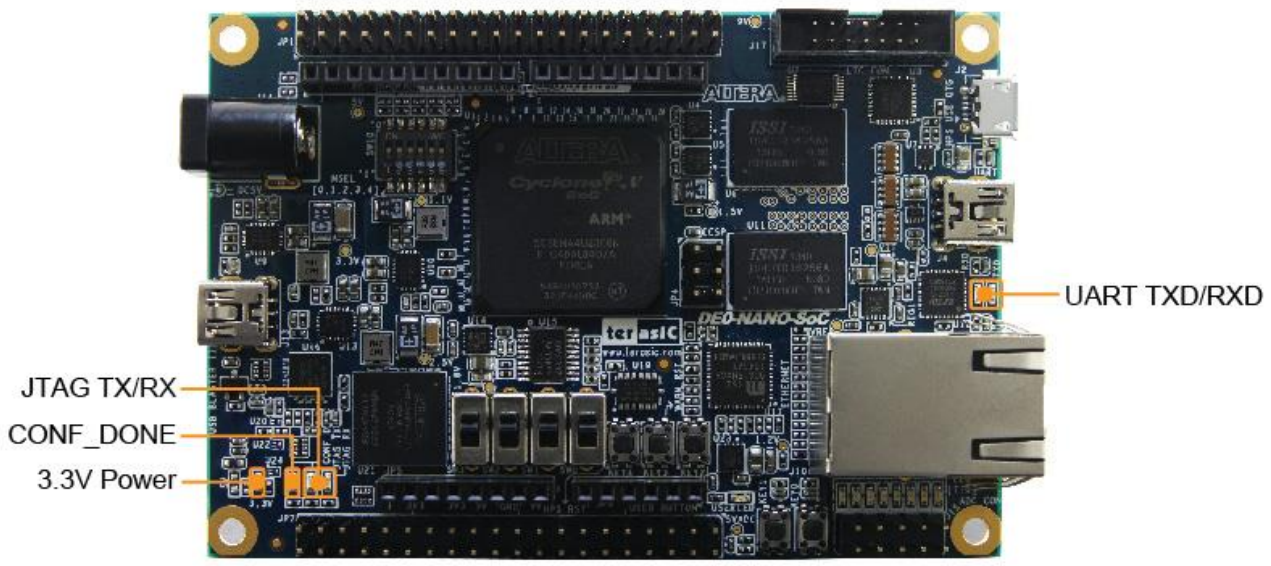

Figure 3-10 LED Indicators on DE0-Nano-SoC

Table 3-3 LED Indicators

Board Reference	*LED Name*	*Description*
LED9	3.3-V Power	Illuminate when 3.3V power is active.
LED10	CONF_DONE	Illuminates when the FPGA is successfully configured.
LED11	JTAG_TX	Illuminate when data is transferred from JTAG to USB Host.
LED12	JTAG_RX	Illuminate when data is transferred from USB Host to JTAG.
TXD	UART TXD	Illuminate when data is transferred from FT232R to USB Host.
RXD	UART RXD	Illuminate when data is transferred from USB Host to FT232R.

3.4 Board Reset Elements

There are two HPS reset buttons on DE0-Nano-SoC, HPS (cold) reset and HPS warm reset, as shown in Figure 3-11. Table 3-4 describes the purpose of these two HPS reset buttons. Figure 3-12 is the reset tree for DE0-Nano-SoC.

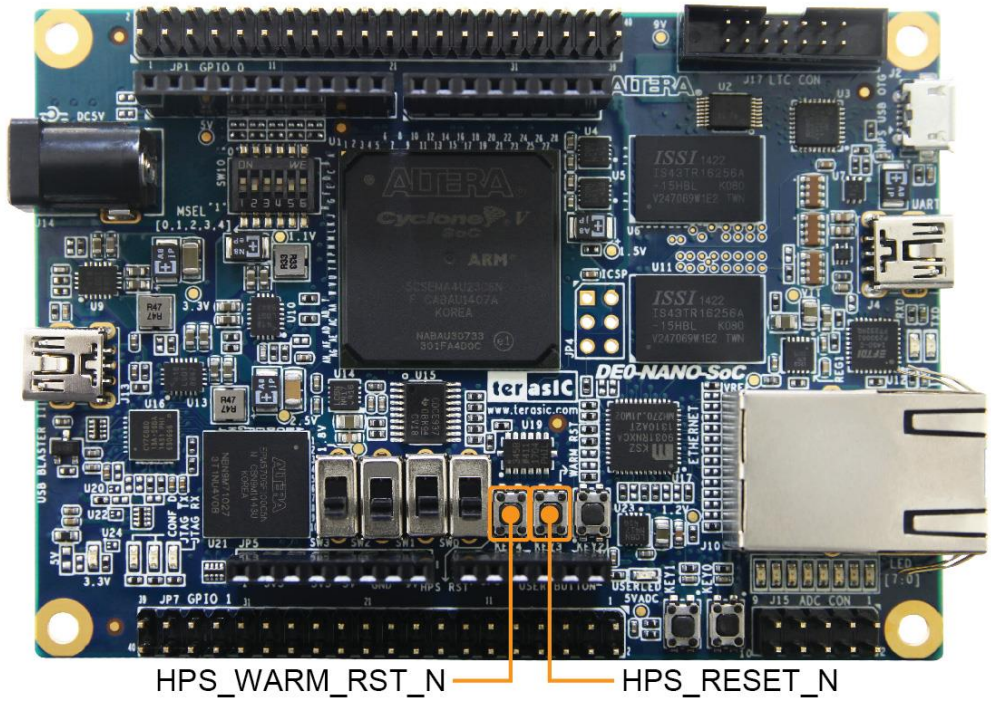

Figure 3-11 HPS cold reset and warm reset buttons on DE0-Nano-SoC

Table 3-4 Description of Two HPS Reset Buttons on DE0-Nano-SoC

Board Reference	*Signal Name*	*Description*
KEY4	HPS_RESET_N	Cold reset to the HPS, Ethernet PHY and USB host device. Active low input which resets all HPS logics that can be reset.
KEY3	HPS_WARM_RST_N	Warm reset to the HPS block. Active low input affects the system reset domain for debug purpose.

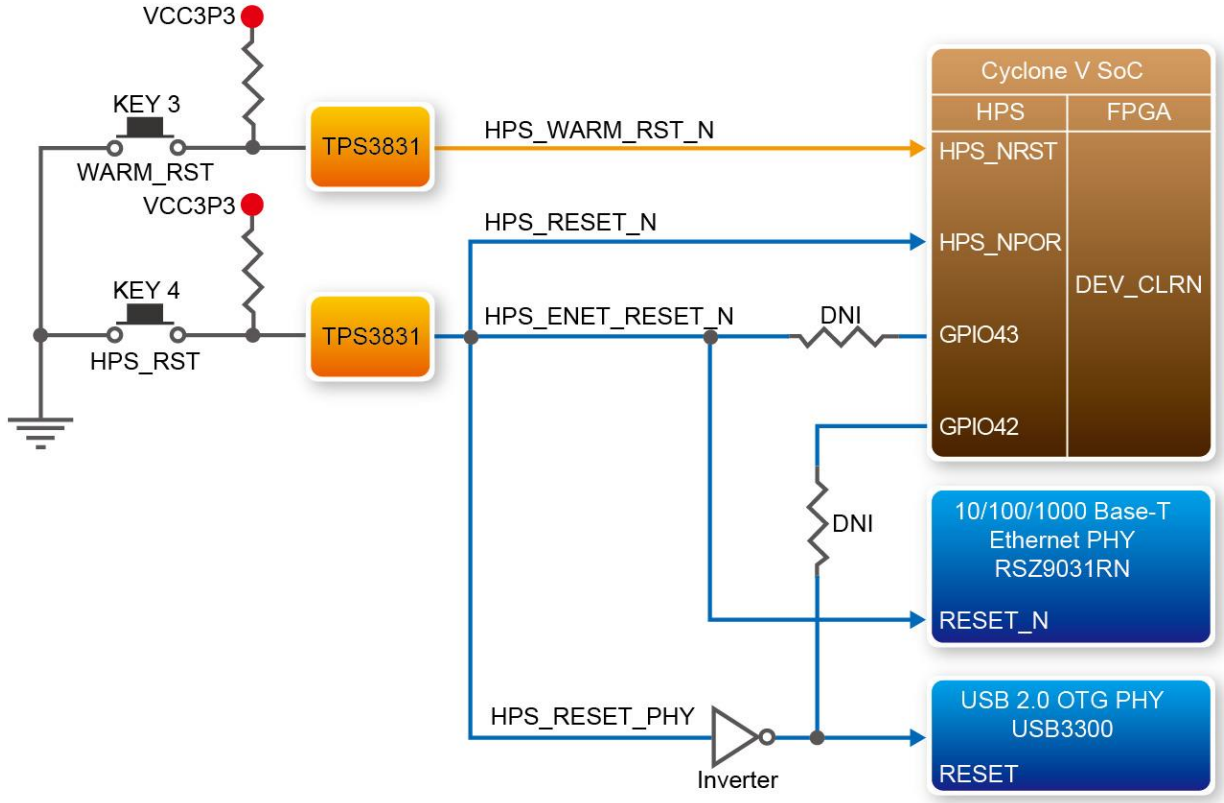

Figure 3-12 HPS reset tree on DE0-Nano-SoC board

3.5 Clock Circuitry

Figure 3-13 shows the default frequency of all external clocks to the Cyclone V SoC FPGA. A clock generator is used to distribute clock signals with low jitter. The two 50MHz clock signals connected to the FPGA are used as clock sources for user logic. Three 25MHz clock signal are connected to two HPS clock inputs, and the other one is connected to the clock input of Gigabit Ethernet Transceiver. One 24MHz clock signal is connected to the USB controller for USB Blaster II circuit and FPGA. One 24MHz clock signals are connected to the clock inputs of USB OTG PHY. The associated pin assignment for clock inputs to FPGA I/O pins is listed in Table 3-5.

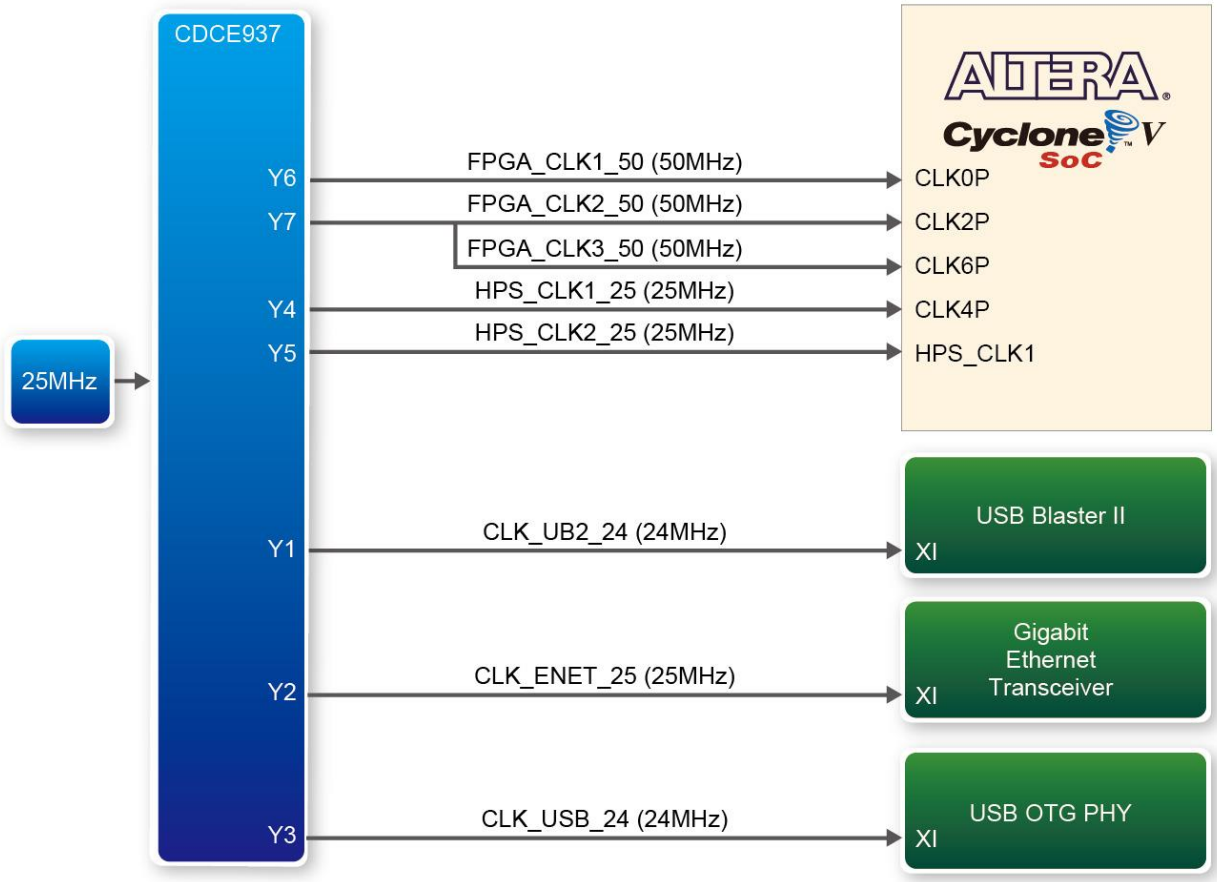

Figure 3-13 Block diagram of the clock distribution on DE0-Nano-SoC

Table 3-5 Pin Assignment of Clock Inputs

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
FPGA_CLK1_50	PIN_V11	50 MHz clock input	3.3V
FPGA_CLK2_50	PIN_Y13	50 MHz clock input	3.3V
FPGA_CLK3_50	PIN_E11	50 MHz clock input (share with FPGA_CLK1_50)	3.3V
HPS_CLK1_25	PIN_E20	25 MHz clock input	3.3V
HPS_CLK2_25	PIN_D20	25 MHz clock input	3.3V

3.6 Peripherals Connected to the FPGA

This section describes the interfaces connected to the FPGA. Users can control or monitor different interfaces with user logic from the FPGA.

3.6.1 User Push-buttons, Switches and LEDs

The board has two push-buttons connected to the FPGA, as shown in Figure 3-14 Connections between the push-buttons and the Cyclone V SoC FPGA. Schmitt trigger circuit is implemented and act as switch debounce in Figure 3-15 for the push-buttons connected. The two push-buttons named KEY0 and KEY1 coming out of the Schmitt trigger device are connected directly to the Cyclone V SoC FPGA. The push-button generates a low logic level or high logic level when it is pressed or not, respectively. Since the push-buttons are debounced, they can be used as clock or reset inputs in a circuit.

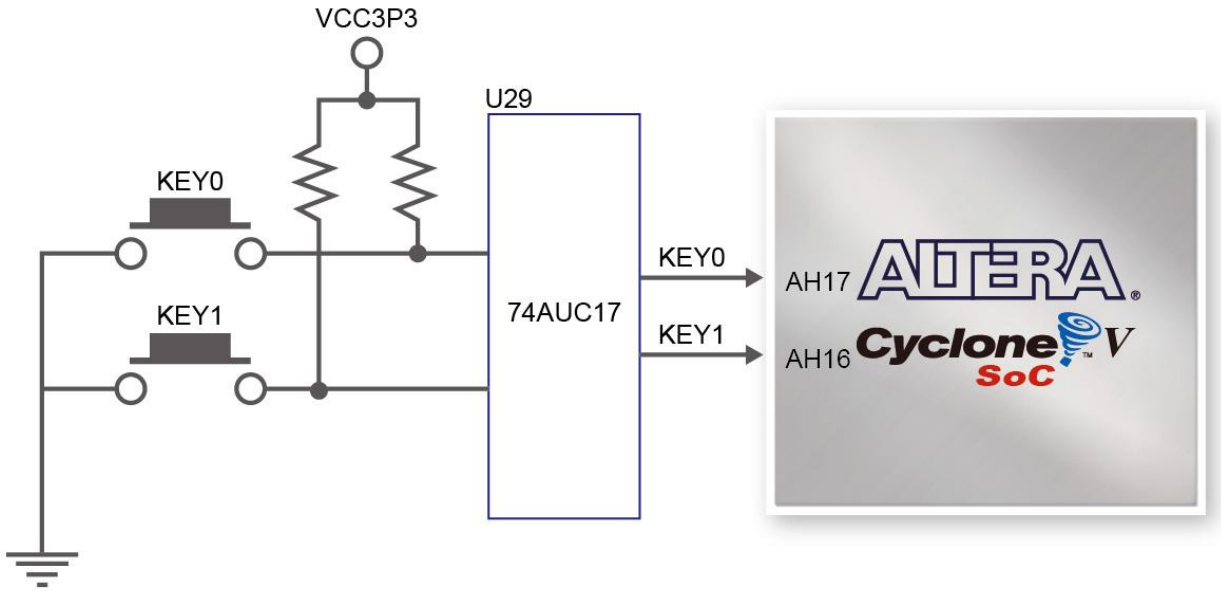

Figure 3-14 Connections between the push-buttons and the Cyclone V SoC FPGA

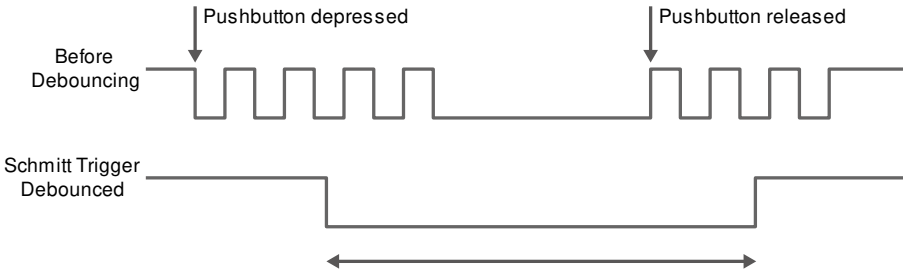

Figure 3-15 Switch debouncing

There are four slide switches connected to the FPGA, as shown in Figure 3-16. These switches are

not debounced and to be used as level-sensitive data inputs to a circuit. Each switch is connected directly and individually to the FPGA. When the switch is set to the DOWN position (towards the edge of the board), it generates a low logic level to the FPGA. When the switch is set to the UP position, a high logic level is generated to the FPGA.

Figure 3-16 Connections between the slide switches and the Cyclone V SoC FPGA

There are also eight user-controllable LEDs connected to the FPGA. Each LED is driven directly and individually by the Cyclone V SoC FPGA; driving its associated pin to a high logic level or low level to turn the LED on or off, respectively. **Figure 3-17** shows the connections between LEDs and Cyclone V SoC FPGA. **Table 3-6**, **Table 3-7** and **Table 3-8** list the pin assignment of user push-buttons, switches, and LEDs.