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DE2 Development and Education Board

User Manual

Version 1.5

CONTENTS

Chapter 1
DE2 Package

The DE2 package contains all components needed to use the DE2 board in conjunction with a computer that runs the Microsoft Windows software.

1.1 Package Contents

Figure 1.1 shows a photograph of the DE2 package.

Figure 1.1. The DE2 package contents.

The DE2 package includes:

- DE2 board
- USB Cable for FPGA programming and control
- CD-ROM containing the DE2 documentation and supporting materials, including the User Manual, the Control Panel utility, reference designs and demonstrations, device datasheets, tutorials, and a set of laboratory exercises
- CD-ROMs containing Altera's Quartus® II Web Edition and the Nios® II Embedded Design Suit Evaluation Edition software.
- Bag of six rubber (silicon) covers for the DE2 board stands. The bag also contains some extender pins, which can be used to facilitate easier probing with testing equipment of the board's I/O expansion headers
- Clear plastic cover for the board
- 9V DC wall-mount power supply

1.2 The DE2 Board Assembly

To assemble the included stands for the DE2 board:

- Assemble a rubber (silicon) cover, as shown in Figure 1.2, for each of the six copper stands on the DE2 board
- The clear plastic cover provides extra protection, and is mounted over the top of the board by using additional stands and screws

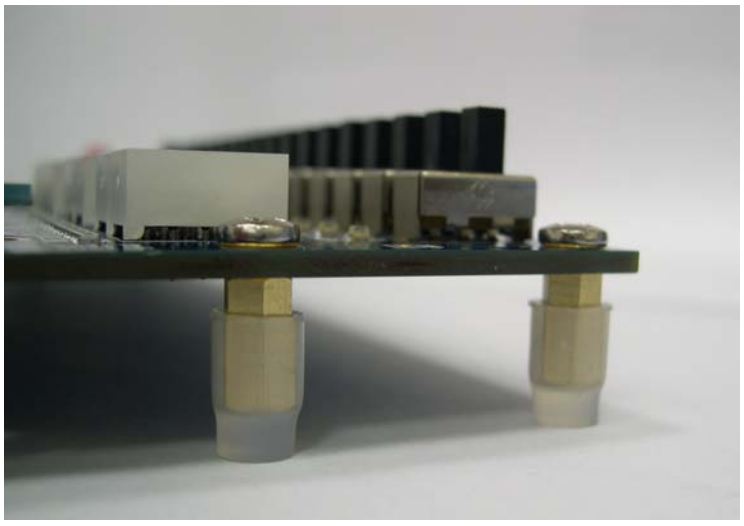

Figure 1.2. The feet for the DE2 board.

1.3 Getting Help

Here are the addresses where you can get help if you encounter problems:

- Altera Corporation
  101 Innovation Drive
  San Jose, California, 95134 USA
  Email: university@altera.com

- Terasic Technologies
  No. 356, Sec. 1, Fusing E. Rd.
  Jhubei City, HsinChu County, Taiwan, 302
  Email: support@terasic.com
  Web: DE2.terasic.com

- Arches Computing
  Unit 708-222 Spadina Ave
  Toronto, Ontario, Canada M5T3A2
  Email: DE2support@archescomputing.com
  Web: DE2.archescomputing.com

A BBS (Bulletin Board System) Forum for the DE2 board has been created at the address shown below. This Forum is meant to serve as a repository for information about the DE2 board, and to provide a resource through which users can ask questions, and share design examples.

- BBS forum: http://www.terasic.com/english/discuss.htm

Chapter 2
Altera DE2 Board

This chapter presents the features and design characteristics of the DE2 board.

2.1 Layout and Components

A photograph of the DE2 board is shown in Figure 2.1. It depicts the layout of the board and indicates the location of the connectors and key components.

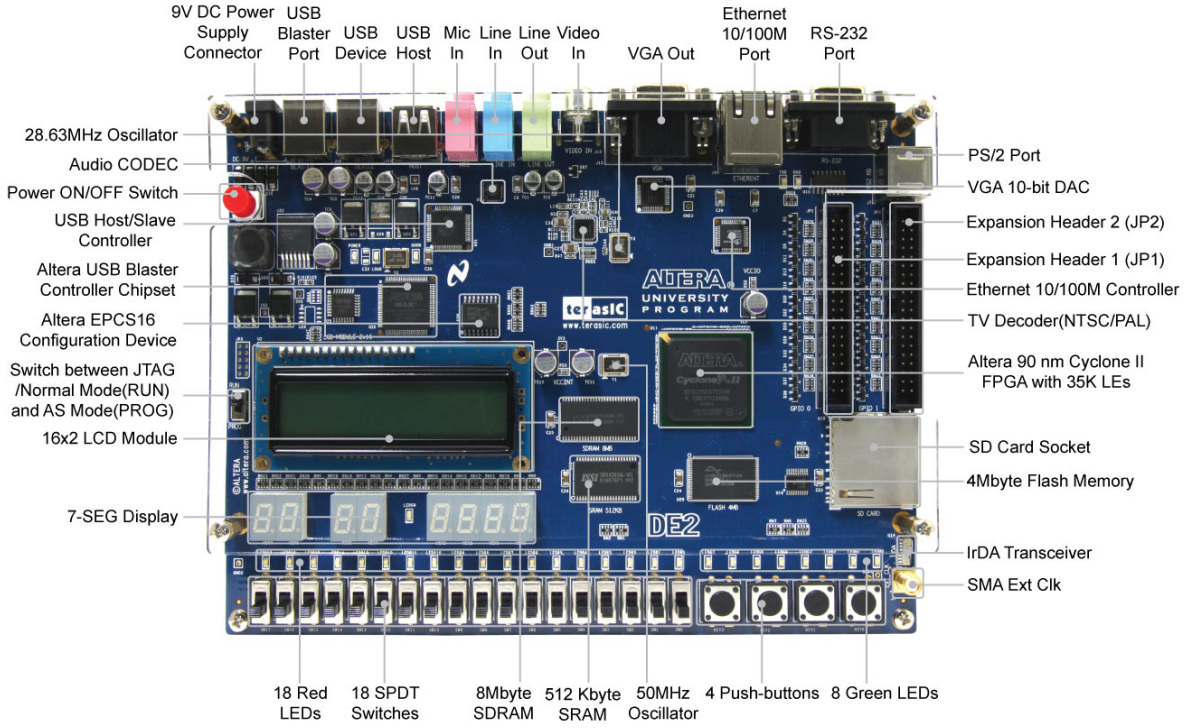

Figure 2.1. The DE2 board.

The DE2 board has many features that allow the user to implement a wide range of designed circuits, from simple circuits to various multimedia projects.

The following hardware is provided on the DE2 board:

- Altera Cyclone® II 2C35 FPGA device
- Altera Serial Configuration device - EPCS16
- USB Blaster (on board) for programming and user API control; both JTAG and Active Serial (AS) programming modes are supported

- 512-Kbyte SRAM
- 8-Mbyte SDRAM
- 4-Mbyte Flash memory (1 Mbyte on some boards)
- SD Card socket
- 4 pushbutton switches
- 18 toggle switches
- 18 red user LEDs
- 9 green user LEDs
- 50-MHz oscillator and 27-MHz oscillator for clock sources
- 24-bit CD-quality audio CODEC with line-in, line-out, and microphone-in jacks
- VGA DAC (10-bit high-speed triple DACs) with VGA-out connector
- TV Decoder (NTSC/PAL) and TV-in connector
- 10/100 Ethernet Controller with a connector
- USB Host/Slave Controller with USB type A and type B connectors
- RS-232 transceiver and 9-pin connector
- PS/2 mouse/keyboard connector
- IrDA transceiver
- Two 40-pin Expansion Headers with diode protection

In addition to these hardware features, the DE2 board has software support for standard I/O interfaces and a control panel facility for accessing various components. Also, software is provided for a number of demonstrations that illustrate the advanced capabilities of the DE2 board.

In order to use the DE2 board, the user has to be familiar with the Quartus II software. The necessary knowledge can be acquired by reading the tutorials *Getting Started with Altera's DE2 Board* and *Quartus II Introduction* (which exists in three versions based on the design entry method used, namely Verilog, VHDL or schematic entry). These tutorials are provided in the directory *DE2_tutorials* on the **DE2 System CD-ROM** that accompanies the DE2 board and can also be found on Altera's DE2 web pages.

2.2 Block Diagram of the DE2 Board

Figure 2.2 gives the block diagram of the DE2 board. To provide maximum flexibility for the user, all connections are made through the Cyclone II FPGA device. Thus, the user can configure the FPGA to implement any system design.

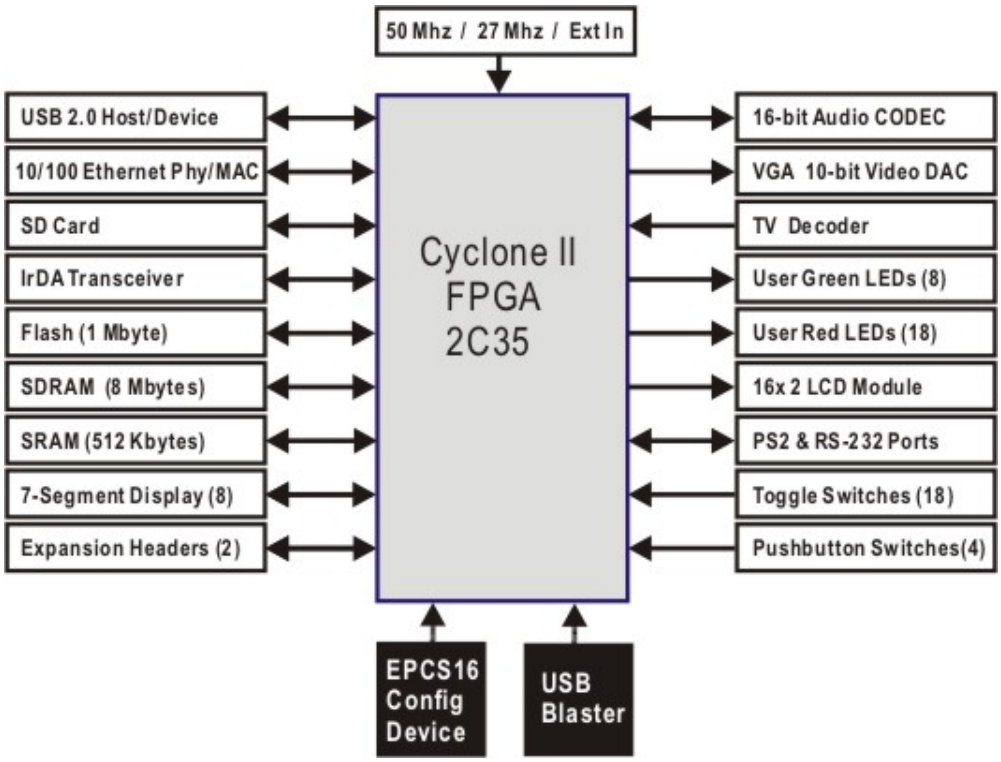

Figure 2.2. Block diagram of the DE2 board.

Following is more detailed information about the blocks in Figure 2.2:

Cyclone II 2C35 FPGA

- 33,216 LEs
- 105 M4K RAM blocks
- 483,840 total RAM bits
- 35 embedded multipliers
- 4 PLLs
- 475 user I/O pins
- FineLine BGA 672-pin package

Serial Configuration device and USB Blaster circuit

- Altera's EPCS16 Serial Configuration device
- On-board USB Blaster for programming and user API control
- JTAG and AS programming modes are supported

SRAM

- 512-Kbyte Static RAM memory chip
- Organized as 256K x 16 bits
- Accessible as memory for the Nios II processor and by the DE2 Control Panel

SDRAM

- 8-Mbyte Single Data Rate Synchronous Dynamic RAM memory chip
- Organized as 1M x 16 bits x 4 banks
- Accessible as memory for the Nios II processor and by the DE2 Control Panel

Flash memory

- 4-Mbyte NOR Flash memory (1 Mbyte on some boards)
- 8-bit data bus
- Accessible as memory for the Nios II processor and by the DE2 Control Panel

SD card socket

- Provides SPI and 4-bit SD mode for SD Card access
- Accessible as memory for the Nios II processor with the DE2 SD Card Driver

Pushbutton switches

- 4 pushbutton switches
- Debounced by a Schmitt trigger circuit
- Normally high; generates one active-low pulse when the switch is pressed

Toggle switches

- 18 toggle switches for user inputs
- A switch causes logic 0 when in the DOWN (closest to the edge of the DE2 board) position and logic 1 when in the UP position

Clock inputs

- 50-MHz oscillator
- 27-MHz oscillator
- SMA external clock input

Audio CODEC

- Wolfson WM8731 24-bit sigma-delta audio CODEC
- Line-level input, line-level output, and microphone input jacks
- Sampling frequency: 8 to 96 KHz
- Applications for MP3 players and recorders, PDAs, smart phones, voice recorders, etc.

VGA output

- Uses the ADV7123 140-MHz triple 10-bit high-speed video DAC
- With 15-pin high-density D-sub connector
- Supports up to 1600 x 1200 at 100-Hz refresh rate
- Can be used with the Cyclone II FPGA to implement a high-performance TV Encoder

NTSC/PAL TV decoder circuit

- Uses ADV7180 Multi-format SDTV Video Decoder
- Supports worldwide NTSC/PAL/SECAM color demodulation
- One 10-bit ADC, 4X over-sampling for CVBS
- Supports Composite Video (CVBS) RCA jack input.
- Supports digital output formats (8-bit/16-bit): ITU-R BT.656 YCrCb 4:2:2 output + HS, VS, and FIELD
- Applications: DVD recorders, LCD TV, Set-top boxes, Digital TV, Portable video devices

10/100 Ethernet controller

- Integrated MAC and PHY with a general processor interface
- Supports 100Base-T and 10Base-T applications
- Supports full-duplex operation at 10 Mb/s and 100 Mb/s, with auto-MDIX
- Fully compliant with the IEEE 802.3u Specification
- Supports IP/TCP/UDP checksum generation and checking
- Supports back-pressure mode for half-duplex mode flow control

USB Host/Slave controller

- Complies fully with Universal Serial Bus Specification Rev. 2.0
- Supports data transfer at full-speed and low-speed
- Supports both USB host and device
- Two USB ports (one type A for a host and one type B for a device)
- Provides a high-speed parallel interface to most available processors; supports Nios II with a Terasic driver
- Supports Programmed I/O (PIO) and Direct Memory Access (DMA)

Serial ports

- One RS-232 port
- One PS/2 port
- DB-9 serial connector for the RS-232 port
- PS/2 connector for connecting a PS2 mouse or keyboard to the DE2 board

IrDA transceiver

- Contains a 115.2-kb/s infrared transceiver
- 32 mA LED drive current
- Integrated EMI shield
- IEC825-1 Class 1 eye safe
- Edge detection input

Two 40-pin expansion headers

- 72 Cyclone II I/O pins, as well as 8 power and ground lines, are brought out to two 40-pin expansion connectors
- 40-pin header is designed to accept a standard 40-pin ribbon cable used for IDE hard drives
- Diode and resistor protection is provided

2.3 Power-up the DE2 Board

The DE2 board comes with a preloaded configuration bit stream to demonstrate some features of the board. This bit stream also allows users to see quickly if the board is working properly. To power-up the board perform the following steps:

1. Connect the provided USB cable from the host computer to the USB Blaster connector on the DE2 board. For communication between the host and the DE2 board, it is necessary to install the Altera USB Blaster driver software. If this driver is not already installed on the host computer, it can be installed as explained in the tutorial *Getting Started with Altera's DE2 Board*. This tutorial is available on the **DE2 System CD-ROM** and from the Altera DE2 web pages.
2. Connect the 9V adapter to the DE2 board
3. Connect a VGA monitor to the VGA port on the DE2 board
4. Connect your headset to the Line-out audio port on the DE2 board
5. Turn the RUN/PROG switch on the left edge of the DE2 board to RUN position; the PROG position is used only for the AS Mode programming
6. Turn the power on by pressing the ON/OFF switch on the DE2 board

At this point you should observe the following:

- All user LEDs are flashing
- All 7-segment displays are cycling through the numbers 0 to F
- The LCD display shows **Welcome to the Altera DE2 Board**
- The VGA monitor displays the image shown in Figure 2.3.
- Set the toggle switch SW17 to the DOWN position; you should hear a 1-kHz sound
- Set the toggle switch SW17 to the UP position and connect the output of an audio player to the Line-in connector on the DE2 board; on your headset you should hear the music played from the audio player (MP3, PC, iPod, or the like)
- You can also connect a microphone to the Microphone-in connector on the DE2 board; your voice will be mixed with the music played from the audio player

Figure 2.3. The default VGA output pattern.

Chapter 3
DE2 Control Panel

The DE2 board comes with a Control Panel facility that allows a user to access various components on the board through a USB connection from a host computer. This chapter first presents some basic functions of the Control Panel, then describes its structure in block diagram form, and finally describes its capabilities.

3.1 Control Panel Setup

To run the Control Panel application, it is first necessary to configure a corresponding circuit in the Cyclone II FPGA. This is done by downloading the configuration file *DE2_USB_API.sof* into the FPGA. The downloading procedure is described in Section 4.1.

In addition to the *DE2_USB_API.sof* file, it is necessary to execute on the host computer the program *DE2_control_panel.exe*. Both of these files are available on the **DE2 System CD-ROM** that accompanies the DE2 board, in the directory *DE2_control_panel*. Of course, these files may already have been installed to some other location on your computer system.

To activate the Control Panel, perform the following steps:

1. Connect the supplied USB cable to the USB Blaster port, connect the 9V power supply, and turn the power switch ON
2. Set the RUN/PROG switch to the RUN position
3. Start the Quartus II software
4. Select **Tools > Programmer** to reach the window in Figure 3.1. Click on **Add File** and in the pop-up window that appears select the *DE2_USB_API.sof* file. Next, click on the **Program/Configure** box which results in the image displayed in the figure. Now, click **Start** to download the configuration file into the FPGA.
5. Start the executable *DE2_control_panel.exe* on the host computer. The Control Panel user interface shown in Figure 3.2 will appear.
6. Open the USB port by clicking **Open > Open USB Port 0**. The DE2 Control Panel application will list all the USB ports that connect to DE2 boards. The DE2 Control Panel can control up to 4 DE2 boards using the USB links. The Control Panel will occupy the USB port until you close that port; you cannot use Quartus II to download a configuration file into the FPGA until you close the USB port.

7. The Control Panel is now ready for use; experiment by setting the value of some 7-segment display and observing the result on the DE2 board.

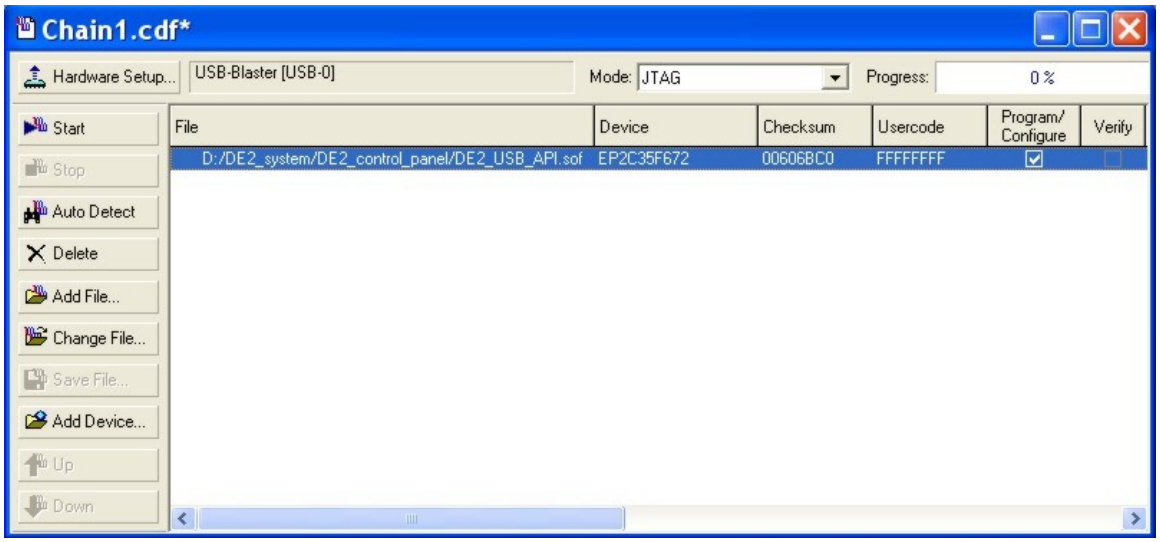

Figure 3.1. Quartus II Programmer window.

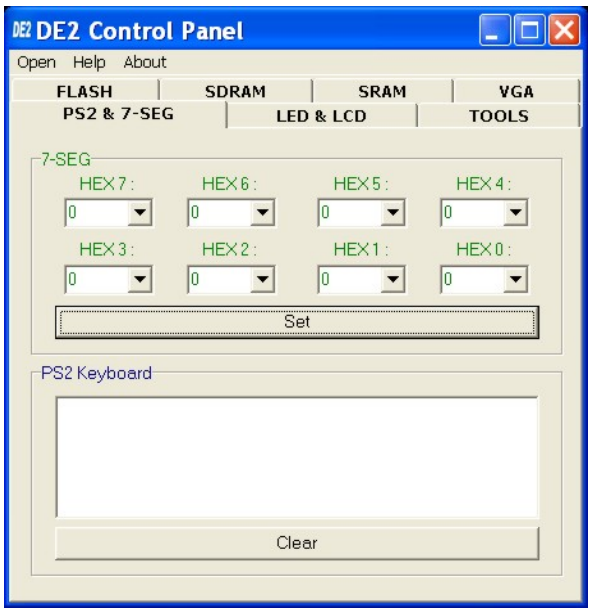

Figure 3.2. The DE2 Control Panel.

The concept of the DE2 Control Panel is illustrated in Figure 3.3. The IP that performs the control functions is implemented in the FPGA device. It communicates with the Control Panel window, which is active on the host computer, via the USB Blaster link. The graphical interface is used to issue commands to the control circuitry. The provided IP handles all requests and performs data transfers between the computer and the DE2 board.

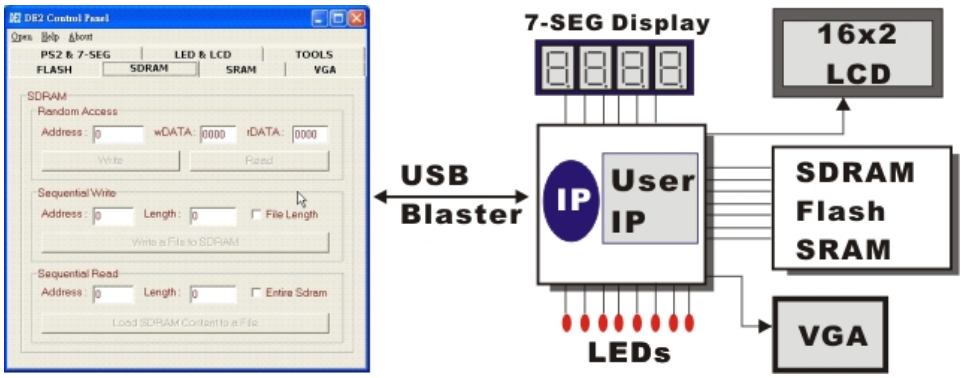

Figure 3.3. The DE2 Control Panel concept.

The DE2 Control Panel can be used to change the values displayed on 7-segment displays, light up LEDs, talk to the PS/2 keyboard, read/write the SRAM, Flash Memory and SDRAM, load an image pattern to display as VGA output, load music to the memory and play music via the audio DAC. The feature of reading/writing a byte or an entire file from/to the Flash Memory allows the user to develop multimedia applications (Flash Audio Player, Flash Picture Viewer) without worrying about how to build a Flash Memory Programmer.

3.2 Controlling the LEDs, 7-Segment Displays and LCD Display

A simple function of the Control Panel is to allow setting the values displayed on LEDs, 7-segment displays, and the LCD character display.

In the window shown in Figure 3.2, the values to be displayed by the 7-segment displays (which are named *HEX*7-0) can be entered into the corresponding boxes and displayed by pressing the **Set** button. A keyboard connected to the PS/2 port can be used to type text that will be displayed on the LCD display.

Choosing the **LED & LCD** tab leads to the window in Figure 3.4. Here, you can turn the individual LEDs on by selecting them and pressing the **Set** button. Text can be written to the LCD display by typing it in the LCD box and pressing the corresponding **Set** button.

The ability to set arbitrary values into simple display devices is not needed in typical design activities. However, it gives the user a simple mechanism for verifying that these devices are functioning correctly in case a malfunction is suspected. Thus, it can be used for troubleshooting purposes.

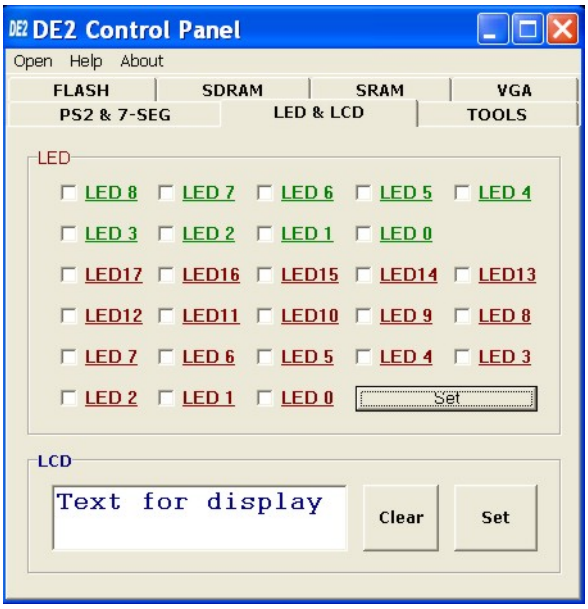

Figure 3.4. Controlling LEDs and the LCD display.

3.3 SDRAM/SRAM Controller and Programmer

The Control Panel can be used to write/read data to/from the SDRAM and SRAM chips on the DE2 board. We will describe how the SDRAM may be accessed; the same approach is used to access the SRAM. Click on the SDRAM tab to reach the window in Figure 3.5.

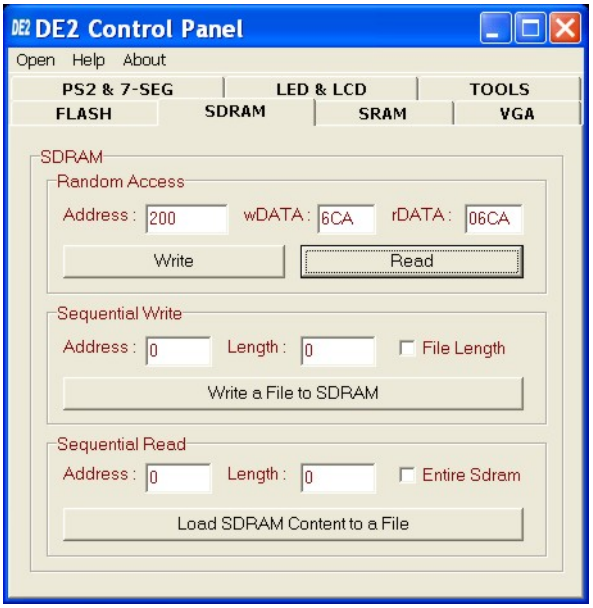

Figure 3.5. Accessing the SDRAM.

A 16-bit word can be written into the SDRAM by entering the address of the desired location, specifying the data to be written, and pressing the **Write** button. Contents of the location can be read by pressing the **Read** button. Figure 3.5 depicts the result of writing the hexadecimal value 6CA into location 200, followed by reading the same location.

The Sequential Write function of the Control Panel is used to write the contents of a file into the SDRAM as follows:

1. Specify the starting address in the **Address** box.
2. Specify the number of bytes to be written in the **Length** box. If the entire file is to be loaded, then a checkmark may be placed in the **File Length** box instead of giving the number of bytes.
3. To initiate the writing of data, click on the **Write a File to SDRAM** button.
4. When the Control Panel responds with the standard Windows dialog box asking for the source file, specify the desired file in the usual manner.

The Control Panel also supports loading files with a *.hex* extension. Files with a *.hex* extension are ASCII text files that specify memory values using ASCII characters to represent hexadecimal values. For example, a file containing the line

0123456789ABCDEF

defines four 16-bit values: 0123, 4567, 89AB, CDEF. These values will be loaded consecutively into the memory.

The Sequential Read function is used to read the contents of the SDRAM and place them into a file as follows:

1. Specify the starting address in the **Address** box.
2. Specify the number of bytes to be copied into the file in the **Length** box. If the entire contents of the SDRAM are to be copied (which involves all 8 Mbytes), then place a checkmark in the **Entire SDRAM** box.
3. Press **Load SDRAM Content to a File** button.
4. When the Control Panel responds with the standard Windows dialog box asking for the destination file, specify the desired file in the usual manner.

3.4 Flash Memory Programmer

The Control Panel can be used to write/read data to/from the Flash memory chip on the DE2 board. It can be used to:

- Erase the entire Flash memory
- Write one byte to the memory
- Read one byte from the memory
- Write a binary file to the memory
- Load the contents of the Flash memory into a file

Note the following characteristics of the Flash memory:

- The Flash memory chip is organized as 4 M (or 1 M on some boards) x 8 bits.
- You must erase the entire Flash memory before you can write into it. (Be aware that the number of times a Flash memory can be erased is limited.)
- The time required to erase the entire Flash memory is about 20 seconds. Do not close the DE2 Control Panel in the middle of the operation.

To open the Flash memory control window, shown in Figure 3.6, select the FLASH tab in the Control Panel.

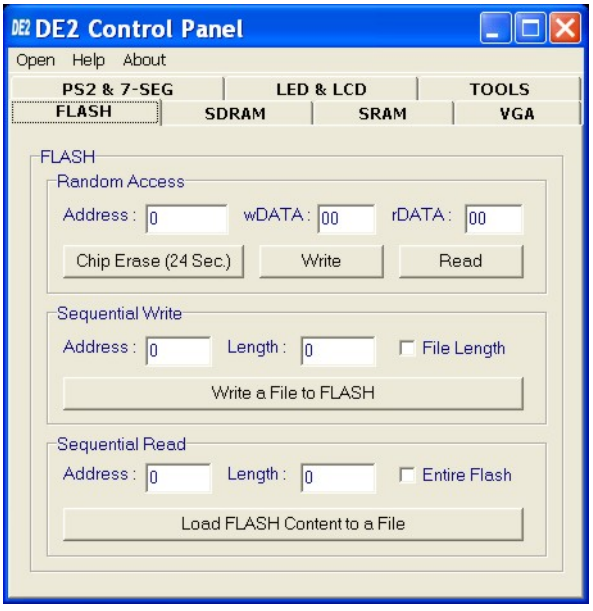

Figure 3.6. Flash memory control window.

A byte of data can be written into a random location on the Flash chip as follows:

1. Click on the **Chip Erase** button. The button and the window frame title will prompt you to wait until the operation is finished, which takes about 20 seconds.

2. Enter the desired address into the **Address** box and the data byte into the **wDATA** box. Then, click on the **Write** button.

To read a byte of data from a random location, enter the address of the location and click on the **Read** button. The **rDATA** box will display the data read back from the address specified.

The Sequential Write function is used to load a file into the Flash chip as follows:

1. Specify the starting address and the length of data (in bytes) to be written into the Flash memory. You can click on the **File Length** checkbox to indicate that you want to load the entire file.
2. Click on the **Write a File to Flash** button to activate the writing process.
3. When the Control Panel responds with the standard Windows dialog box asking for the source file, specify the desired file in the usual manner.

The Sequential Read function is used to read the data stored in the Flash memory and write this data into a file as follows:

1. Specify the starting address and the length of data (in bytes) to be read from the Flash memory. You can click on the **Entire Flash** checkbox to indicate that you want to copy the entire contents of the Flash memory into a specified file.
2. Click on the **Load Flash Content to a File** button to activate the reading process.
3. When the Control Panel responds with the standard Windows dialog box asking for the destination file, specify the desired file in the usual manner.

3.5 Overall Structure of the DE2 Control Panel

The DE2 Control Panel facility communicates with a circuit that is instantiated in the Cyclone II FPGA. This circuit is specified in Verilog code, which makes it possible for a knowledgeable user to change the functionality of the Control Panel. The code is located inside the *DE2_demonstrations* directory on the **DE2 System CD-ROM**.

To run the Control Panel, the user must first set it up as explained in Section 3.1. Figure 3.7 depicts the structure of the Control Panel. Each input/output device is controlled by a controller instantiated in the FPGA chip. The communication with the PC is done via the USB Blaster link. A Command Controller circuit interprets the commands received from the PC and performs the appropriate actions. The SDRAM, SRAM, and Flash Memory controllers have three user-selectable asynchronous ports in addition to the Host port that provides a link with the Command Controller. The connection between the VGA DAC Controller and the FPGA memory allows displaying of the default image shown on the left side of the figure, which is stored in an M4K block in the Cyclone

II chip. The connection between the Audio DAC Controller and a lookup table in the FPGA is used to produce a test audio signal of 1 kHz.

To let users implement and test their IP cores (written in Verilog) without requiring them to implement complex API/Host control software and memory (SRAM/SDRAM/Flash) controllers, we provide an integrated control environment consisting of a software controller in C++, a USB command controller, and a multi-port SRAM/SDRAM/Flash controller.

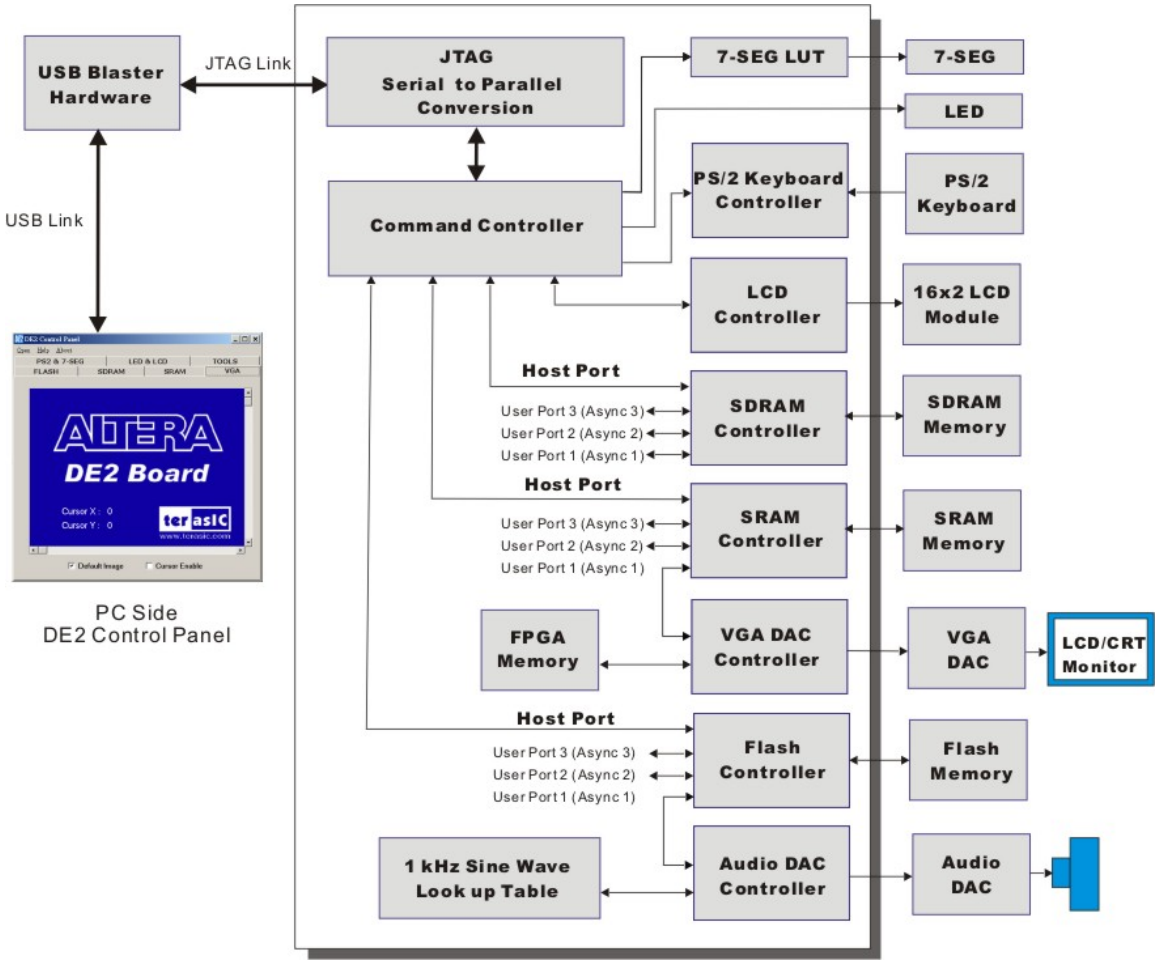

Figure 3.7. The DE2 Control Panel block diagram.

Users can connect circuits of their own design to one of the User Ports of the SRAM/SDRAM/Flash controller. Then, they can download binary data into the SRAM/SDRAM/Flash. Once the data is downloaded to the SDRAM/Flash, users can configure the memory controllers so that their circuits can read/write the SDRAM/Flash via the User Ports connected.

3.6 TOOLS – Multi-Port SRAM/SDRAM/Flash Controller

The TOOLS page of the Control Panel GUI allows selection of the User Ports. We will illustrate a typical process by implementing a Flash Music Player. The music data is loaded into the Flash memory. User Port 1 in the Flash Controller is used to send the music data to the Audio DAC Controller and hence to the audio output jack.

You can implement this application as follows:

1. Erase the Flash memory (as explained in Section 3.4). Then, write a music file into the Flash memory. You can use the file *music.wav* in the directory *DE2_demonstrations\music* on the **DE2 System CD-ROM**.
2. In the DE2 Control Panel, select the TOOLS tab to reach the window in Figure 3.8.

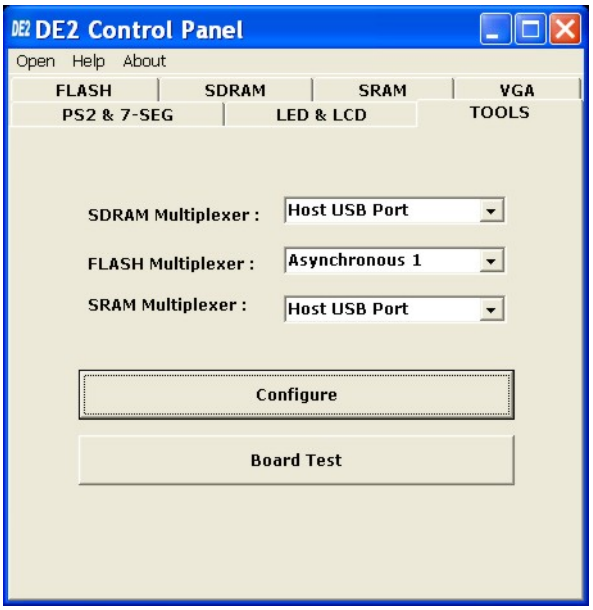

Figure 3.8. TOOLS window of the DE2 Control Panel.

3. Select the Asynchronous 1 port for the Flash Multiplexer and then click on the **Configure** button to activate the port. You need to click the Configure button to enable the connection from the Flash Memory to the Asynchronous Port 1 of the Flash Controller (indicated in Figure 3.7).
4. Set toggle switches SW1 and SW0 to OFF (DOWN position) and ON (UP position), respectively.
5. Plug your headset or a speaker into the audio output jack and you should hear the music played from the Audio DAC circuit.
6. Note that the Asynchronous Port 1 is connected to the Audio DAC part, as shown in Figure 3.7. Once you selected Asynchronous Port 1 and clicked the Configure button, the Audio DAC Controller will communicate with the Flash memory directly. In our example, the

AUDIO_DAC Verilog module defines a circuit that reads the contents of the Flash memory and sends it to the external audio chip.

3.7 VGA Display Control

The Control Panel provides a tool with the associated IP that allows the user to display an image via the VGA output port. To illustrate this feature, we will show how an image can be displayed on a VGA monitor. Perform the following steps to display a default image:

- Select the VGA tab in the Control Panel to reach the window in Figure 3.9.

Figure 3.9. Displayed image and the cursor controlled by the scroll bars

- Make sure that the checkboxes **Default Image** and **Cursor Enable** are checked.
- Connect a VGA monitor to the DE2 board and you should see on the screen the default image shown in Figure 3.9. The image includes a cursor which can be controlled by means of the X/Y-axes scroll bars on the DE2 Control Panel.

The image in Figure 3.9 is stored in an M4K memory block in the Cyclone II FPGA. It is loaded into the M4K block in the MIF/Hex(Intel) format during the default bit stream configuration stage. We will next describe how you can display other images and use your own images to generate the binary data patterns that can be displayed on the VGA monitor.

Another image is provided in the file *picture.dat* in the folder *DE2_demonstrations\pictures* on the **DE2 System CD-ROM**. You can display this image as follows:

- Select the **SRAM** page of the Control Panel and load the file *picture.dat* into the SRAM.

- Select the **TOOLS** page and choose **Asynchronous 1** for the **SRAM multiplexer** port as shown in Figure 3.10. Click on the **Configure** button to activate the multi-port setup.

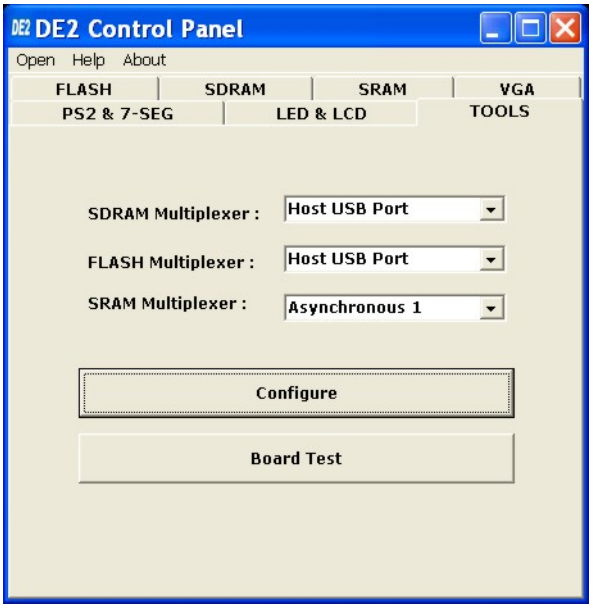

Figure 3.10. Use the Asynchronous Port 1 to access the image data in the SRAM.

- The FPGA is now configured as indicated in Figure 3.11.
- Select the **VGA** page and deselect the checkbox **Default Image**.
- The VGA monitor should display the *picture.dat* image from the SRAM, as depicted in Figure 3.12. You can turn off the cursor by deselecting the **Cursor Enable** checkbox.

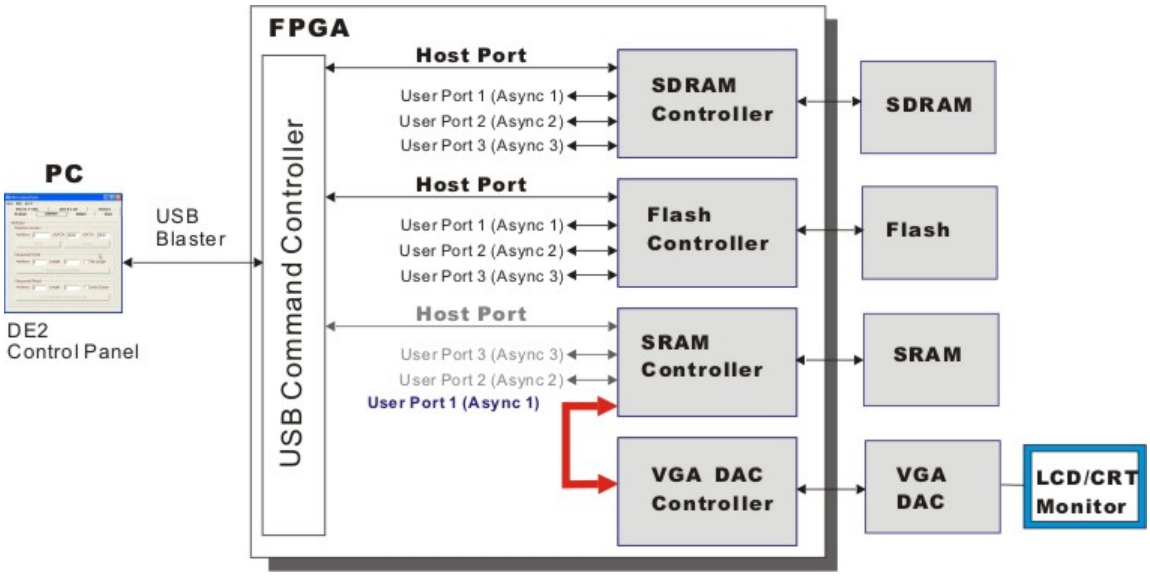

Figure 3.11. Multi-Port Controller configured to display an image from the SRAM.

Figure 3.12. A displayed image.

You can display any image file by loading it into the SRAM chip or into an M4K memory block in the Cyclone II chip. This requires generating a bitmap file, which may be done as follows:

1. Load the desired image into an image processing tool, such as Corel PhotoPaint.
2. Resample the original image to have a 640 x 480 resolution. Save the modified image in the Windows Bitmap format.
3. Execute *DE2_control_panel\ImgConv.exe*, an image conversion tool developed for the DE2 board, to reach the window in Figure 3.13.
4. Click on the **Open Bitmap** button and select the 640 x 480 Grayscale photo for conversion.
5. When the processing of the file is completed, click on the **Save Raw Data** button and a file named *Raw_Data_Gray.dat* will be generated and stored in the same directory as the original image file. You can change the file name prefix from *Raw_Data* to another name by changing the File Name field in the displayed window.
6. *Raw_Data_Gray.dat* is the raw data that can be downloaded directly into the SRAM on the DE2 board and displayed on the VGA monitor using the VGA controller IP described in the *DE2_USB_API* project.
7. The *ImgConv* tool will also generate *Raw_Data_BW.dat* (and its corresponding TXT format) for the black and white version of the image – the threshold for judging black or white level is defined in the BW Threshold.