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TRDB_LTM

4.3 Inch Digital Touch Panel Development Kit

With complete reference design and source code for digital photo display
and pattern generator using Altera DE2/ DE1 board

Document Version 1.22 9 NOV, 2007 by Terasic

Preliminary Version

Page Index

Chapter 1

About the Kit

The TRDB_LTM (LTM) Kit provides everything you need to develop applications using a digital touch panel on an Altera DE2/DE1 board. The kit contains complete reference designs and source code for implementing a photo viewer demonstration and a color pattern generator using the LTM kit and an Altera DE2/DE1 board. This chapter provides users key information about the kit.

1-1 Kit Contents

Figure 1.1 shows the picture of the TRDB_LTM package. The package includes:

1. The Terasic **L**CD **T**ouch Panel **M**odule **(LTM)** board
2. A 40-pin IDE cable
3. Complete reference design with source code

Figure 1.1. The TRDB_LTM Package

1-2 Connecting LTM to the Altera DE Board

Please follow the two steps below to connect LTM to the Altera DE2/DE1 board:

1. Connect the IDE cable to the back of the LTM board, as shown in Figure 1.2
2. Connect the other end of the IDE cable to your DE2/DE1 board's innermost expansion port (JP1) as shown in Figure 1.3 and Figure 1.4

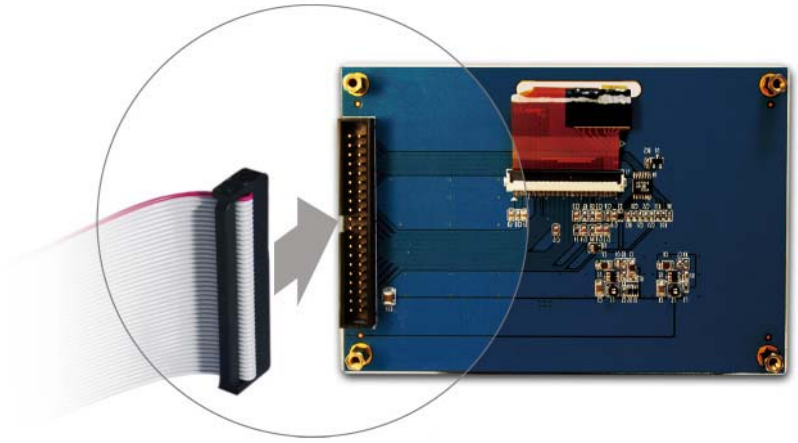

Figure 1.2 Connect the IDE cable to the TRDB_LTM board

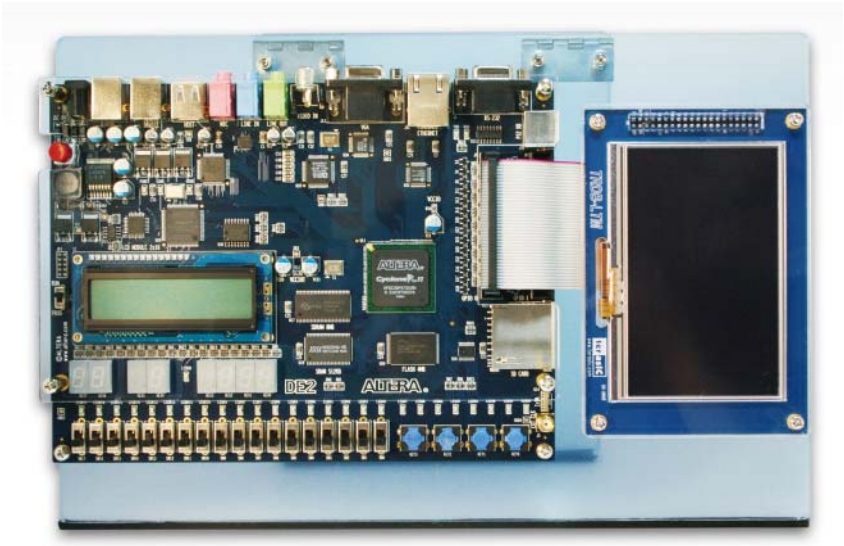

Figure 1.3 Connect the other end of IDE cable to the DE2 board's expansion port (innermost expansion port)

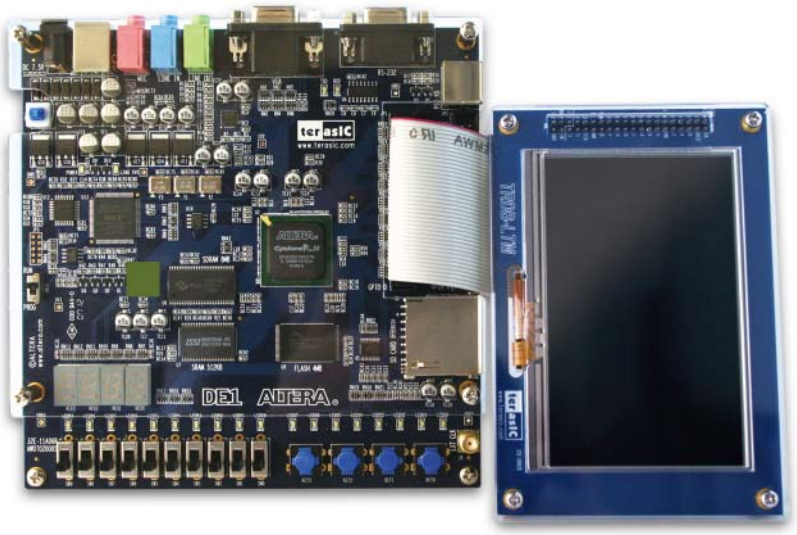

Figure 1.4 Connect the other end of IDE cable to the DE1 board's expansion port (innermost expansion port)

1-3 Getting Help

Here are some places to get help if you encounter any problem:

- ✓ Email to support@terasic.com
- ✓ Taiwan & China: +886-3-550-8800
- ✓ Korea : +82-2-512-7661
- ✓ Japan: +81-428-77-7000

Chapter

2 Architecture of the LTM

This chapter will illustrate the architecture of the LTM including device features and block diagram.

2-1 Features

The feature set of the LTM is listed below:

1. Equipped with Toppoly TD043MTEA1 active matrix color TFT LCD module.
2. Support 24-bit parallel RGB interface.
3. 3-wire register control for display and function selection.
4. Built-in contrast, brightness, and gamma modulation.
5. Converting the X/Y coordination of the touch point to its corresponding digital data via the Analog Devices AD7843 AD converter.
6. The general specifications of the LTM are listed below:

Item	Description	Unit
Display Size (Diagonal)	4.3	Inch
Aspect ratio	15:9	-
Display Type	Transmissive	-
Active Area (HxV)	93.6 x 56.16	mm
Number of Dots (HxV)	800 x RGB x480	dot
Dot Pitch (HxV)	0.039 x 0.117	mm
Color Arrangement	Stripe	-
Color Numbers	16Million	-

2-2 Block Diagram of the LTM

The block diagram of the LTM is listed below:

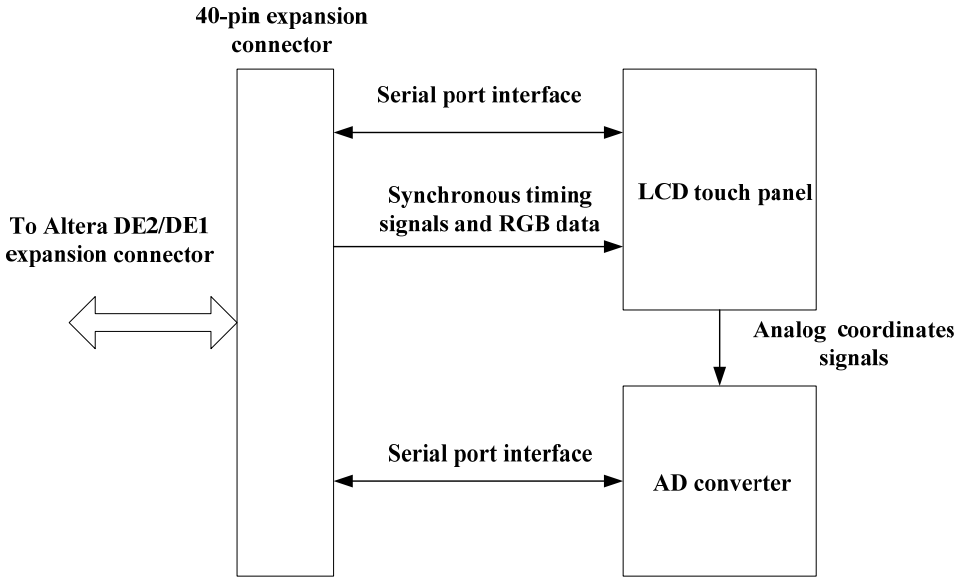

Figure 2.1 The block diagram of the LTM.

The LTM consists of three major components: LCD touch panel module, AD converter, and 40-pin expansion header. All of the interfaces on the LTM are connected to Altera DE2/DE1 board via the 40-pin expansion connector. The LCD and touch panel module will take the control signals provided directly from FPGA as input and display images on the LCD panel. Finally, the AD converter will convert the coordinates of the touch point to its corresponding digital data and output to the FPGA via the expansion header.

2-3 Pin Description of the 40-pin Interface of LTM

The pin description of the 40-pin connector follows:

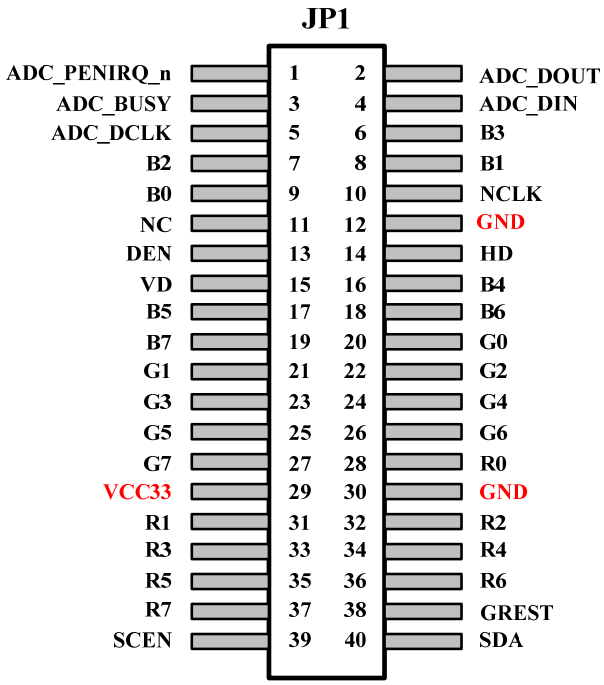

Figure 2.2 The pin-out of the 40-pin connector.

Pin Numbers	Name	Direction	Description
1	ADC_PENIRQ_n	output	ADC pen Interrupt
2	ADC_DOUT	output	ADC serial interface data out
3	ADC_BUSY	output	ADC serial interface busy
4	ADC_DIN	input	ADC serial interface data in
5	ADC_DCLK	input	ADC/LCD serial interface clock
6	B3	Input	LCD blue data bus bit 3
7	B2	Input	LCD blue data bus bit 2
8	B1	Input	LCD blue data bus bit 1
9	B0	Input	LCD blue data bus bit 0
10	NCLK	Input	LCD clock signal
11	NC	N/A	N/A
12	GND	N/A	Ground
13	DEN	Input	LCD RGB data enable
14	HD	Input	LCD Horizontal sync input
15	VD	Input	LCD Vertical sync input
16	B4	Input	LCD blue data bus bit 4
17	B5	Input	LCD blue data bus bit 5
18	B6	Input	LCD blue data bus bit 6
19	B7	Input	LCD blue data bus bit 7
20	G0	Input	LCD green data bus bit 0
21	G1	Input	LCD green data bus bit 1
22	G2	Input	LCD green data bus bit 2
23	G3	Input	LCD green data bus bit 3

24	G4	Input	LCD green data bus bit 4
25	G5	Input	LCD green data bus bit 5
26	G6	Input	LCD green data bus bit 6
27	G7	Input	LCD green data bus bit 7
28	R0	Input	LCD red data bus bit 0
29	VCC33	N/A	Power 3.3V
30	GND	N/A	Ground
31	R1	Input	LCD red data bus bit 1
32	R2	Input	LCD red data bus bit 2
33	R3	Input	LCD red data bus bit 3
34	R4	Input	LCD red data bus bit 4
35	R5	Input	LCD red data bus bit 5
36	R6	Input	LCD red data bus bit 6
37	R7	Input	LCD red data bus bit 7
38	GREST	Input	Global reset, low active
39	SCEN	Input	3-wire serial interface enable
40	SDA	Input/Output	3-wire serial interface data

Table 2.1 The pin description of the 40-pin connector.

Chapter

3

Using the LTM

This chapter illustrates how to use the LTM including how to control the serial port interface of the LCD driver IC and AD converter. Also, the timing requirement of the synchronous signal and RGB data which are outputted to the LCD panel module will be described.

3-1 The Serial Port Interface of the LCD Driver IC

This section will describe how to control the register value of the LCD driver IC on the LTM.

The LCD and touch panel module on the LTM is equipped with a LCD driver IC to support three display resolution and with functions of source driver, serial port interface, timing controller, and power supply circuits. To control these functions, users can use FPGA to configure the registers in the LCD driver IC via serial port interface.

Also, there is an analog to digital converter (ADC) on the LTM to convert the analog X/Y coordinates of the touch point to digital data and output to FPGA through the serial port interface of the ADC. Both LCD driver IC and ADC serial port interfaces are connected to the FPGA via the 40-pin expansion header and IDE cable.

Because of the limited number of I/O on the expansion header, the serial interfaces of the LCD driver IC and ADC need to share the same clock (ADC_DCLK) and chip enable (SCEN) signal I/O on the expansion header. To avoid both the serial port interfaces may interfere with each other when sharing the same clock and chip enable signals, the chip enable signal (CS), which is inputted into the ADC will come up with a logic inverter. Users need to pay attention controlling the shared signals when designing the serial port interface controller. The detailed register maps of the LCD driver IC are listed in appendix chapter. The specifications of the serial port interface of the LCD driver IC are described below.

The LCD driver IC supports a clock synchronous serial interface as the interface to a FPGA to enable instruction setting. Please notice that in addition to the serial port interface signals, NCLK input should also be provided while setting the registers. Figure 3.1 and Table 3.1 show the frame format and timing diagram of the serial port interface. The LCD driver IC recognizes the start of data

transfer on the falling edge of SCEN input and starts data transfer. When setting instruction, the TPG110 inputs the setting values via SDA on the rising edge of input SCL.

The first 6 bits (A5 ~ A0) specify the address of the register. The next bit means Read/Write command. “0” is write command. “1” is read command. Then, the next cycle is turn-round cycle. Finally, the last 8 bits are for Data setting (D7 ~ D0). The address and data are transferred from the MSB to LSB sequentially. The data is written to the register of assigned address when “End of transfer” is detected after the 16th SCL rising cycles. Data is not accepted if there are less or more than 16 cycles for one transaction.

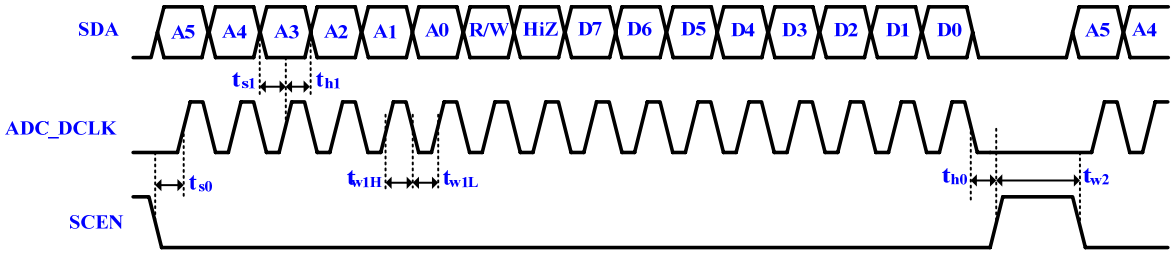

Figure 3.1 the frame format and timing diagram of the serial port interface.

Item	Symbol	Conditions	Min.	Max.	Unit
SDA Setup Time	ts0	SCEN to SCL	150		ns
	ts1	SDA to SCL	150		ns
SDA Hold Time	th0	SCEN to SCL	150		ns
	th1	SDA to SCL	150		ns
Pulse Width	tw1L	SCL pulse width	160		ns
	tw1H	SCL pulse width	160		ns
	tw2	SCEN pulse width	1.0		ns
Clock duty			40	60	%

Table 3.1 The timing parameters of the serial port interface

3-2 Input timing of the LCD panel display function

This section will describe the timing specification of the LCD synchronous signals and RGB data.

To determine the sequencing and the timing of the image signals displayed on the LCD panel, the corresponding synchronous signals from FPGA to the LCD panel should follow the timing specification.

Figure 3.2 illustrates the basic timing requirements for each row (horizontal) that is displayed on the LCD panel. An active-low pulse of specific duration (time t_{hpw} in the figure) is applied to the horizontal synchronization (HD) input of the LCD panel, which signifies the end of one row of data and the start of the next. The data (RGB) inputs on the LCD panel are not valid for a time period called the hsync back porch (t_{hbp}) after the hsync pulse occurs, which is followed by the display area (t_{hd}). During the data display area the RGB data drives each pixel in turn across the row being displayed. Also, during the period of the data display area, the data enable signal (DEN) must be driven to logic high. Finally, there is a time period called the hsync front porch (t_{hfp}) where the RGB signals are not valid again before the next hsync pulse can occur.

The timing of the vertical synchronization (VD) is the same as shown in Figure 3.3, except that a vsync pulse signifies the end of one frame and the start of the next, and the data refers to the set of rows in the frame (horizontal timing). Table 3.2 and 3.3 show for different resolutions, the durations of time periods t_{hpw}, t_{hbp}, t_{hd}, and t_{hfp} for both horizontal and vertical timing. Finally, the timing specification of the synchronous signals is shown in the Table 3.4.

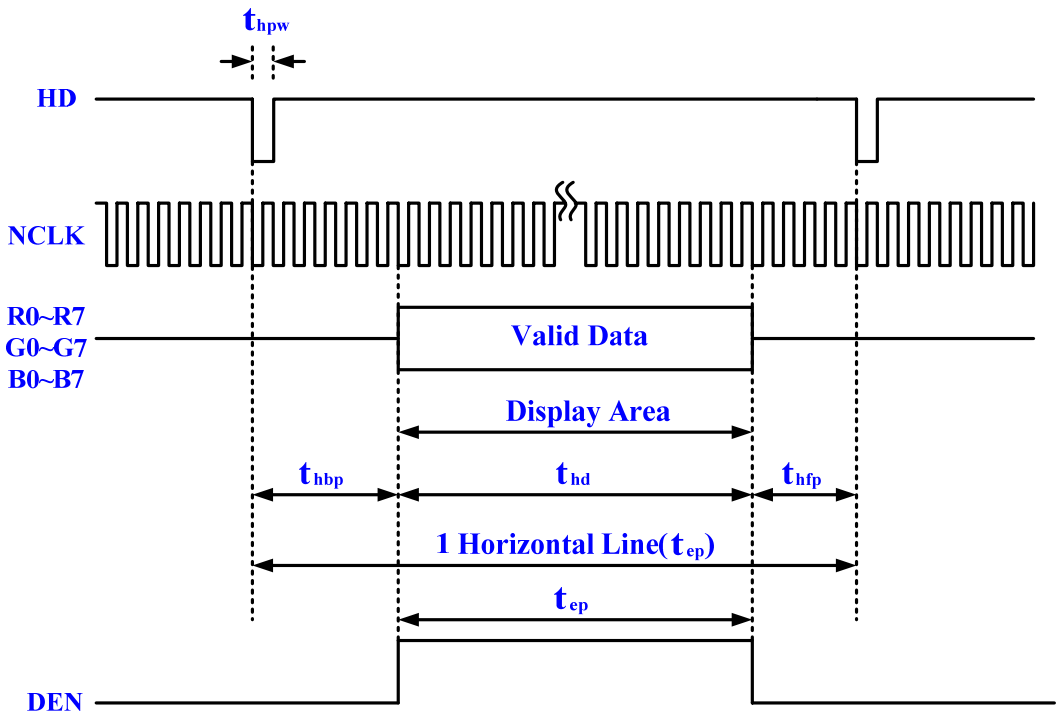

Figure 3.2 LCD horizontal timing specification

Parameter		Symbol	Panel Resolution			Unit
			800xRGBx480	480xRGBx272	400xRGBx240	
NCLK Frequency		FNCLK	33.2	9	8.3	MHz
Horizontal valid data		t_{hd}	800	480	400	NCLK
1 Horizontal Line		t_h	1056	525	528	NCLK
HSYNC Pulse Width	Min.	t_{hpw}	1			NCLK
	Typ.		-			
	Max.		-			
Hsync back porch		t_{hbp}	216	43	108	NCLK
Hsync front porch		t_{hfp}	40	2	20	NCLK
DEN Enable Time		t_{ep}	800	480	400	NCLK

Table 3.2 LCD horizontal timing parameters

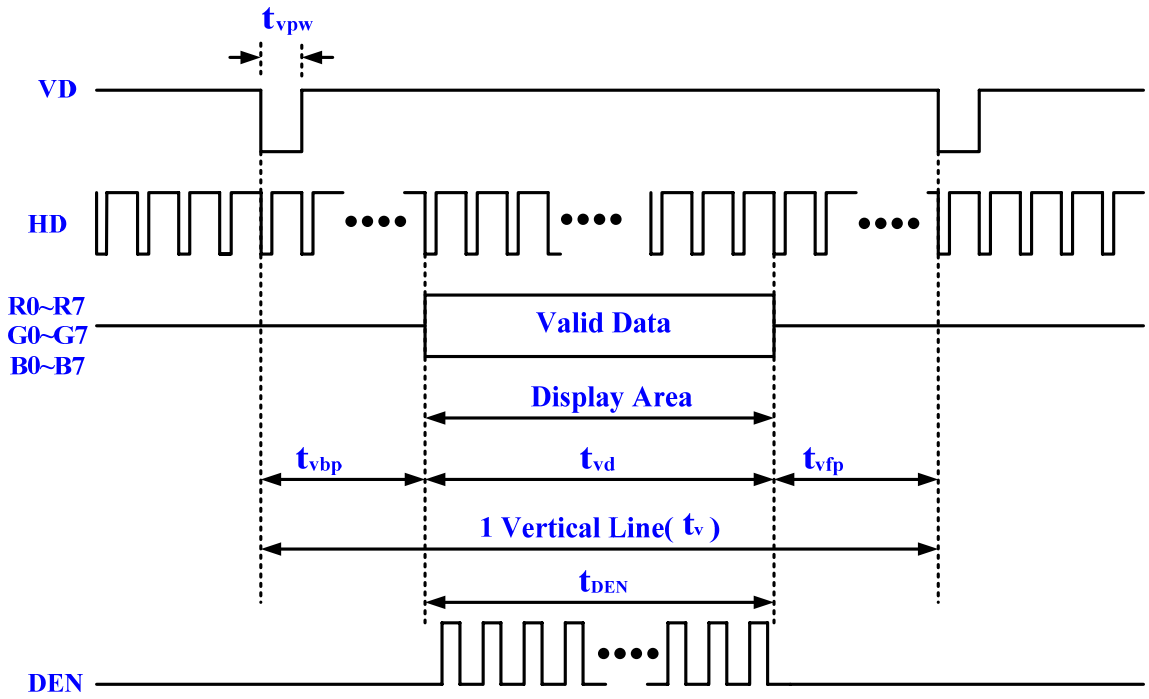

Figure 3.3 LCD vertical timing specification

Parameter		Symbol	Panel Resolution			Unit
			800xRGBx480	480xRGBx272	400xRGBx240	
Vertical valid data		t_{vd}	480	272	240	H
Vertical period		t_v	525	286	262	H
VSYNC Pulse Width	Min.	t_{vpw}	1			H
	Typ.		-			
	Max.		-			
Vertical back porch		t_{vbp}	35	12	20	H
Vertical front porch		t_{vfp}	10	2	2	H
Vertical blanking		t_{vb}	45	14	22	H
DEN Enable Time		T_{DEN}	480	272	240	H

Table 3.3 LCD vertical timing parameters

Parameter	Symbol	Min.	Unit
NCLK period	PW_{CLK*1}	25	ns
NCLK pulse high period	PWH_{*1}	10	ns
NCLK pulse low period	PWL_{*1}	10	ns
HD,VD, DEN, data setup time	t_{ds}	5	ns
HD,VD, DEN, data hold time	t_{dh}	5	ns

Table 3.4 The timing parameters of the LCD synchronous signals

3-3 The serial interface of the AD converter

This section will describe how to obtain the X/Y coordinates of the touch point from the AD converter.

The LTM also equipped with an Analog Devices AD7843 touch screen digitizer chip. The AD7843 is a 12-bit analog to digital converter (ADC) for digitizing x and y coordinates of touch points applied to the touch screen. The coordinates of the touch point stored in the AD7843 can be obtained by the serial port interface.

To obtain the coordinate from the ADC, the first thing users need to do is monitor the interrupt signal ADC_PENIRQ_n outputted from the ADC. By connecting a pull high resistor, the ADC_PENIRQ_n output remains high normally. When the touch screen connected to the ADC is touched via a pen or finger, the ADC_PENIRQ_n output goes low, initiating an interrupt to a FPGA that can then instruct a control word to be written to the ADC via the serial port interface.

The control word provided to the ADC via the DIN pin is shown in Table 3.5. This provides the conversion start, channel addressing, ADC conversion resolution, configuration, and power-down of the ADC. The detailed information on the order and description of these control bits can be found from the datasheet of the ADC in the *DATASHEET* folder on the LTM System CD-ROM.

MSB							LSB
S	A2	A1	A0	MODE	SER / $\overline{\text{DEF}}$	PD1	PD0

Bit	Mnemonic	Comment
7	S	Start Bit. The control word starts with the first high bit on DIN. A new control word can start every 15th DCLK cycle when in the 12-bit conversion mode, or every 11th DCLK cycle when in 8-bit conversion mode.
6-4	A2-A0	Channel Select Bits. These three address bits, along with the SER / $\overline{\text{DEF}}$ bit, control the setting of the multiplexer input, switches, and reference inputs.
3	MODE	12-Bit/8-Bit Conversion Select Bit. This bit controls the resolution of the following conversion. With 0 in this bit, the conversion has a 12-bit resolution, or with 1 in this bit, the conversion has a 8-bit resolution.
2	SER / $\overline{\text{DEF}}$	Single-Ended/Differential Reference Select Bit. Along with Bits A2– A0, this bit controls the setting of the multiplexer input, switches, and reference inputs.
1,0	PD1,PD0	Power Management Bits. These two bits decode the power-down mode of the AD7843.

Table 3.5 Control register bit function description.

Figure 3.4 shows the typical operation of the serial interface of the ADC. The serial clock provides the conversion clock and also controls the transfer of information to and from the ADC. One complete conversion can be achieved with 24 ADC_DCLK cycles. The detailed behavior of the serial port interface can be found in the datasheet of the ADC. Note that the clock (ADC_DCLK) and chip enable signals (SCEN) of the serial port interface SHRAE the same signal I/O with LCD driver IC. Users should avoid controlling the LCD driver IC and ADC at the same time when designing the serial port interface controller. Also, because the chip enable signal (SCEN) inputted to the ADC comes up with a logic inverter, the logic level of the SCEN should be inverse when it is used to control the ADC.

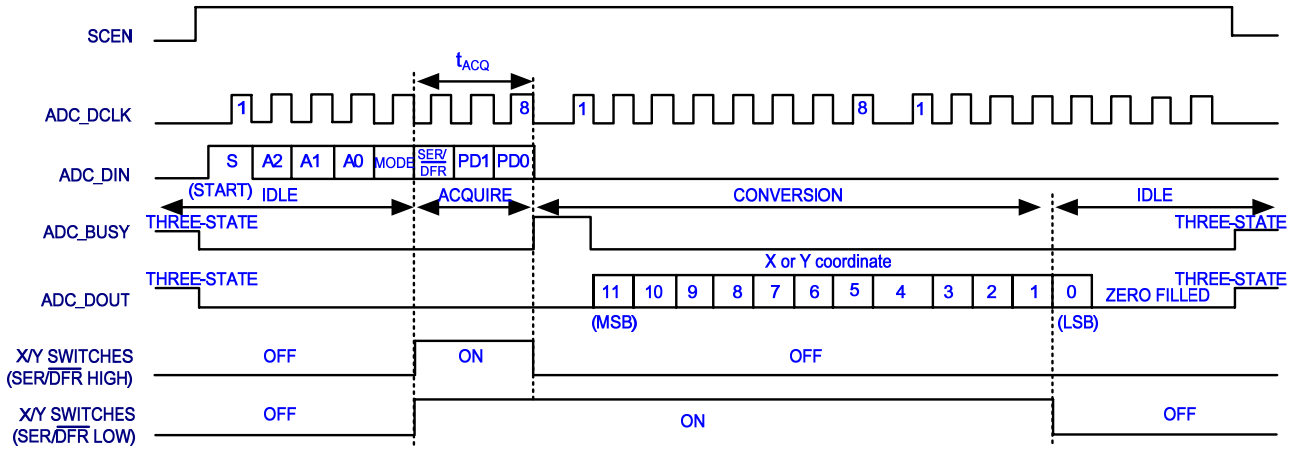

Figure 3.4 Conversion timing of the serial port interface

Chapter 4

Digital Panel Design Demonstration

This chapter illustrates how to exercise the LTM reference design provided with the kit. Users can follow the instructions in this chapter to build a 4.3 inch Ephoto demonstration and pattern generator using the DE2/DE1/DEN in 10 minutes.

4-1 Demonstration Setup

The demonstration configuration is illustrated as Figure 4.1. Display the bmp format photos, which are saved into the flash of DE2/DE1, on LTM module, through the control of FPGA on DE2/DE1 board. Users can change the displayed photo by touching the LTM touch panel.

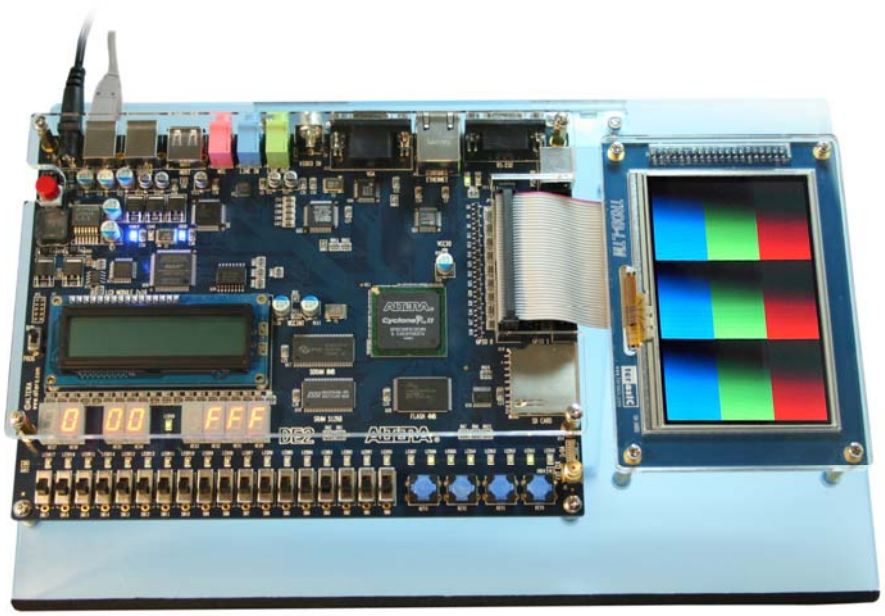

Figure 4.1. The Ephoto demonstration configuration setup

4-2 Loading Photos into the Flash

Locate the project directory from the CD-ROM and follow the steps below:

A: For Altera DE2 Board

Quartus II Project Directory: DE2_Control_Panel_V1.04

FPGA Bitstream Used: DE2_USB_API.sof or **DE2_USB_API.pof**

B: For Altera DE1 Board

Quartus II Project Directory: DE1_Control_Panel_V1.00

FPGA Bitstream Used: DE1_USB_API.sof or **DE1_USB_API.pof**

1. Make sure the USB-Blaster download cable is connected into the host PC
2. Load the Control Panel bit stream (**DE2_USB_API**/ **DE1_USB_API**) into the FPGA. Please also refer to **Chapter 3 DE2/DE1 Control Panel** in the **Altera DE2/DE1 User Manual** for more details in the **Control Panel Software**

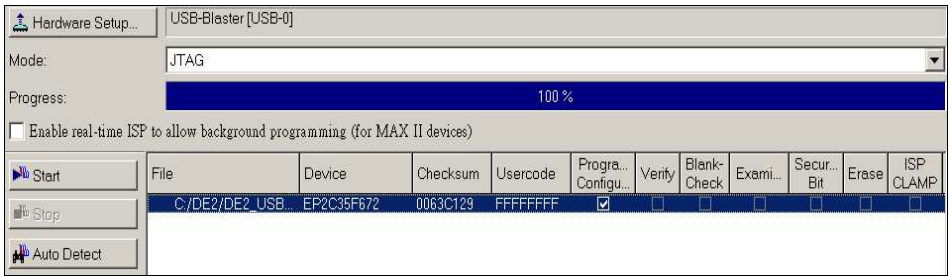

Figure 4.2. Programming window

3. Execute the Control Panel application software
4. Open the USB port by clicking Open > Open USB Port 0. The DE2/DE1 Control Panel application will list all the USB ports that connect to DE2/DE1 board
5. Switch to FLASH page and click on the "**Chip Erase(40 Sec)**" bottom to erase Flash data

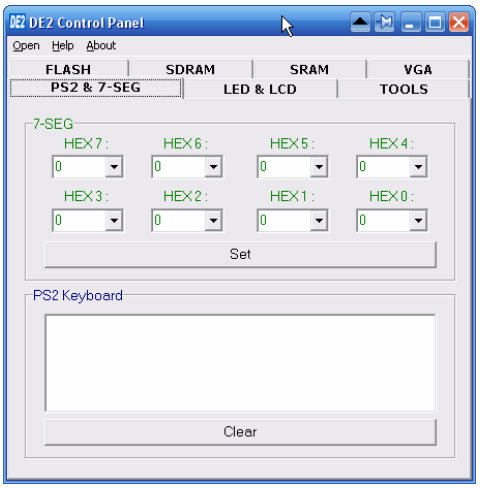

Figure 4.3. DE2 control panel window

6. Click on the "**File Length**" checkbox to indicate that you want to load the entire file
7. Click on the "**Write a File to FLASH**" bottom. When the Control Panel responds with the standard Windows dialog box and asks for the source file, select the "**480x3.bmp**" file in the "**Photo**" directory

4-3 Configuring the Ephoto Demonstration

Locate the project directory from the CD-ROM and follow the steps below:

A: For Altera DE2 Board

Quartus II Project Directory: DE2_LTM_Ephoto

FPGA Bitstream Used: DE2_LTM_Ephoto.sof or **DE2_LTM_Ephoto.pof**

B: For Altera DE1 Board

Quartus II Project Directory: DE1_LTM_Ephoto

FPGA Bitstream Used: DE1_LTM_Ephoto.sof or **DE1_LTM_Ephoto.pof**

1. Ensure the connection is made correctly as shown in Figure 4.4 and Figure 4.5. Make sure the IDE cable is connected to JP1 of the DE2/DE1 board
2. Download the bitstream (**DE2_LTM_Ephoto**/ **DE1_LTM_Ephoto**) to the DE2/DE1 board
3. As shown in Figurate 4.5, touch the bottom left corner and top right corner of the LTM touch panel to display the next and previous photos respectively

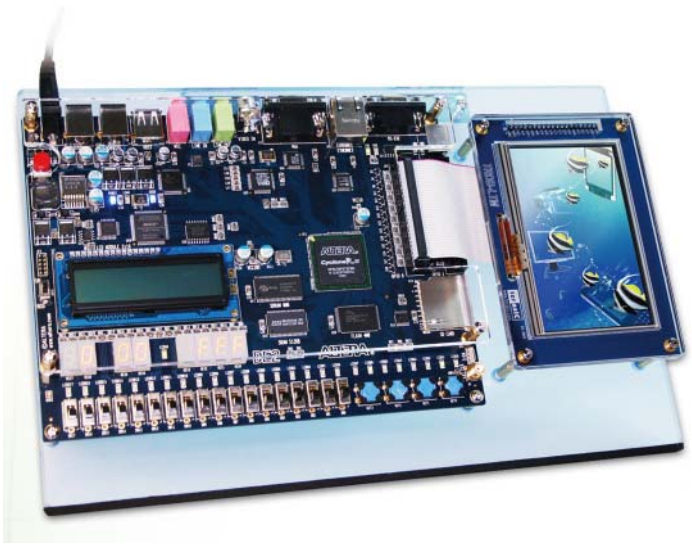

Figure 4.4. The connection setup for the Ephoto demonstration with DE2 board

Figure 4.5. The connection setup for the Ephoto demonstration with DE1 board

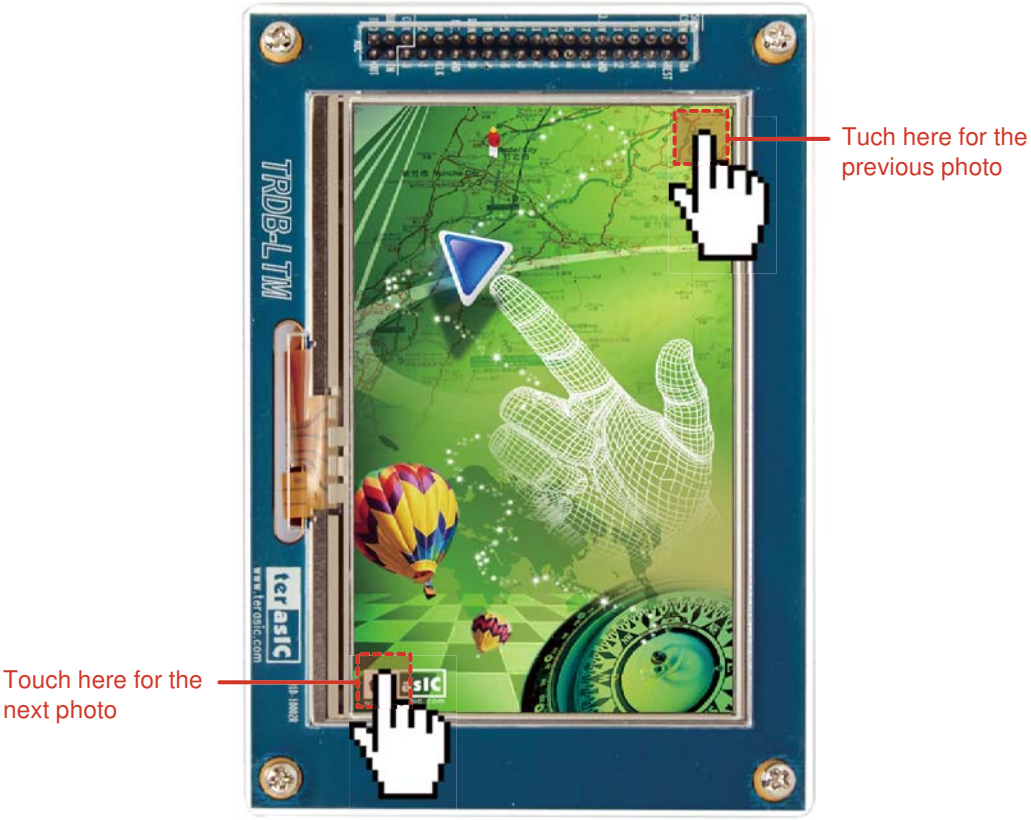

Figure 4.6. The touch function of changing displayed photo

4. When users touch the LTM screen, the 7-segment displays "HEX6~HEX4" and "HEX2~HEX0" on the DE2 board will display the X and Y coordinates (in Hexadecimal format) of the touch point respectively (DE2 board only). Figure 4.7 indicates that the x and y coordinates of the corners on the LTM touch screen

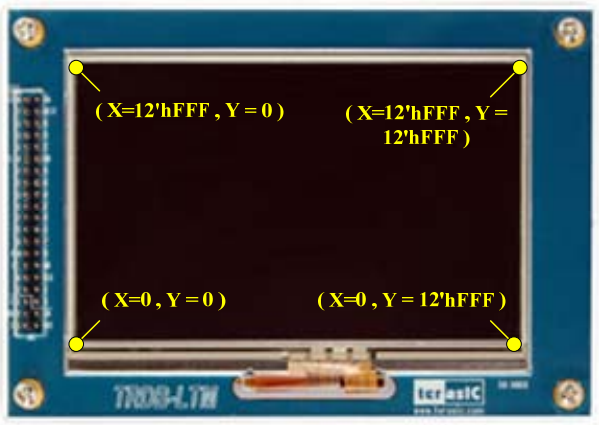

Figure 4.7 The x and y coordinates of the corners on the LTM touch screen

4-4 Block Diagram of the Ephoto Design

This section will describe the block diagram of the Ephoto demonstration to help users in reading the code provided.

Figure 4.8 shows the block diagram of the EPhoto demonstration. As soon as the bit stream is downloaded into the FPGA, the register values of the LCD driver IC using to control the LCD display function will be configured by the *LCD_SPI_Controller* block, which uses the serial port interface to communicate with the LCD driver IC. Meanwhile, the *Flash_to_SDRAM_Controller* block will read the RGB data of one picture stored in the Flash, and then write the data into SDRAM buffer. Accordingly, both the synchronous control signals and the picture data stored in the SDRAM buffer will be sent to the LTM via the *LCD_Timing_Controller* block.

When users touch LTM screens, the x and y coordinates of the touch point will be obtained by the *ADC_SPI_Controller* block through the ADC serial port interface. Then the *Touch_Point_Detector* block will determine whether these coordinates are in a specific range. If the coordinates fit the range, the *Touch_Point_Detector* block will control the *Flash_to_SDRAM_Controller* block to read the next or previous picture's data from the Flash and repeat the steps as mentioned before to command the LTM to display the next or previous picture.

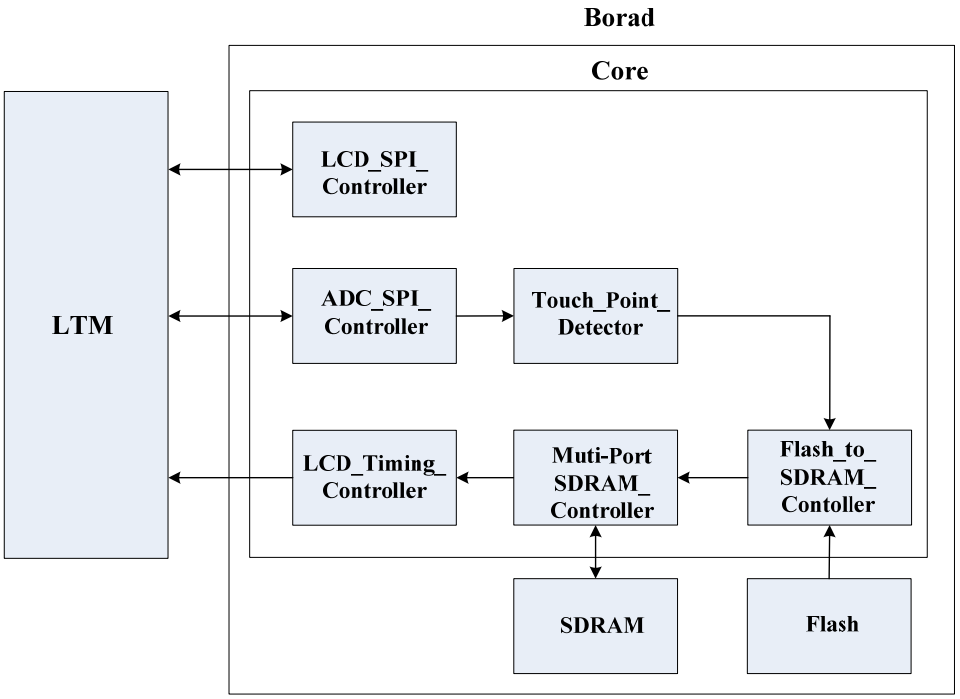

Figure 4.8 The block diagram of the Ephoto demonstration

4-5 Preprocessing the Desired Display Photo

If users want to display their own photos on the LTM ,they can follow the steps below:

1. Prepar three 24 bit *bmp* format photos and image resolution should be 800(high) x 480(width), as shown in Figure 4.9

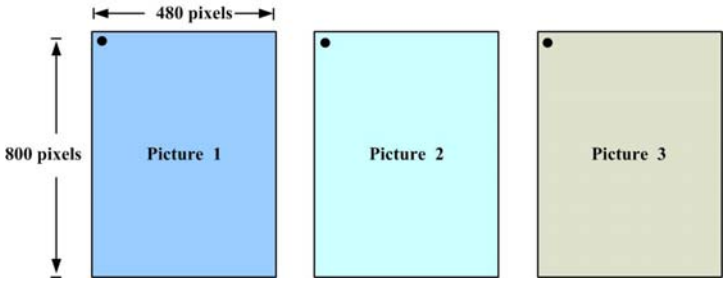

Figure 4.9. Original photo‘s resolution format

2. Use the image processing software (such as Photoshop or Photoimpact) to rotate the images counterclockwise and then merge these photos into a new photo image. The new photo‘s image resolution should be 1440(high) x 800 (width), as shown in Figure 4.10

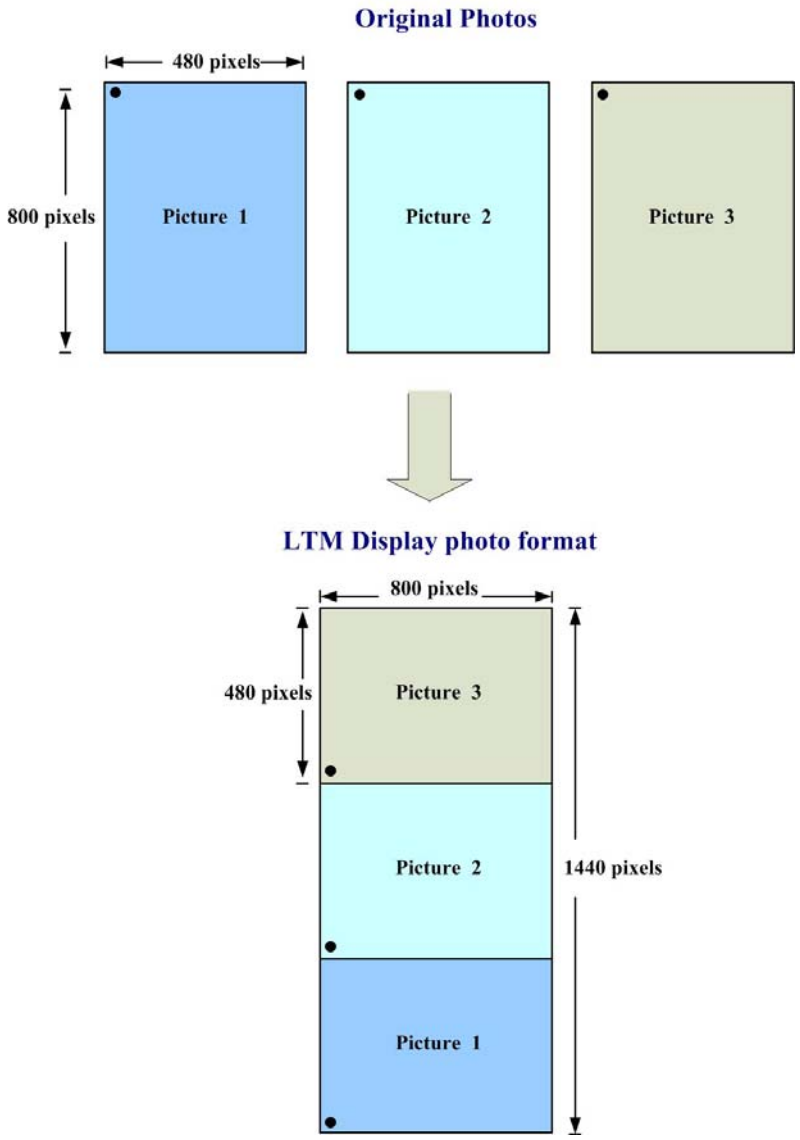

Figure 4.10 The photo format of the DE2_LTM_Ephoto/ DE1_LTM_Ephoto demonstration

4-6 Configuring the Pattern Generator for DE2/DE1 Board

Locate the project directory from the CD-ROM and follow the steps below:

A: For Altera DE2 Board

Quartus II Project Directory: DE2_LTM_Test

FPGA Bitstream Used: DE2_LTM_Test.sof or **DE2_LTM_Test.pof**

B: For Altera DE1 Board

Quartus II Project Directory: DE1_LTM_Test

FPGA Bitstream Used: DE1_LTM_Test.sof or **DE1_LTM_Test.pof**

1. Ensure the connection is made correctly as shown in Figure 4.11 and Figure 4.12 Make sure the IDE cable is connected to JP1 of the DE2/DE1 board

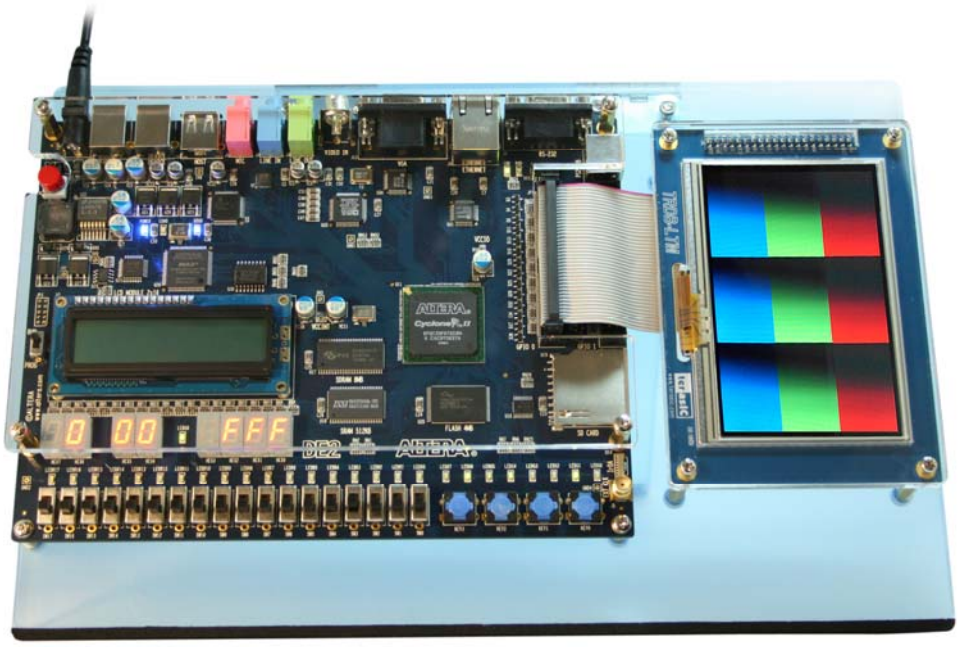

Figure 4.11. The connection setup for the pattern generator demo with DE2 board