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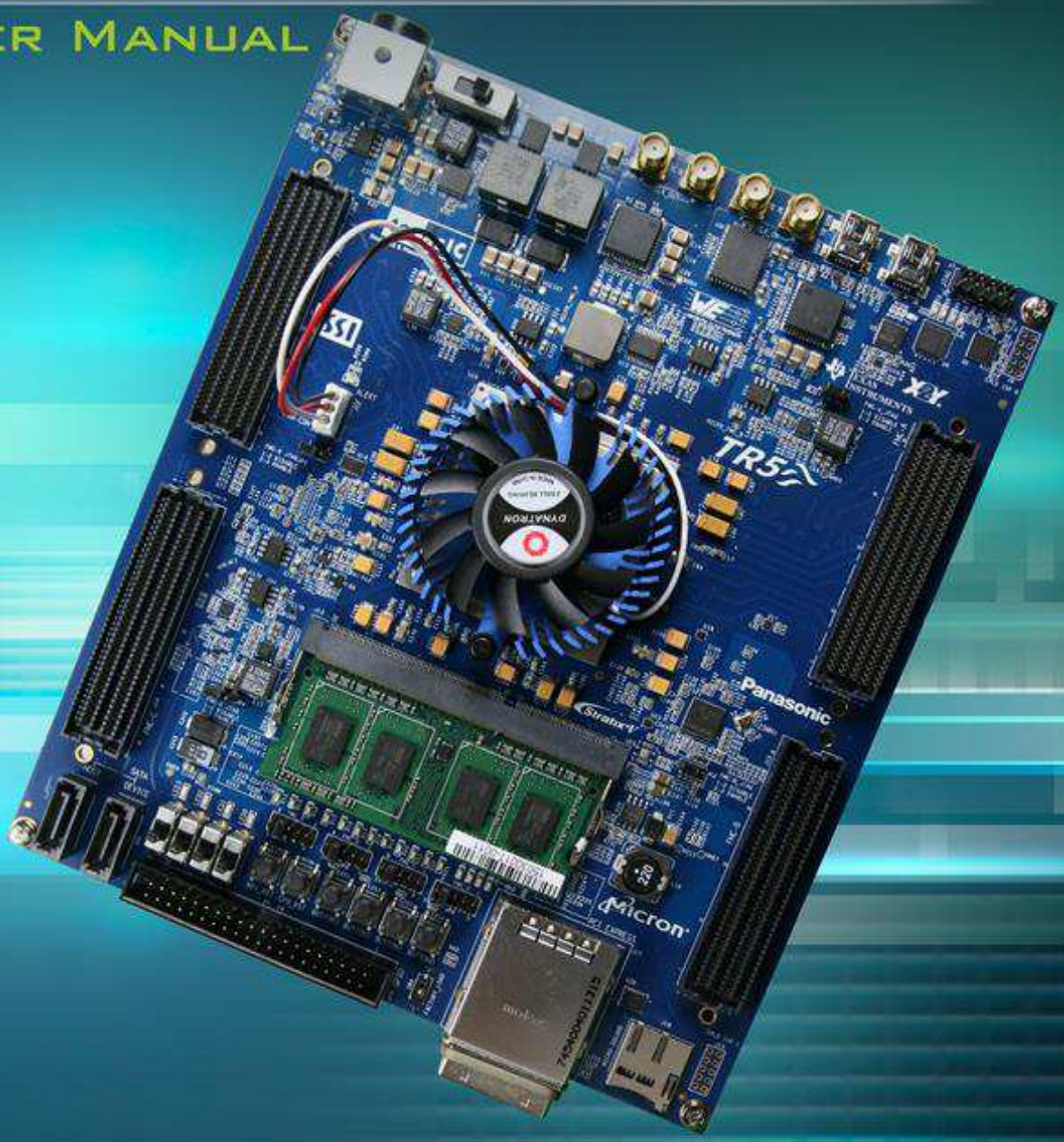
TR5

FPGA Development Kit

User Manual



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CONTENTS

Chapter 1

Overview

This chapter provides an overview of the TR5 Development Board and installation guide.

1.1 General Description

The Terasic TR5 Stratix V GX FPGA Development Kit provides the ideal hardware solution for designs that demand high capacity and bandwidth interface, ultra-low latency communication, high pin count and power efficiency. With an iPass PCIe gen3 connector, the TR5 is designed for the most demanding high-end applications, empowered with the Altera 28 nm Stratix V GX, delivering the best system-level integration and flexibility in the industry.

The Stratix® V GX FPGA features integrated transceivers that transfer at a maximum of 12.5Gbps, this allows the TR5 to be fully compliant with version 3.0 of the PCI Express standard. Not relying on an external PHY will accelerate mainstream development of network applications enabling customers to deploy designs for a broad range of high-speed connectivity applications. For designs that demand high capacity and high speed for memory and storage, the TR5 delivers with one independent bank of DDR3 SO-DIMM RAM, one ZBT SSRAM, and high-speed parallel flash memory. The feature-set of the TR5 fully supports all high-intensity applications such as ASIC verification, data acquisition, and signal processing.

1.2 Key Features

The following hardware is implemented on the TR5 board:

- FPGA
  - Altera Stratix® V GX FPGA
  - 5SGXEA7N2F45C2 /5SGXEABN3F45I3YY

■ FPGA Configuration

- On-Board USB Blaster II or JTAG header for FPGA programming
- Fast passive parallel (FPPx16) configuration via MAX II CPLD and flash memory

■ General user input/output:

- 4 LEDs
- 4 push-buttons
- 4 slide switches

■ Clock System

- 50MHz Oscillator
- CDCM6208 Programmable PLL
- LMK04096B Programmable PLL
- SMA connector pairs for differential clock input and output

■ Memory

- DDR3 SO-DIMM SDRAM
- QDRII+ SRAM
- FLASH
- SD Card

■ Communication Ports

- PCI Express (PCIe) x4 iPass connector
- Serial ATA host and device ports
- PCI Express (PCIe) x8 edge connector
- One mini Uart to USB connector

■ System Monitor and Control

- Temperature sensor
- Fan control
- Power monitor

■ Mechanical Specification

- 4 FPGA Mezzanine Card (FMC) Connectors
- One 40-pin Expansion Header

- Power
  - 12V DC Input

1.3 Block Diagram

Figure 1-1 shows the block diagram of the TR5 board. To provide maximum flexibility for the users, all key components are connected with the Stratix V GX FPGA device. Thus, users can configure the FPGA to implement any system design.

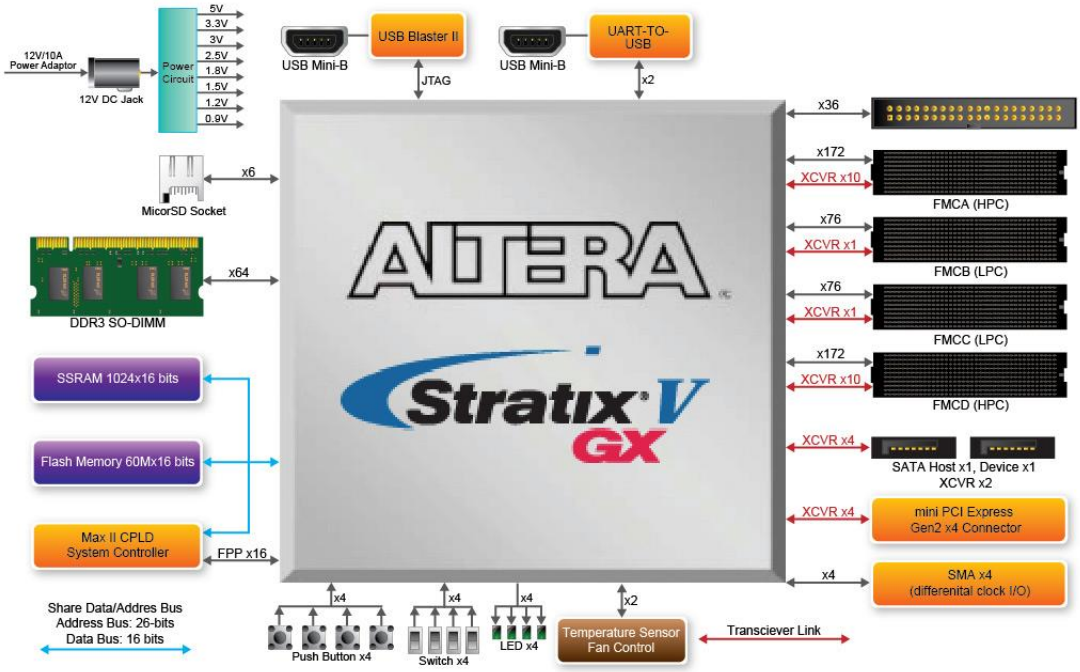

Figure 1-1 Block diagram of the TR5 board

Below is more detailed information regarding the blocks in Figure 1-1.

Stratix V GX FPGA

- 5SGXEA7N2F45C2
  - 622K logic elements (LEs)
  - 57.16-Mbits embedded memory

- 48 transceivers (12.5Gbps)
- 512 18 x18 multipliers
- 256 Variable-precision DSP blocks
- 28 Fractional PLLs and 4DLLs

- 5SGXEABN3F45I3YY
  - 952K logic elements (LEs)
  - 62.96-Mbits embedded memory
  - 48 transceivers (12.5Gbps)
  - 704 18 x18 multipliers
  - 352 Variable-precision DSP blocks
  - 28 Fractional PLLs and 4DLLs

JTAG Header and FPGA Configuration

- On-board USB Blaster II or JTAG header for use with the Quartus II Programmer
- MAXII CPLD EPM2210 System Controller and Fast Passive Parallel (FPP) configuration

Memory devices

- 2MB ZBT SSRAM
- Up to 8GB DDR3 SO-DIMM SDRAM
- 256MB FLASH

General user I/O

- 4 user controllable LEDs
- 4 user push buttons
- 4 user slide switches

On-Board Clock

- 50MHz oscillator
- Programming PLL providing clock for FMC transceivers
- Programming PLL providing clock for PCIe transceiver
- Programming PLL providing clocks for DDR3 SDRAM

Two Serial ATA ports

- SATA 3.0 standard at 6Gbps signaling rate

Four FMC Connectors

- 2 HPC (high-pin count) FMC connectors up to 172 x2 Single-end I/O
- 2 LPC (low-pin count) FMC connectors up to 76 x2 Single-end I/O
- 10 Transceiver Channels for HPC and 1 Transceiver Channel for LPC
- FMC VITA 57.1 Compliant
- Adjustable VADJ: 1.2V/1.5V/1.8V/2.5V/3.0V
- Don't support bidirectional LVDS due to Stratix V device only support single directional LVDS

One 40-pin GPIO Expansion Header

- 36 FPGA I/O pins; 4 power and ground lines
- I/O standards: 3.3V (with level shift from 2.5V to 3.3V)

External PCI Express x4 iPass Connector

- Support for PCIe x4 Gen1/2/3
- iPass connector with x4 PCI Express slot

Power Source

- DC 12V power adapter

Chapter 2

Board Components

This chapter introduces all the important components on the TR5.

2.1 Board Overview

Figure 2-1 is the top and bottom view of the TR5 development board. It depicts the layout of the board and indicates the location of the connectors and key components. Users can refer to this figure for relative location of the connectors and key components.

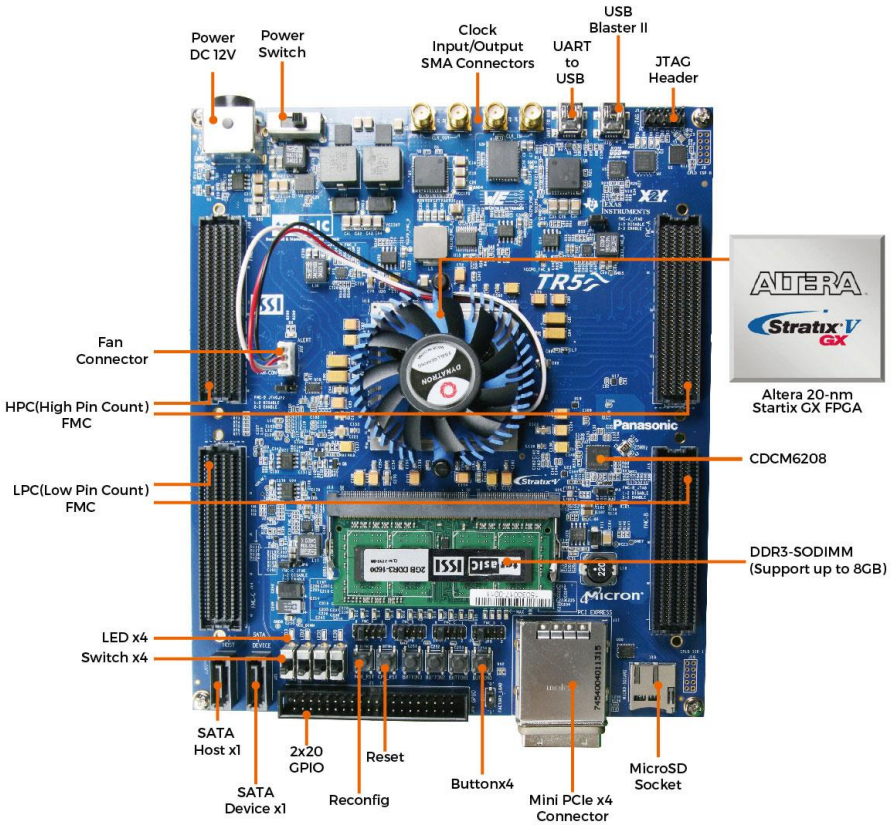

Figure 2-1 FPGA Board (Top)

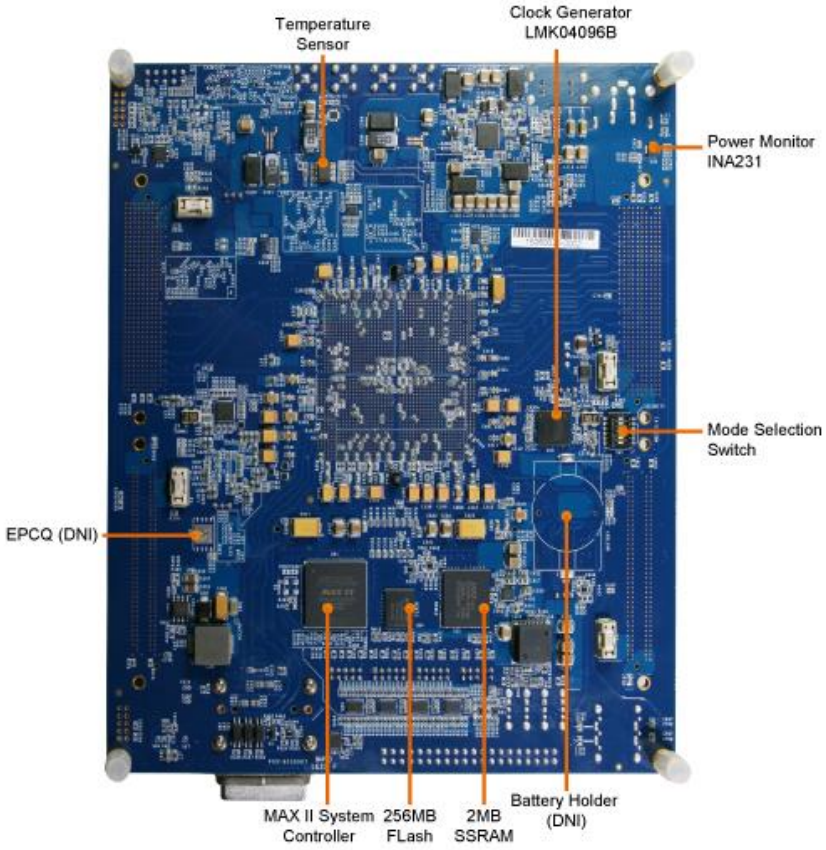

Figure 2-2 FPGA Board (Bottom)

2.2 Configuration, Status and Setup

■ Configure

The FPGA board supports two configuration methods for the Stratix V FPGA:

- Configure the FPGA using the on-board USB-Blaster II.
- Flash memory configuration of the FPGA using stored images from the flash memory on power-up.

For programming by on-board USB-Blaster II, the following procedures show how to download a configuration bit stream into the Stratix V GX FPGA:

- Make sure that power is provided to the FPGA board.
- Connect your PC to the FPGA board using a mini-USB cable and make sure the USB-Blaster II driver is installed on PC.
- Launch Quartus II programmer and make sure the USB-Blaster II is detected.
- In Quartus II Programmer, add the configuration bit stream file (.sof), check the associated "Program/Configure" item, and click "Start" to start FPGA programming.

■ Status LED

The FPGA Board development board includes board-specific status LEDs to indicate board status. Please refer to Table 2-1 for the description of the LED indicator.

Table 2-1 Status LED

Board Reference	*LED Name*	*Description*
D6	12-V Power	Illuminates when 12-V power is active.
D1	3.3-V Power	Illuminates when 3.3-V power is active.
D21	CONF_DONE	Illuminates when the FPGA is successfully configured. Driven by the MAX II CPLD EPM2210 System Controller.
D22	LOAD	Illuminates when the MAX II CPLD EPM2210 System Controller is actively configuring the FPGA. Driven by the MAX II CPLD EPM2210 System Controller with the Embedded Blaster CPLD.
D23	ERROR	Illuminates when the MAX II CPLD EPM2210 System Controller fails to configure the FPGA. Driven by the MAX II CPLD EPM2210 System Controller.
D24	BOOT_PAGE	Illuminates when FPGA is configured by the factory configuration bit stream.
D12~D20,D33~D35	FMC Voltage Value Indicator	See Section 2.8 FMC Connectors

■ Setup Configure Mode Control DIP switch

The Configure Mode Control DIP switch (SW5) is provided to specify the configuration mode of the FPGA. As currently only one mode is supported, please set all positions as shown in Figure 2-3.

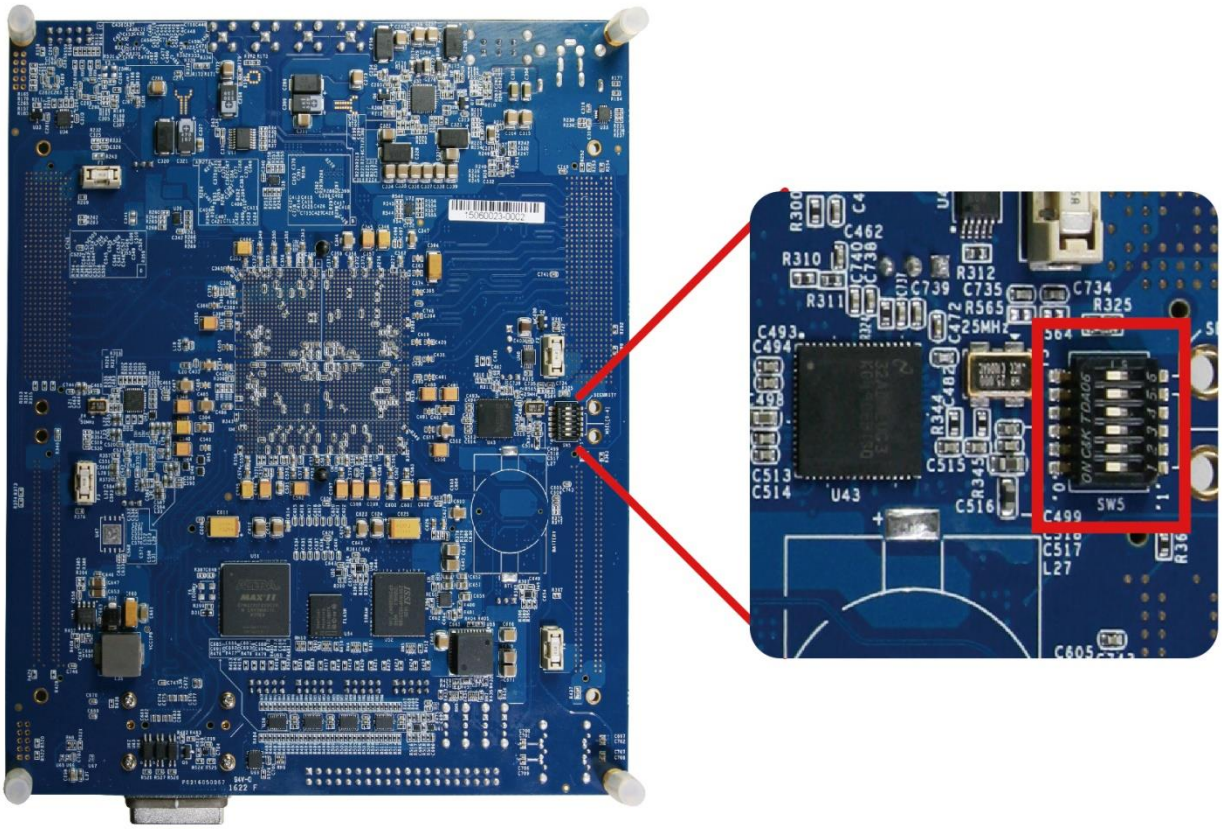

Figure 2-3 4-Position DIP switch for Configure Mode

■ Select Flash Image for Configuration

The Image Select DIP switch (SW4) is provided to specify the image for configuration of the FPGA. Setting SW4 to high (‘0’) specifies the default factory image to be loaded, setting SW4 to low (‘1’) specifies the TR5 to load a user-defined image, as shown in Figure 2-4.

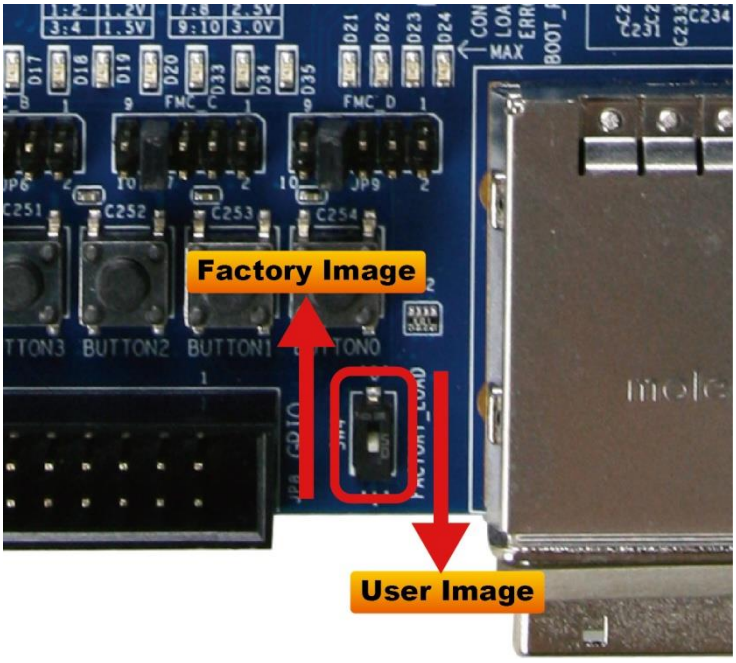

Figure 2-4 2-position DIP switch for Image Select

■ FMC VCCIO Voltage Setting Header

The I/O voltage of all the four FMC connectors is adjustable within 1.2/1.5/1.8/2.5/3.0V. For example, user can adjust the I/O voltage to 2.5V to support LVDS differential I/O stand. The user can independently control the voltage of FMCA~FMCD through JP5, JP6, JP7 and JP9. As shown in **Figure 2-5**, make short circuit onto JP5 pin 7 and pin 8, the status of D12, D13 and D14 will be set as "ON/OFF/ON" for representing the FMCA VCCIO is 2.5V. **Table 2-2, Table 2-3, Table 2-4** and **Table 2-5** lists the voltage settings of the FMCA~FMCD VCCIO and their corresponding LED display status.

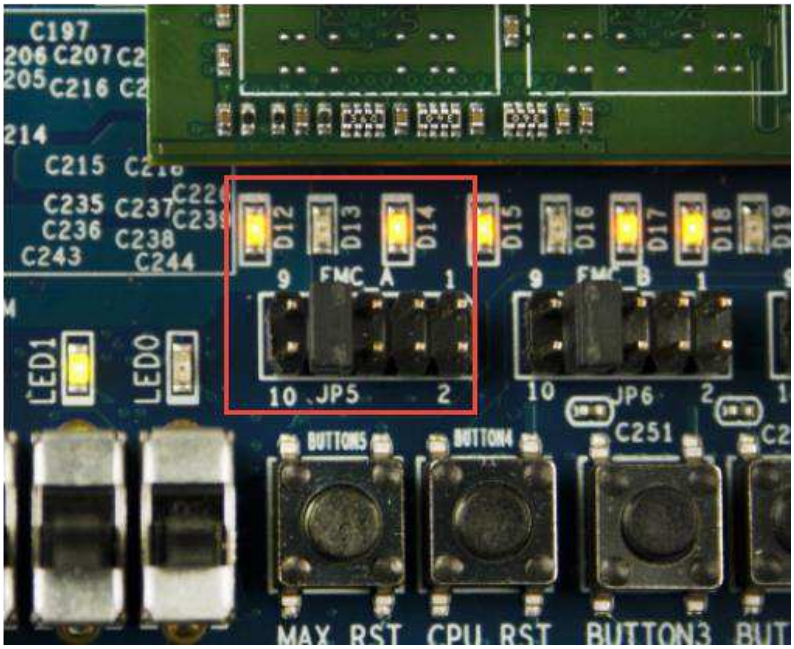

Figure 2-5 FMC A VCCIO Voltage Setting to 2.5V

Table 2-2 FMC A VCCIO Voltage Setting

JP5 Setting	*LED Status*			*FMC A VCCIO Voltage*
	D12	*D13*	*D14*	
Short Pin 1 & 2	**OFF**	**OFF**	**ON**	**1.2V**
Short Pin 3 & 4	**OFF**	**ON**	**OFF**	**1.5V**
Short Pin 5 & 6	**OFF**	**ON**	**ON**	**1.8V**
Short Pin 7 & 8	**ON**	**OFF**	**ON**	**2.5V(Default)**
Short Pin 9 & 10	**ON**	**ON**	**OFF**	**3.0V**

Table 2-3 FMC B VCCIO Voltage Setting

JP6 Setting	*LED Status*			*FMC B VCCIO Voltage*
	D15	*D16*	*D17*	
Short Pin 1 & 2	**OFF**	**OFF**	**ON**	**1.2V**
Short Pin 3 & 4	**OFF**	**ON**	**OFF**	**1.5V**
Short Pin 5 & 6	**OFF**	**ON**	**ON**	**1.8V**
Short Pin 7 & 8	**ON**	**OFF**	**ON**	**2.5V(Default)**
Short Pin 9 & 10	**ON**	**ON**	**OFF**	**3.0V**

Table 2-4 FMC C VCCIO Voltage Setting

JP7 Setting	LED Status			FMC C VCCIO Voltage
	D18	D19	D20	
Short Pin 1 & 2	OFF	OFF	ON	1.2V
Short Pin 3 & 4	OFF	ON	OFF	1.5V
Short Pin 5 & 6	OFF	ON	ON	1.8V
Short Pin 7 & 8	ON	OFF	ON	2.5V(Default)
Short Pin 9 & 10	ON	ON	OFF	3.0V

Table 2-5 FMC D VCCIO Voltage Setting

JP9 Setting	LED Status			FMC D VCCIO Voltage
	D33	D34	D35	
Short Pin 1 & 2	OFF	OFF	ON	1.2V
Short Pin 3 & 4	OFF	ON	OFF	1.5V
Short Pin 5 & 6	OFF	ON	ON	1.8V
Short Pin 7 & 8	ON	OFF	ON	2.5V(Default)
Short Pin 9 & 10	ON	ON	OFF	3.0V

■ FMC JTAG Header

The TR5 supports individual JTAG interfaces on each FMC connector. This feature allows users to extend the JTAG chain to FMC daughter cards. The JTAG signals on each FMC connector can be removed or included in the active JTAG chain via 3-Pin header (See **Figure 2-6**). **Table 2-6** lists the setting of the headers and their associated interfaces. Note that if the JTAG interface on FMC connector is enabled, make sure that the active JTAG chain must be a closed loop or the FPGA may not be detected.

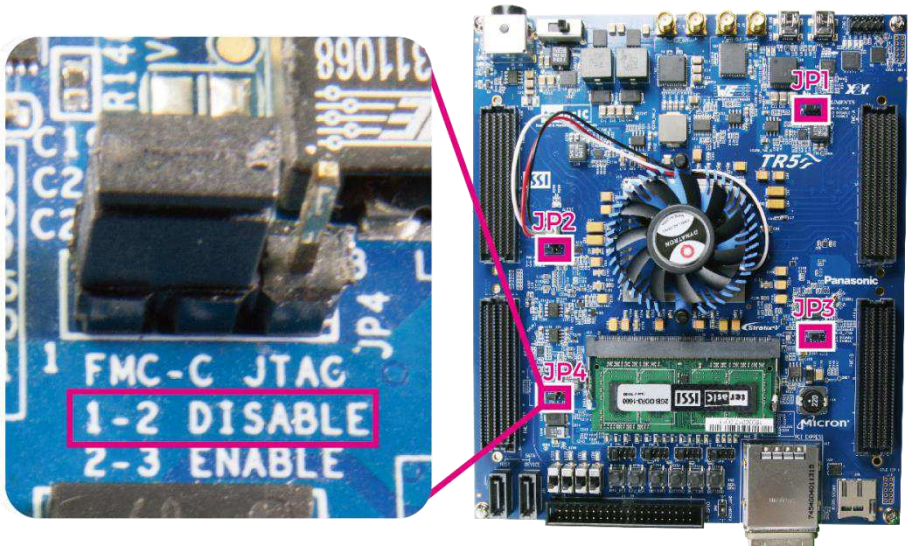

Figure 2-6 FMCC JTAG Header

Table 2-6 FMC JTAG Header Setting

Headers	*Setting*	*Description*
JP1	Short Pin 1 & 2	Disable FMCA JTAG
	Short Pin 2 & 3	Enable FMCA JTAG
JP2	Short Pin 1 & 2	Disable FMCD JTAG
	Short Pin 2 & 3	Enable FMCD JTAG
JP3	Short Pin 1 & 2	Disable FMCB JTAG
	Short Pin 2 & 3	Enable FMCB JTAG
JP4	Short Pin 1 & 2	Disable FMCC JTAG
	Short Pin 2 & 3	Enable FMCC JTAG

2.3 General User Input/Output

This section describes the user I/O interface to the FPGA.

■ User Defined Push-buttons

The FPGA board includes four user defined push-buttons that allow users to interact with the Stratix V GX device. Each push-button provides a high logic level or a low logic level when it is not pressed

or pressed, respectively. Table 2-7 lists the board references, signal names and their corresponding Stratix V GX device pin numbers.

Table 2-7 Push-button Pin Assignments, Schematic Signal Names, and Functions

Board Reference	*Schematic Signal Name*	*Description*	*I/O Standard*	*Stratix V GX Pin Number*
BUTTON0	BUTTON0	High Logic Level when the button is not pressed	1.5-V	PIN_BC7
BUTTON1	BUTTON1		1.5-V	PIN_BD7
BUTTON 2	BUTTON2		1.5-V	PIN_BB8
BUTTON 3	BUTTON3		1.5-V	PIN_BB9

■ User-Defined Slide Switch

There are four slide switches on the FPGA board to provide additional FPGA input control. When a slide switch is in the DOWN position or the UPPER position, it provides a low logic level or a high logic level to the Stratix V GX FPGA. The down position provides a low logic level and the upper position provides a high logic level.

Table 2-8 lists the signal names and their corresponding Stratix V GX device pin numbers.

Table 2-8 Slide Switch Pin Assignments, Schematic Signal Names, and Functions

Board Reference	*Schematic Signal Name*	*Description*	*I/O Standard*	*Stratix V GX Pin Number*
SW0	SW0	High logic level when SW in the UPPER position.	1.5-V	PIN_AT9
SW1	SW1		1.5-V	PIN_AU8
SW2	SW2		1.5-V	PIN_AK9
SW3	SW3		1.5-V	PIN_AL9

■ User-Defined LEDs

The FPGA board consists of four user-controllable LEDs to allow status and debugging signals to be driven to the LEDs from the designs loaded into the Stratix V GX device. Each LED is driven directly by the Stratix V GX FPGA. The LEDs are turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin names on the FPGA that are connected to the LEDs is given in Table 2-9.

Table 2-9 User LEDs Pin Assignments, Schematic Signal Names, and Functions

Board Reference	*Schematic Signal Name*	*Description*	*I/O Standard*	*Stratix V GX Pin Number*
LED0	LED0	Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	1.5-V	PIN_AT32
LED1	LED1		1.5-V	PIN_BA31
LED2	LED2		1.5-V	PIN_AN27
LED3	LED3		1.5-V	PIN_AH27

■ UART-To-USB

The UART is designed to perform communication between the board and the PC, allowing a transmission speed of up to 3Mbps. This interface wouldn't support HW flow control signals. The physical interface is done using UART-USB on-board bridge from a FT232R chip and connects to the host using a USB Type-B connector. For detailed information on how to use the transceiver, please refer to the datasheet, which is available on the manufacturer's website, or under the Datasheets\FT232 folder on the Kit System CD. Figure 2-7 shows the related schematics, and Table 2-10 lists the UART pin assignments, signal names and functions.

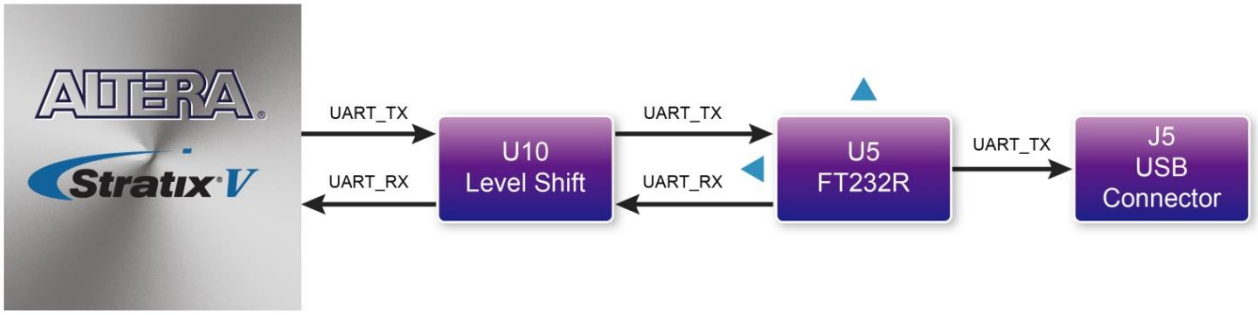

Figure 2-7 Connection between UART-To-USB and Stratix V GX FPGA

Table 2-10 UART-To-USB Pin Assignments, Schematic Signal Names, and Functions

Board Reference	*Schematic Signal Name*	*Description*	*I/O Standard*	*Stratix V GX Pin Number*
UART_TX	UART_TX	Uart TX output from FPGA	1.2/1.5/1.8/2.5/3.0-	PIN_T26

			V	
UART_RX	UART_RX	Uart RX input to FPGA	1.2/1.5/1.8/2.5/3.0-V	PIN_T25

■ Micro SD-Card

The development board supports Micro SD card interface using 4 data lines. Figure 2-8 shows the related signals connections between the SD Card and Stratix V GX FPGA. Table 2-11 lists all the associated pins

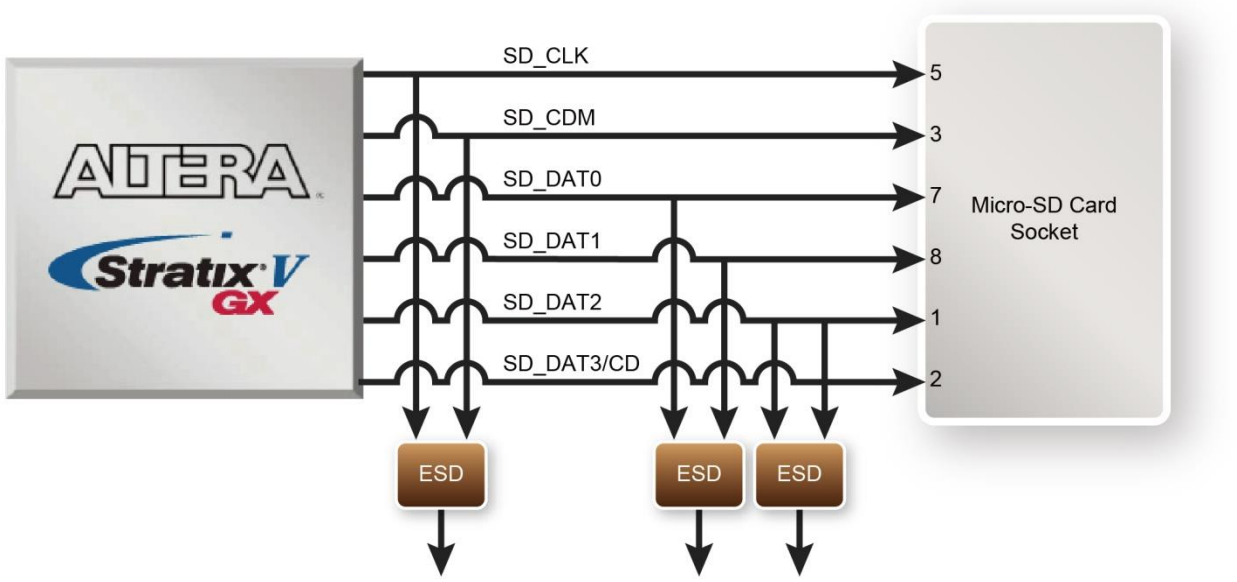

Figure 2-8 Connection between the SD Card Socket and Stratix V GX FPGA

Table 2-11 Micro SD Card Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	*Description*	*I/O Standard*	*Stratix V GX Pin Number*
SD_CLK	Serial Clock	1.5-V	PIN_BB39
SD_CMD	Command, Response	1.5-V	PIN_BA36
SD_DAT0	Serial Data 0	1.5-V	PIN_AV37
SD_DAT1	Serial Data 1	1.5-V	PIN_AY37

SD_DAT2	Serial Data 2	1.5-V	PIN_BB36
SD_DAT3	Serial Data 3	1.5-V	PIN_AW37

2.4 Temperature Sensor, Fan Control and Power Monitor

The FPGA board is equipped with a temperature sensor, MAX1619, which provides temperature sensing and over-temperature alert. These functions are accomplished by connecting the temperature sensor to the internal temperature sensing diode of the Stratix V GX device. The temperature status and alarm threshold registers of the temperature sensor can be programmed by a two-wire SMBus, which is connected to the Stratix V GX FPGA. In addition, the 7-bit POR slave address for this sensor is set to '0011000b'.

A 3-pin +12V fan located on J12 of the FPGA board is intended to reduce the temperature of the FPGA. The board is equipped with a Fan-Speed regulator and monitor MAX6650 with an I2C/SMBus interfaces, Users regulate and monitor the speed of fan depending on the measured system temperature.

The TR5 has implemented a power monitor chip to monitor the board input power voltage and current. Figure 2-9 shows the connection between the power monitor chip and the Stratix V GX FPGA. The power monitor chip monitors both shunt voltage drops and board input power voltage allows user to monitor the total board power consumption. Programmable calibration value, conversion times, and averaging, combined with an internal multiplier, enable direct readouts of current in amperes and power in watts. Note that, the temperature sensor, fan control and power monitor share the same I2C/SMBUS.

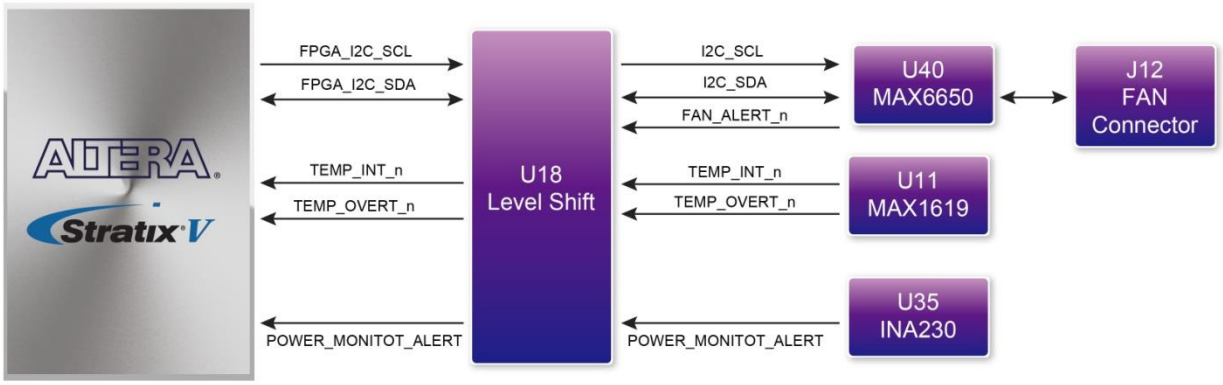

Figure 2-9 Connections between the temperature sensor/fan control/power monitor and the Stratix V GX FPGA

Table 2-12 Temperature Sensor and Fan Speed Control Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	*Description*	*I/O Standard*	*Stratix V GX Pin Number*
TEMPDIODEp	Positive pin of temperature diode in Stratix V	-	PIN_P6
TEMPDIODEn	Negative pin of temperature diode in Stratix V	-	PIN_P7
FPGA_I2C_SCL	SMBus clock	1.5-V	PIN_AN11
FPGA_I2C_SDA	SMBus data	1.5-V	PIN_AP9
TEMP_OVERT_n	SMBus alert (interrupt)	1.5-V	PIN_AR9
TEMP_INT_n	SMBus alert (interrupt)	1.5-V	PIN_AT8
POWER_MONITOR_ALERT	Active-high ALERT input	1.5-V	PIN_AY9
FAN_ALERT_n	Active-low ALERT input	1.5-V	PIN_AM11

2.5 Clock Circuit

The development board includes one 50 MHz and two programmable clock generators. **Figure 2-10** shows the default frequencies of on-board all external clocks going to the Stratix V GX FPGA.

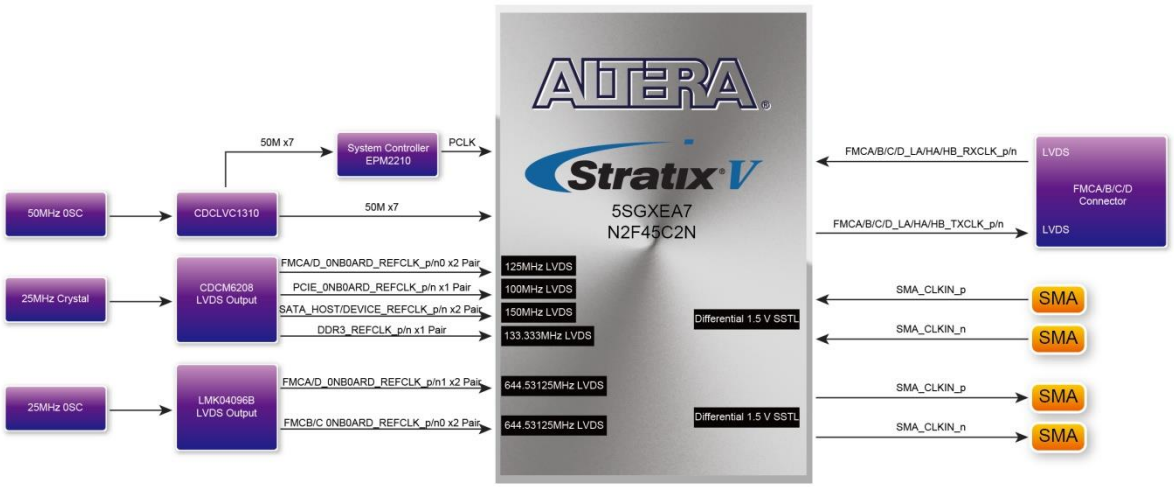

Figure 2-10 Clock circuit of the FPGA Board

A clock buffer is used to duplicate the 50 MHz oscillator, so there are seven 50MHz clocks fed into seven different FPGA banks. The two programming clock generators are low-jitter oscillators which are used to provide special and high quality clock signals for high-speed transceivers and high bandwidth memory. Through I2C serial interface, the clock generator controllers in the Stratix V GX FPGA can be used to program the CDCM6208 and LMK04096B to generate PCIe, SATA and high bandwidth memory reference clocks respectively. Two SMA connectors and Four FMC connectors provide external differential clock input(s) and clock output(s) respectively.

Table 2-9 lists the clock source, signal names, default frequency and their corresponding Stratix V GX device pin numbers.

Table 2-9 Clock Source, Signal Name, Default Frequency, Pin Assignments and Functions

Source	*Schematic Signal Name*	*Default Frequency*	*I/O Standard*	*Stratix V GX Pin Number*	*Application*
Y1	CLK_50_B3B	50.0 MHz	1.5-V	PIN_AW35	
	CLK_50_B4A		1.5-V	PIN_AP10	
	CLK_50_B4D		1.2/1.5/1.8/2.5/3.0-V	PIN_AY18	
	CLK_50_B7A		1.2/1.5/1.8/2.5/3.0-V	PIN_M8	

	CLK_50_B7D		1.2/1.5/1.8/2.5/3.0-V	PIN_J18	
	CLK_50_B8A		1.2/1.5/1.8/2.5/3.0-V	PIN_R36	
	CLK_50_B8D		1.2/1.5/1.8/2.5/3.0-V	PIN_R25	
J3	SMA_CLKIN_p	User Defined	1.5-V	PIN_BC8	External Clock Input
J4	SMA_CLKIN_n	User Defined	1.5-V	PIN_BD8	Clock Output
J1	SMA_CLKOUT_p	User Defined	1.5-V	PIN_AV8	
J2	SMA_CLKOUT_n	User Defined	1.5-V	PIN_AW9	
U21	FMCA_ONBOARD_REFCLK_p0	125 MHz	LVDS	PIN_Y38	FMCA port xcvr reference clock
	FMCD_ONBOARD_REFCLK_p0	125 MHz	LVDS	PIN_Y7	FMCD port xcvr reference clock
	PCIE_ONBOARD_REFCLK_p	100 MHz	LVDS	PIN_AH39	PCIe reference clock
	SATA_DEVICE_REFCLK_p	150 MHz	LVDS	PIN_AK7	SATA Device reference clock
	SATA_HOST_REFCLK_p	150 MHz		PIN_BB33	SATA Host reference clock
	DDR3_REFCLK_p	133.333 MHz			DDR3 reference clock
U43	FMCA_ONBOARD_REFCLK_p1	644.53125 MHz	LVDS	PIN_T38	FMCA port xcvr reference clock
	FMCD_ONBOARD_REFCLK_p1	644.53125 MHz	LVDS	PIN_T7	FMCD port xcvr reference clock
	FMCC_ONBOARD_REFCLK_p0	644.53125 MHz	LVDS	PIN_AD39	FMCB port xcvr reference clock
	FMCC_ONBOARD_REFCLK_p1	644.53125 MHz	LVDS	PIN_AD6	FMCC port xcvr reference clock

Table 2-10 lists the programmable oscillator control pins, signal names, I/O standard and their corresponding Stratix V GX device pin numbers.

Table 2-10 Programmable oscillator control pin, Signal Name, I/O standard, Pin Assignments and Descriptions

Programmable Oscillator	*Schematic Signal Name*	*I/O Standard*	*Stratix V GX Pin Number*	*Description*
CDCM6208 (U21)	CLOCK_SCL	2.5-V	PIN_AR25	I2C bus, connected with CDCM6208
	CLOCK_SDA	2.5-V	PIN_BC25	
LMK04906B (U43)	LMK04906_CLK	2.5-V	PIN_AT24	I2C bus master output only, connected with LMK04096B
	LMK04906_DATAIN	2.5-V	PIN_BD25	
	LMK04906_DATAOUT	1.5-V	PIN_BC29	I2C bus master input signal
	LMK04906_LE	1.5-V	PIN_AT33	LMK04096B PLL locked signal

2.6 FLASH and SSRAM Memory

The development board has a 1G bit CFI-compatible synchronous flash device for non-volatile storage of FPGA configuration data, user application data, and user code space, and a 2M byte ZBT SSRAM for data Cache.

The flash has a 16-bit data bus and allow for FPP x16 configuration. This device is part of the shared flash and MAX (FM) bus, which connects to the flash memory and MAX II CPLD (EPM2210) System Controller. The SSRAM also has a 16-bit data bus and share address and data bus with the flash. Figure 2-11 shows the connections between the Flash, SSRAM, MAX and Stratix V GX FPGA.