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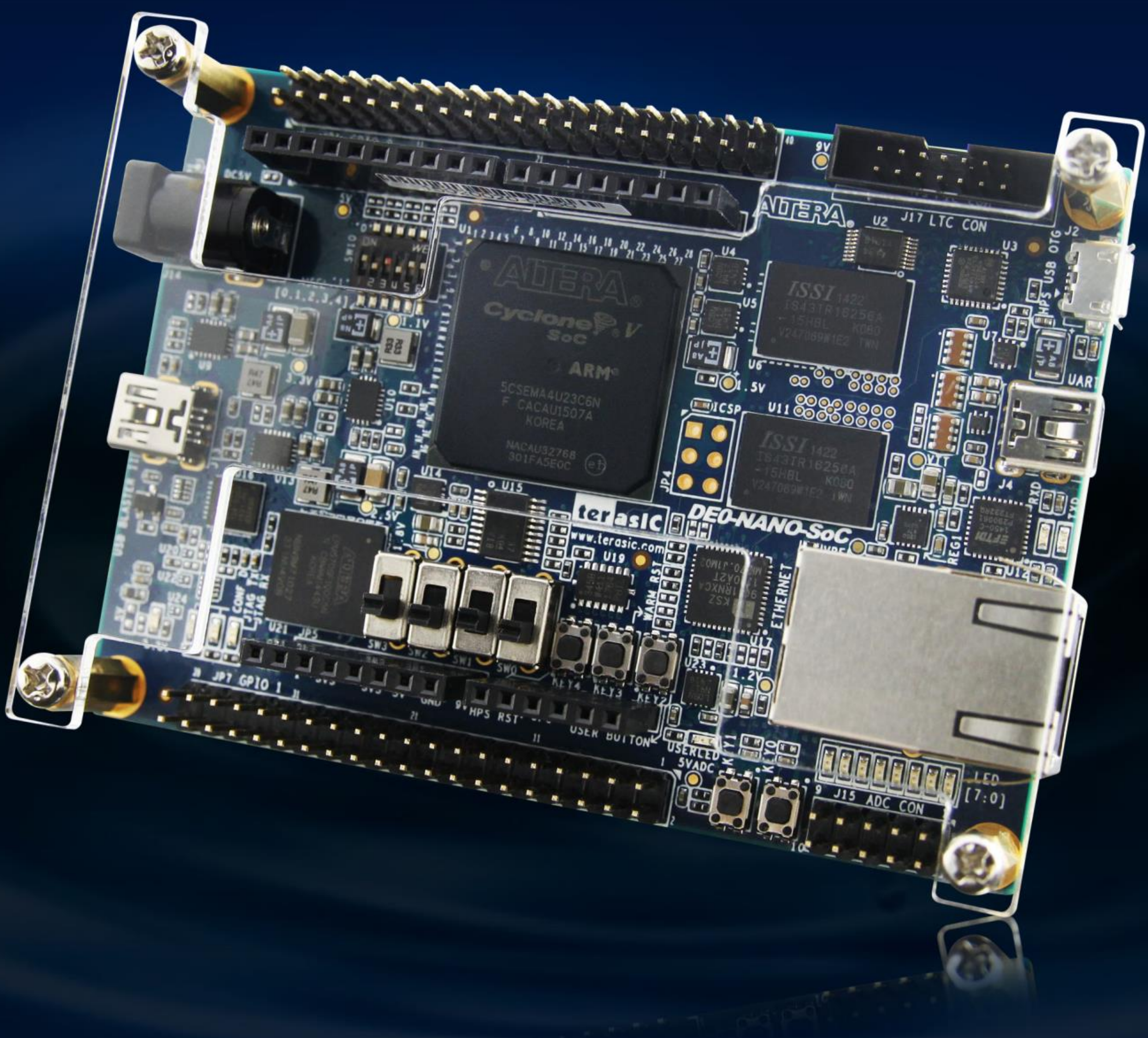
Atlas-SoC kit

User Manual



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CONTENTS

Chapter 1

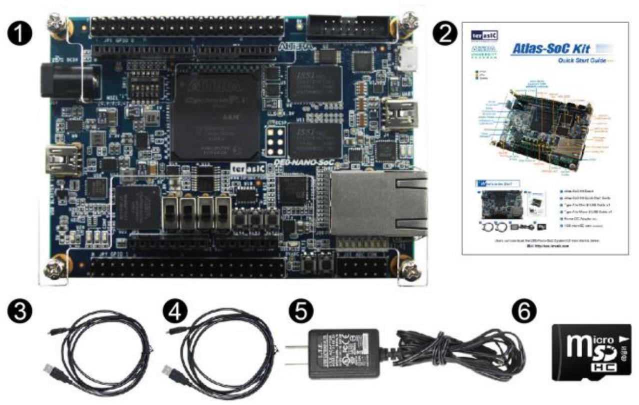
Atlas-SoC Software Development Kit

The Atlas-SoC Software Development Kit presents a robust hardware design platform built around the Altera System-on-Chip (SoC) FPGA, which combines the latest dual-core Cortex-A9 embedded cores with industry-leading programmable logic for ultimate design flexibility. Users can now leverage the power of tremendous re-configurability paired with a high-performance, low-power processor system. Altera's SoC integrates an ARM-based hard processor system (HPS) consisting of processor, peripherals and memory interfaces tied seamlessly with the FPGA fabric using a high-bandwidth interconnect backbone. The Atlas-SoC development board is equipped with high-speed DDR3 memory, analog to digital capabilities, Ethernet networking, and much more that promise many exciting applications.

The Atlas-SoC Software Development Kit contains all the tools needed to use the board in conjunction with a computer that runs the Microsoft Windows XP or later.

1.1 Package Contents

Figure 1-1 shows a photograph of the Atlas-SoC package.



❶ Atlas-SoC Kit Board
❷ Atlas-SoC Kit Quick Start Guide
❸ Type A to Mini-B USB Cable x1
❹ Type A to Micro-B USB Cable x1
❺ Power DC Adapter (5V)
❻ 4GB microSD card (installed)

Figure 1-1 The Atlas-SoC package contents

The Atlas-SoC package includes:

- The Atlas-SoC development board
- Atlas-SoC Quick Start Guide
- USB cable (Type A to Mini-B) for FPGA programming and control
- USB cable (Type A to Mini-B) for UART control
- 5V/2A DC power adapter
- 4GB microSD Card (Installed)

1.2 Atlas-SoC System CD

The Atlas-SoC System CD contains all the documents and supporting materials associated with Atlas-SoC, including the user manual, system builder, reference designs, and device datasheets. Users can download this system CD from the link: http://soc.terasic.com.

1.3 Getting Help

Here are the addresses where you can get help if you encounter any problems:

Community Support

http://www.rocketboards.org/atlas-soc

Terasic Technologies

9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan

Email: support@terasic.com

Tel.: +886-3-575-0880

Website: Atlas-SoC.terasic.com

Chapter 2

Introduction of the Atlas-SoC Board

This chapter provides an introduction to the features and design characteristics of the board.

2.1 Layout and Components

Figure 2-1 and **Figure 2-2** shows a photograph of the board. It depicts the layout of the board and indicates the location of the connectors and key components.

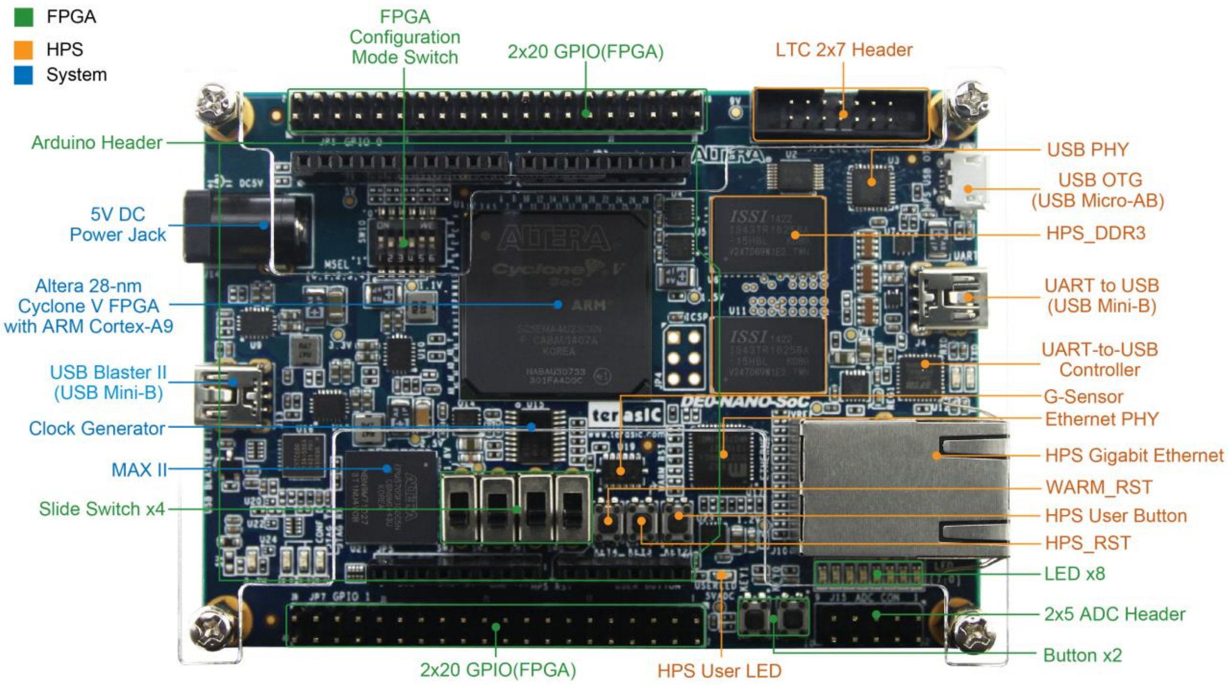


Figure 2-1 Atlas-SoC development board (top view)

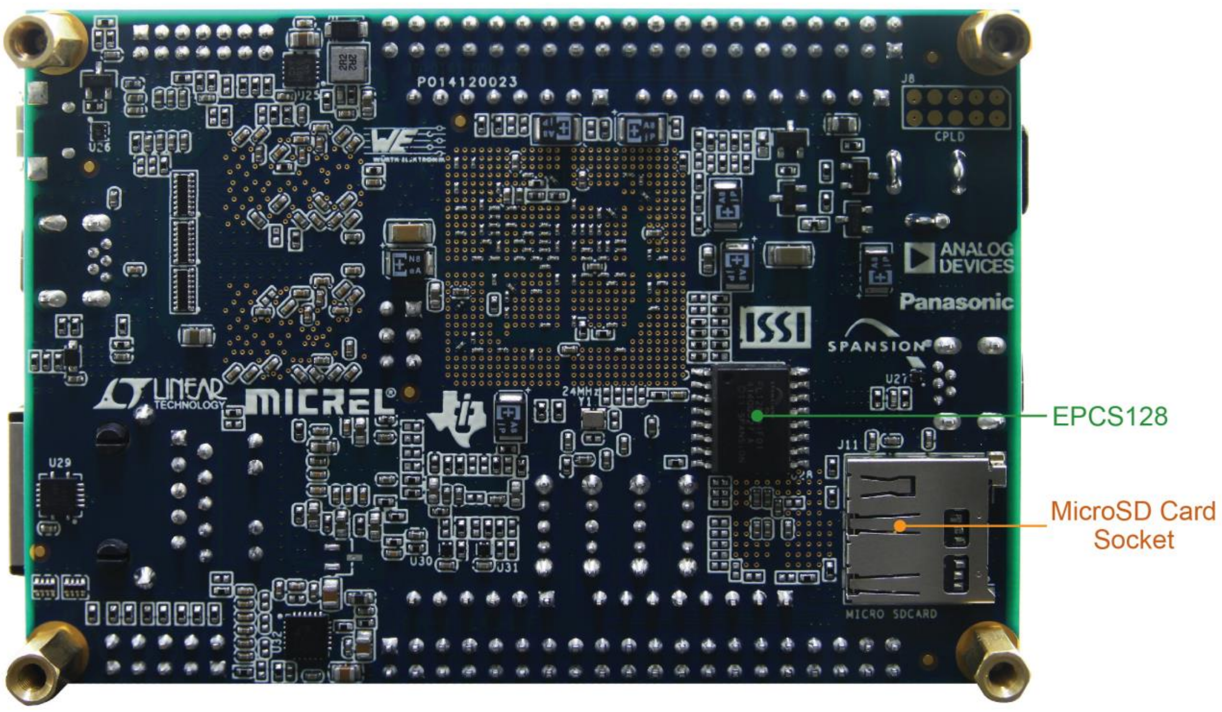


Figure 2-2 Atlas-SoC development board (bottom view)

The Atlas-SoC board has many features that allow users to implement a wide range of designed circuits, from simple circuits to various multimedia projects.

The following hardware is provided on the board:

■ FPGA

- Altera Cyclone® V SE 5CSEMA4U23C6N device
- Serial configuration device – EPCS128
- USB-Blaster II onboard for programming; JTAG Mode
- 2 push-buttons
- 4 slide switches
- 8 green user LEDs
- Three 50MHz clock sources from the clock generator
- Two 40-pin expansion header
- One Arduino expansion header (Uno R3 compatibility), can connect with Arduino shields.
- One 10-pin Analog input expansion header. (shared with Arduino Analog input)
- A/D converter, 4-wire SPI interface with FPGA

■ HPS (Hard Processor System)

- 925MHz Dual-core ARM Cortex-A9 processor
- 1GB DDR3 SDRAM (32-bit data bus)
- 1 Gigabit Ethernet PHY with RJ45 connector
- port USB OTG, USB Micro-AB connector
- Micro SD card socket
- Accelerometer (I2C interface + interrupt)
- UART to USB, USB Mini-B connector
- Warm reset button and cold reset button
- One user button and one user LED
- LTC 2x7 expansion header

2.2 Block Diagram of the Atlas-SoC Board

Figure 2-3 is the block diagram of the board. All the connections are established through the Cyclone V SoC FPGA device to provide maximum flexibility for users. Users can configure the FPGA to implement any system design.

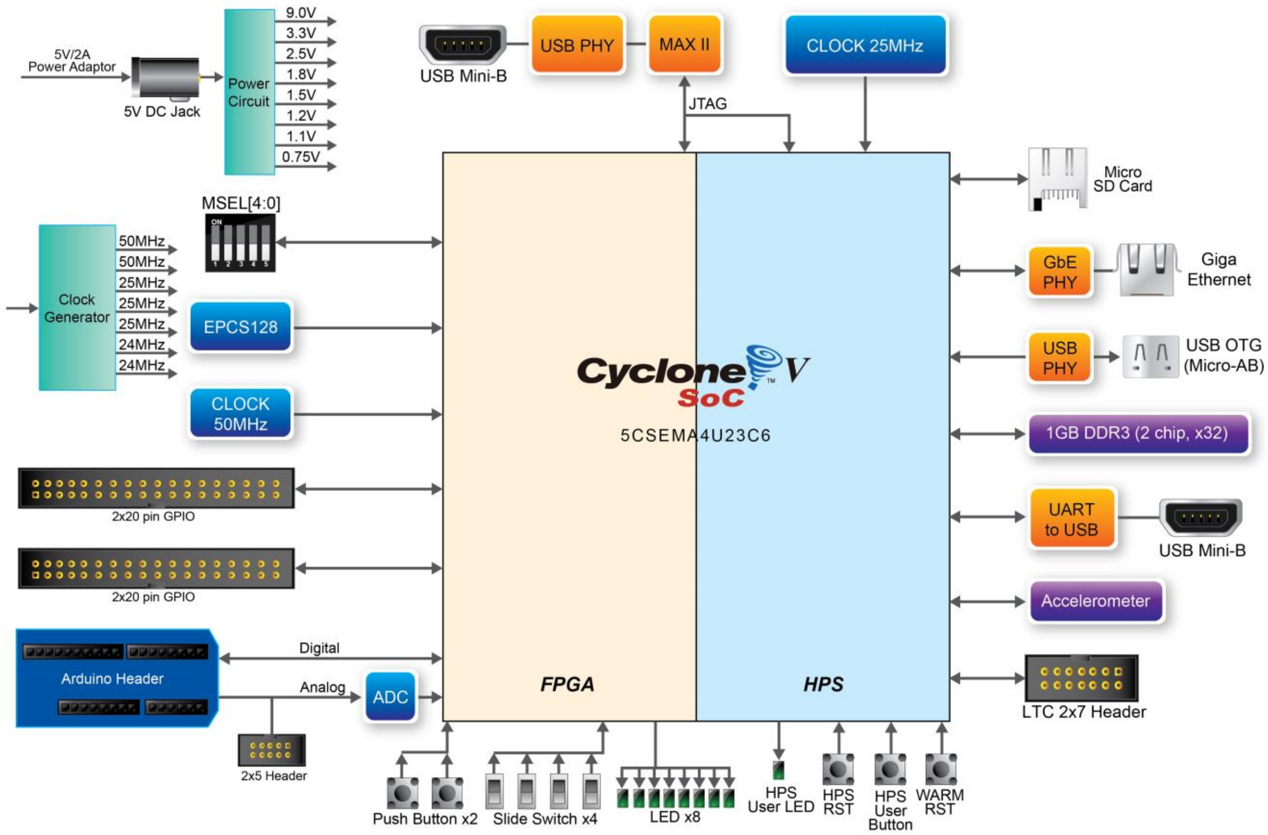


Figure 2-3 Block diagram of Atlas-SoC

Detailed information about Figure 2-3 are listed below.

FPGA Device

- Cyclone V SoC 5CSEMA4U23C6N Device
- Dual-core ARM Cortex-A9 (HPS)
- 40K programmable logic elements
- 2,460 Kbits embedded memory
- 5 fractional PLLs
- 2 hard memory controllers

Configuration and Debug

- Serial configuration device – EPCS128 on FPGA
- Onboard USB-Blaster II (Mini-B USB connector)

Memory Device

- 1GB (2x256Mx16) DDR3 SDRAM on HPS
- Micro SD card socket on HPS

Communication

- One USB 2.0 OTG (ULPI interface with USB Micro-AB connector)
- UART to USB (USB Mini-B connector)
- 10/100/1000 Ethernet

Connectors

- Two 40-pin expansion headers
- Arduino expansion header
- One 10-pin ADC input header
- One LTC connector (one Serial Peripheral Interface (SPI) Master ,one I2C and one GPIO interface)

ADC

- 12-Bit Resolution, 500Ksps Sampling Rate. SPI Interface.
- 8-Channel Analog Input. Input Range : 0V ~ 4.096V.

Switches, Buttons, and Indicators

- 3 user Keys (FPGA x2, HPS x1)
- 4 user switches (FPGA x4)
- 9 user LEDs (FPGA x8, HPS x 1)
- 2 HPS reset buttons (HPS_RESET_n and HPS_WARM_RST_n)

Sensors

- G-Sensor on HPS

Power

- 5V DC input

Chapter 3

Using the Atlas-SoC Board

This chapter provides an instruction to use the board and describes the peripherals.

3.1 Settings of FPGA Configuration Mode

When the Atlas-SoC board is powered on, the FPGA can is configured from the SD Card (default), but it can also be configured by the EPCS flash device as well. The MSEL[4:0] pins are used to select the configuration scheme. It is implemented as a 6-pin DIP switch **SW10** on the Atlas-SoC board, as shown in **Figure 3-1**.

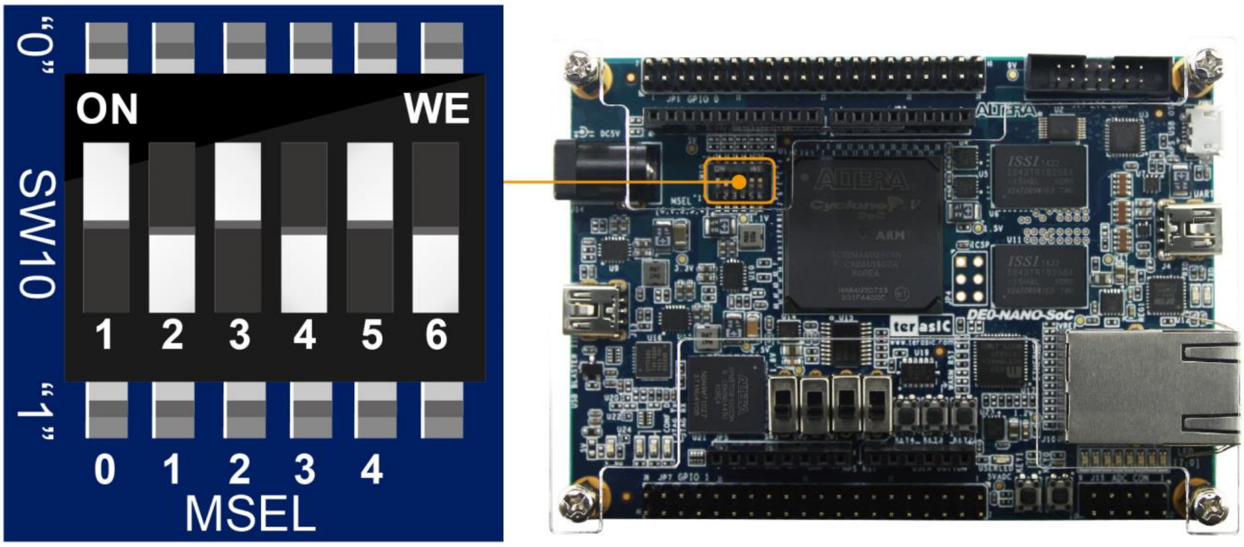


Figure 3-1 DIP switch (SW10) setting of FPP x32 mode

Table 3-1 shows the relation between MSEL[4:0] and DIP switch (SW10).

Table 3-1 FPGA Configuration Mode Switch (SW10)

Board Reference	*Signal Name*	*Description*	*Default*
SW10.1	MSEL0	Use these pins to set the FPGA Configuration scheme	ON ("0")
SW10.2	MSEL1		OFF ("1")
SW10.3	MSEL2		ON ("0")
SW10.4	MSEL3		OFF ("1")
SW10.5	MSEL4		ON ("0")
SW10.6	N/A	N/A	N/A

Table 3-2 shows MSEL[4:0] setting for FPGA configure, and default setting is FPPx32 mode on Atlas-SoC.

When the board is powered on and MSEL[4:0] set to "10010", the FPGA is configured from EPCS, which is pre-programmed with the default code. If developers wish to configure FPGA from an application software running on Linux, the MSEL[4:0] needs to be set to "01010" before the programming process begins. If developers using the "Linux Console with frame buffer" or "Linux LXDE Desktop" SD Card image, the MSEL[4:0] needs to be set to "00000" before the board is powered on.

Table 3-2 MSEL Pin Settings for FPGA Configure of Atlas-SoC

Configuration	*SW10.1 MSEL0*	*SW10.2 MSEL1*	*SW10.3 MSEL2*	*SW10.4 MSEL3*	*SW10.5 MSEL4*	*SW10.6*	*Description*
AS	ON	OFF	ON	ON	OFF	N/A	FPGA configured from EPCS
FPPx32 (Default)	ON	OFF	ON	OFF	ON	N/A	FPGA configured from HPS software: Linux (default)
FPPx16	ON	ON	ON	ON	ON	N/A	FPGA configured from HPS software: U-Boot, with image stored on the SD card, like LXDE Desktop or console Linux with frame buffer edition.

3.2 Board Status Elements

In addition to the 9 LEDs that FPGA/HPS device can control, there are 6 indicators which can indicate the board status (See Figure 3-2), please refer the details in Table 3-3

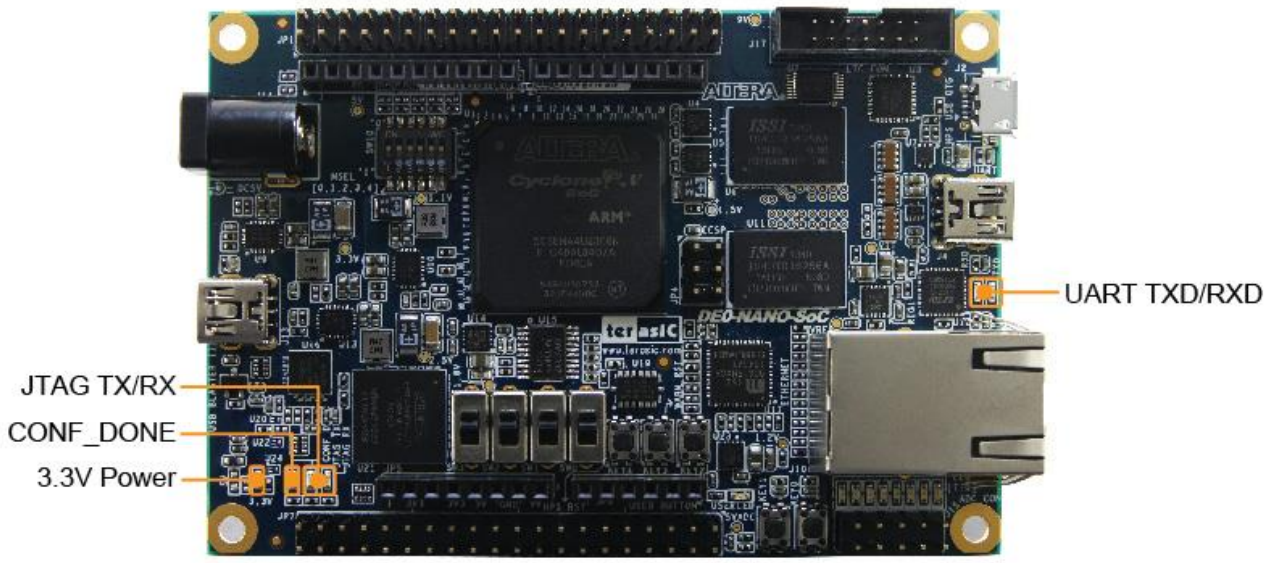


Figure 3-2 LED Indicators on Atlas-SoC

Table 3-3 LED Indicators

Board Reference	*LED Name*	*Description*
LED9	3.3-V Power	Illuminate when 3.3V power is active.
LED10	CONF_DONE	Illuminates when the FPGA is successfully configured.
LED11	JTAG_TX	Illuminate when data is transferred from JTAG to USB Host.
LED12	JTAG_RX	Illuminate when data is transferred from USB Host to JTAG.
TXD	UART TXD	Illuminate when data is transferred from FT232R to USB Host.
RXD	UART RXD	Illuminate when data is transferred from USB Host to FT232R.

3.3 Board Reset Elements

There are two HPS reset buttons on Atlas-SoC, HPS (cold) reset and HPS warm reset, as shown in Figure 3-3. Table 3-4 describes the purpose of these two HPS reset buttons. Figure 3-4 is the reset tree for Atlas-SoC.

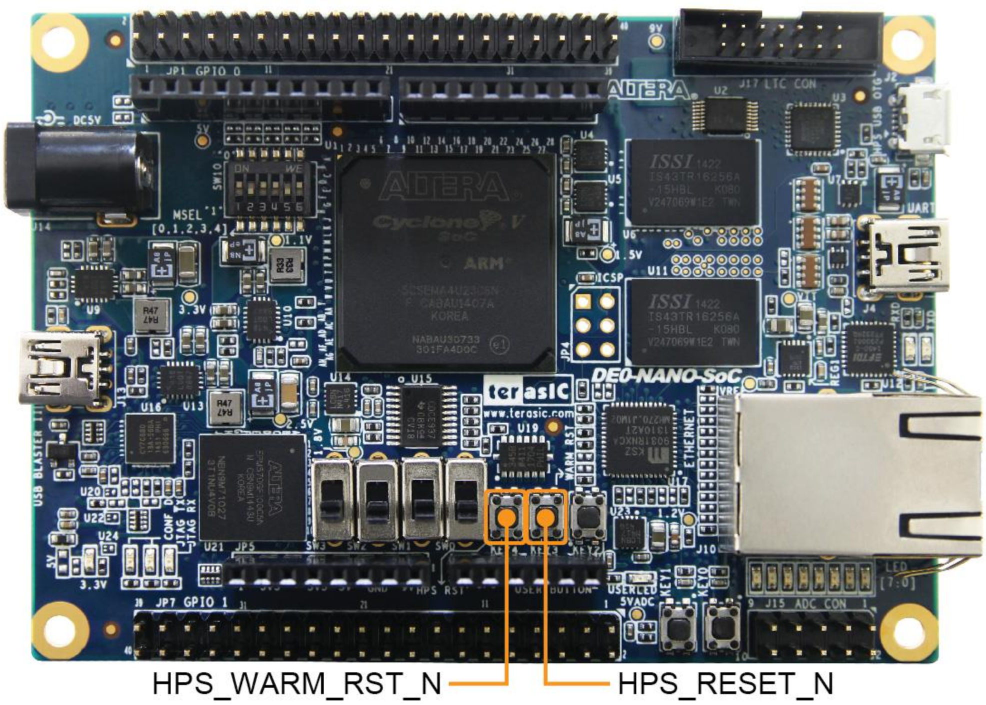


Figure 3-3 HPS cold reset and warm reset buttons on Atlas-SoC

Table 3-4 Description of Two HPS Reset Buttons on Atlas-SoC

Board Reference	*Signal Name*	*Description*
KEY4	HPS_RESET_N	Cold reset to the HPS, Ethernet PHY and USB host device. Active low input which resets all HPS logics that can be reset.
KEY3	HPS_WARM_RST_N	Warm reset to the HPS block. Active low input affects the system reset domain for debug purpose.

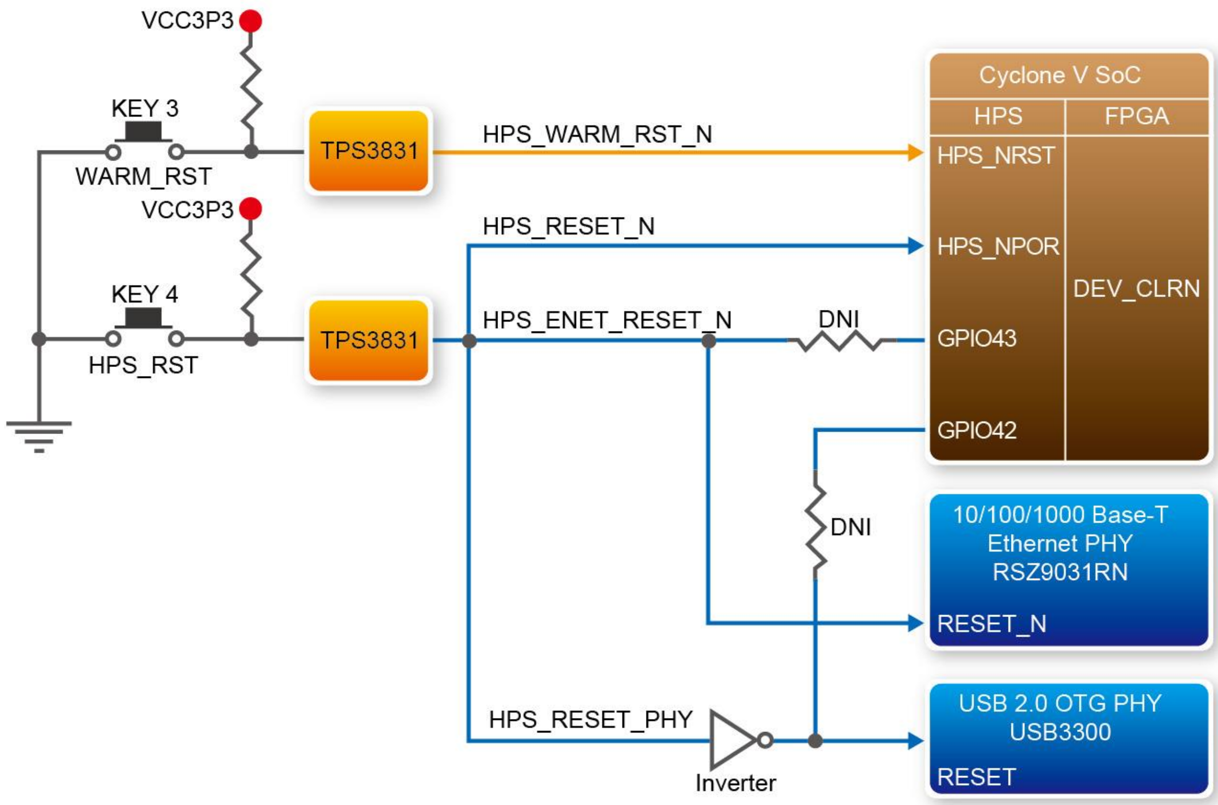


Figure 3-4 HPS reset tree on Atlas-SoC board

3.4 Clock Circuitry

Figure 3-5 shows the default frequency of all external clocks to the Cyclone V SoC FPGA. A clock generator is used to distribute clock signals with low jitter. The two 50MHz clock signals connected to the FPGA are used as clock sources for user logic. Three 25MHz clock signal are connected to two HPS clock inputs, and the other one is connected to the clock input of Gigabit Ethernet Transceiver. One 24MHz clock signal is connected to the USB controller for USB Blaster II circuit and FPGA. One 24MHz clock signals are connected to the clock inputs of USB OTG PHY. The associated pin assignment for clock inputs to FPGA I/O pins is listed in Table 3-5.

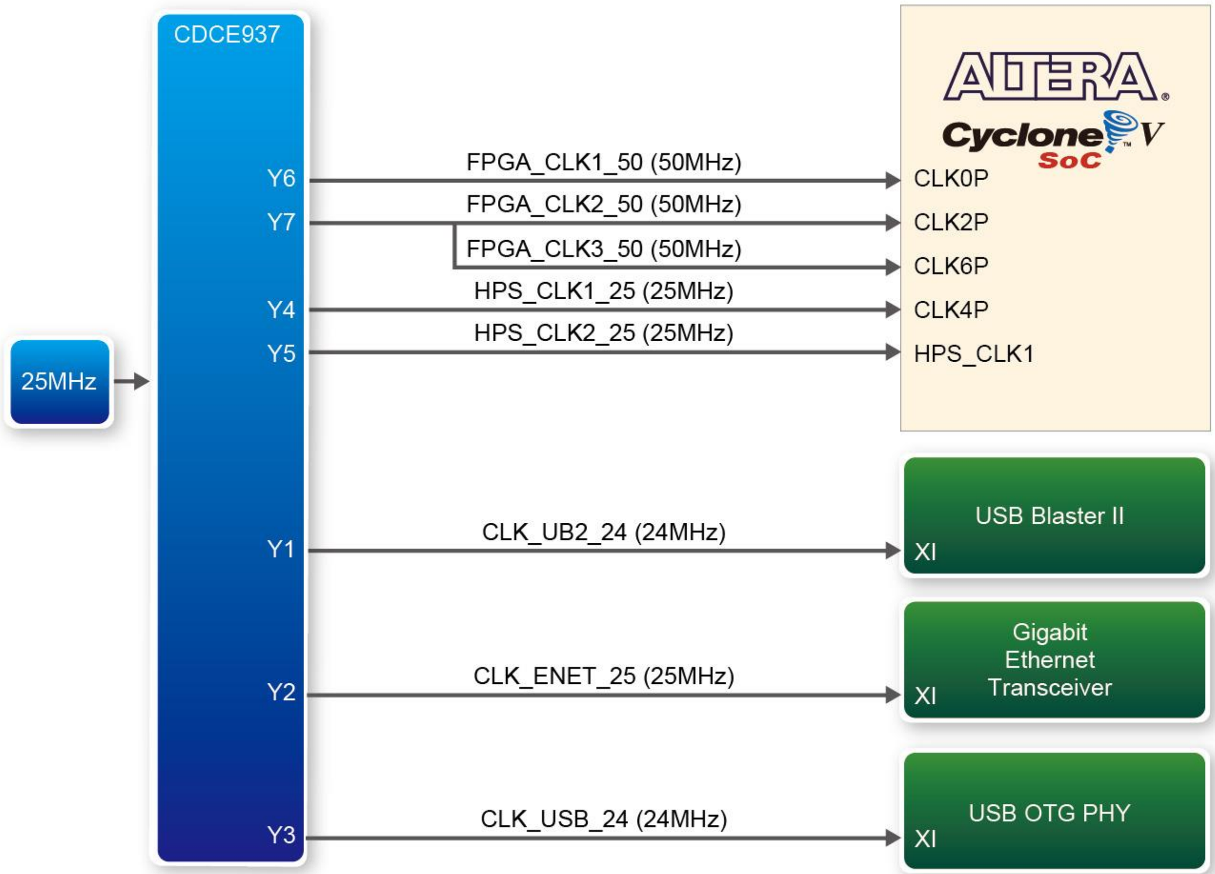


Figure 3-5 Block diagram of the clock distribution on Atlas-SoC

Table 3-5 Pin Assignment of Clock Inputs

Signal Name	***FPGA Pin No.***	***Description***	***I/O Standard***
FPGA_CLK1_50	PIN_V11	50 MHz clock input	3.3V
FPGA_CLK2_50	PIN_Y13	50 MHz clock input	3.3V
FPGA_CLK3_50	PIN_E11	50 MHz clock input (share with FPGA_CLK1_50)	3.3V
HPS_CLK1_25	PIN_E20	25 MHz clock input	3.3V
HPS_CLK2_25	PIN_D20	25 MHz clock input	3.3V

3.5 Peripherals Connected to the FPGA

This section describes the interfaces connected to the FPGA. Users can control or monitor different interfaces with user logic from the FPGA.

3.6.1 User Push-buttons, Switches and LEDs

The board has two push-buttons connected to the FPGA, as shown in **Figure 3-6** Connections between the push-buttons and the Cyclone V SoC FPGA. Schmitt trigger circuit is implemented and act as switch debounce in **Figure 3-7** for the push-buttons connected. The two push-buttons named KEY0 and KEY1 coming out of the Schmitt trigger device are connected directly to the Cyclone V SoC FPGA. The push-button generates a low logic level or high logic level when it is pressed or not, respectively. Since the push-buttons are debounced, they can be used as clock or reset inputs in a circuit.

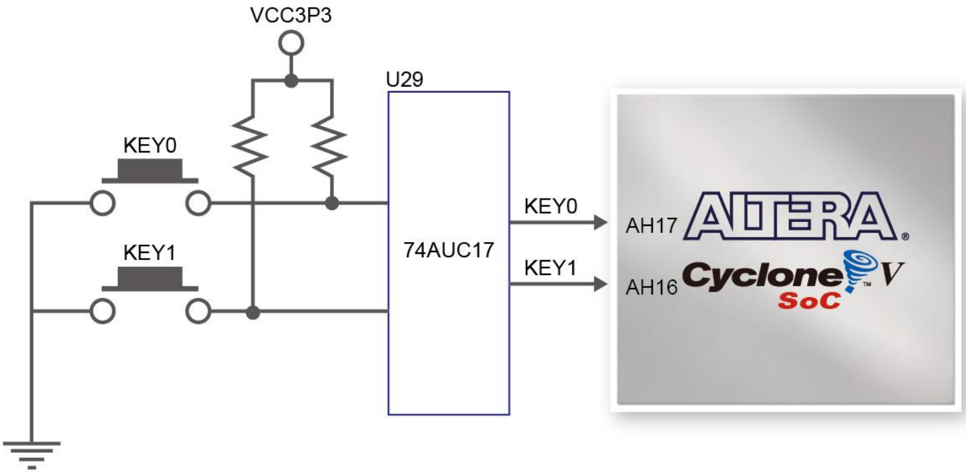


Figure 3-6 Connections between the push-buttons and the Cyclone V SoC FPGA

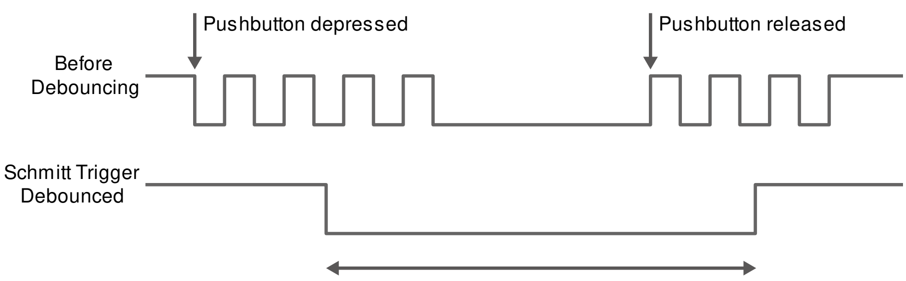


Figure 3-7 Switch debouncing

There are four slide switches connected to the FPGA, as shown in **Figure 3-8**. These switches are not debounced and to be used as level-sensitive data inputs to a circuit. Each switch is connected directly and individually to the FPGA. When the switch is set to the DOWN position (towards the edge of the board), it generates a low logic level to the FPGA. When the switch is set to the UP position, a high logic level is generated to the FPGA.

Figure 3-8 Connections between the slide switches and the Cyclone V SoC FPGA

There are also eight user-controllable LEDs connected to the FPGA. Each LED is driven directly and individually by the Cyclone V SoC FPGA; driving its associated pin to a high logic level or low level to turn the LED on or off, respectively. **Figure 3-9** shows the connections between LEDs and Cyclone V SoC FPGA. **Table 3-6**, **Table 3-7** and **Table 3-8** list the pin assignment of user push-buttons, switches, and LEDs.

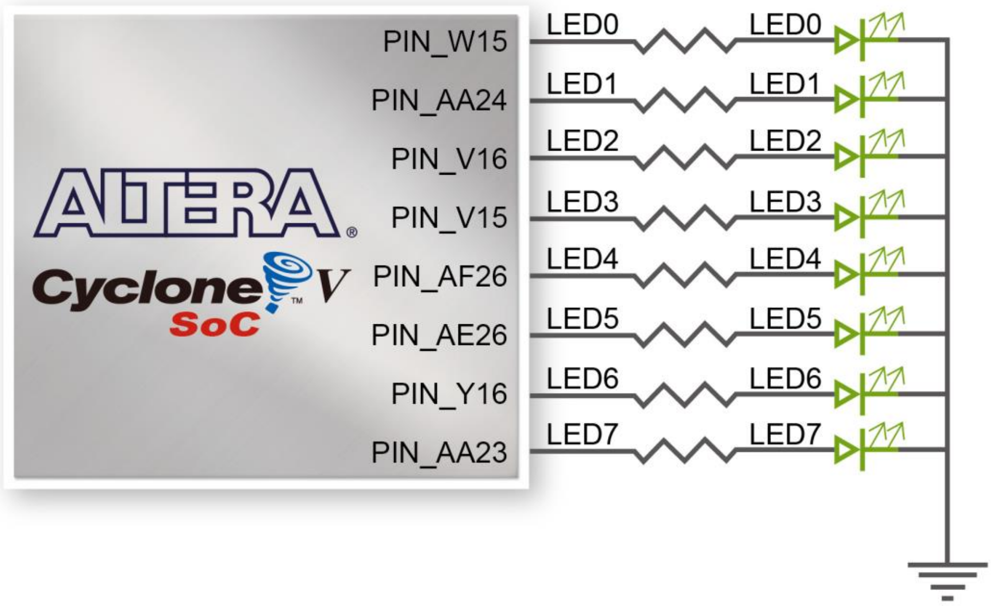


Figure 3-9 Connections between the LEDs and the Cyclone V SoC FPGA

Table 3-6 Pin Assignment of Slide Switches

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
SW[0]	PIN_L10	Slide Switch[0]	3.3V
SW[1]	PIN_L9	Slide Switch[1]	3.3V
SW[2]	PIN_H6	Slide Switch[2]	3.3V
SW[3]	PIN_H5	Slide Switch[3]	3.3V

Table 3-7 Pin Assignment of Push-buttons

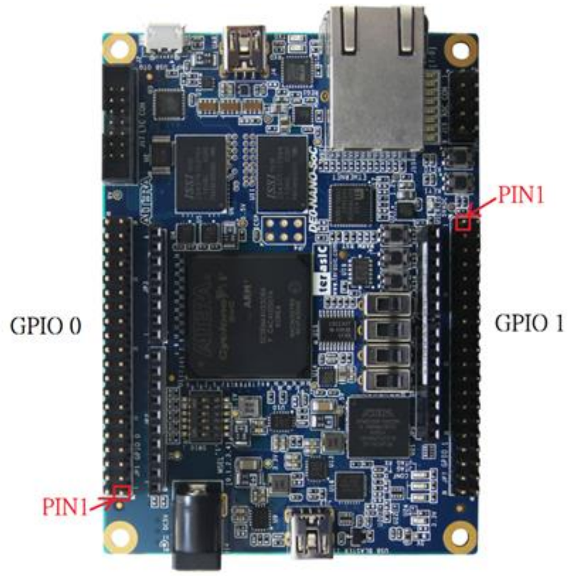
Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
KEY[0]	PIN_AH17	Push-button[0]	3.3V
KEY[1]	PIN_AH16	Push-button[1]	3.3V

Table 3-8 Pin Assignment of LEDs

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
LED[0]	PIN_W15	LED [0]	3.3V
LED[1]	PIN_AA24	LED [1]	3.3V
LED[2]	PIN_V16	LED [2]	3.3V
LED[3]	PIN_V15	LED [3]	3.3V
LED[4]	PIN_AF26	LED [4]	3.3V
LED[5]	PIN_AE26	LED [5]	3.3V
LED[6]	PIN_Y16	LED [6]	3.3V
LED[7]	PIN_AA23	LED [7]	3.3V

3.6.2 2x20 GPIO Expansion Headers

The board has two 40-pin expansion headers. Each header has 36 user pins connected directly to the Cyclone V SoC FPGA. It also comes with DC +5V (VCC5), DC +3.3V (VCC3P3), and two GND pins. Figure 3-18 shows the I/O distribution of the GPIO connector. The maximum power consumption allowed for a daughter card connected to one or two GPIO ports is shown in Table 3-9 and Table 3-10 shows all the pin assignments of the GPIO connector.



GPIO 0 (JP1)

PIN_V12	GPIO_0[0]	1	2	GPIO_0[1]	PIN_AF7
PIN_W12	GPIO_0[2]	3	4	GPIO_0[3]	PIN_AF8
PIN_Y8	GPIO_0[4]	5	6	GPIO_0[5]	PIN_AB4
PIN_W8	GPIO_0[6]	7	8	GPIO_0[7]	PIN_Y4
PIN_Y5	GPIO_0[8]	9	10	GPIO_0[9]	PIN_U11
	5V	11	12	GND	
PIN_T8	GPIO_0[10]	13	14	GPIO_0[11]	PIN_T12
PIN_AH5	GPIO_0[12]	15	16	GPIO_0[13]	PIN_AH6
PIN_AH4	GPIO_0[14]	17	18	GPIO_0[15]	PIN_AG5
PIN_AH3	GPIO_0[16]	19	20	GPIO_0[17]	PIN_AH2
PIN_AF4	GPIO_0[18]	21	22	GPIO_0[19]	PIN_AG6
PIN_AF5	GPIO_0[20]	23	24	GPIO_0[21]	PIN_AE4
PIN_T13	GPIO_0[22]	25	26	GPIO_0[23]	PIN_T11
PIN_AE7	GPIO_0[24]	27	28	GPIO_0[25]	PIN_AF6
	3.3V	29	30	GND	
PIN_AF9	GPIO_0[26]	31	32	GPIO_0[27]	PIN_AE8
PIN_AD10	GPIO_0[28]	33	34	GPIO_0[29]	PIN_AE9
PIN_AD11	GPIO_0[30]	35	36	GPIO_0[31]	PIN_AF10
PIN_AD12	GPIO_0[32]	37	38	GPIO_0[33]	PIN_AE11
PIN_AF11	GPIO_0[34]	39	40	GPIO_0[35]	PIN_AE12

GPIO 1 (JP7)

PIN_Y15	GPIO_1[0]	1	2	GPIO_1[1]	PIN_AG28
PIN_AA15	GPIO_1[2]	3	4	GPIO_1[3]	PIN_AH27
PIN_AG26	GPIO_1[4]	5	6	GPIO_1[5]	PIN_AH24
PIN_AF23	GPIO_1[6]	7	8	GPIO_1[7]	PIN_AE22
PIN_AF21	GPIO_1[8]	9	10	GPIO_1[9]	PIN_AG20
	5V	11	12	GND	
PIN_AG19	GPIO_1[10]	13	14	GPIO_1[11]	PIN_AF20
PIN_AC23	GPIO_1[12]	15	16	GPIO_1[13]	PIN_AG18
PIN_AH26	GPIO_1[14]	17	18	GPIO_1[15]	PIN_AA19
PIN_AG24	GPIO_1[16]	19	20	GPIO_1[17]	PIN_AF25
PIN_AH23	GPIO_1[18]	21	22	GPIO_1[19]	PIN_AG23
PIN_AE19	GPIO_1[20]	23	24	GPIO_1[21]	PIN_AF18
PIN_AD19	GPIO_1[22]	25	26	GPIO_1[23]	PIN_AE20
PIN_AE24	GPIO_1[24]	27	28	GPIO_1[25]	PIN_AD20
	3.3V	29	30	GND	
PIN_AF22	GPIO_1[26]	31	32	GPIO_1[27]	PIN_AH22
PIN_AH19	GPIO_1[28]	33	34	GPIO_1[29]	PIN_AH21
PIN_AG21	GPIO_1[30]	35	36	GPIO_1[31]	PIN_AH18
PIN_AD23	GPIO_1[32]	37	38	GPIO_1[33]	PIN_AE23
PIN_AA18	GPIO_1[34]	39	40	GPIO_1[35]	PIN_AC22

Figure 3-10 GPIO Pin Arrangement

Table 3-9 Voltage and Max. Current Limit of Expansion Header(s)

Supplied Voltage	*Max. Current Limit*
5V	1A (depend on the power adapter specification.)
3.3V	1.5A

Table 3-10 Pin Assignment of Expansion Headers

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
GPIO_0[0]	PIN_V12	GPIO Connection 0[0]	3.3V
GPIO_0[1]	PIN_AF7	GPIO Connection 0[1]	3.3V
GPIO_0[2]	PIN_W12	GPIO Connection 0[2]	3.3V
GPIO_0[3]	PIN_AF8	GPIO Connection 0[3]	3.3V
GPIO_0[4]	PIN_Y8	GPIO Connection 0[4]	3.3V
GPIO_0[5]	PIN_AB4	GPIO Connection 0[5]	3.3V
GPIO_0[6]	PIN_W8	GPIO Connection 0[6]	3.3V
GPIO_0[7]	PIN_Y4	GPIO Connection 0[7]	3.3V
GPIO_0[8]	PIN_Y5	GPIO Connection 0[8]	3.3V
GPIO_0[9]	PIN_U11	GPIO Connection 0[9]	3.3V
GPIO_0[10]	PIN_T8	GPIO Connection 0[10]	3.3V
GPIO_0[11]	PIN_T12	GPIO Connection 0[11]	3.3V
GPIO_0[12]	PIN_AH5	GPIO Connection 0[12]	3.3V
GPIO_0[13]	PIN_AH6	GPIO Connection 0[13]	3.3V
GPIO_0[14]	PIN_AH4	GPIO Connection 0[14]	3.3V
GPIO_0[15]	PIN_AG5	GPIO Connection 0[15]	3.3V
GPIO_0[16]	PIN_AH3	GPIO Connection 0[16]	3.3V
GPIO_0[17]	PIN_AH2	GPIO Connection 0[17]	3.3V
GPIO_0[18]	PIN_AF4	GPIO Connection 0[18]	3.3V
GPIO_0[19]	PIN_AG6	GPIO Connection 0[19]	3.3V
GPIO_0[20]	PIN_AF5	GPIO Connection 0[20]	3.3V
GPIO_0[21]	PIN_AE4	GPIO Connection 0[21]	3.3V
GPIO_0[22]	PIN_T13	GPIO Connection 0[22]	3.3V
GPIO_0[23]	PIN_T11	GPIO Connection 0[23]	3.3V
GPIO_0[24]	PIN_AE7	GPIO Connection 0[24]	3.3V
GPIO_0[25]	PIN_AF6	GPIO Connection 0[25]	3.3V
GPIO_0[26]	PIN_AF9	GPIO Connection 0[26]	3.3V
GPIO_0[27]	PIN_AE8	GPIO Connection 0[27]	3.3V
GPIO_0[28]	PIN_AD10	GPIO Connection 0[28]	3.3V
GPIO_0[29]	PIN_AE9	GPIO Connection 0[29]	3.3V
GPIO_0[30]	PIN_AD11	GPIO Connection 0[30]	3.3V
GPIO_0[31]	PIN_AF10	GPIO Connection 0[31]	3.3V
GPIO_0[32]	PIN_AD12	GPIO Connection 0[32]	3.3V
GPIO_0[33]	PIN_AE11	GPIO Connection 0[33]	3.3V
GPIO_0[34]	PIN_AF11	GPIO Connection 0[34]	3.3V
GPIO_0[35]	PIN_AE12	GPIO Connection 0[35]	3.3V
GPIO_1[0]	PIN_Y15	GPIO Connection 1[0]	3.3V
GPIO_1[1]	PIN_AG28	GPIO Connection 1[1]	3.3V

GPIO_1[2]	PIN_AA15	GPIO Connection 1[2]	3.3V
GPIO_1[3]	PIN_AH27	GPIO Connection 1[3]	3.3V
GPIO_1[4]	PIN_AG26	GPIO Connection 1[4]	3.3V
GPIO_1[5]	PIN_AH24	GPIO Connection 1[5]	3.3V
GPIO_1[6]	PIN_AF23	GPIO Connection 1[6]	3.3V
GPIO_1[7]	PIN_AE22	GPIO Connection 1[7]	3.3V
GPIO_1[8]	PIN_AF21	GPIO Connection 1[8]	3.3V
GPIO_1[9]	PIN_AG20	GPIO Connection 1[9]	3.3V
GPIO_1[10]	PIN_AG19	GPIO Connection 1[10]	3.3V
GPIO_1[11]	PIN_AF20	GPIO Connection 1[11]	3.3V
GPIO_1[12]	PIN_AC23	GPIO Connection 1[12]	3.3V
GPIO_1[13]	PIN_AG18	GPIO Connection 1[13]	3.3V
GPIO_1[14]	PIN_AH26	GPIO Connection 1[14]	3.3V
GPIO_1[15]	PIN_AA19	GPIO Connection 1[15]	3.3V
GPIO_1[16]	PIN_AG24	GPIO Connection 1[16]	3.3V
GPIO_1[17]	PIN_AF25	GPIO Connection 1[17]	3.3V
GPIO_1[18]	PIN_AH23	GPIO Connection 1[18]	3.3V
GPIO_1[19]	PIN_AG23	GPIO Connection 1[19]	3.3V
GPIO_1[20]	PIN_AE19	GPIO Connection 1[20]	3.3V
GPIO_1[21]	PIN_AF18	GPIO Connection 1[21]	3.3V
GPIO_1[22]	PIN_AD19	GPIO Connection 1[22]	3.3V
GPIO_1[23]	PIN_AE20	GPIO Connection 1[23]	3.3V
GPIO_1[24]	PIN_AE24	GPIO Connection 1[24]	3.3V
GPIO_1[25]	PIN_AD20	GPIO Connection 1[25]	3.3V
GPIO_1[26]	PIN_AF22	GPIO Connection 1[26]	3.3V
GPIO_1[27]	PIN_AH22	GPIO Connection 1[27]	3.3V
GPIO_1[28]	PIN_AH19	GPIO Connection 1[28]	3.3V
GPIO_1[29]	PIN_AH21	GPIO Connection 1[29]	3.3V
GPIO_1[30]	PIN_AG21	GPIO Connection 1[30]	3.3V
GPIO_1[31]	PIN_AH18	GPIO Connection 1[31]	3.3V
GPIO_1[32]	PIN_AD23	GPIO Connection 1[32]	3.3V
GPIO_1[33]	PIN_AE23	GPIO Connection 1[33]	3.3V
GPIO_1[34]	PIN_AA18	GPIO Connection 1[34]	3.3V
GPIO_1[35]	PIN_AC22	GPIO Connection 1[35]	3.3V

3.6.3 Arduino Uno R3 Expansion Header

The board provides Arduino Uno revision 3 compatibility expansion header which comes with four independent headers. The expansion header has 17 user pins (16pins GPIO and 1pin Reset) connected directly to the Cyclone V SoC FPGA. 6-pins Analog input connects to ADC, and also provides DC +9V (VCC9), DC +5V (VCC5), DC +3.3V (VCC3P3 and IOREF), and three GND pins.

Please refer to **Figure 3-11** for detailed pin-out information. The blue font represents the Arduino Uno R3 board pin-out definition.

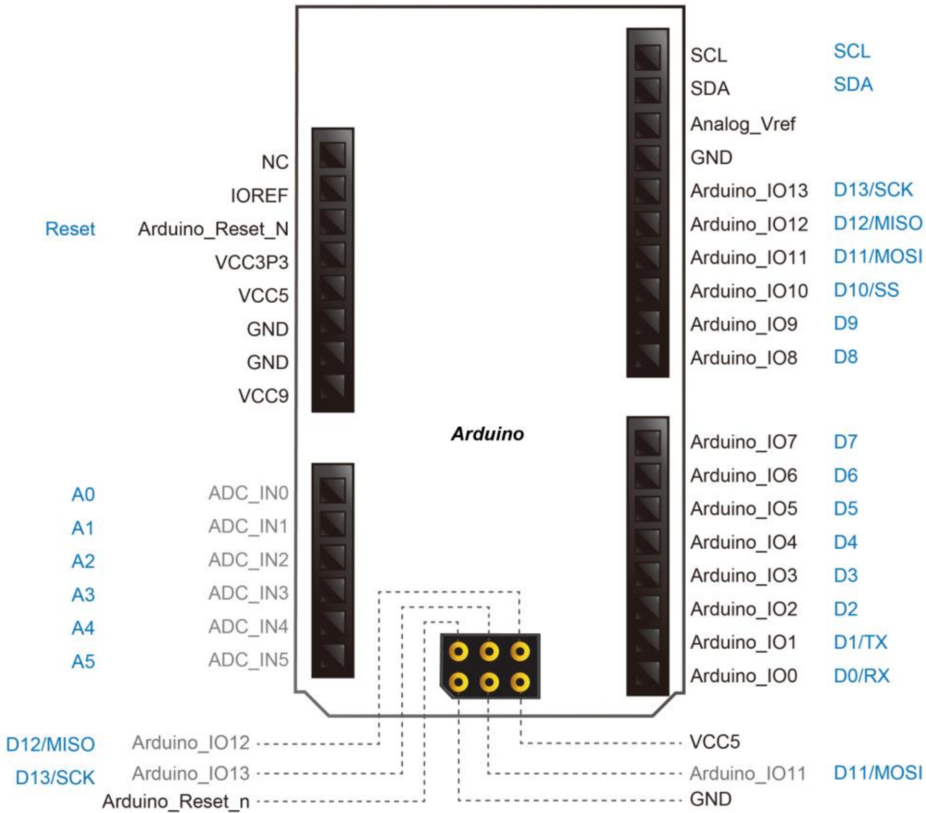


Figure 3-11 lists the all the pin-out signal name of the Arduino Uno connector. The blue font represents the Arduino pin-out definition.

The 16 GPIO pins are provided to the Arduino Header for digital I/O. **Table 3-11** lists the all the pin assignments of the Arduino Uno connector (digital), signal names relative to the Cyclone V SoC FPGA.

Table 3-11 Pin Assignments for Arduino Uno Expansion Header connector

Schematic Signal Name	*FPGA Pin No.*	*Description*	*Specific features For Arduino*	*I/O Standard*
Arduino_IO0	PIN_AG13	Arduino IO0	RXD	3.3-V
Arduino_IO1	PIN_AF13	Arduino IO1	TXD	3.3-V
Arduino_IO2	PIN_AG10	Arduino IO2		3.3-V
Arduino_IO3	PIN_AG9	Arduino IO3		3.3-V
Arduino_IO4	PIN_U14	Arduino IO4		3.3-V
Arduino_IO5	PIN_U13	Arduino IO5		3.3-V
Arduino_IO6	PIN_AG8	Arduino IO6		3.3-V
Arduino_IO7	PIN_AH8	Arduino IO7		3.3-V
Arduino_IO8	PIN_AF17	Arduino IO8		3.3-V
Arduino_IO9	PIN_AE15	Arduino IO9		3.3-V
Arduino_IO10	PIN_AF15	Arduino IO10	SS	3.3-V
Arduino_IO11	PIN_AG16	Arduino IO11	MOSI	3.3-V
Arduino_IO12	PIN_AH11	Arduino IO12	MISO	3.3-V
Arduino_IO13	PIN_AH12	Arduino IO13	SCK	3.3-V
Arduino_IO14	PIN_AH9	Arduino IO14	SDA	3.3-V
Arduino_IO15	PIN_AG11	Arduino IO15	SCL	3.3-V
Arduino_Reset_n	PIN_AH7	Reset signal, low active.		3.3-V

Besides 16 pins for digital GPIO, there are also 6 analog inputs on the Arduino Uno R3 Expansion Header (ADC_IN0 ~ ADC_IN5). Consequently, we use ADC LTC2308 from Linear Technology on the board for possible future analog-to-digital applications. We will introduce in the next section.

3.6.4 A/D Converter and Analog Input

The Atlas-SoC has an analog-to-digital converter (LTC2308).

The LTC2308 is a low noise, 500ksps, 8-channel, 12-bit ADC with a SPI/MICROWIRE compatible serial interface. This ADC includes an internal reference and a fully differential sample-and-hold circuit to reduce common mode noise. The internal conversion clock allows the external serial output data clock (SCK) to operate at any frequency up to 40MHz.

It can be configured to accept eight input signals at inputs ADC_IN0 through ADC_IN7. These eight input signals are connected to a 2x5 header, as shown in **Figure 3-12**.

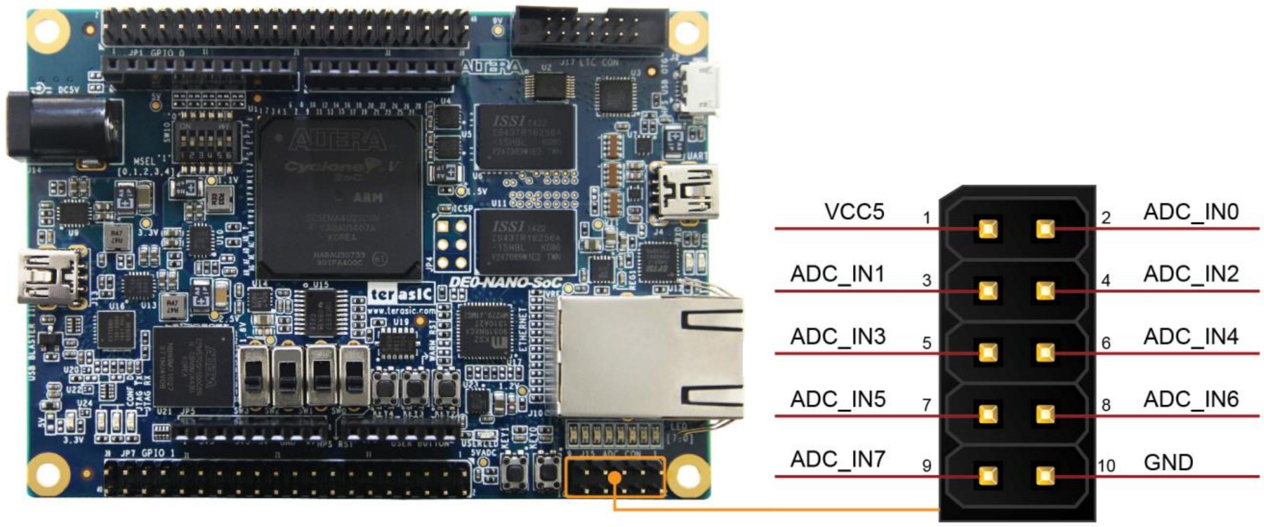


Figure 3-12 Signals of the 2x5 Header

These Analog inputs are shared with the Arduino's analog input pin (ADC_IN0 ~ ADC_IN5), Figure 3-13 shows the connections between the FPGA, 2x5 header, Arduino Analog input, and the A/D converter.

More information about the A/D converter chip can be found on manufacturer's website (http://www.linear.com/product/LTC2308).

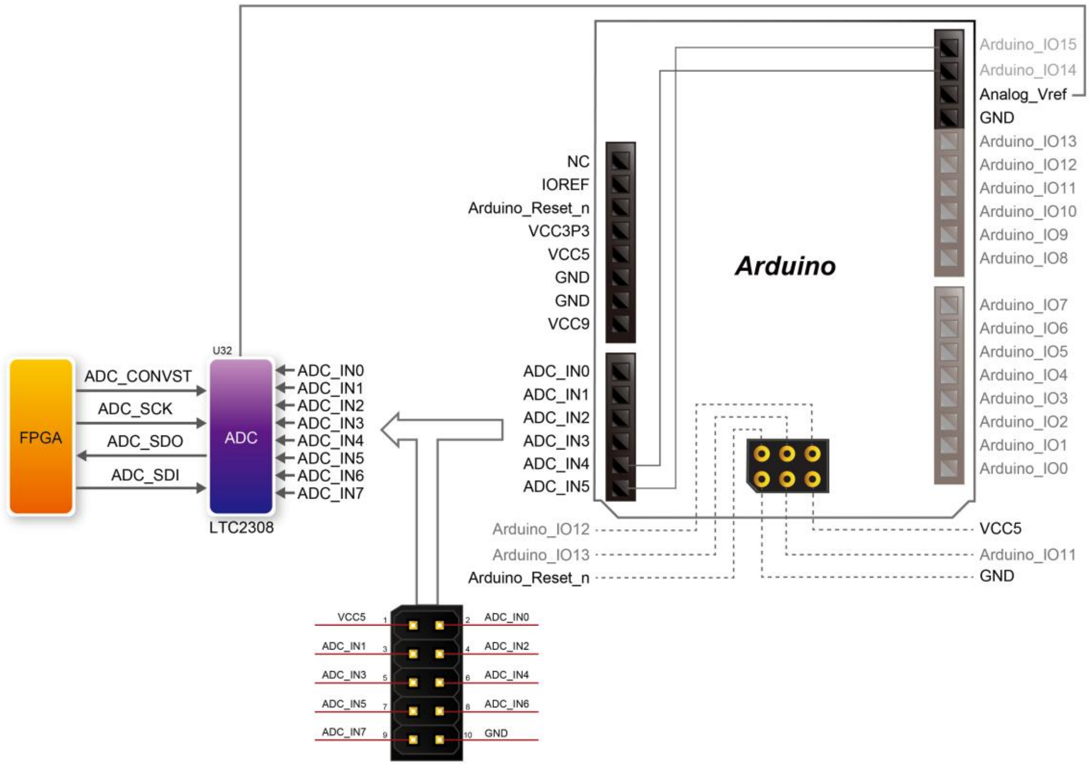


Figure 3-13 Connections between the FPGA, 2x5 header, and the A/D converter