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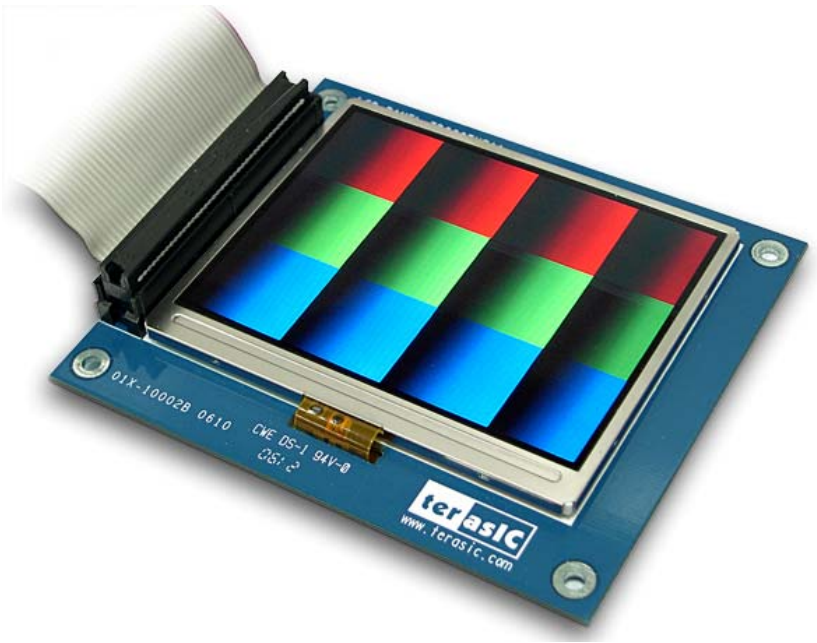
TRDB_LCM



3.6 Inch Digital Panel Development Kit

With Complete Reference Design and source code for NTSC/PAL TV Player and Pattern Generator using Altera DE2/DE1 Board

TRDB_LCM

Document Version 1.2 NOV. 30, 2006 by Terasic

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Chapter 1

About the Kit

The TRDB_LCM Kit provides everything you need to develop applications using a digital panel on the Altera DE2/DE1 board. The kit contains complete reference designs and source code for implementing a TV player or a Color Pattern Generator using the TRDB_LCM and Altera DE2/DE1. This chapter provides users key information about the kit.

Kit Contents

Figure 1.1 shows the photo of the key LCD module in the TRDB_LCM package. The package includes:

1. The TRDB_LCM board.
2. An 40-pin IDE cable.
3. A reference design CD-ROM.

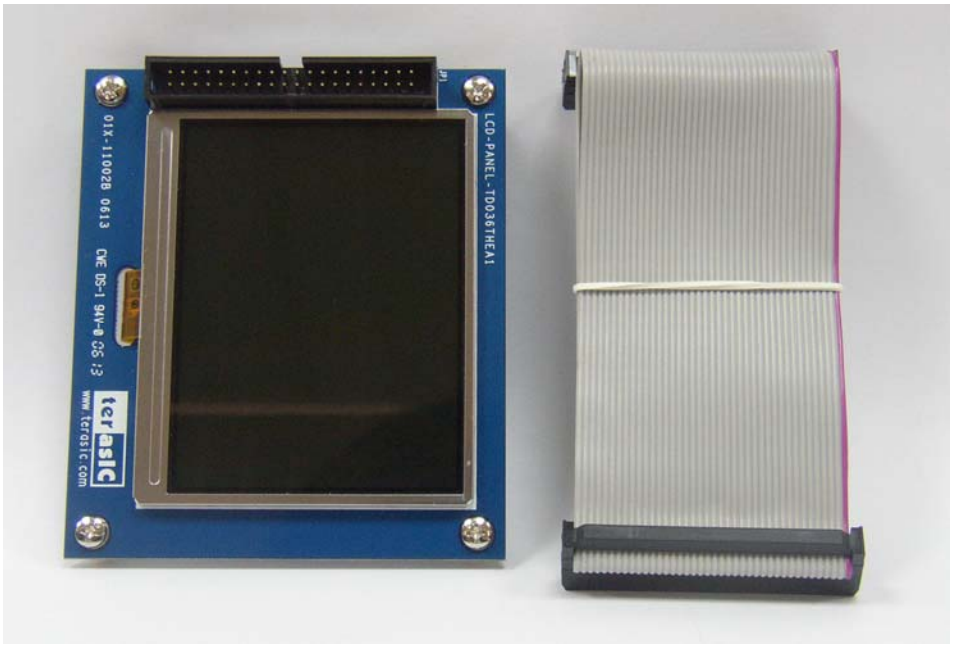

Figure 1.1. The TRDB_LCM Module and Cable

Assemble the Digital Panel

Please follow the two steps below to assemble your camera:

1. Connect the IDE cable to the back of the TRDB_LCM board, as shown in Figure 1.2.
2. Connect the other end of the IDE cable to your DE2/DE1 board as shown in Figure 1.3.

Figure 1.2 Connect the IDE cable to the TRDB_LCM board

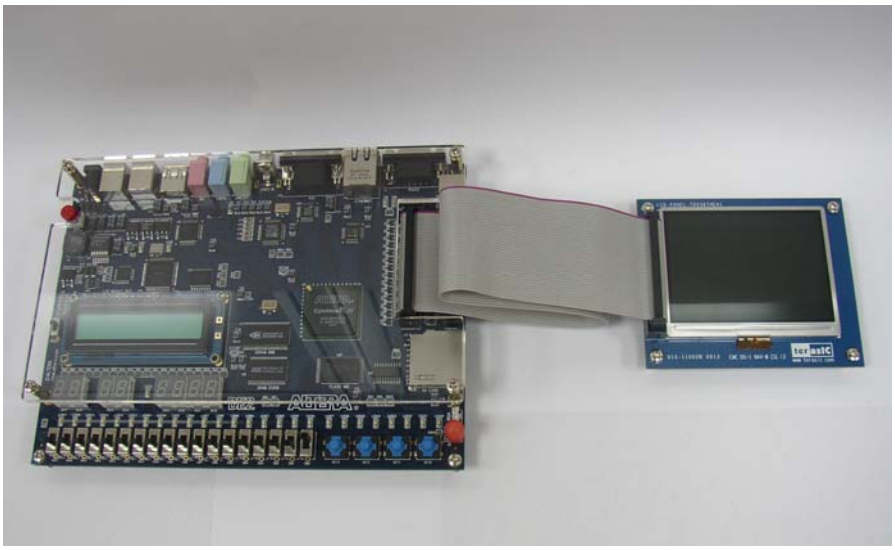

Figure 1.3 Connect the other end of IDE cable to the DE2/DE1 board's expansion port (innermost port)

Getting Help

Here are some places to get help if you encounter any problem:

- ✓ Email to support@terasic.com
- ✓ Taiwan & China: +886-3-550-8800
- ✓ Korea : +82-2-512-7661
- ✓ Japan: +81-428-77-7000
- ✓ English Support Line: +1-408-512-1336

Chapter 2

TRDB_LCM

This chapter will illustrate the technical details users need to know to modify the reference design for their own purpose.

Features

The feature set of the TRDB_LCM is listed below:

1. Equipped with Toppoly TD036THEA1 compact TFT LCD module.
2. Handle digital signals of serial 8-bit (RGB or YUV).
3. Support NTSC and PAL timings.
4. 3-wire register control for display and function selection.
5. Built-in contrast, brightness and gamma modulation.
6. Support strip color filter 960x240(through mode, RGB dummy, YUV input).
7. The general specifications of Panel is listed below:

Item	Description	Unit
Display Size (Diagonal)	3.6	Inch
Display Type	Transmissive	-
Active Area (HxV)	72.96 x 54.72	mm
Number of Dots (HxV)	320 x RGB x 240	dot
Dot Pitch (HxV)	0.076 x 0.228	mm
Color Arrangement	RGB Stripe	-
Color Numbers	8 bit RGB (16M color)	-

Schematic of the Board

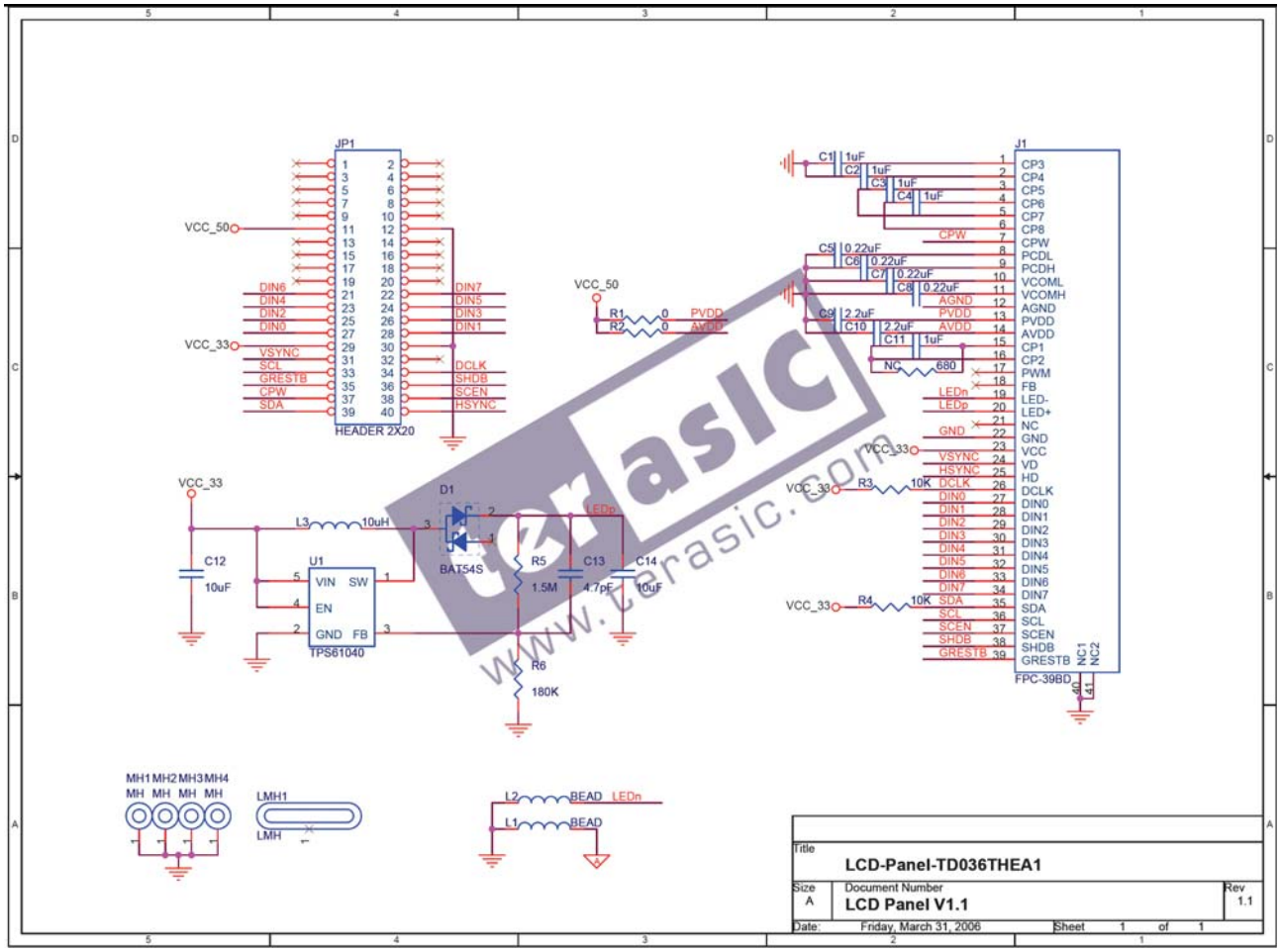

Figure 2.1. Schematic of the TRDB_LCM

Pin Description of the 40-pin Interface of TRDB_LCM

The TRDB_LCM has a 40-pin connector. The pin description of the 40-pin connector follows:

Pin Numbers	Name	Direction	Description
1~10	NC	N/A	Not connect
11	VCC5	N/A	Power 5V
12	GND	N/A	Ground
13~20	NC	N/A	Not connect
21	DIN6	Input	LCD data bus bit 7
22	DIN7	Input	LCD data bus bit 6
23	DIN4	Input	LCD data bus bit 4
24	DIN5	Input	LCD data bus bit 5
25	DIN2	Input	LCD data bus bit 2
26	DIN3	Input	LCD data bus bit 3
27	DIN0	Input	LCD data bus bit 0
28	DIN1	Input	LCD data bus bit 1
29	VCC33	N/A	Power 3.3V
30	NC	N/A	Not connect
31	VSYNC	Input	Vertical sync input
32	NC	N/A	Not connect
33	SCL	Input	3-wire serial interface clock
34	DCLK	Input	LCD data clock
35	GRESTB	Input	Global reset, low active
36	SHDB	Input	Shutdown control, low active
37	CPW	N/A	Reserved
38	SCEN	Input	3-wire serial interface enable
39	SDA	Input/Output	3-wire serial interface data
40	HSYNC	Input	Horizontal sync input

Chapter 3

Digital Panel Design Demonstration

This chapter illustrates how to exercise the digital panel reference design provided with the kit. Users can follow the instructions in this chapter to build a 3.6 inch TV player (DE2 user only) and pattern generator using the DE2/DE1 in 5 minutes.

Demonstration Setup

The Demonstration configuration is illustrated as Figure 3.1. The YUV 4:2:2 data is sent from TV decoder to the cyclone II 2C35 FPGA. The FPGA on the DE2/DE1 board is handling image processing part and set the LCD module control register to display on the TRDB_LCM.

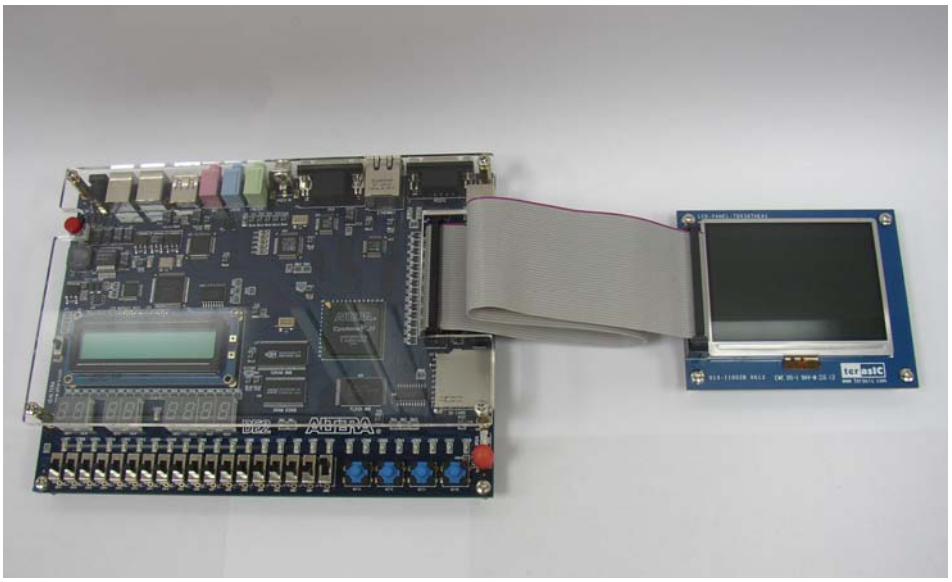

Figure 3.1. The TV player Demo configuration setup

Configuring the TV Player (DE2 User Only)

Locate the project directory from the CD-ROM included and follow the steps below:

For DE2 boards with Serial Number (S/N) starting with Digit 0

Quartus II Project Directory: DE2_LCM_TV/For_DE2_SN_0X

For DE2 boards with Serial Number (S/N) starting with Digit 1

Quartus II Project Directory: DE2_LCM_TV/For_DE2_SN_1X

FPGA Bitstream Used: DE2_LCM_TV.sof or **DE2_LCM_TV.pof**

1. Ensure the connection is made correctly as shown in Figure 3.2. Make sure the IDE cable is connected to JP1 of the DE2 board.
2. Download the bitstream (DE2_LCM_TV.sof/pof) to the DE2 board.
3. Connect a DVD player's composite video output (yellow plug) to the Video-in RCA jack of the DE2 board.
4. Press KEY0 on the DE2 board to reset the circuit.

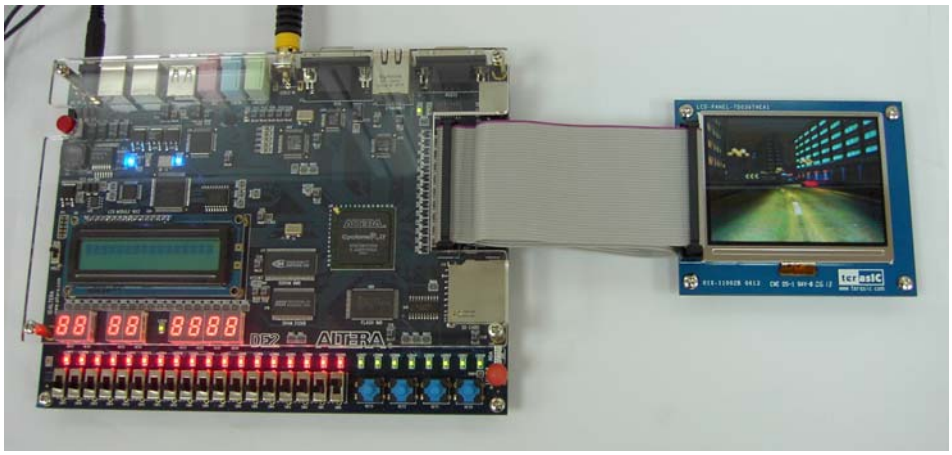

Figure 3.2. The connection setup for the TV player demo

Configuring the Pattern Generator

Locate the project directory from the CD-ROM included and follow the steps below:

For DE2 User:

Quartus II Project Directory: DE2_LCM_Test

FPGA Bitstream Used: DE2_LCM_Test.sof or **DE2_LCM_Test.pof**

For DE1 User:

Quartus II Project Directory: DE1_LCM_Test

FPGA Bitstream Used: DE1_LCM_Test.sof or **DE1_LCM_Test.pof**

1. Ensure the connection is made correctly as shown in Figure 3.3. Make sure the IDE cable is connected to JP1 of the DE2/DE1 board.
2. Download the bitstream to the DE2/DE1 board.
3. Press KEY0 on the DE2/DE1 board to reset the circuit.
4. You can press SW0 and SW1 to switch to the other Pattern.
5. The following table summarize the functional keys of the this demonstration.

Switch Setting	Function Description
SW[1:0] =[OFF,OFF]	Gray bar.
SW[1:0] =[OFF,ON]	Color bar.
SW[1:0] =[ON,OFF]	50% gray level pattern.
SW[1:0] =[ON,ON]	White pattern.

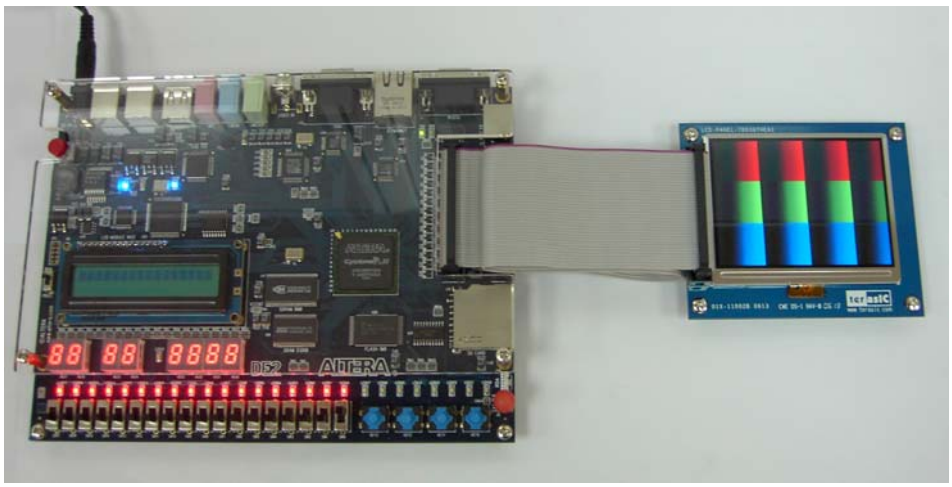

Figure 3.3. The connection setup for the pattern generator demo

Chapter 4

Appendix

Revision History

Date	Change Log
APR, 6, 2006	Initial Version (Preliminary)
OCT, 17, 2006	Added Labs for Altera DE1 Board (Cyclone II Starter Kit)
NOV, 30, 2006	Updated DE2_LCM_TV project for DE2 v2.0 PCB.

Always Visit TRDB_LCM Webpage for New Applications

We will be continuing providing interesting examples and labs on our TRDB_LCM webpage. Please visit www.altera.com or **lcm.terasic.com** for more information.