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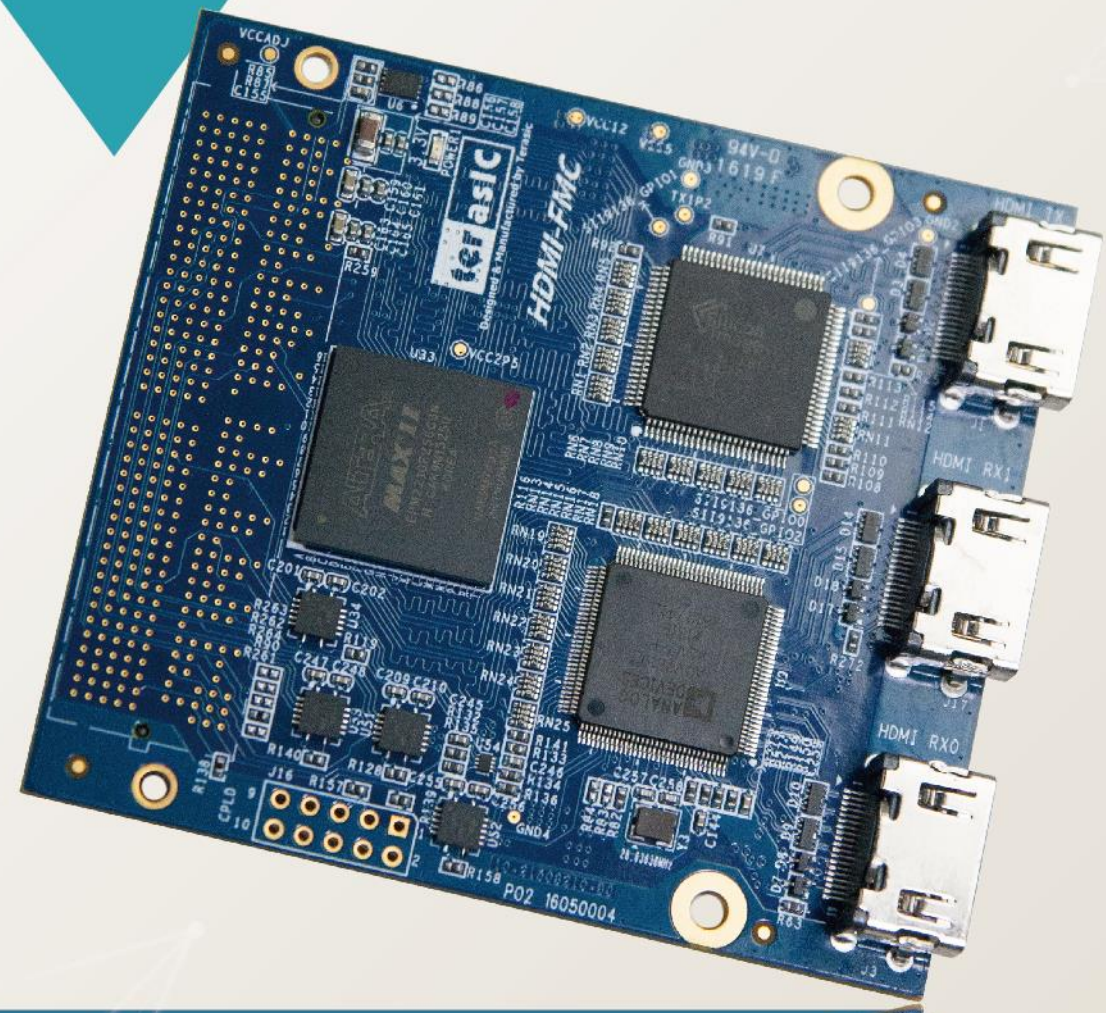
HDMI-FMC

User Manual



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HDMI-FMC
CONTENT

Chapter 1

HDMI-FMC Development Kit

Terasic HDMI-FMC is a HDMI transmitter/receiver daughter board with FMC(FPGA Mezzanine card) interface. The user can connect the HDMI module with the FPGA development kit via the FMC connector for HDMI image & video capture, processing and display up to 4K@30fps resolution.

The HDMI-FMC provides both the HDMI Tx and Rx Module with the HDMI 1.4a features supported. The Tx module is able to supports most common standard and non-standard video input format, most common 3D formats and the video resolution up to 8-bit 4K(30Hz)、12-bit 1080p(60Hz)、12-bit 720p/1080i (120 Hz),and 16-bit 1080p (30 Hz). The audio interface supports S/PDIF, DSD , I2S and HBR audio format input.

The Rx module is able to support all mandatory and additional 3D video formats and extended colorimetry(sYCC601, Adobe® RGB,Adobe YCC601, xvYCC extended gamut color CEC 1.4-compatible) with up to 36-bit Deep Color. the audio interface supports S/PDIF, SACD, DSD , I2S and HBR audio format output.

We also provide complete demo source codes for the HDMI-FMC working with different FPGA development kits. These demos are created by using Verilog HDL & ALTERA VIP, By referring to these demos, users can quickly develop their own applications.

1-1 Package Contents

The HDMI-FMC package includes:

- Product Box
- System CD Download Guide
- One HDMI-FMC module

Figure 1-1 The HDMI-FMC package contents

1-2 HDMI-FMC System CD

The HDMI-FMC System CD contains all the documents and supporting materials associated with HDMI-FMC, including the user manual, reference designs, and device datasheets. Users can download this system CD from the link: http://hdmi-fmc.terasic.com/cd.

1-3 Assemble the HDMI-FMC

Terasic HDMI-FMC is able to connect on to any FPGA development kit equiped with FMC(High-Pin Count) connector. The Below pictures **Figure 1-2** and **Figure 1-3** show the connections with 2 different Terasic FPGA Boards:

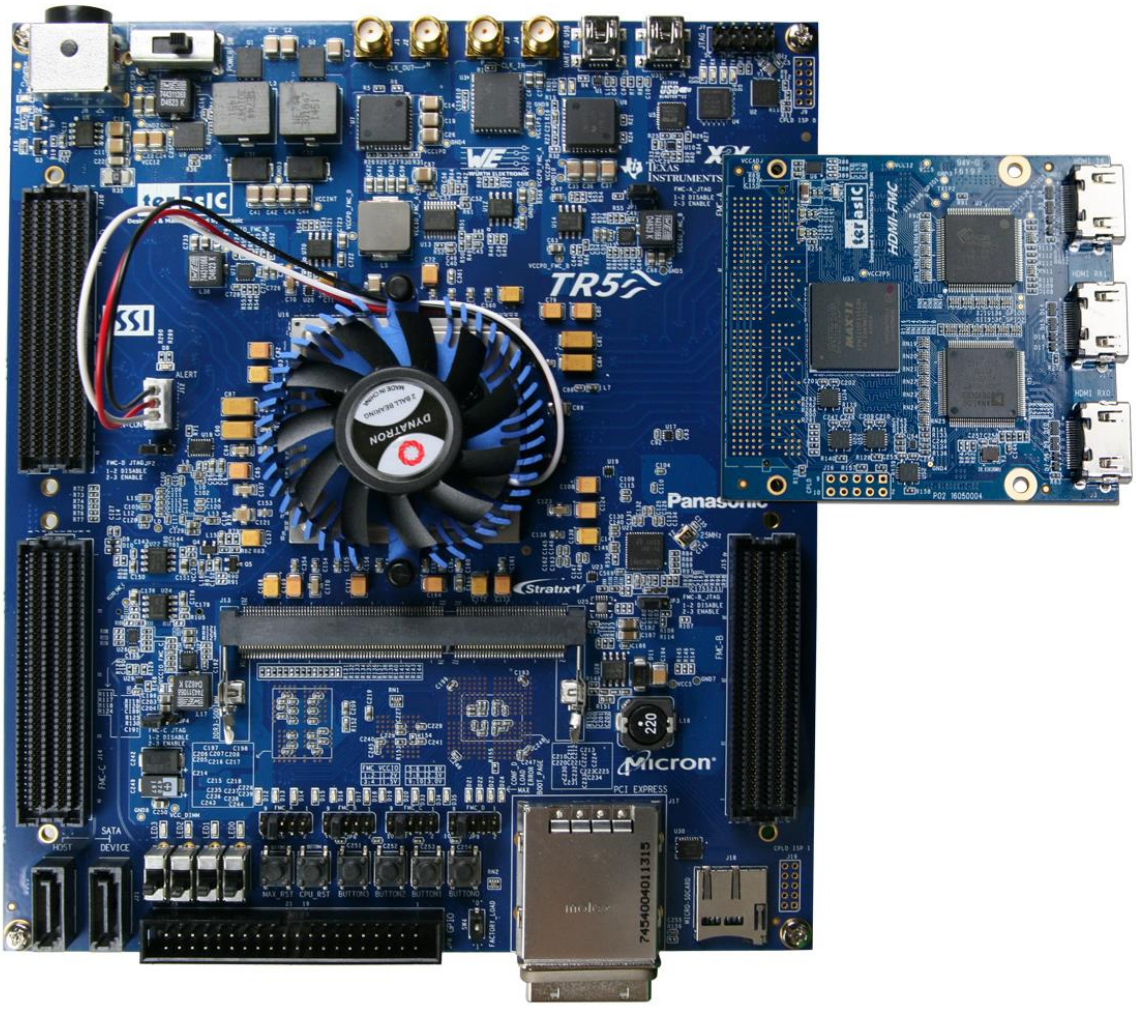

Figure 1-2 Connect the HDMI-FMC to TR5 board's FMCA port

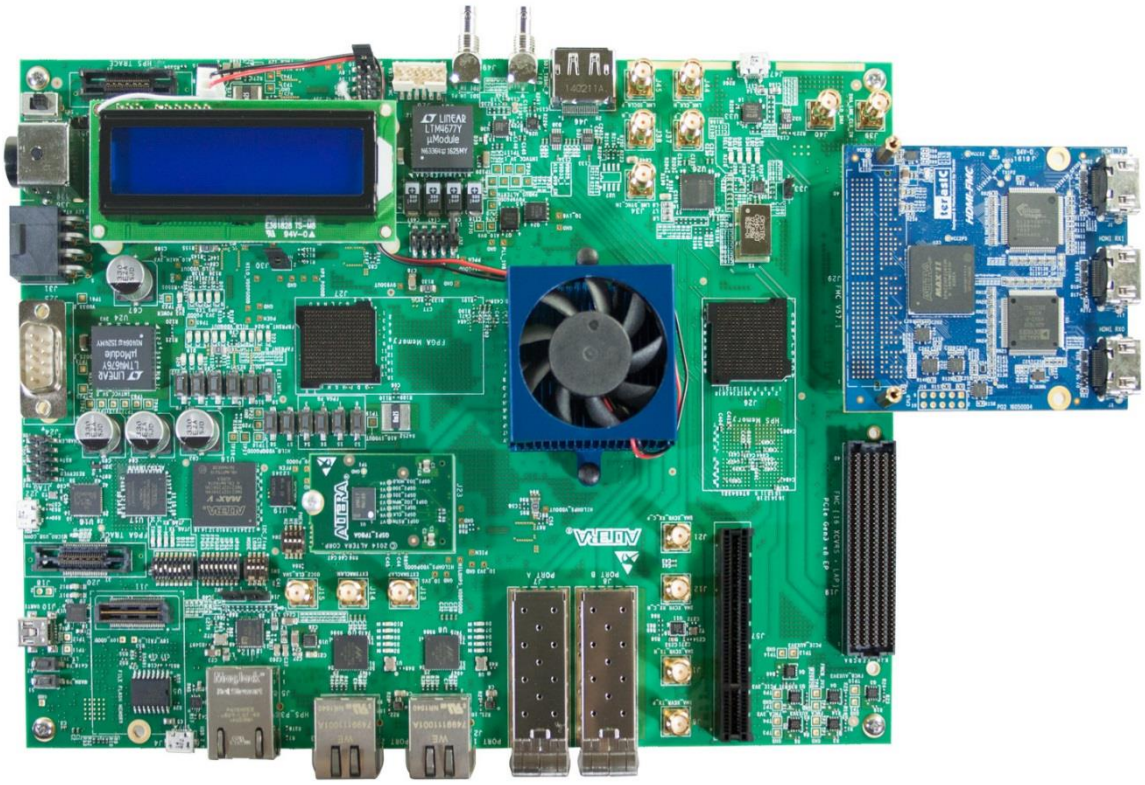

Figure 1-3 Connect the HDMI-FMC to A10SoC board's FMCA port

1-4 Getting Help

Here are the addresses where you can get help if you encounter any problems:

Terasic Technologies
9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan
Email: support@terasic.com
Tel.: +886-3-575-0880
Website:http://www.terasic.com

Chapter 2

Introduction of the HDMI-FMC Card

2-1 Features

Figure 2-1 shows a photograph of the card.

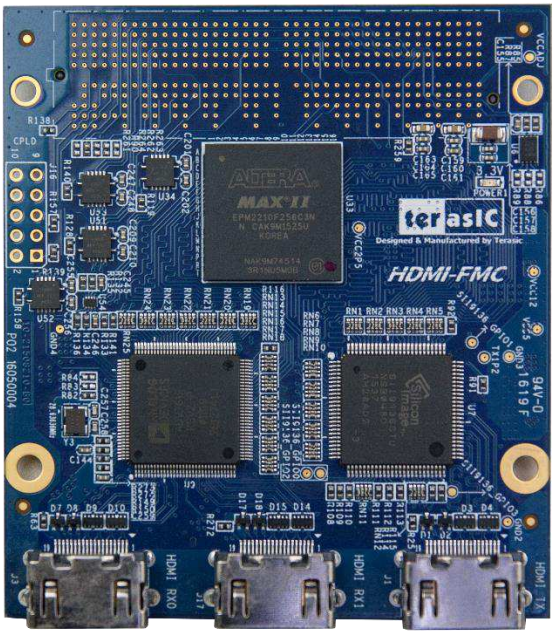

Figure 2-1 HDMI-FMC daughter card

The HDMI-FMC card has many features that allow users to implement a wide range of design circuits, from simple circuits to various multimedia projects.

The following hardware is provided on the board:

Package Interface：VITA 57.1 FMC, adjustable I/O-standard(1.5/1.8/2.5/3.0V).

Tx Module：

Tx Module

Color Space	Video Format	Clock Edge Mode	Bus Width/ Color Depth	SYNC	Input Pixel Clock (MHz)								
					480i	VGA 480p	XGA	720p	1080i	SXGA	1080p	UXGX	4k
RGB	4:4:4	Single	36/12	Sep	27	25/27	65	74.25	74.25	108	148.5	—	—
		Single	30/10	Sep	27	25/27	65	74.25	74.25	108	148.5	162	—
		Single	24/8	Sep	27	25/27	65	74.25	74.25	108	148.5	162	297
		Dual	12/8	Sep	27	25/27	65	74.25	74.25	—	—	—	—
		Dual	15/10	Sep	27	25/27	65	74.25	74.25	—	—	—	—
		Dual	18/12	Sep	27	25/27	65	74.25	74.25	—	—	—	—
		Dual	24/16	Sep	27	25/27	65	74.25	74.25	—	—	—	—
YCbCr xvYCC	4:4:4	Single	36/12	Sep	27	25/27	65	74.25	74.25	108	148.5	—	—
		Single	30/10	Sep	27	25/27	65	74.25	74.25	108	148.5	162	—
		Single	24/8	Sep	27	25/27	65	74.25	74.25	108	148.5	162	297
		Dual	12/8	Sep	27	25/27	65	74.25	74.25	—	—	—	—
		Dual	15/10	Sep	27	25/27	65	74.25	74.25	—	—	—	—
		Dual	18/12	Sep	27	25/27	65	74.25	74.25	—	—	—	—
		Dual	24/16	Sep	27	25/27	65	74.25	74.25	—	—	—	—
	4:2:2	Single	16/8 20/10 24/12	Sep	27	25/27	65	74.25	74.25	108	148.5	162	297
				Emb	27	25/27	65	74.25	74.25	108	148.5	162	297
		Single/ YC Mux	8/8 10/10 12/12	Sep	27	50/54	130	148.5	148.5	—	—	—	—
				Emb	27	50/54	130	148.5	148.5	—	—	—	—
				T1004	—	50/54	130	—	—	—	—	—	—

- **Chip P/N：Sil9136-3**
- **HDMI 1.4a/1.3, HDCP 1.4 and DVI Compliant**
- **Video fromats：4:4:4 RGB, 4:4:4/4:2:2 YCbCr**
- **Pixels resolution：4Kx2K@30Hz**
- **Pixels clock：DDR/SDR up to 300MHz**
- **3D format support**
- **High Bitrate Audio support**
- **It supports the following input video formats:**

Rx Module：

Rx Module

Color Space	Video Format	Clock Edge Mode	Bus Width/ Color Depth	SYNC	Input Pixel Clock (MHz)								
					480i	VGA 480p	XGA	720p	1080i	SXGA	1080p	UXGX	4k
RGB	4:4:4	Single	36/12	Sep	27	25/27	65	74.25	74.25	108	148.5	—	—
		Single	30/10	Sep	27	25/27	65	74.25	74.25	108	148.5	162	—
		Single	24/8	Sep	27	25/27	65	74.25	74.25	108	148.5	162	297
		Dual	12/8	Sep	27	25/27	65	74.25	74.25	—	—	—	—
		Dual	15/10	Sep	27	25/27	65	74.25	74.25	—	—	—	—
		Dual	18/12	Sep	27	25/27	65	74.25	74.25	—	—	—	—
		Dual	24/16	Sep	27	25/27	65	74.25	74.25	—	—	—	—
YCbCr xvYCC	4:4:4	Single	36/12	Sep	27	25/27	65	74.25	74.25	108	148.5	—	—
		Single	30/10	Sep	27	25/27	65	74.25	74.25	108	148.5	162	—
		Single	24/8	Sep	27	25/27	65	74.25	74.25	108	148.5	162	297
		Dual	12/8	Sep	27	25/27	65	74.25	74.25	—	—	—	—
		Dual	15/10	Sep	27	25/27	65	74.25	74.25	—	—	—	—
		Dual	18/12	Sep	27	25/27	65	74.25	74.25	—	—	—	—
		Dual	24/16	Sep	27	25/27	65	74.25	74.25	—	—	—	—
	4:2:2	Single	16/8 20/10 24/12	Sep	27	25/27	65	74.25	74.25	108	148.5	162	297
				Emb	27	25/27	65	74.25	74.25	108	148.5	162	297
		Single/ YC Mux	8/8 10/10 12/12	Sep	27	50/54	130	148.5	148.5	—	—	—	—
				Emb	27	50/54	130	148.5	148.5	—	—	—	—
				T1004	—	50/54	130	—	—	—	—	—	—

- **Chip P/N: ADV7619**
- **HDMI 1.4a/1.3, HDCP 1.4 and DVI Compliant**
- **Video formats: 4:4:4 RGB, 4:4:4/4:2:2 YCbCr**
- **Pixels resolution: 3840x2160@30Hz**
- **Pixels clock: DDR/SDR up to 297MHz**
- **It supports the following output video formats:**

Level Shift：

- **EPM2210**
- **I/O-Standard(1.5/1.8/2.5/3.0V)**

2-2 Block Diagram of the HDMI-FMC Board

Below **Figure 2-2** shows the HDMI-FMC Block Diagram. Level shift module outputs audio and video image data from FMC connector, which can be converted to TDMS data by passing through the Sil9136-3 to the HDMI TX connector. Similarly, HDMI RX connector receives all mandatory 3D TV formats defined in the HDMI 1.4a specification through a dual input HDMI-capable, which can be converted to audio and video image data by the ADV7619,and send to the FMC connector through Level shift. Both Sil9136-3 and ADV7619 can be controlled by FPGA I2C interface.

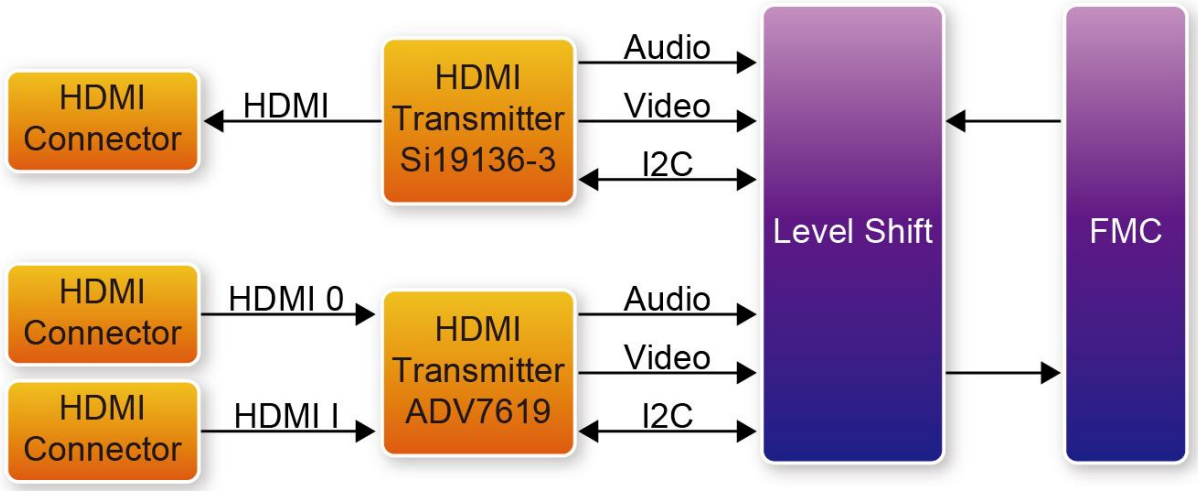

Figure 2-2 Block diagram of HDMI-FMC Board

Chapter 3

Using the HDMI-FMC Board

This chapter provides instructions on how to use Sil9136-3, ADV7619, Level shift and FMC connector on the HDMI-FMC board.

3-1 Sil9136-3

Sil9136-3 is a HDMI Deep Color transmitter and can deliver up to 16-bit Deep Color at 1080p/30Hz resolutions and 12-bit Deep Color at 1080p/60Hz resolutions. It merge independent video and audio streams for transmission over HDMI. For video data input, Sil9136-3 support most standard and non-standard video input formats and resolutions up to 8-bit 4K/30Hz, 12-bit 1080p/60Hz, 12-bit 720p/120 Hz, 12-bit 1080i/120 Hz, and 16-bit 1080p/30Hz. For audio input, it supports I2S, Direct Stream Digital, and S/PDIF audio input formats.
For HDMI output, DVI and HDMI transmitter with xvYCC extended color gamut, Deep Color up to 16-bit color, and high bitrate audio are all supported. The I2C address for TPI/CR of Sil9136-3 is 0x72/0x7A. **Figure 3-1** shows the system block diagram of Sil9136-3.

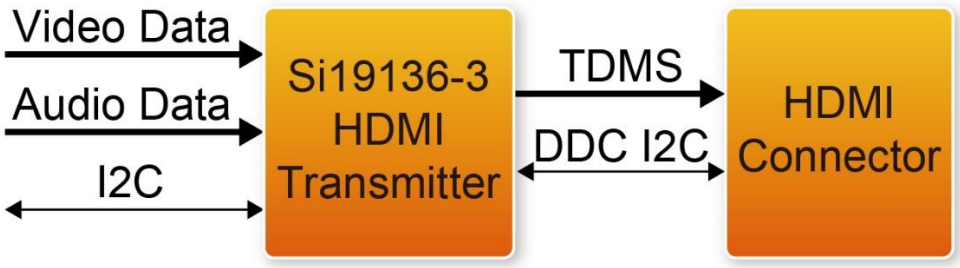

Figure 3-1 Sil9136-3 HDMI transmitter

The Sil9136-3 transmitter has four GPIO pins, and the value of each pin can be read or set through the local I2C bus. The sil9136-3 also contains a Consumer Electronics Control (CEC) interface which incorporates an HDMI-compliant CEC I/O and the Lattice CEC Programming Interface (CPI); this reduces the need for system-level control by the system microcontroller and simplifies firmware overhead.
There are individual components processing the video and audio input data. In the video data input and conversion block, the bus configurations support most standardized video input formats as well as other widely used non-standard formats. After configuration and processing, the clock, data, and sync information are combined into a complete set of signals required for further processing as follows. The

upsampler and downsampler block convert the 4:2:2 sampled video to 4:4:4 and 4:4:4 sampled video to 4:2:2 seperately. The two color space converters (CSCs, convert YCbCr to RGB and RGB to YCbCr) are available to interface to the many video formats supplied by A/V processors and provide full DVI backward compatibility. RGB range expression block scales the input color range from limited-range into full-range and RGB/YCbCr range compression compresses full-range data into limited-range data for each video channel. The clipping and dither function are also employed in the transmitter. The audio capture block supports I2S, Direct Stream Digital, and S/PDIF audio input formats. The appropriate registers must be configured to describe the audio format provided to the SiI9136-3 transmitter.

There is a TMDS transmitter for the output. The TMDS digital core performs 8-to-10-bit TMDS encoding and is then sent over three TMDS data and a TMDS clock differential lines. All of the above operations can be controlled by the configuration registers which can be accessed via the I2C interface.

3-2 ADV7619

A DV7619 is a high quality with two input ports and one output multiplexed High-Definition Multimedia Interface receiver. It supports all mandatory 3D TV formats defined in the HDMI 1.4 specification, HDTV formats up to 1080p 36-bit Deep Color/2160p 8-bit, and display resolutions up to 4k × 2k (3840 × 2160 at 30 Hz).

ADV7619 also supports extended colorimetry, including sYCC601, Adobe RGB, Adobe YCC601, xvYCC extended gamut color with a dual input HDMI-cable and 297MHz maximum TMDS clock frequency. The audio interface supports HBR、DSD、S/PDIF、SACD and four I2S output format. The receiver has advanced audio functionality, such as a mute controller, that prevents audible extraneous noise in the audio output. **Figure 3-2** shows the system block diagram of ADV7619.

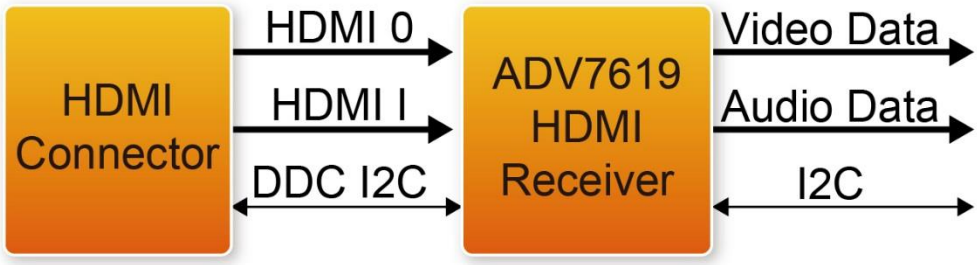

Figure 3-2 ADV7619 HDMI receiver

The HDMI-compatible receiver on the ADV7619 allows active equalization of the HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at longer cable lengths and higher frequencies. The HDMI-compatible receiver is capable of equalizing for cable lengths up to 30 meters to achieve robust receiver performance.

For video format with pixel clock higher than 170MHz, the video signals received on the HDMI receiver are outputed directly to the pixel port output. To accommodate the higher bandwidth required for these

higher resolutions, the output on the pixel bus consists of two 24-bit buses running at up to 150 MHz: one bus contains the even pixels, and the other bus contains the odd pixels. When these two buses are combined, they allow the transfer of video data with pixel clocks up to 300 MHz. In this mode, both 4:4:4 RGB 8-bit and 4:2:2 12-bit are supported.

3-3 Level shift

For the voltage matching between FMC connector and HDMI transmitter/receiver IC, EPM2210, LSF 0102 and TXB0104 are employed for the level shift. For HDMI transmitter/receiver IC, the I/O voltage is 3.3V while the I/O voltage of all four FMC connectors is adjustable within 1.2/1.5/1.8/2.5/3.0V.
The MAX II architecture supports the MultiVolt I/O interface feature, which allow the EPM2210 to interface with systems of different supply voltages. EPM2210 has one set of VCC pins for internal operation(VCCINT), and up to four sets for input buffering and I/O output drivers buffers(VCCIO). Users can connect VCCIO pins to either a 1.5/1.8/2.5/3.3V power supply, depending on the output requirement. The output levels are compatible with systems of the same voltage as the power supply. When VCCIO pins are connected to a 3.3V power supply, the output high is 3.3V and is compatible with 3.3V systems. When VCCIO pins are connect to 2.5V power supply, the output high is 2.5V and is compatible with 2.5V systems.
LSF0102 is a 2 channel bidirectional voltage level translator operational from 0.95 to 4.5 V on A port 1.8 to 5.5 V on B port. TXB0104 is a 4-bit bidirectional voltage level translator with auto direction sensing operational 1.2 to 3.6 V on A port and 1.65 to 5.5 V on B port. LSF0102 and TXB0104 are employed for the voltage translation of I2C and audio data.

Figure 3-3, Figure 3-4, Figure 3-5 gives an illustration of the level shift.

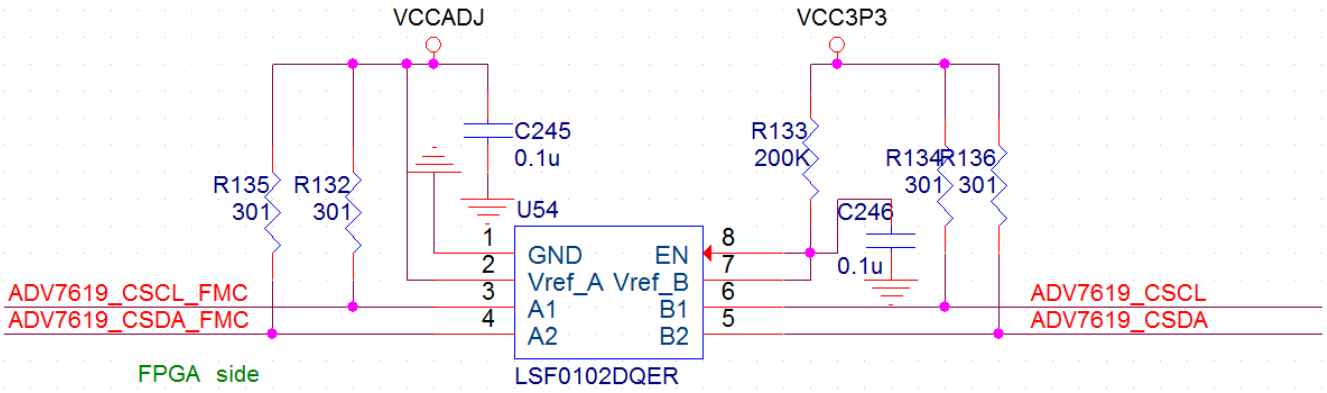

Figure 3-3 Voltage translation of I2C for Receiver

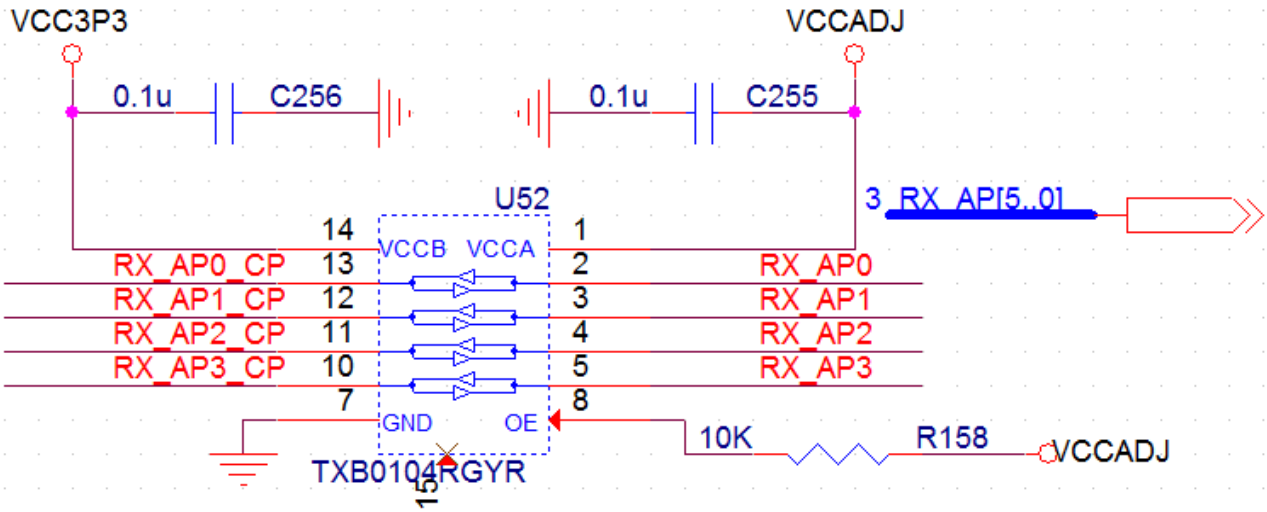

Figure 3-4 Voltage translation of audio data for receiver

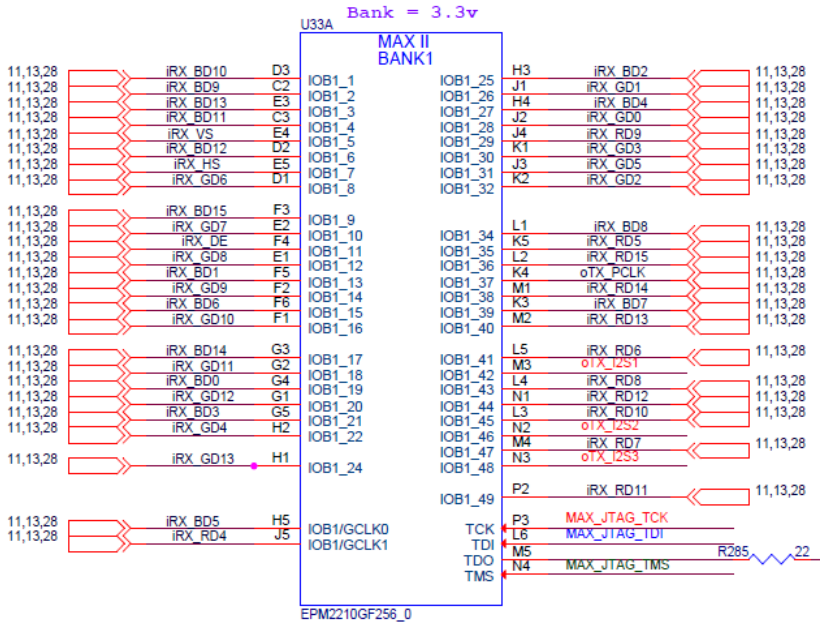

Figure 3-5 Level shift（EPM2210）

3-4 FMC Connector

Table 3-1 shows the pin out and pin definitions of the FMC connector.

Table 3-1 Pin Assignment of HDMI-FMC FMC interface

Signal Name	Pin Direction	Description	I/O Standard
TX_PCLK	Input	Transmitter pixel data clock	1.5/1.8/2.5/3.0/3.3V
TX_HS	Input	Transmitter Horizontal Synchronization signal	1.5/1.8/2.5/3.0/3.3V
TX_VS	Input	Transmitter Vertical Synchronization signal	1.5/1.8/2.5/3.0/3.3V
TX_DE	Input	Transmitter data enable	1.5/1.8/2.5/3.0/3.3V
TX_BD0	Input	Transmitter video blue data 0	1.5/1.8/2.5/3.0/3.3V
TX_BD1	Input	Transmitter video blue data 1	1.5/1.8/2.5/3.0/3.3V
TX_BD2	Input	Transmitter video blue data 2	1.5/1.8/2.5/3.0/3.3V
TX_BD3	Input	Transmitter video blue data 3	1.5/1.8/2.5/3.0/3.3V
TX_BD4	Input	Transmitter video blue data 4	1.5/1.8/2.5/3.0/3.3V
TX_BD5	Input	Transmitter video blue data 5	1.5/1.8/2.5/3.0/3.3V
TX_BD6	Input	Transmitter video blue data 6	1.5/1.8/2.5/3.0/3.3V
TX_BD7	Input	Transmitter video blue data 7	1.5/1.8/2.5/3.0/3.3V
TX_BD8	Input	Transmitter video blue data 8	1.5/1.8/2.5/3.0/3.3V
TX_BD9	Input	Transmitter video blue data 9	1.5/1.8/2.5/3.0/3.3V
TX_BD10	Input	Transmitter video blue data 10	1.5/1.8/2.5/3.0/3.3V
TX_BD11	Input	Transmitter video blue data 11	1.5/1.8/2.5/3.0/3.3V
TX_GD0	Input	Transmitter video green data 0	1.5/1.8/2.5/3.0/3.3V
TX_GD1	Input	Transmitter video green data 1	1.5/1.8/2.5/3.0/3.3V
TX_GD2	Input	Transmitter video green data 2	1.5/1.8/2.5/3.0/3.3V
TX_GD3	Input	Transmitter video green data 3	1.5/1.8/2.5/3.0/3.3V
TX_GD4	Input	Transmitter video green data 4	1.5/1.8/2.5/3.0/3.3V
TX_GD5	Input	Transmitter video green data 5	1.5/1.8/2.5/3.0/3.3V
TX_GD6	Input	Transmitter video green data 6	1.5/1.8/2.5/3.0/3.3V
TX_GD7	Input	Transmitter video green data 7	1.5/1.8/2.5/3.0/3.3V
TX_GD8	Input	Transmitter video green data 8	1.5/1.8/2.5/3.0/3.3V
TX_GD9	Input	Transmitter video green data 9	1.5/1.8/2.5/3.0/3.3V
TX_GD10	Input	Transmitter video green data 10	1.5/1.8/2.5/3.0/3.3V
TX_GD11	Input	Transmitter video green data 11	1.5/1.8/2.5/3.0/3.3V
TX_RD0	Input	Transmitter video red data 0	1.5/1.8/2.5/3.0/3.3V
TX_RD1	Input	Transmitter video red data 1	1.5/1.8/2.5/3.0/3.3V
TX_RD2	Input	Transmitter video red data 2	1.5/1.8/2.5/3.0/3.3V
TX_RD3	Input	Transmitter video red data 3	1.5/1.8/2.5/3.0/3.3V

TX_RD4	Input	Transmitter video red data 4	1.5/1.8/2.5/3.0/3.3V
TX_RD5	Input	Transmitter video red data 5	1.5/1.8/2.5/3.0/3.3V
TX_RD6	Input	Transmitter video red data 6	1.5/1.8/2.5/3.0/3.3V
TX_RD7	Input	Transmitter video red data 7	1.5/1.8/2.5/3.0/3.3V
TX_RD8	Input	Transmitter video red data 8	1.5/1.8/2.5/3.0/3.3V
TX_RD9	Input	Transmitter video red data 9	1.5/1.8/2.5/3.0/3.3V
TX_RD10	Input	Transmitter video red data 10	1.5/1.8/2.5/3.0/3.3V
TX_RD11	Input	Transmitter video red data 11	1.5/1.8/2.5/3.0/3.3V
TX_MCLK	Input	Transmitter audio input master clock(I2S、S/PDIF Mode)	1.5/1.8/2.5/3.0/3.3V
TX_SCK	Input	Transmitter I2S serial clock(I2S、S/PDIF Mode)、DSD clock(DSD Mode)	1.5/1.8/2.5/3.0/3.3V
TX_WS	Input	Transmitter I2S word select(I2S、S/PDIF Mode)、DSD data（DSD Mode）	1.5/1.8/2.5/3.0/3.3V
TX_SPDIF	Input	Transmitter S/PDIF input.(SPDIF Mode)、DSD data（DSD Mode）	1.5/1.8/2.5/3.0/3.3V
TX_I2S0	Input	Transmitter I2S data 0(I2S、S/PDIF Mode)	1.5/1.8/2.5/3.0/3.3V
TX_I2S1	Input	Transmitter I2S data 1(I2S、S/PDIF Mode)	1.5/1.8/2.5/3.0/3.3V
TX_I2S2	Input	Transmitter I2S data 2(I2S、S/PDIF Mode)	1.5/1.8/2.5/3.0/3.3V
TX_I2S3	Input	Transmitter I2S data 3(I2S、S/PDIF Mode)	1.5/1.8/2.5/3.0/3.3V
TX_DSR3R	Input	Transmitter DSD data(DSD Mode)	1.5/1.8/2.5/3.0/3.3V
TX_DSR3L	Input	Transmitter DSD data(DSD Mode)	1.5/1.8/2.5/3.0/3.3V
SIL9136_RST_N	Input	Transmitter asynchronous reset signal, active low	1.5/1.8/2.5/3.0/3.3V
SIL9136_INT	Output	Transmitter interrupt signal	1.5/1.8/2.5/3.0/3.3V
SIL9136_CSCL_FMC	Input	Transmitter configuration/status I2C	1.5/1.8/2.5/3.0/3.3V

		serial clock	
SIL9136_CSDA_FMC	Input/Output	Transmitter configuration/status I2C serial data	1.5/1.8/2.5/3.0/3.3V
RX_PCLK	Output	Receiver pixel data clock	1.5/1.8/2.5/3.0/3.3V
RX_HS	Output	Receiver Horizontal Synchronization signal	1.5/1.8/2.5/3.0/3.3V
RX_VS	Output	Receiver Vertical Synchronization signal	1.5/1.8/2.5/3.0/3.3V
RX_DE	Output	Receiver data enable	1.5/1.8/2.5/3.0/3.3V
RX_BD0	Output	Receiver video blue data 0	1.5/1.8/2.5/3.0/3.3V
RX_BD1	Output	Receiver video blue data 1	1.5/1.8/2.5/3.0/3.3V
RX_BD2	Output	Receiver video blue data 2	1.5/1.8/2.5/3.0/3.3V
RX_BD3	Output	Receiver video blue data 3	1.5/1.8/2.5/3.0/3.3V
RX_BD4	Output	Receiver video blue data 4	1.5/1.8/2.5/3.0/3.3V
RX_BD5	Output	Receiver video blue data 5	1.5/1.8/2.5/3.0/3.3V
RX_BD6	Output	Receiver video blue data 6	1.5/1.8/2.5/3.0/3.3V
RX_BD7	Output	Receiver video blue data 7	1.5/1.8/2.5/3.0/3.3V
RX_BD8	Output	Receiver video blue data 8	1.5/1.8/2.5/3.0/3.3V
RX_BD9	Output	Receiver video blue data 9	1.5/1.8/2.5/3.0/3.3V
RX_BD10	Output	Receiver video blue data 10	1.5/1.8/2.5/3.0/3.3V
RX_BD11	Output	Receiver video blue data 11	1.5/1.8/2.5/3.0/3.3V
RX_BD12	Output	Receiver video blue data 12	1.5/1.8/2.5/3.0/3.3V
RX_BD13	Output	Receiver video blue data 13	1.5/1.8/2.5/3.0/3.3V
RX_BD14	Output	Receiver video blue data 14	1.5/1.8/2.5/3.0/3.3V
RX_BD15	Output	Receiver video blue data 15	1.5/1.8/2.5/3.0/3.3V
RX_GD0	Output	Receiver video green data 0	1.5/1.8/2.5/3.0/3.3V
RX_GD1	Output	Receiver video green data 1	1.5/1.8/2.5/3.0/3.3V
RX_GD2	Output	Receiver video green data 2	1.5/1.8/2.5/3.0/3.3V
RX_GD3	Output	Receiver video green data 3	1.5/1.8/2.5/3.0/3.3V
RX_GD4	Output	Receiver video green data 4	1.5/1.8/2.5/3.0/3.3V
RX_GD5	Output	Receiver video green data 5	1.5/1.8/2.5/3.0/3.3V
RX_GD6	Output	Receiver video green data 6	1.5/1.8/2.5/3.0/3.3V
RX_GD7	Output	Receiver video green data 7	1.5/1.8/2.5/3.0/3.3V
RX_GD8	Output	Receiver video green data 8	1.5/1.8/2.5/3.0/3.3V
RX_GD9	Output	Receiver video green data 9	1.5/1.8/2.5/3.0/3.3V
RX_GD10	Output	Receiver video green data 10	1.5/1.8/2.5/3.0/3.3V
RX_GD11	Output	Receiver video green data 11	1.5/1.8/2.5/3.0/3.3V
RX_GD12	Output	Receiver video green data 12	1.5/1.8/2.5/3.0/3.3V
RX_GD13	Output	Receiver video green data 13	1.5/1.8/2.5/3.0/3.3V
RX_GD14	Output	Receiver video green data 14	1.5/1.8/2.5/3.0/3.3V
RX_GD15	Output	Receiver video green data 15	1.5/1.8/2.5/3.0/3.3V

RX_RD0	Output	Receiver video red data 0	1.5/1.8/2.5/3.0/3.3V
RX_RD1	Output	Receiver video red data 1	1.5/1.8/2.5/3.0/3.3V
RX_RD2	Output	Receiver video red data 2	1.5/1.8/2.5/3.0/3.3V
RX_RD3	Output	Receiver video red data 3	1.5/1.8/2.5/3.0/3.3V
RX_RD4	Output	Receiver video red data 4	1.5/1.8/2.5/3.0/3.3V
RX_RD5	Output	Receiver video red data 5	1.5/1.8/2.5/3.0/3.3V
RX_RD6	Output	Receiver video red data 6	1.5/1.8/2.5/3.0/3.3V
RX_RD7	Output	Receiver video red data 7	1.5/1.8/2.5/3.0/3.3V
RX_RD8	Output	Receiver video red data 8	1.5/1.8/2.5/3.0/3.3V
RX_RD9	Output	Receiver video red data 9	1.5/1.8/2.5/3.0/3.3V
RX_RD10	Output	Receiver video red data 10	1.5/1.8/2.5/3.0/3.3V
RX_RD11	Output	Receiver video red data 11	1.5/1.8/2.5/3.0/3.3V
RX_RD12	Output	Receiver video red data 12	1.5/1.8/2.5/3.0/3.3V
RX_RD13	Output	Receiver video red data 13	1.5/1.8/2.5/3.0/3.3V
RX_RD14	Output	Receiver video red data 14	1.5/1.8/2.5/3.0/3.3V
RX_RD15	Output	Receiver video red data 15	1.5/1.8/2.5/3.0/3.3V
RX_MCLK	Output	Receiver audio master clock	1.5/1.8/2.5/3.0/3.3V
RX_SCLK	Output	Receiver audio serial clock	1.5/1.8/2.5/3.0/3.3V
RX_AP0	Output	Receiver audio data 0	1.5/1.8/2.5/3.0/3.3V
RX_AP1	Output	Receiver audio data 1	1.5/1.8/2.5/3.0/3.3V
RX_AP2	Output	Receiver audio data 2	1.5/1.8/2.5/3.0/3.3V
RX_AP3	Output	Receiver audio data 3	1.5/1.8/2.5/3.0/3.3V
RX_AP4	Output	Receiver audio data 4	1.5/1.8/2.5/3.0/3.3V
RX_AP5	Output	Receiver audio data 5	1.5/1.8/2.5/3.0/3.3V
ADV7619_CS_N	Input	Receiver chip select, active low	1.5/1.8/2.5/3.0/3.3V
ADV7619_INT	Output	Receiver interrupt signal	1.5/1.8/2.5/3.0/3.3V
ADV7619_RESET_N	Input	Receiver reset signal, active low	1.5/1.8/2.5/3.0/3.3V
ADV7619_CSCL_FMC	Input	Receiver I2C serial clock	1.5/1.8/2.5/3.0/3.3V
ADV7619_CSDA_FMC	Input/Output	Receiver I2C serial data	1.5/1.8/2.5/3.0/3.3V
RX0_DDC_SCL	Input	Receiver EDID controller serial clock port A	1.5/1.8/2.5/3.0/3.3V
RX0_DDC_SDA	Input/Output	Receiver EDID controller serial data port A	1.5/1.8/2.5/3.0/3.3V
RX1_DDC_SCL	Input	Receiver EDID controller serial clock port B	1.5/1.8/2.5/3.0/3.3V
RX1_DDC_SDA	Input/Output	Receiver EDID controller serial data port B	1.5/1.8/2.5/3.0/3.3V

Note : 1. For I/O standard, 3.0 V is applied to High-end FPGAs and 3.3 V is applied to Low Cost and Power FPGAs.

2. The RX pixel color-bit plane is adjustable accord to the video interface data format settings,including video format and data width.

Chapter 4

Example Codes

This chapter provides NIOS based examples for users to get started using the HDMI-FMC board.

4-1 4K HDMI Loopback Demonstration

The Loopback demonstration establishes connection between the HDMI Receiver input to the transmitter output of the HDMI daughter board. The Loopback (Internal bypass) generates the HDMI video and/or audio signals, as the audio and video output pins of the receiver are directly connected to the input audio and video pins of the transmitter with a buffer to realize the synchronous operation.

Figure 4-1 shows the system block diagram of loopback demonstration,**Figure 4-2** shows the hardware setup of loopback demonstration.

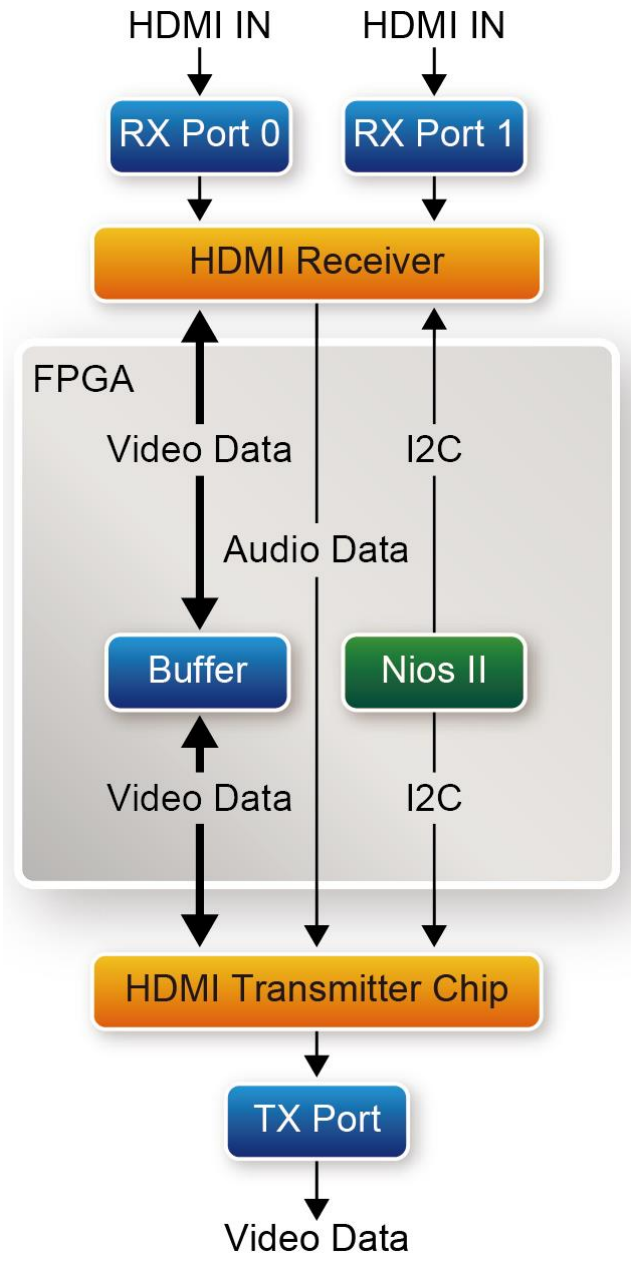

Figure 4-1 system Block diagram of the HDMI loopback demonstration

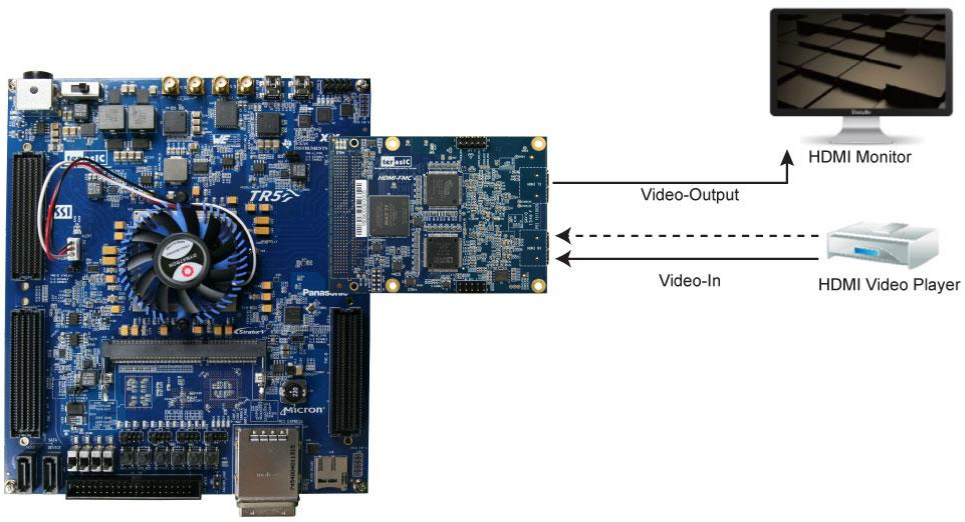

Figure 4-2 hardware setup of HDMI loopback demonstration

Chapter 5

Appendix

Revision History

Version	Change Log
V1.0	Initial Version

Copyright Statement