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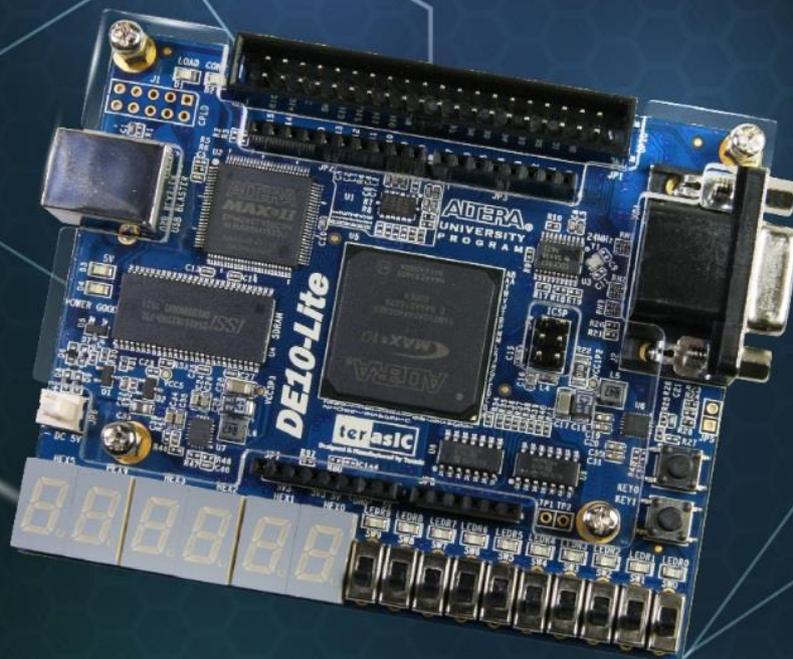
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# DE10-Lite

## User Manual



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# Chapter 1

## *Introduction*

The DE10-Lite presents a robust hardware design platform built around the Altera MAX 10 FPGA. The MAX 10 FPGA is well equipped to provide cost effective, single-chip solutions in control plane or data path applications and industry-leading programmable logic for ultimate design flexibility. With MAX 10 FPGA, you can get lower power consumption / cost and higher performance. When you need high-volume applications, including protocol bridging, motor control drive, analog to digital conversion, image processing, and handheld devices, the MAX 10 Lite FPGA is your best choice.

The DE10-Lite development board includes hardware such as on-board USB Blaster, 3-axis accelerometer, video capabilities and much more. By leveraging all of these capabilities, the DE10-Lite is the perfect solution for showcasing, evaluating, and prototyping the true potential of the Altera MAX 10 FPGA.

The DE10-Lite contains all components needed to use the board in conjunction with a computer that runs the Microsoft Windows XP or later.

### 1.1 Package Contents

Figure 1-1 shows a photograph of the DE10-Lite package.

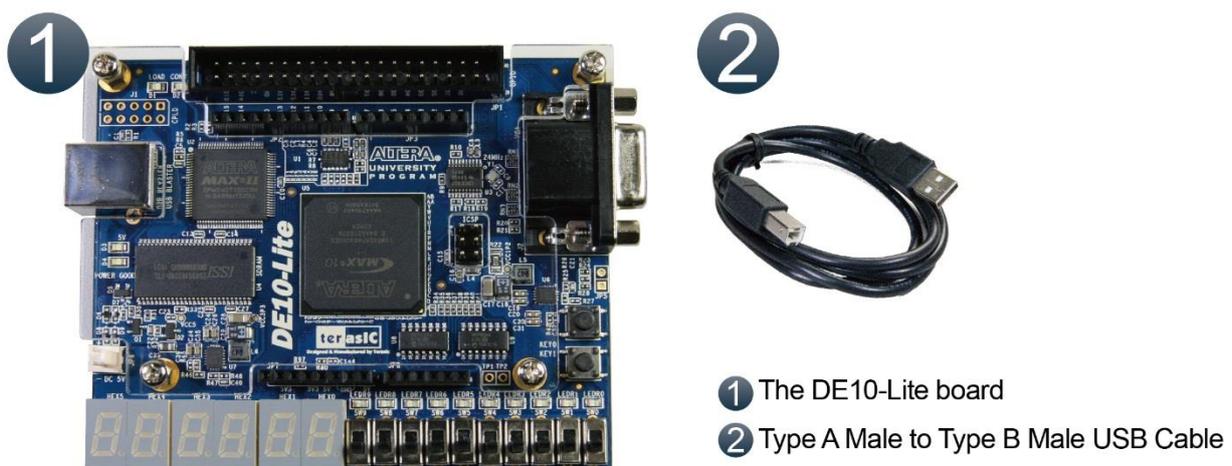


Figure 1-1 The DE10-Lite package contents

The DE10-Lite package includes:

- The DE10-Lite board
- Type A Male to Type B Male USB Cable

## 1.2 DE10-Lite System CD

The DE10-Lite System CD contains the documentation and supporting materials, including the User Manual, Control Panel, System Builder, reference designs and device datasheets.

User can download this System CD from the web (<http://DE10-Lite.terasic.com/cd>).

## 1.3 Layout and Components

This section presents the features and design characteristics of the board.

A photograph of the board is shown in **Figure 1-2** and **Figure 1-3**. It depicts the layout of the board and indicates the location of the connectors and key components.

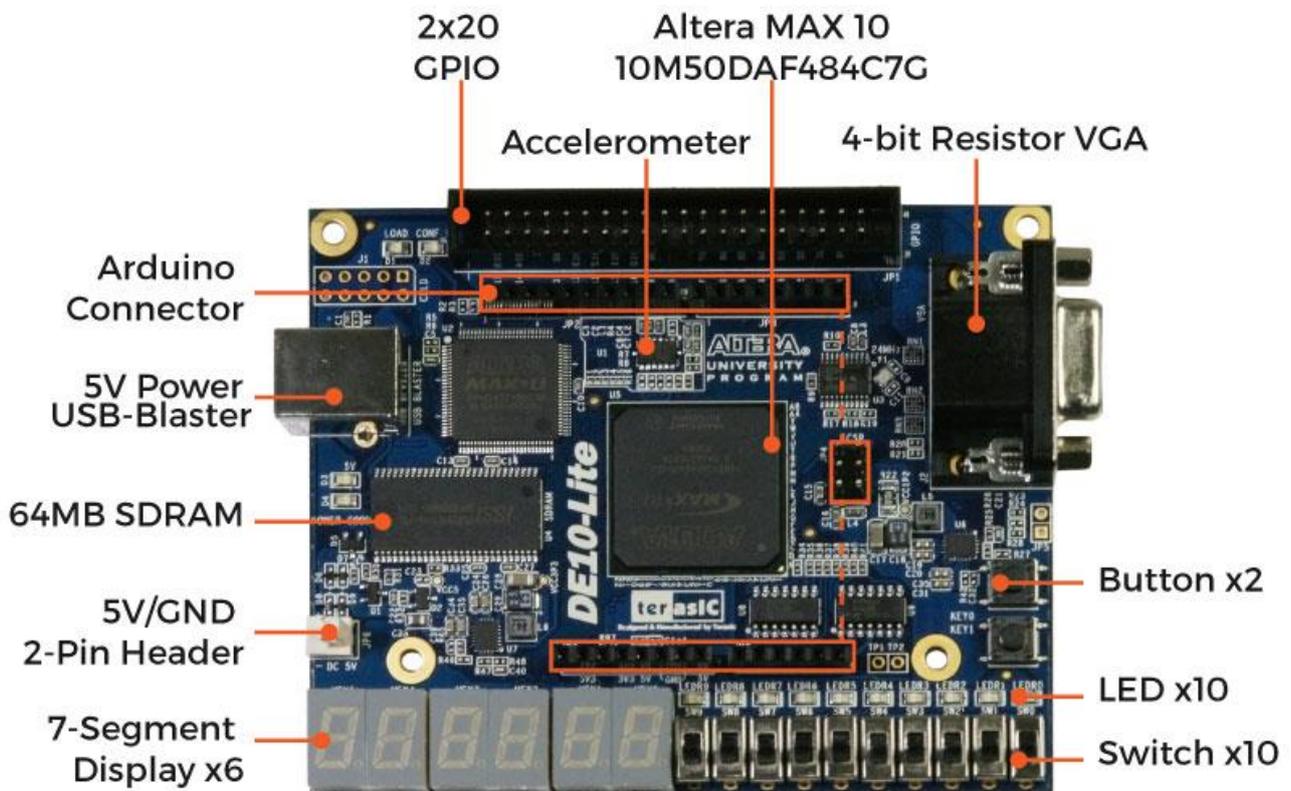


Figure 1-2 Development Board (top view)

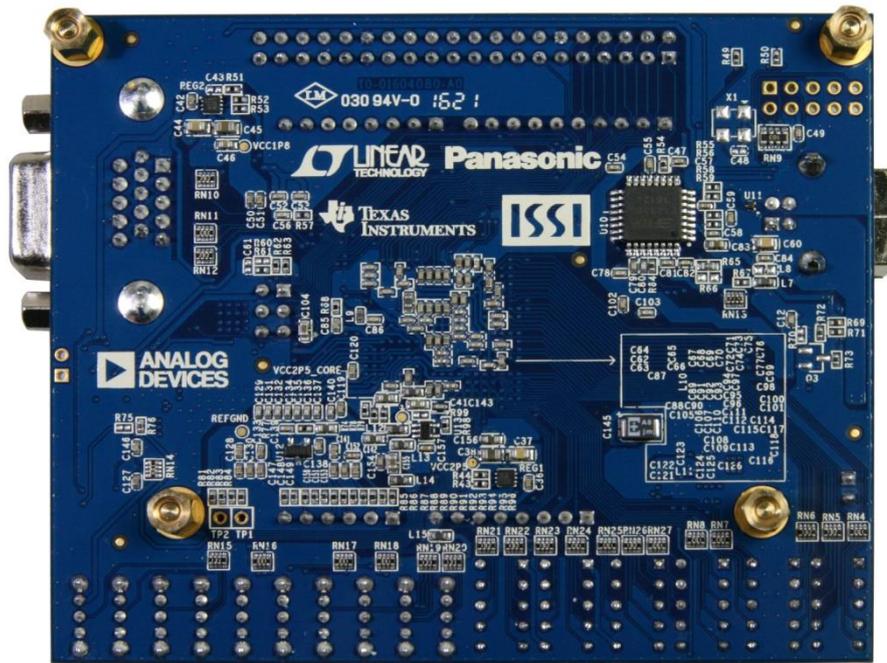


Figure 1-3 Development Board (bottom view)

This board has many features that allow users to implement a wide range of designed circuits, from simple circuits to various multimedia projects.

The following hardware are provided on the board:

## FPGA Device

- MAX 10 10M50DAF484C7G Device
- Integrated dual ADCs, each ADC supports 1 dedicated analog input and 8 dual function pins
- 50K programmable logic elements
- 1,638 Kbits M9K Memory
- 5,888 Kbits user flash memory
- 144 18 × 18 Multiplier
- 4 PLLs

## Programming and Configuration

- On-Board USB Blaster (Normal type B USB connector)

## Memory Device

- 64MB SDRAM, x16 bits data bus

## Connectors

- 2x20 GPIO Header
- Arduino Uno R3 Connector, including six ADC channels.

## Display

- 4-bit resistor-network DAC for VGA (With 15-pin high-density D-sub connector)

## Switches, Buttons and LEDs

- 10 LEDs
- 10 Slide Switches
- 2 Push Buttons with Debounced.
- Six 7-Segments

## Power

- 5V DC input from USB or external power connector.

### 1.4 Block Diagram of the Board

Figure 1-4 gives the block diagram of the board. To provide maximum flexibility for the user, all connections are made through the MAX 10 FPGA device. Thus, the user can configure the FPGA to implement any system design.

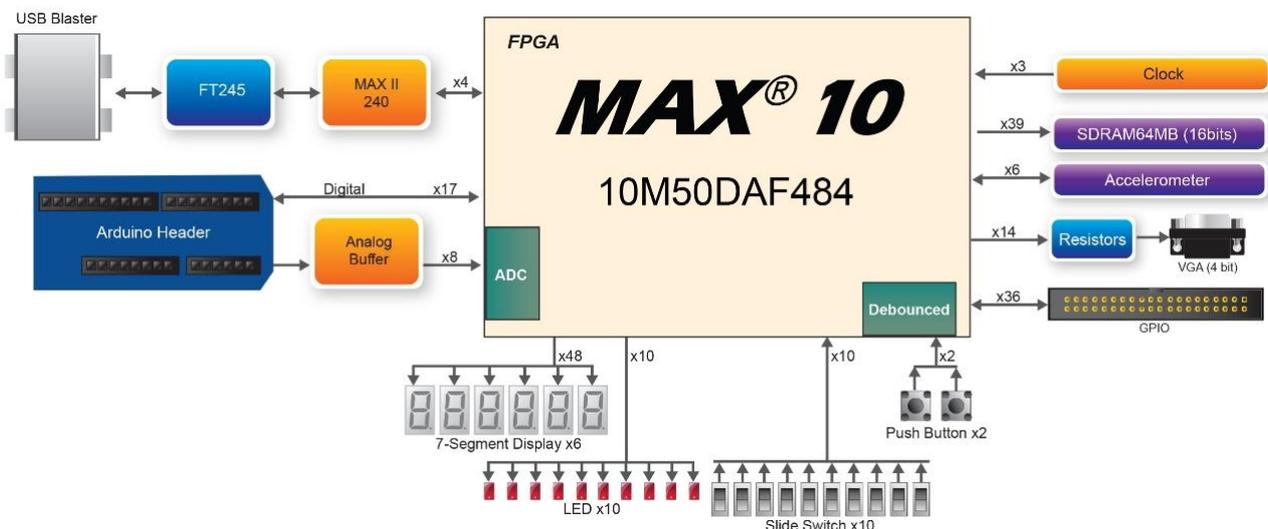


Figure 1-4 Board Block Diagram

## 1.5 Getting Help

Here are the addresses where you can get help if you encounter any problem:

- Terasic Inc.

9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan

Email: [support@terasic.com](mailto:support@terasic.com)

Tel.: +886-3-5750-880

Web: <http://DE10-Lite.terasic.com>

The DE10-Lite board comes with a Control Panel program that allows users to access various components on the board from a host computer. The host computer communicates with the board through a USB connection. The program can be used to verify the functionality of components on the board or be used as a debug tool while developing any RTL code.

This chapter first presents some basic functions of the Control Panel, then describes its structure in the block diagram form, and finally describes its capabilities.

## 2.1 Control Panel Setup

The Control Panel Software Utility is located in the directory “Tools/ControlPanel” in the **DE10-Lite System CD**. It's free of installation, just copy the whole folder to your host computer and launch the control panel by executing the “DE10\_Lite\_ControlPanel.exe”.

Specific control circuits should be downloaded to your FPGA board before the control panel can request it to perform required tasks. The program will call Quartus II tools to download the control circuit to the FPGA board through the USB-Blaster[USB-0] connection.

To activate the Control Panel, perform the following steps:

1. Make sure Quartus II 16.0 or a later version is installed successfully on your PC.
2. Connect the USB cable provided to the USB Blaster port.
3. Start the executable *DE10\_Lite\_ControlPanel.exe* on the host computer. The Control Panel user interface shown in **Figure 2-1** will appear.
4. The *DE10\_Lite\_ControlPanel.sof* bit stream is loaded automatically as soon as the *DE10\_Lite\_ControlPanel.exe* is launched.
5. In case of a disconnection, click on CONNECT where the .sof will be re-loaded onto the board.

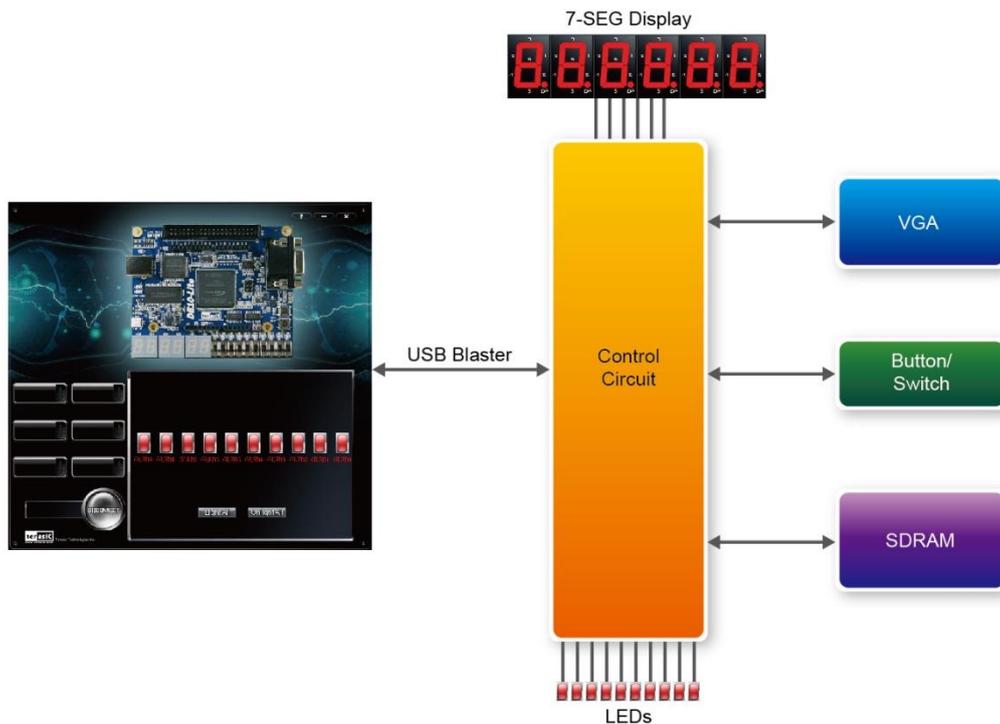
*Please note that the Control Panel will occupy the USB port until you close that port; you cannot use Quartus II to download a configuration file into the FPGA until the USB port is closed.*

6. The Control Panel is now ready to use; experience it by setting the ON/OFF status for some LEDs and observing the result on the DE10-Lite board.



**Figure 2-1 The DE10-Lite Control Panel**

The concept of the DE10-Lite Control Panel is illustrated in **Figure 2-2**. The “Control Circuit” that performs the control functions is implemented in the FPGA board. It communicates with the Control Panel window, which is active on the host computer, via the USB Blaster link. The graphical interface is used to send commands to the control circuit. It handles all the requests and performs data transfers between the computer and the DE10-Lite board.



**Figure 2-2 The DE10-Lite Control Panel concept**

The DE10-Lite Control Panel can be used to light up LEDs, change the values displayed on the 7-segment, monitor buttons/switches status, read/write the SDRAM Memory, output VGA color pattern to VGA monitor. The feature of reading/writing a word or an entire file from/to the Memory allows the user to develop multimedia applications without worrying about how to build a Memory Programmer.

## **2. 2 Controlling the LEDs, 7-segment Displays**

A simple function the Control Panel is capable of is the modification of settings for the 7-segment LED displays.

Choosing the **LED** tab leads you to the window in **Figure 2-3**. Here, you can directly turn the LEDs on or off individually or by clicking “Light All” or “Unlight All”.



Figure 2-3 Controlling LEDs

Choosing the 7-SEG tab leads you to the window shown in **Figure 2-4**. From the window, directly use the left-right arrows to control the 7-SEG patterns on the DE10-Lite board which are updated immediately. Note that the dots of the 7-SEGs are not enabled on the DE10-Lite board.

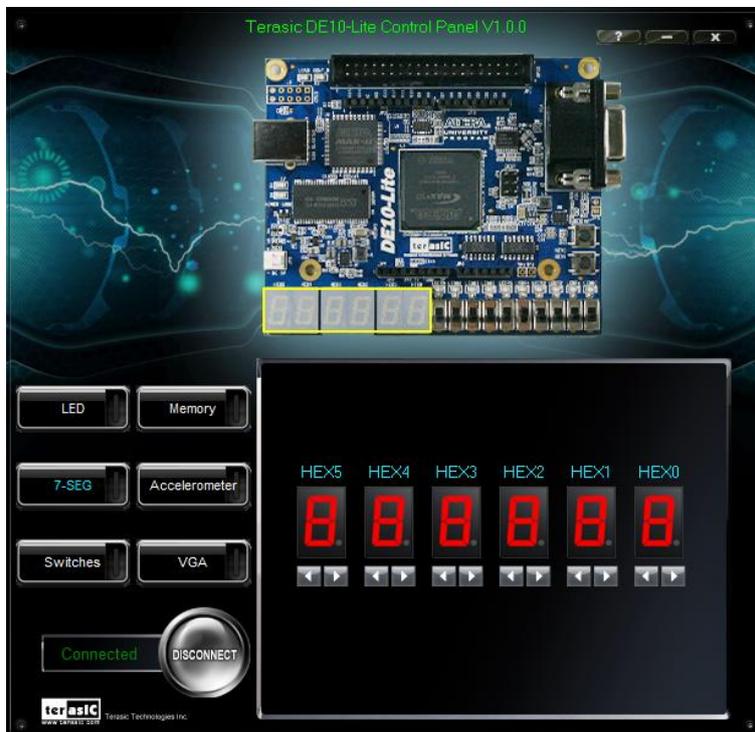


Figure 2-4 Controlling 7-SEG display

The ability to set arbitrary values into simple display devices is not needed in typical design activities. However, it gives users a simple mechanism for verifying that these devices are functioning correctly in case a malfunction is suspected. Thus, it can be used for troubleshooting purposes.

## 2.3 Switches and Push-buttons

Choosing the Switches tab leads you to the window in **Figure 2-5**. The function is designed to monitor the status of slide switches and push buttons in real time and show the status in a graphical user interface. It can be used to verify the functionality of the slide switches and push-buttons.



**Figure 2-5 Monitoring switches and buttons**

The ability to check the status of push-button and slide switch is not needed in typical design activities. However, it provides users a simple mechanism to verify if the buttons and switches are functioning correctly. Thus, it can be used for troubleshooting purposes.

## 2.4 SDRAM Controller and Programmer

The Control Panel can be used to write/read data to/from the SDRAM chips on the DE10-Lite board. As shown below, we will describe how the SDRAM may be accessed; Click on the Memory tab and select “SDRAM” to reach the window in **Figure 2-6**.



**Figure 2-6 Accessing the SDRAM**

A 8-bit word can be written into the SDRAM by entering the address of the desired location, specifying the data to be written, and pressing the Write button. Contents of the location can be read by pressing the Read button. **Figure 2-6** depicts the result of writing the **hexadecimal** value AB into **hexadecimal** offset address C00, followed by reading the same location.

The Sequential Write function of the Control Panel is used to write the contents of a file into the SDRAM as follows:

1. Specify the hexadecimal starting address in the Address box.
2. Specify the hexadecimal number of bytes to be written in the Length box. If the entire file is to be loaded, then a checkmark may be placed in the File Length box instead of giving the number of bytes.
3. To initiate the writing process, click on the Write a File to Memory button.
4. When the Control Panel responds with the standard Windows dialog box asking for the source file, specify the desired file location in the usual manner.

The Control Panel also supports loading files with a .hex extension. Files with a .hex extension are ASCII text files that specify memory values using ASCII characters to represent hexadecimal values. For example, a file containing the line

0123456789ABCDEF



## 2.6 VGA

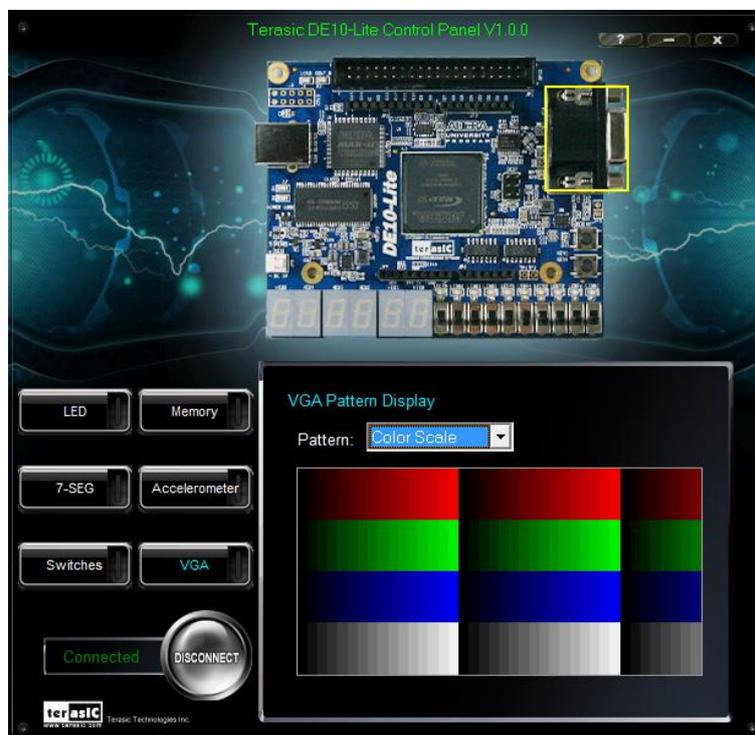
DE10-Lite Control Panel provides VGA pattern function that allows users to output color pattern to LCD/CRT monitor using the DE10-Lite board. Follow the steps below to generate the VGA pattern function:

Choosing the VGA tab leads you to the window in **Figure 2-8**.

Plug a D-sub cable to the VGA connector of the DE10-Lite board and LCD /CRT monitor.

The LCD/CRT monitor will display the same color pattern on the control panel window.

Click the drop down menu shown in **Figure 2-8** where you can output the selected pattern individually.



**Figure 2-8 Controlling VGA display under Control Panel**

## 2.7 Overall Structure of the DE10-Lite Control Panel

The DE10-Lite Control Panel is based on a Nios II Qsys system instantiated in the MAX 10 FPGA with software running on the on-chip memory. The software was implemented in coding Language C; and the hardware was implemented in Verilog HDL code with Qsys builder. The source code is not available on the DE10-Lite System CD.

To run the Control Panel, users should follow the configuration setting according to Section 3.1. **Figure 2-9** depicts the structure of the Control Panel. Each input/output device is controlled by the Nios II Processor instantiated in the FPGA chip. The communication with the PC is done via the USB Blaster link. The Nios II interprets the commands sent from the PC and performs the corresponding actions.

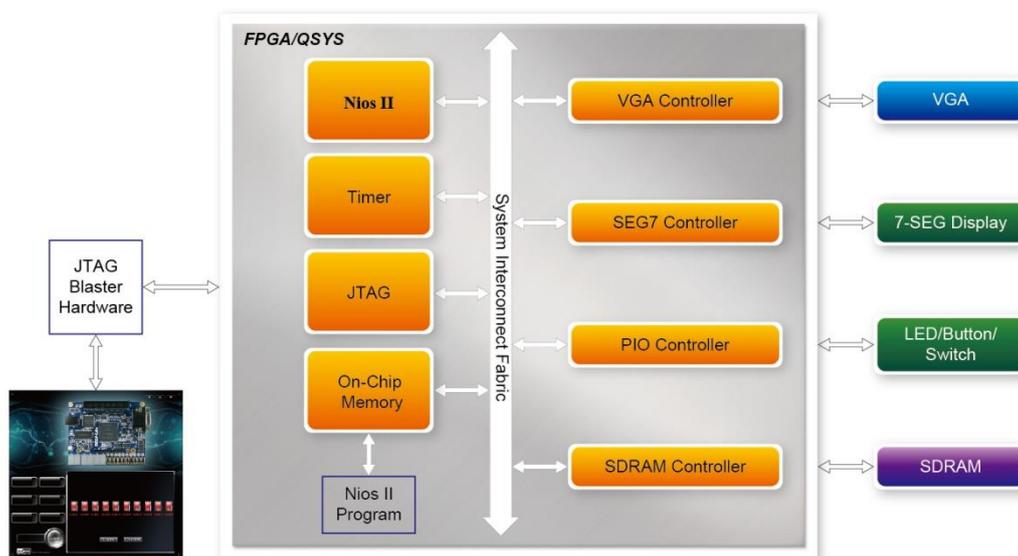


Figure 2-9 The block diagram of the DE10-Lite control panel

This chapter provides instructions to use the board and describes the peripherals.

### 3.1 Configuration of MAX 10 FPGA on DE10-Lite

There are two types of configuration method supported by DE10-Lite:

1. JTAG configuration: configuration using JTAG ports.

JTAG configuration scheme allows you to directly configure the device core through JTAG pins - TDI, TDO, TMS, and TCK pins. The Quartus II software automatically generates .sof files that are used for JTAG configuration with a download cable in the Quartus II software program.

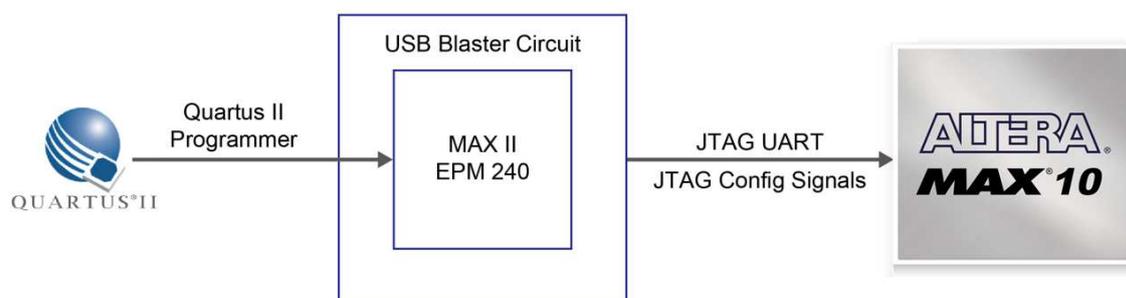
2. Internal configuration: configuration using internal flash.

Before internal configuration, you need to program the configuration data into the configuration flash memory (CFM) which provides non-volatile storage for the bit stream. The information is retained within CFM even if the DE10-Lite board is turned off. When the board is powered on, the configuration data in the CFM is automatically loaded into the MAX 10 FPGA.

#### ■ JTAG Chain on DE10-Lite Board

The FPGA device can be configured through JTAG interface on DE10-Lite board, but the JTAG chain must form a closed loop, which allows Quartus II programmer to detect FPGA device.

**Figure 3-1** illustrates the JTAG chain on DE10-Lite board

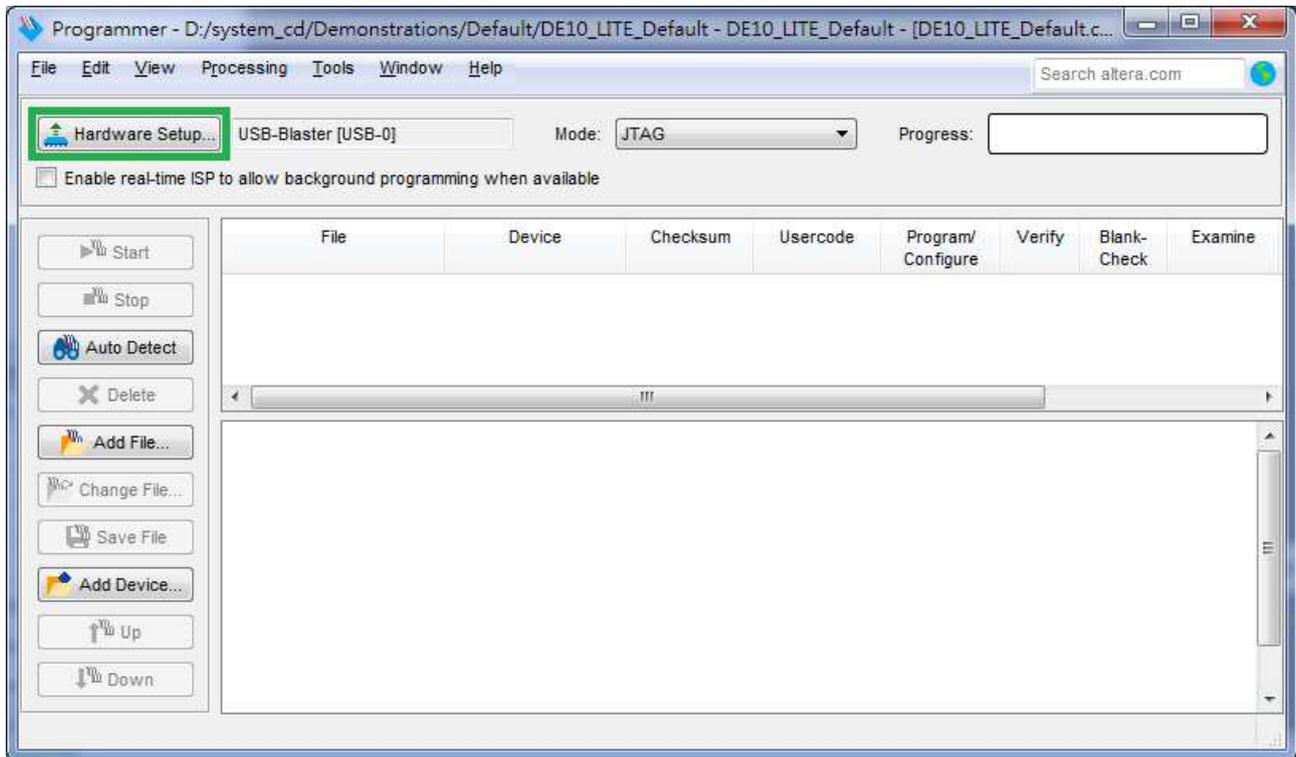


**Figure 3-1** The JTAG configuration scheme

## ■ Configure the FPGA in JTAG Mode

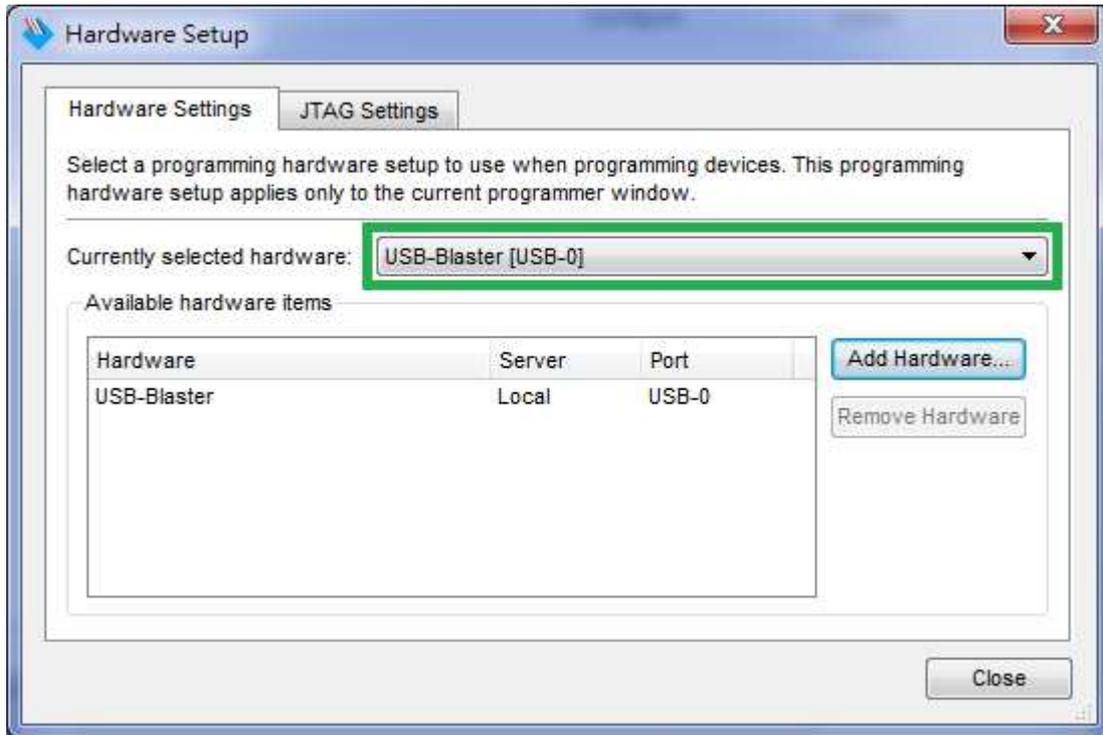
The following shows how the FPGA is programmed in JTAG mode step by step.

1. Open the Quartus II programmer, please Choose Tools > Programmer. The Programmer window opens. See [Figure 3-2](#).



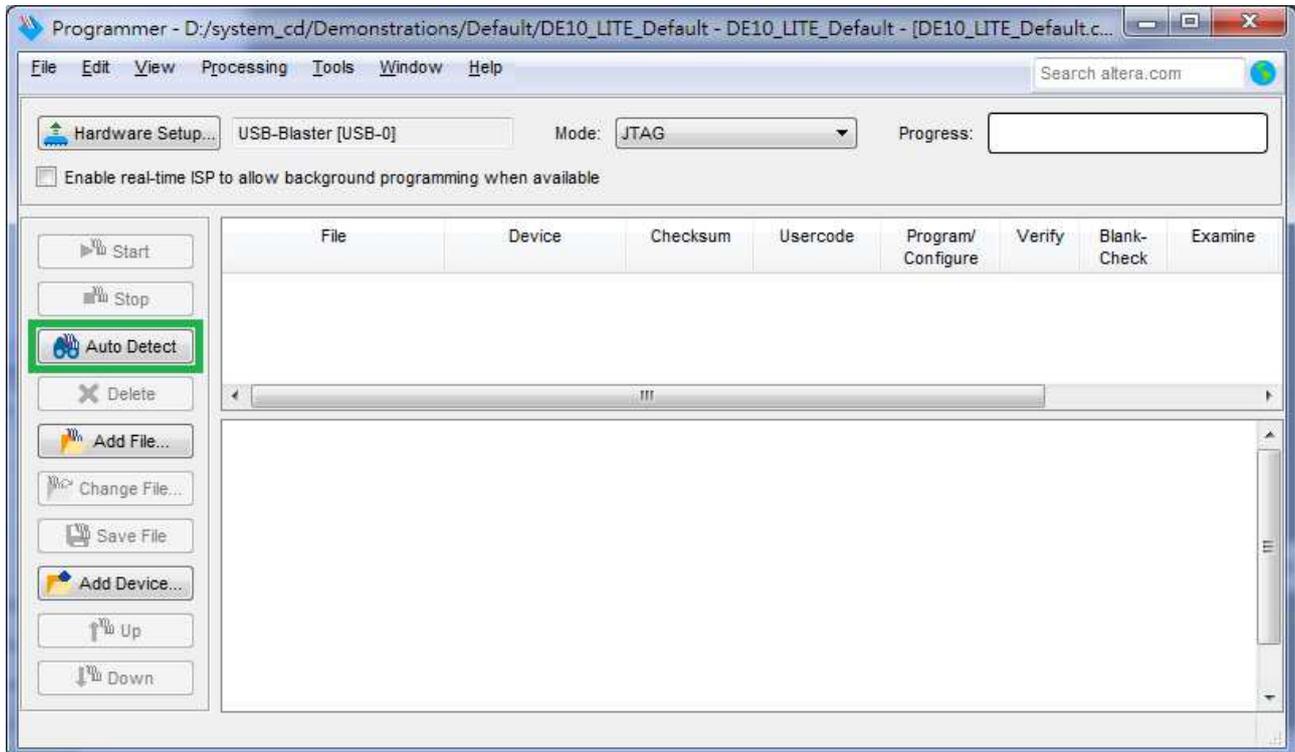
**Figure 3-2 Programmer Window**

2. Click “Hardware Setup”, as circled in [Figure 3-2](#).
3. If it is not already turned on, turn on the USB-Blaster [USB-0] option under currently selected hardware and click “Close” to close the window. See [Figure 3-3](#).



**Figure 3-3 Hardware Setting**

4. Click “Auto Detect” to detect all the devices on the JTAG chain, as circled in **Figure 3-4**.



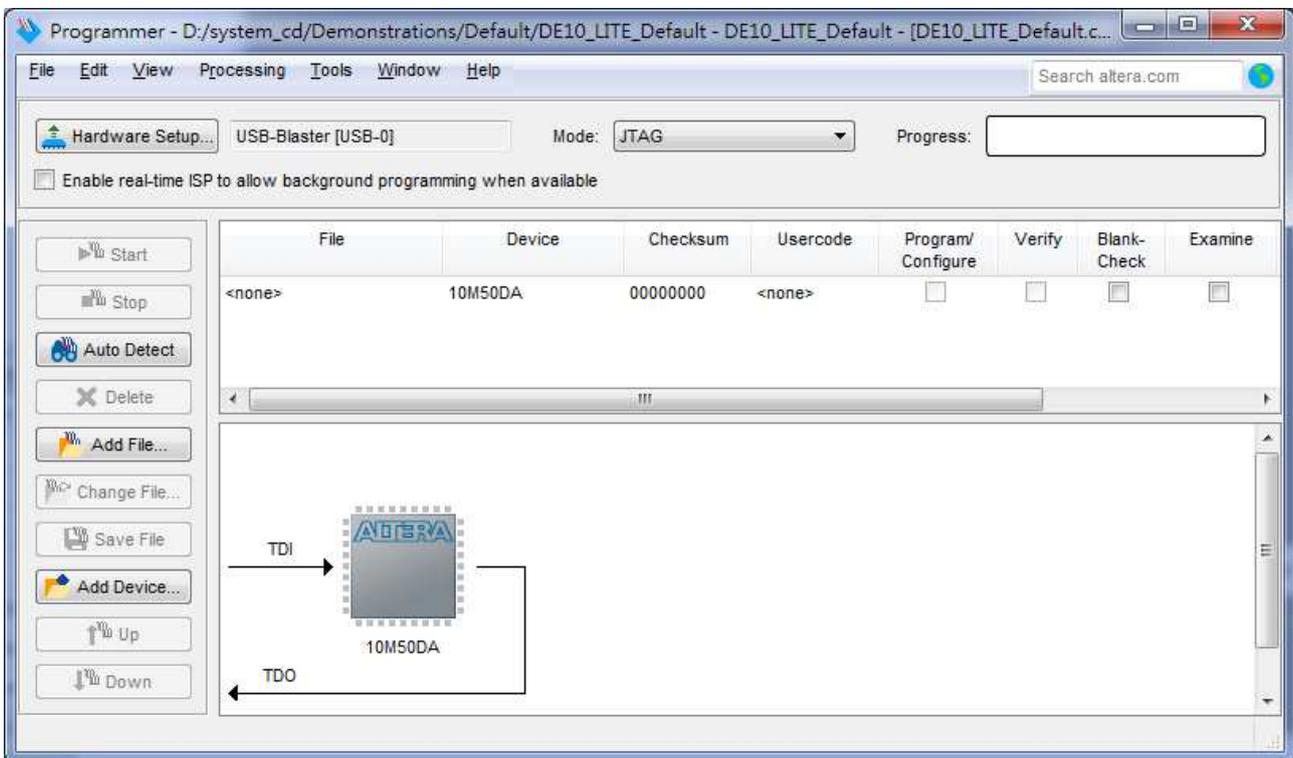
**Figure 3-4 Detect FPGA device in JTAG mode**

5. Select detected device associated with the board, as circled in **Figure 3-5**.



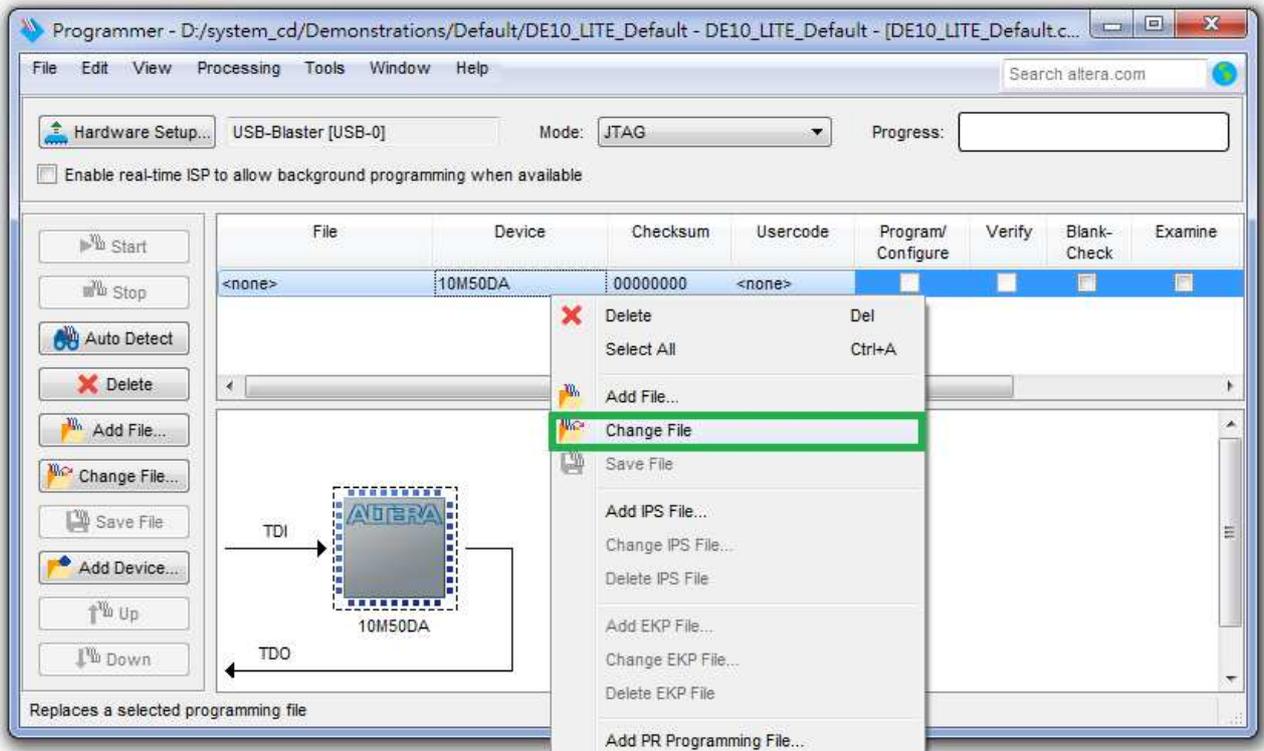
**Figure 3-5 Select 10M50DA device**

6. FPGA is detected, as shown in **Figure 3-6**.



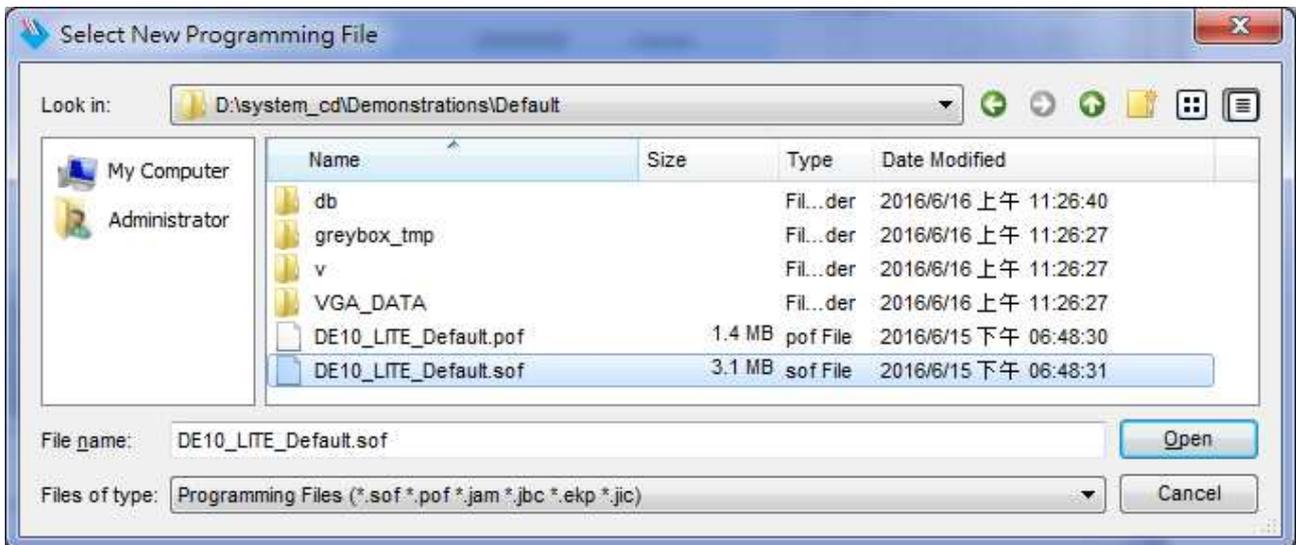
**Figure 3-6 FPGA detected in Quartus II programmer**

7. Right click on the FPGA device and click “Change File” to open the .sof file to be programmed, as highlighted in **Figure 3-7**.



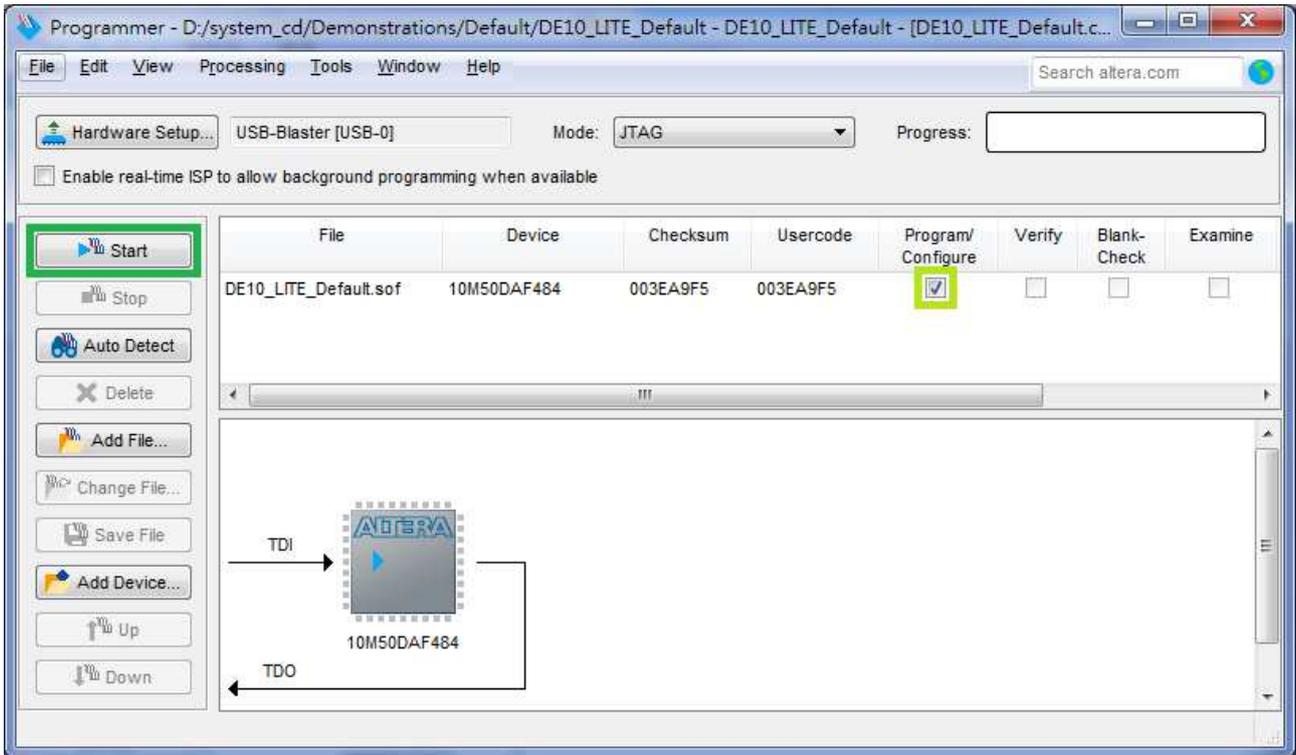
**Figure 3-7** Open the .sof file to be programmed into the FPGA device

8. Select the .sof file to be programmed, as shown in **Figure 3-8**.



**Figure 3-8** Select the .sof file to be programmed into the FPGA device

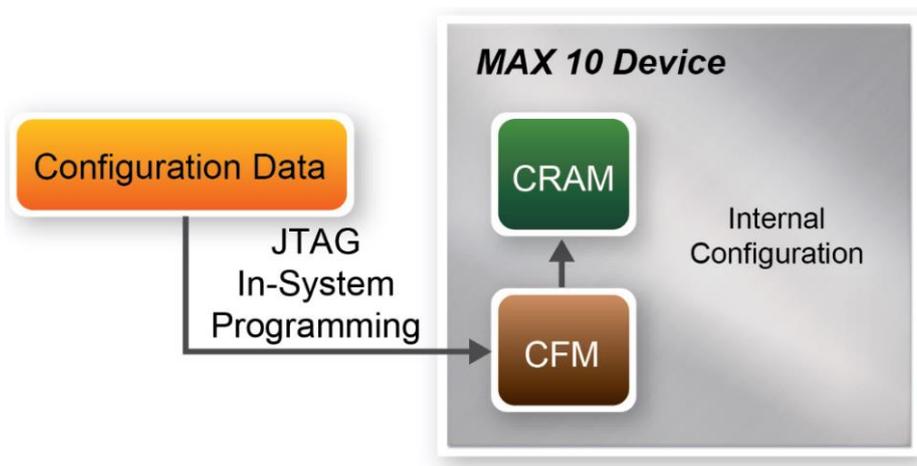
- Click “Program/Configure” check box and then click “Start” button to download the .sof file into the FPGA device, as shown in **Figure 3-9**.



**Figure 3-9 Program .sof file into the FPGA device**

### ■ Internal Configuration

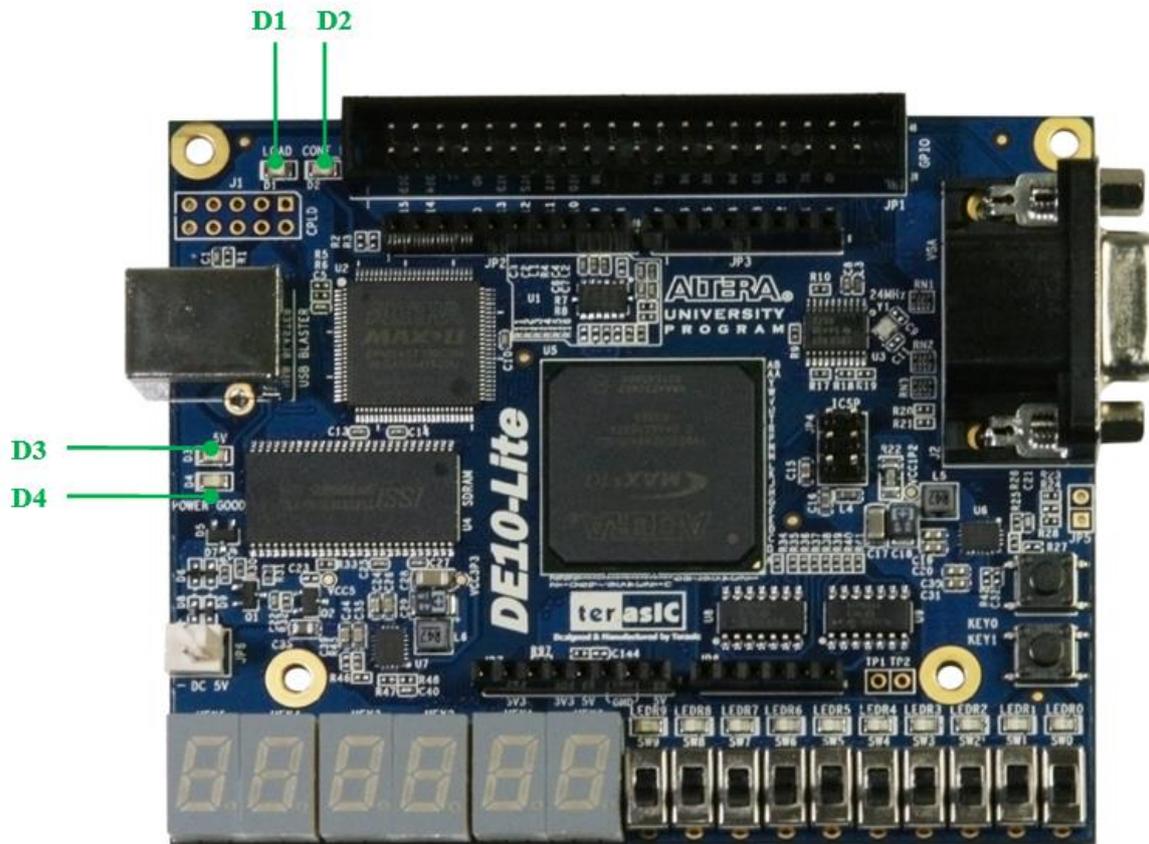
- The configuration data to be written to CFM will be part of the programmer object file (.pof). This configuration data is automatically loaded from the CFM into the MAX 10 devices when the board is powered up.
- Please refer to Chapter 8: Programming the Configuration Flash Memory (CFM) for the basic programming instruction on the configuration flash memory (CFM).



**Figure 3-10 High-Level Overview of Internal Configuration for MAX 10 Devices**

## ■ Status LED

The DE10-Lite development board includes board-specific status LEDs to indicate board status. Please refer to **Table 3-1** for the description of the LED indicator. Please refer to **Figure 3-11** for detailed LED location.



**Figure 3-11 Status LED position**

**Table 3-1 Status LED**

Reference	LED Name	Description
D1	ULED	Illuminates when the on-board USB-Blaster is working
D2	CONF_DONE	Illuminates when the FPGA is successfully configured.
D3	5V	Illuminates when Input power is active. Not Installed.
D4	Power Good	Illuminates when board power system is OK.

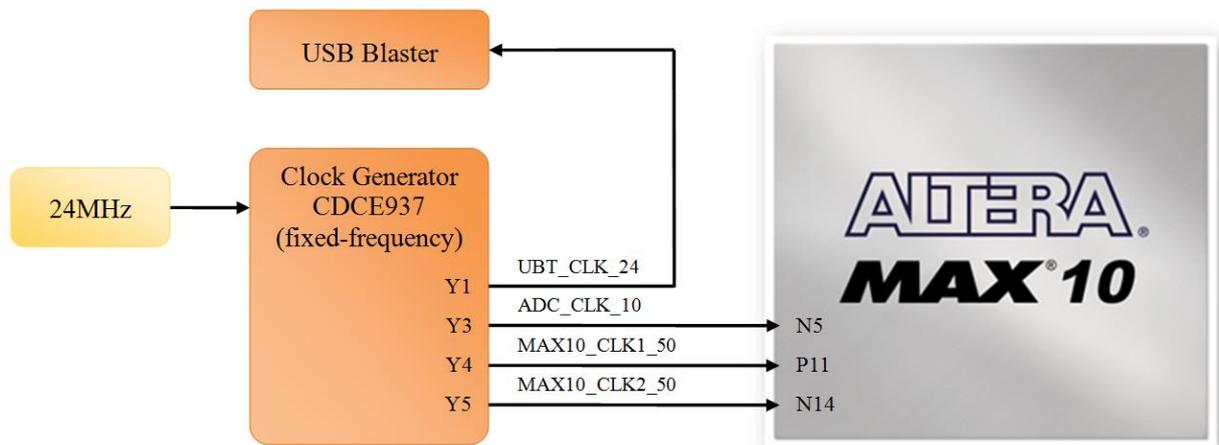
## 3.2 Clock Circuitry

Figure 3-12 shows the default frequency of all external clocks to the MAX 10 FPGA. A clock generator is used to distribute clock signals with low jitter. The two 50MHz clock signals connected to the FPGA are used as clock sources for user logic. One 24MHz clock signal is connected to the clock inputs of USB microcontroller of USB Blaster. One 10MHz clock signal is connected to the PLL1 and PLL3 of FPGA, the outputs of these two PLLs can drive ADC clock. The associated pin assignment for clock inputs to FPGA I/O pins is listed in Table 3-2.

**Warning !!**

*Do not modify the clock generator settings.*

*Incorrect setting will cause the system to not work.*



**Figure 3-12 Clock circuit of the FPGA Board**

**Table 3-2 Pin Assignment of Clock Inputs**

Signal Name	FPGA Pin No.	Description	I/O Standard
ADC_CLK_10	PIN_N5	10 MHz clock input for ADC (Bank 3B)	3.3-V LVTTTL
MAX10_CLK1_50	PIN_P11	50 MHz clock input(Bank 3B)	3.3-V LVTTTL
MAX10_CLK2_50	PIN_N14	50 MHz clock input(Bank 3B)	3.3-V LVTTTL