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VEEK-MT2

VEEK with Multi-touch Capacitive Panel

User Manual

CONTENTS

Chapter 1

Introduction of the VEEK-MT2

The Video and Embedded Evaluation Kit - Multi-touch, Second Edition (VEEK-MT2) is a comprehensive design environment with everything embedded developers need to create processing-based systems. VEEK-MT2 delivers an integrated platform that includes hardware, design tools, intellectual property (IP) and reference designs for developing embedded software and hardware platform in a wide range of applications. The fully integrated kit allows developers to rapidly customize their processor and IP to best suit their specific application. The VEEK-MT2 features the DE2-115 development board targeting the Cyclone IV E FPGA, as well as a capacitive LCD multimedia color touch panel which natively supports multi-touch gestures. An 8-megapixel digital image sensor, ambient light sensor, and 3-axis accelerometer make up the rich feature-set
The VEEK-MT2 is preconfigured with an FPGA hardware reference design including several ready-to-run demonstration applications stored on the provided SD card. Software developers can use these reference designs as their platform to quickly architect, develop and build complex embedded systems. By simply scrolling through the demos of your choice on the LCD touch panel, you can evaluate numerous processor system designs.

The all-in-one embedded solution offered on the VEEK-MT2, in combination of the LCD touch panel and digital image module, provides embedded developers the ideal platform for multimedia applications with unparallel processing performance. Developers can benefit from the use of FPGA-based embedded processing system such as mitigating design risk and obsolescence, design reuse, reducing bill of material (BOM) costs by integrating powerful graphics engines within the FPGA, and lower cost.
Figure 1-1 shows a photograph of VEEK-MT2.

Figure 1-1 The VEEK-MT2 board overview

The key features of the board are listed below:

■ DE2-115 Development Board

- **Cyclone IV EP4CE115 FPGA**
  - 114,480 LEs
  - 432 M9K memory blocks
  - 3,888 Kb embedded memory
  - 4 PLLs
- **Configuration**
  - On-board USB-Blaster circuitry
  - JTAG and AS mode configuration supported
  - EPCS64 serial configuration device
- **Memory Devices**
  - 128MB SDRAM
  - 2MB SRAM
  - 8MB Flash with 8-bit mode
  - 32Kb EEPROM
- **Switches and Indicators**
  - 18 switches and 4 push-buttons
  - 18 red and 9 green LEDs
  - Eight 7-segment displays
- **Audio**
  - 24-bit encoder/decoder (CODEC)
  - 3.5mm line-in, line-out, and microphone-in jacks
- **Character Display**
  - 16x2 LCD module
- **On-board Clocking Circuitry**
  - Three 50MHz oscillator clock inputs
  - SMA connectors (external clock input/output)
- **SD Card Socket**
  - Provides SPI and 4-bit SD mode for SD Card access
- **Two Gigabit Ethernet Ports**
  - Integrated 10/100/1000 Ethernet
- **High Speed Mezzanine Card (HSMC)**
  - Configurable I/O standards (voltage levels: 3.3/2.5/1.8/1.5V)
- **USB Type A and B**
  - Provides host and device controller compliant with USB 2.0
  - Supports data transfer at full-speed and low-speed
  - PC driver available

- **40-pin Expansion Port**
  - Configurable I/O standards (voltage levels: 3.3/2.5/1.8/1.5V)
- **VGA-out Connector**
  - VGA DAC (high speed triple DACs)
- **DB9 Serial Connector**
  - RS232 port with flow control
- **PS/2 Connector**
  - PS/2 connector for connecting a PS2 mouse or keyboard
- **TV-in Connector**
  - TV decoder (NTSC/PAL/SECAM)
- **Remote Control**
  - Infrared receiver module
- **Power**
  - 12V DC input
  - Switching and step-down regulators LM3150MH

■ Capacitive LCD Touch Screen

- Equipped with an 7-inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module
- Module composed of LED backlight
- Support 24-bit parallel RGB interface
- Converting the X/Y coordination of touch point to its corresponding digital data via the Touch controller.
- Five-point touch support
- Gesture support

•

Table 1-1 shows the general physical specifications of the touch screen (Note*).

Table 1-1 General physical specifications of the LCD

Item	*Specification*	*Unit*
LCD size	7-inch (Diagonal)	-
Resolution	800 x3(RGB) x 480	dot
Dot pitch	0.0642(H) x0.1790 (V)	mm
Active area	154.08 (H) x 85.92 (V)	mm
Module size	179.4(H) x 117.4(V) x 7.58(D)	mm
Surface treatment	Anti-Glare	-
Color arrangement	RGB-stripe	-
Interface	Digital	-

■ 8-Megapixel Digital Image Sensor

- 8-Mega Pixels(3264x2448)
- Support Focus Control
- Automatic black level calibration (ABLC)
- Programmable controls for frame rate, mirror and flip, cropping, and windowing
- MIPI to Parallel Port Converter

Table 1-2 shows the key parameters of the CMOS sensor (Note*).

Table 1-2 Key performance parameters of the CMOS sensor

Parameter	*Value*
Active Pixels	3264Hx2448V
Pixel size	1.4umx1.4um
Color filter array	RGB Bayer pattern
ADC resolution	10-bit
Pixel dynamic range	68.8dB
SNRMAX	36.7dB

■ Ambient Light Sensor

- Approximates human-eye response
- Precise luminance measurement under diverse lighting conditions
- Programmable interrupt function with user-defined upper and lower threshold setting
- 16-bit digital output with I2C fast-mode at 400 kHz
- Programmable analog gain and integration time
- 50/60-Hz lighting ripple rejection

■ Accelerometer Features

- Digital-output triple-axis accelerometer
- Programmable full scale range of ±2g, ±4g, ±8g and ±16g and integrated 16-bit
- Self-test

■ Gyroscope Features

- Digital-output X-, Y-, and Z-Axis angular rate sensors
- User-programmable full-scale range of ±250, ±500, ±1000, and ±2000°/sec and integrated 16-bit ADCs
- Self-test

■ Magnetometer

- 3-axis silicon monolithic Hall-effect magnetic sensor with magnetic concentrator
- Wide dynamic measurement range and high resolution with lower current consumption
- Output data resolution of 14 bit (0.6μT/LSB) or 16 bit (15μT/LSB)
- Full scale measurement range is ±4800μT
- Magnetometer normal operating current: 280μA at 8Hz repetition rate
- Self-test function with internal magnetic source to confirm magnetic sensor operation on end products

Note:

for more detailed information of the LCD touch panel and CMOS sensor module, please refer to their datasheets respectively.

1.1 About the Kit

The kit contains all users needed to run the demonstrations and develop custom designs, as shown in **Figure 1-2**.
The system CD contains technical documents of the VEEK-MT2 which includes component datasheets, demonstrations, schematic, and user manual.

Figure 1-2 VEEK-MT2 kit package contents

1.2 Getting Help

Here is information of how to get help if you encounter any problem:

- **Terasic Technologies**
- **9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan**
- **Tel: +886-3-5750-880**
- **Email: support@terasic.com**

Chapter 2

Architecture

This chapter describes the architecture of the VEEK-MT2 including block diagram and components.

2.1 Layout and Components

The picture of the VEEK-MT2 is shown in **Figure 2-1** and **Figure 2-2**. It depicts the layout of the board and indicates the locations of the connectors and key components.

Figure 2-1 VEEK-MT2 PCB and Component Diagram (top view)

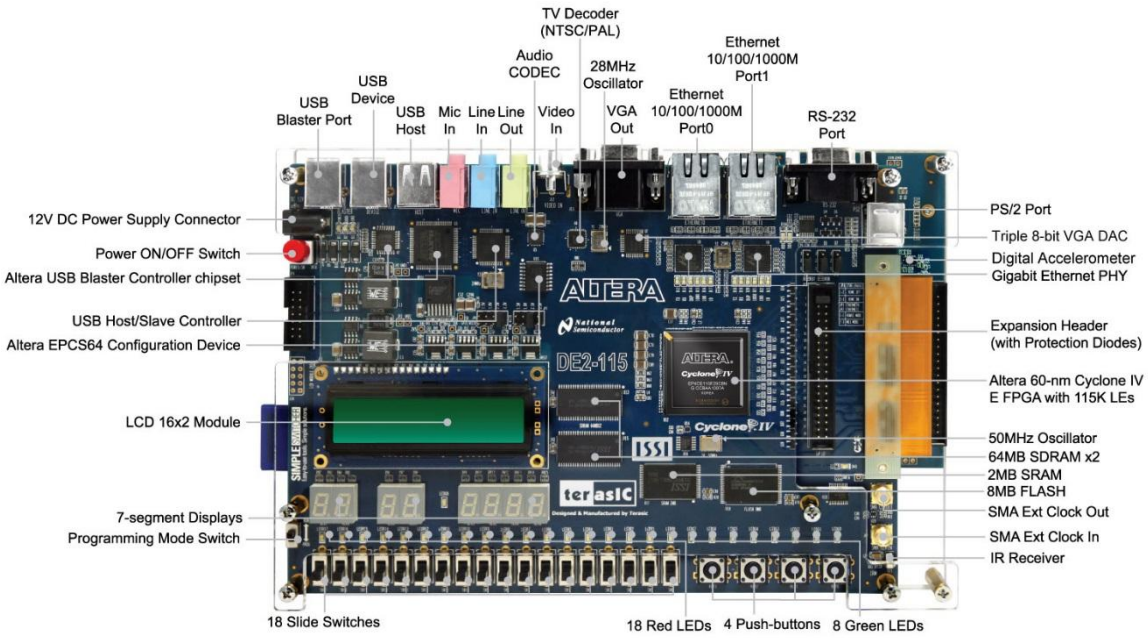

Figure 2-2 VEEK-MT2 PCB and Component Diagram (bottom view)

2.2 Block Diagram of the VEEK-MT2

Figure 2-3 gives the block diagram of the VEEK-MT2 board. To provide maximum flexibility for the user, all connections are made through the Cyclone IV E FPGA device. Thus, the user can configure the FPGA to implement any system design.

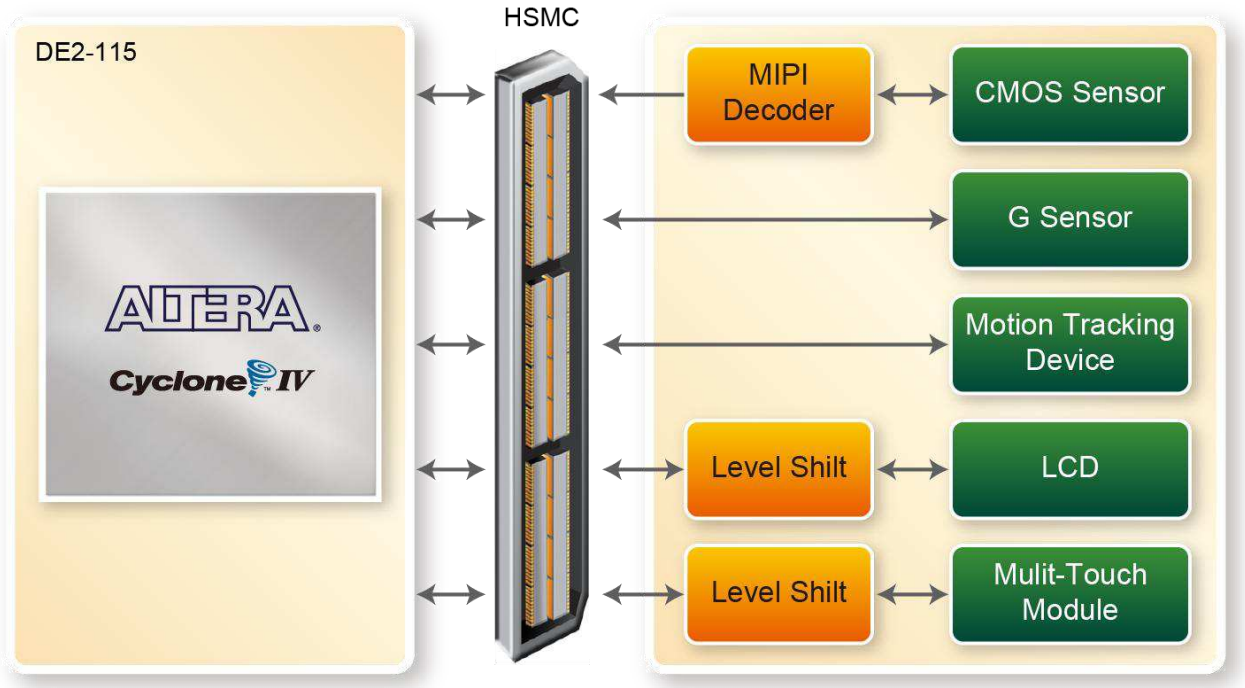

Figure 2-3 Block Diagram of VEEK-MT2

2.3 What's Difference Between VEEK-MT2 and VEEK-MT

Table 2-1 gives the difference between VEEK-MT2 and VEEK-MT.

Table 2-1 Difference between VEEK-MT2 and VEEK-MT

Signal Name	*VEEK-MT2*	*VEEK-MT*
LCD Touch Point	5 Point Touch	2 Point Touchs
Camera Module	◦ 8-Mega Pixel ◦ Auto Focus ◦ MIPI Decoder	5-Mega Pixel
Motion Sensors	◦ Gyroscope ◦ Accelerometer ◦ Magnetometer	Accelerometer

Chapter 3

Using VEEK-MT2

This section describes the detailed information of the components, connectors, and pin assignments of the VEEK-MT2.

3.1 Configuring the Cyclone IV E FPGA

The Video and Embedded Evaluation Kit (VEEK-MT2) contains a serial configuration device that stores configuration data for the Cyclone IV E FPGA. This configuration data is automatically loaded from the configuration device into the FPGA every time while power is applied to the board. Using the Quartus II software, it is possible to reconfigure the FPGA at any time, and it is also possible to change the non-volatile data that is stored in the serial configuration device. Both types of programming methods are described below.

1. JTAG programming: In this method of programming, named after the IEEE standards Joint Test Action Group, the configuration bit stream is downloaded directly into the Cyclone IV E FPGA. The FPGA will retain this configuration as long as power is applied to the board; the configuration information will be lost when the power is turned off.
2. AS programming: In this method, called Active Serial programming, the configuration bit stream is downloaded into the Altera EPCS64 serial configuration device. It provides non-volatile storage of the bit stream, so that the information is retained even when the power supply to the VEEK-MT2 is turned off. When the board's power is turned on, the configuration data in the EPCS64 device is automatically loaded into the Cyclone IV E FPGA.

■ JTAG Chain on VEEK-MT2

To use the JTAG interface for configuring FPGA device, the JTAG chain on the VEEK-MT2 must form a closed loop that allows Quartus II programmer to detect the FPGA device. **Figure 3-1** illustrates the JTAG chain on the VEEK-MT2. Shorting pin1 and pin2 on JP3 can disable the JTAG signals on the HSMC connector that will form a close JTAG loopback on DE2-115 (See **Figure 3-2**). Thus, only the on-board FPGA device (Cyclone IV E) will be detected by Quartus II programmer. By default, a jumper is placed on pin1 and pin2 of JP3. To prevent any changes to the bus controller (Max II EPM240) described in later sections, users should not adjust the jumper on JP3.

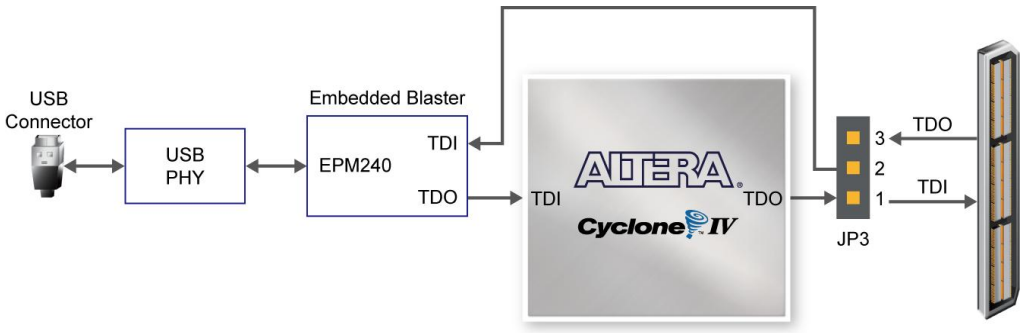

Figure 3-1 JTAG Chain

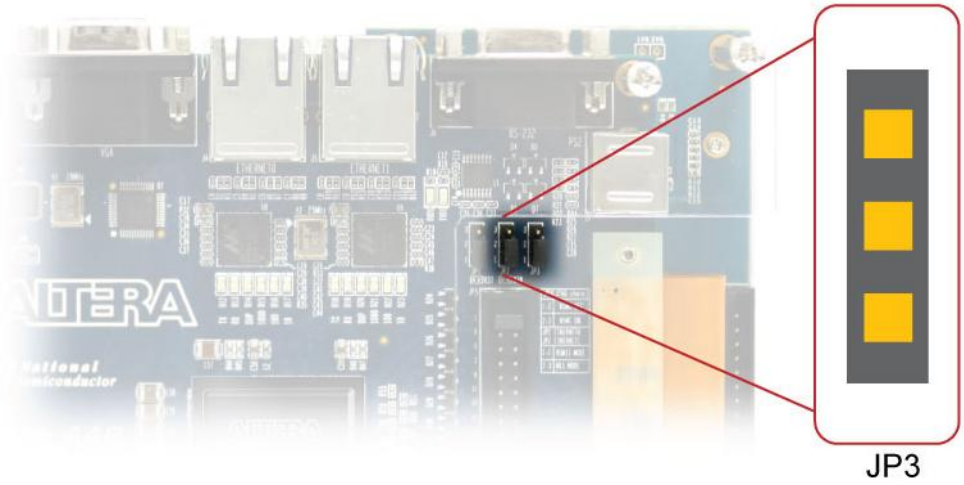

Figure 3-2 JTAG Chain Configuration Header

■ Configuring the FPGA in JTAG Mode

Figure 3-3 illustrates the JTAG configuration setup. To download a configuration bit stream into the Cyclone IV E FPGA, perform the following steps:

- Ensure that power is applied to the VEEK-MT2
- Configure the JTAG programming circuit by setting the RUN/PROG slide switch (SW19) to the RUN position (See Figure 3-4)
- Connect the supplied USB cable to the USB-Blaster port on the VEEK-MT2
- The FPGA can now be programmed by using the Quartus II Programmer module to select a configuration bit stream file with the .sof filename extension

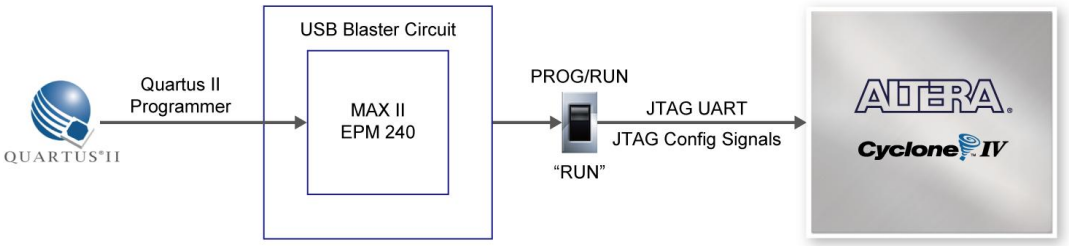

Figure 3-3 JTAG Chain Configuration Scheme

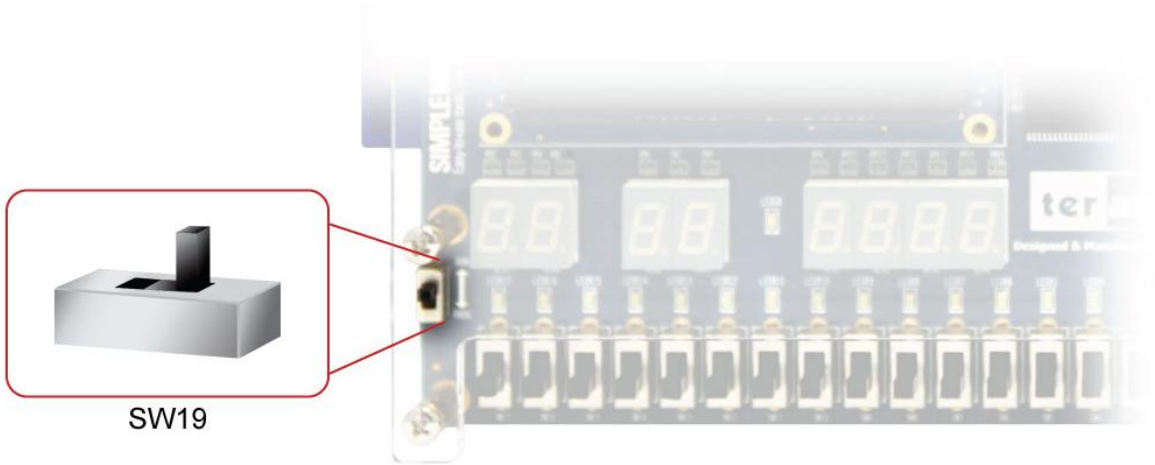

Figure 3-4 The RUN/PROG switch (SW19) is set to JTAG mode

■ Configuring the EPCS64 in AS Mode

Figure 3-5 illustrates the AS configuration set up. To download a configuration bit stream into the EPCS64 serial configuration device, perform the following steps:

- Ensure that power is applied to the VEEK-MT2
- Connect the supplied USB cable to the USB-Blaster port on the VEEK-MT2
- Configure the JTAG programming circuit by setting the RUN/PROG slide switch (SW19) to the PROG position
- The EPCS64 chip can now be programmed by using the Quartus II Programmer module to select a configuration bit stream file with the .pof filename extension
- Once the programming operation is finished, set the RUN/PROG slide switch back to the RUN position and then reset the board by turning the power switch off and back on; this action causes the new configuration data in the EPCS64 device to be loaded into the FPGA chip

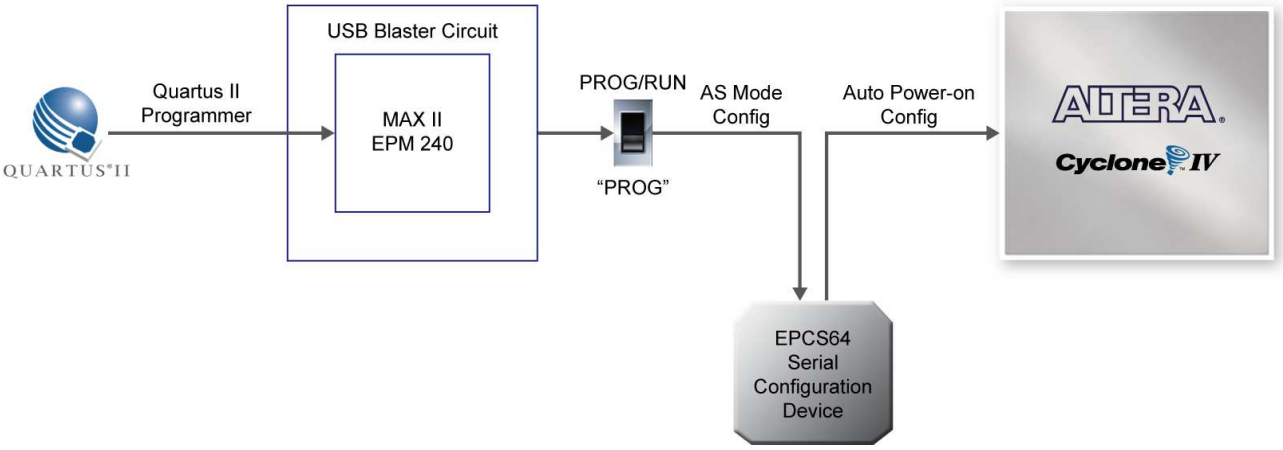

Figure 3-5 The AS Configuration Scheme

3.2 Bus Controller

The VEEK-MT2 comes with a bus controller using the Max II EPM240 that allows user to access the touch screen module through the HSMC connector. This section describes its structure in block diagram-form and its capabilities.

■ Bus Controller Introduction

The bus controller provides level shifting functionality from 2.5V (HSMC) to 3.3V domains.

■ Block Diagram of the Bus Controller

Figure 3-6 gives the block diagram of the connection setup from the HSMC connector to the bus controller on the Max II EPM240 to the touch screen module. To provide maximum flexibility for the user, all connections are established through the HSMC connector. Thus, the user can configure the Cyclone IV E FPGA on the VEEK-MT2 to implement any system design.

Figure 3-6 Block Diagram of the Bus Controller

3.3 Using the 7” LCD Capacitive Touch Screen

The VEEK-MT2 features a 7-inch capacitive amorphous TFT-LCD panel. The LCD touch screen offers resolution of (800x480) to provide users the best display quality for developing applications. The LCD panel supports 24-bit parallel RGB data interface.

The VEEK-MT2 is also equipped with a Touch controller touch controller, which can read the coordinates of the touch points through the serial port interface of Touch controller

To display images on the LCD panel correctly, the RGB color data along with the data enable and clock signals must act according to the timing specification of the LCD touch panel as shown in Table 3-1 and Table 3-2.

Table 3-3 gives the pin assignment information of the LCD touch panel.

Table 3-1 LCD Horizontal Timing Specifications

Item	Symbol	Typical Value			Unit
		Min.	Typ.	Max.	
Horizontal Display Area	thd	-	800	-	DCLK
DCLK Frequency	fclk	26.4	33.3	46.8	MHz
One Horizontal Line	th	862	1056	1200	DCLK
HS pulse width	thpw	1		40	DCLK
HS Blanking	thb	46	46	46	DCLK
HS Front Porch	thfp	16	210	354	DCLK

Table 3-2 LCD Vertical Timing Specifications

Item	Symbol	Typical Value			Unit
		Min.	Typ.	Max.	
Vertical Display Area	tvd	-	480	-	TH
VS period time	tv	510	525	650	TH
VS pulse width	tvpw	1	-	20	TH
VS Blanking	tvb	23	23	23	TH
VS Front Porch	tvfp	7	22	147	TH

Table 3-3 Pin assignment of the LCD touch panel

Signal Name	FPGA Pin No.	Description	I/O Standard
LCD_B0	P28	LCD blue data bus bit 0	2.5V
LCD_B1	P27	LCD blue data bus bit 1	2.5V
LCD_B2	J24	LCD blue data bus bit 2	2.5V
LCD_B3	J23	LCD blue data bus bit 3	2.5V
LCD_B4	T26	LCD blue data bus bit 4	2.5V
LCD_B5	T25	LCD blue data bus bit 5	2.5V
LCD_B6	R26	LCD blue data bus bit 6	2.5V
LCD_B7	R25	LCD blue data bus bit 7	2.5V
LCD_DCLK	V24	LCD Clock	2.5V
LCD_DE	H23	Data Enable signal	2.5V
LCD_DIM	P21	LCD backlight enable	2.5V
LCD_DITH	L23	Dithering setting	2.5V
LCD_G0	P26	LCD green data bus bit 0	2.5V
LCD_G1	P25	LCD green data bus bit 1	2.5V
LCD_G2	N26	LCD green data bus bit 2	2.5V
LCD_G3	N25	LCD green data bus bit 3	2.5V
LCD_G4	L22	LCD green data bus bit 4	2.5V
LCD_G5	L21	LCD green data bus bit 5	2.5V
LCD_G6	U26	LCD green data bus bit 6	2.5V
LCD_G7	U25	LCD green data bus bit 7	2.5V
LCD_HSD	U22	Horizontal sync input.	2.5V
LCD_MODE	L24	DE/SYNC mode select	2.5V
LCD_POWER_CTL	M25	LCD power control	2.5V
LCD_R0	V28	LCD red data bus bit 0	2.5V
LCD_R1	V27	LCD red data bus bit 1	2.5V
LCD_R2	U28	LCD red data bus bit 2	2.5V
LCD_R3	U27	LCD red data bus bit 3	2.5V
LCD_R4	R28	LCD red data bus bit 4	2.5V
LCD_R5	R27	LCD red data bus bit 5	2.5V
LCD_R6	V26	LCD red data bus bit 6	2.5V
LCD_R7	V25	LCD red data bus bit 7	2.5V
LCD_RSTB	K22	Global reset pin	2.5V
LCD_SHLR	H24	Left or Right Display Control	2.5V
LCD_UPDN	K21	Up / Down Display Control	2.5V
LCD_VSD	V22	Vertical sync input.	2.5V
TOUCH _I2C_SCL	T22	touch I2C clock	2.5V
TOUCH _I2C_SDA	T21	touch I2C data	2.5V
TOUCH _INT_n	R23	touch interrupt	2.5V

3.4 Using 8-megapixel Digital Image Sensor

Terasic VEEK-MT2 board equips with an 8M pixel MIPI camera module named OV8865 (See Figure 3-7). The OV8865 color image sensor is a high performance, 8 megapixel RAW image sensor that

delivers 3264x2448. It provides options for multiple resolutions while maintaining full field of view. Users can program image resolution, frame rate, and image quality parameters. Camera functions are controlled via I2C bus (CAMERA_I2C_SDA and CAMERA_I2C_SCL). The I2C device address is 0x6C. For more hardware description and register information about this camera module, please refer to the datasheet named OV8865 Data Sheet.pdf in the VEEK-MT2 System CD.

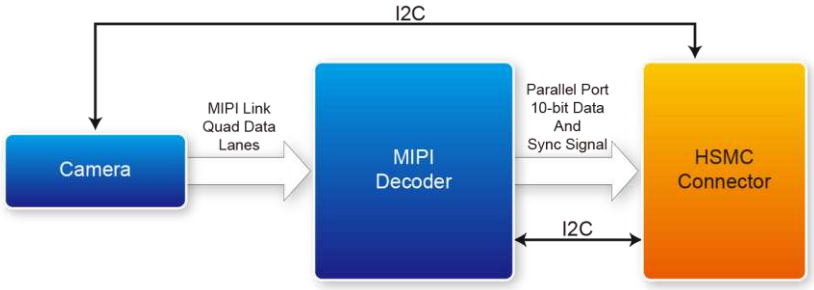

Figure 3-7 Block Diagram of the Bus Controller

■ Voice Coil Motor (VCM)

There is a Voice Coil Motor (VCM) driver chip named VCM149C on the MIPI camera module. Users can use the same I2C bus (I2C device address is 0x18) to modify the DAC value in the VCM driver chip that can allow the VCM to move its lens to the desired position for getting a sharp image and realizing the Auto Focus (AF) feature. Terasic also provides an AF demonstration and IP in the System CD, see section 4.6 for details. The datasheet of this VMC driver IC named VM149C VCM Driver IC.pdf also can be found in the System CD.

■ MIPI Decoder

The MIPI camera module output interface is MIPI interface, which can not directly connect to the Terasic FPGA board; therefore, a MIPI Decoder (TC358748XBG) is added to convert MIPI interface to a parallel port interface. Decoder users can quickly obtain the image data and process it. MIPI Decoder can convert MIPI Interface up to 24-bit data. The Camera module used on the D8M can only output 10 bit data, MIPI_PIXEL_D[9:0] the HSMC connector is the camera image output data bus.
FPGA also can read/write MIPI Decoder through a I2C bus (MIPI_I2C_SDA / MIPI_I2C_SCL ; I2C device address is 0x1C), which is different from the camera module I2C bus. On the VEEK-MT2 board, MIPI Decoder can output clocks to the MIPI camera and FPGA board. So in the demonstrations, most of them show how to control IC PLL parameters as well as others. Detailed clock functions are described in blow.

■ Clock Tree

Figure 3-8 is the VEEK-MT2 board's camera clock tree block diagram. MIPI Decoder PLL receives FPGA Reference Clock (MIPI_REFCLK) and outputs Clock to Camera sensor (MCLK), at the same time, MIPI Decoder PLL will also output a parallel port clock (MIPI_PIXEL_CLK) and feedback to the FPGA to deal with parallel data.

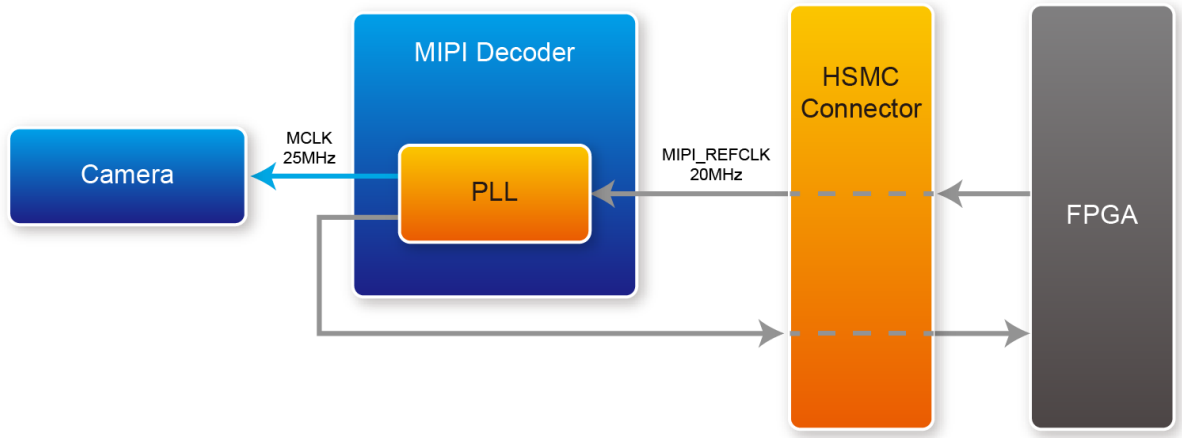

Figure 3-8 Block Diagram of the Bus Controller

In the provided demonstrations, MIPI_REFCLK is set to 20MHz, FPGA transmits this clock to the VEEK-MT2's MIPI Decoder PLL through the HSMC connector. No matter how much the camera resolution is, the MCLK fixed output is 25MHz. According to the output resolution, MIPI_PIXEL_CLK can be set as 25MHz for 640x480@60fps and 50MHz for 1920x1080@15fps.
For more MIPI Decoder PLL setting details, please refer to TC358746AXBG_748XBG_rev09.pdf "Chapter 5: Clock and System" or refer to Terasic demonstrations.

■ Pin Assignment

Table 3-4 Pin assignment of the Camera sensor

Signal Name	FPGA Pin No.	Description	I/O Standard
MIPI_PIXEL_D[0]	F24	Parallel Port Data	2.5V
MIPI_PIXEL_D[1]	F25	Parallel Port Data	2.5V
MIPI_PIXEL_D[2]	D26	Parallel Port Data	2.5V
MIPI_PIXEL_D[3]	C27	Parallel Port Data	2.5V
MIPI_PIXEL_D[4]	F26	Parallel Port Data	2.5V
MIPI_PIXEL_D[5]	E26	Parallel Port Data	2.5V
MIPI_PIXEL_D[6]	G25	Parallel Port Data	2.5V
MIPI_PIXEL_D[7]	G26	Parallel Port Data	2.5V
MIPI_PIXEL_D[8]	H25	Parallel Port Data	2.5V
MIPI_PIXEL_D[9]	H26	Parallel Port Data	2.5V
MIPI_PIXEL_D[10]	M26	Reserve	2.5V
MIPI_PIXEL_D[11]	M25	Reserve	2.5V
MIPI_PIXEL_D[12]	AF27	Reserve	2.5V
MIPI_PIXEL_D[13]	AE28	Reserve	2.5V
MIPI_RESET_n	D27	Master Reset signal for MIPI camera and bridge device	2.5V
MIPI_PIXEL_CLK	J27	Parallel Port Clock signal	2.5V
MIPI_PIXEL_HS	K26	Parallel Port Horizontal Synchronization signal	2.5V
MIPI_PIXEL_VS	K25	Parallel Port Vertical Synchronization signal	2.5V
MIPI_CS_n	F28	Chip Select	2.5V
MIPI_REFCLK	G23	Reference Clock Input of bridge device	2.5V
MIPI_I2C_SCL	AE26	I2C Clock for bridge device	2.5V
MIPI_I2C_SDA	AE27	I2C Data for bridge device	2.5V
CAMERA_PWDN_n	R22	Power Down signal of MIPI camera	2.5V
CAMERA_I2C_SCL	R21	I2C Clock for MIPI camera	2.5V
CAMERA_I2C_SDA	F27	I2C Data for MIPI camera	2.5V
MIPI_MCLK	G24	MIPI camera system clock (Reserve)	2.5V

3.5 Using the Gyroscope, Accelerometer and Magnetometer

The VEEK-MT2 is equipped with a Motion-Tracking device named MPU-9250. The MPU-9250 is a 9-axis Motion-Tracking device that combines a 3-axis gyroscope, 3-axis accelerometer and 3-axis magnetometer. Detail features of these sensors are listed below:

■ Gyroscope

The MPU-9250 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±250, ±500, ±1000, or ±2000 degrees per second (dps). The ADC sample rate is programmable from 8,000 samples per second, down to 3.9 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

■ Accelerometer

The MPU-9250's 3-Axis accelerometer uses separate proof masses for each axis. Acceleration along a particular axis induces displacement on the corresponding proof mass, and capacitive sensors detect the displacement differentially. The MPU-9250's architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0g on the X- and Y-axes and +1g on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. Each sensor has a dedicated sigma-delta ADC for providing digital outputs. The full scale range of the digital output can be adjusted to ±2g, ±4g, ±8g, or ±16g.

■ Magnetometer

The 3-axis magnetometer uses highly sensitive Hall sensor technology. The magnetometer portion of the IC incorporates magnetic sensors for detecting terrestrial magnetism in the X-, Y-, and Z- Axes, a sensor driving circuit, a signal amplifier chain, and an arithmetic circuit for processing the signal from each sensor. Each ADC has a 16-bit resolution and a full scale range of ±4800 μT.

Communication with all registers of the device is performed using either I2C at 400kHz or SPI at 1MHz. For applications requiring faster communications, the sensor and interrupt registers may be read using SPI at 20MHz. For more detailed information of better using this chip, please refer to its datasheet which is available on manufacturer's website or under the /datasheet folder of the system CD. **Table 3-5** gives the pin assignment information of the LCD touch panel. For more detailed information of better using this chip, please refer to its datasheet which is available on manufacturer's website or under the /datasheet folder of the system CD.

Table 3-5 contains the pin names and descriptions of the MPU-9250.

Signal Name	FPGA Pin No.	Description	I/O Standard
MPU_AD0_SDO	K27	I2C Slave Address LSB (AD0); SPI serial data output (SDO)	2.5V
MPU_CS_n	F28	Chip select (SPI mode only)	2.5V
MPU_FSYNC	G28	Frame synchronization digital input	2.5V
MPU_INT	G27	Interrupt digital output	2.5V
MPU_SCL_SCLK	M27	I2C serial clock (SCL); SPI serial clock (SCLK)	2.5V
MPU_SDA_SDI	K28	I2C serial data (SDA); SPI serial data input (SDI)	2.5V

3.6 Using the Ambient Light Sensor

The APDS-9300 is a low-voltage digital ambient light sensor that converts light intensity to digital signal output capable of direct I2C communication. Each device consists of one broadband photodiode (visible plus infrared) and one infrared photodiode. Two integrating ADCs convert the photodiode currents to a digital output that represents the irradiance measured on each channel. This digital output can be input to a microprocessor where illuminance (ambient light level) in lux is derived using an empirical formula to approximate the human-eye response. For more detailed information of better using this chip, please refer to its datasheet which is available on manufacturer's website or under the /datasheet folder of the system CD.

Table 3-6 contains the pin names and descriptions of the ambient light sensor module.

Signal Name	FPGA Pin No.	Description	I/O Standard
LSENSOR_ADDR_SEL	J25	Chip select	2.5V
LSENSOR_INT	L28	Interrupt output	2.5V
LSENSOR_SCL	J26	Serial Communications Clock	2.5V
LSENSOR_SDA	L27	Serial Data	2.5V

3.7 Using Terasic Multi-touch IP

Terasic Multi-touch IP is provided for developers to retrieve user inputs, including multi-touch gestures and single-touch. The file name of this IP is i2c_touch_config.v, which is located in System CD \IP folder.

The IP decodes I2C information and outputs coordinates and gesture information. The inputs and outputs of this IP module are shown below:

```
module  i2c_touch_config(
                //Host Side
                iCLK,
                iRSTN,
                oREADY,
                INT_n,
                oREG_X1,
                oREG_Y1,
                oREG_X2,
                oREG_Y2,
                oREG_X3,
                oREG_Y3,
                oREG_X4,
                oREG_Y4,
                oREG_X5,
                oREG_Y5,
                oREG_GESTURE,
                oREG_TOUCH_COUNT,
                //I2C Side
                I2C_SDAT,
                I2C_SCLK

);
```

The purpose of signals for this IP is described in

Table 3-8. The IP requires a 50 MHz signal as a reference clock to the iCLK pin and system reset signal to the iRSTN. INT_n, The signals of I2C_SCLK, and I2C_SDAT pins should be connected to the MTL_TOUCH_INT_n, MTL_TOUCH_I2C_SCL, and MTL_TOUCH_I2C_SDA signals in the 2x20 GPIO header, respectively.

When touch activity occurs, the control application should check whether the value of oREG_GESTURE matches a pre-defined gesture ID defined in Table 3 4 and the relative X/Y coordinates can be derived from oREG_X and oREG_Y. Figure 3 1 shows the signaltap II waveform of the IP. When the oREADY rises, it indicates touch activity, and the associated information can be collected from the oREG_X1~ oREG_X5, oREG_Y1~ oREG_Y5, oREG_TOUCH_COUNT, and oREG_GESTURE pins.

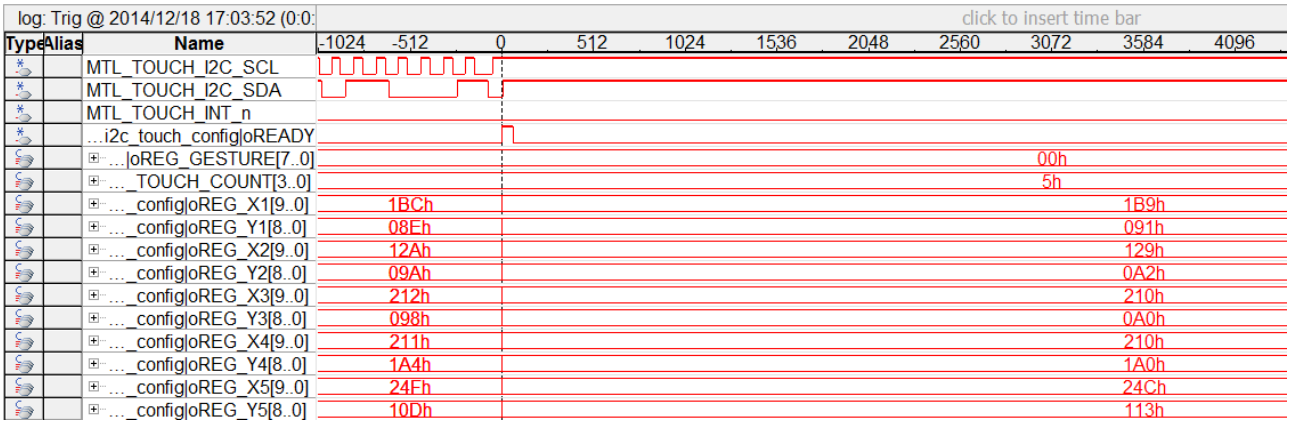

Figure 3-9 Signaltap II Waveform for Multi-Touch IP

Table 3-7 Definition of Terasic Multi-touch IP Signals

Pin Name	Direction	Description
iCLK	Input	Connect to 50MHz clock
iRSTN	Input	Connect to system reset signal
INT_n	Input	Connect to interrupt pin of touch IC
oREADY	Output	Triggered when the data of following six outputs are valid
oREG_X1	Output	10-bit X coordinate of first touch point
oREG_Y1	Output	9-bit Y coordinate of first touch point
oREG_X2	Output	10-bit X coordinate of second touch point
oREG_Y2	Output	9-bit Y coordinate of second touch point
oREG_X3	Output	10-bit X coordinate of first touch point
oREG_Y3	Output	9-bit Y coordinate of second touch point
oREG_X4	Output	10-bit X coordinate of first touch point
oREG_Y4	Output	9-bit Y coordinate of second touch point
oREG_X5	Output	10-bit X coordinate of first touch point
oREG_Y5	Output	9-bit Y coordinate of second touch point
oREG_TOUCH_COUNT	Output	2-bit touch count. Valid value is 0, 1, or 2.
oREG_GESTURE	Output	8-bit gesture ID (See Table 3-8)
I2C_SCLK	Output	Connect to I2C clock pin of touch IC
I2C_SDAT	Inout	Connect to I2C data pin of touch IC

The gestures and IDs supported are shown in

Table 3-8.

Table 3-8 Gestures and Its IDs

Gesture	ID (hex)
Move Up	0x10
Move Left	0x14
Move Down	0x18
Move Right	0x1C
Zoom In	0x48
Zoom Out	0x49
No Gesture	0x00

Note:

The Terasic IP Multi-touch IP can also be found under the \IP folder in the system CD, as well as the reference designs.