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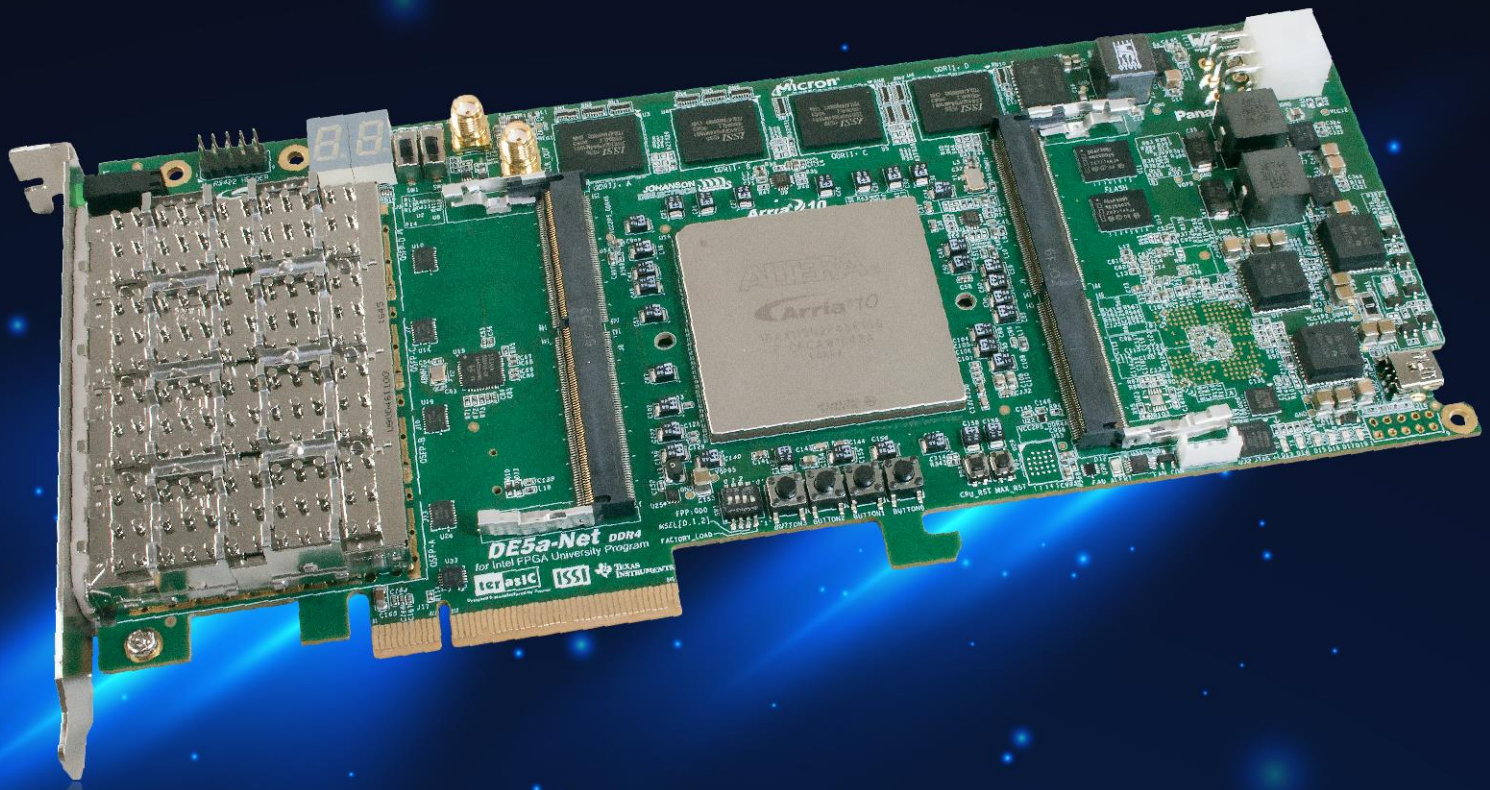
DE5a-Net

DDR4 Edition

FPGA Development Kit User Manual



Arria 10 | Flash | PCI EXPRESS | DDR4 | QDRII+ | QSFP+

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Contents

Chapter 1

Overview

This chapter provides an overview of the DE5a-Net DDR4 Edition Development Board and installation guide.

1.1 General Description

The Terasic DE5a-Net DDR4 Edition Arria 10 GX FPGA Development Kit provides the ideal hardware solution for designs that demand high capacity and bandwidth memory interfacing, ultra-low latency communication, and power efficiency. With a full-height, 3/4-length form-factor package, the DE5a-Net is designed for the most demanding high-end applications, empowered with the top-of-the-line Altera Arria 10 GX, delivering the best system-level integration and flexibility in the industry.

The Arria® 10 GX FPGA features integrated transceivers that transfer at a maximum of 12.5 Gbps, allowing the DE5a-Net to be fully compliant with version 3.0 of the PCI Express standard, as well as allowing an ultra low-latency, straight connections to four external 40G QSFP+ modules. Not relying on an external PHY will accelerate mainstream development of network applications enabling customers to deploy designs for a broad range of high-speed connectivity applications. For designs that demand high capacity and high speed for memory and storage, the DE5a-Net delivers with two independent banks of DDR4 SO-DIMM RAM, four independent banks of QDRII+ SRAM, high-speed parallel flash memory. The feature-set of the DE5a-Net fully supports all high-intensity applications such as low-latency trading, cloud computing, high-performance computing, data acquisition, network processing, and signal processing.

1.2 Key Features

The following hardware is implemented on the DE5a-Net board:

■ FPGA

- Intel Arria® 10 GX FPGA (10AX115N2F45E1SG)

■ FPGA Configuration

- On-Board USB Blaster II or JTAG header for FPGA programming
- Fast passive parallel (FPPx32) configuration via MAX II CPLD and flash memory

■ General user input/output:

- 8 LEDs
- 4 push-buttons
- 2 slide switches
- 2 seven-segment displays

■ Clock System

- 50MHz Oscillator
- Programmable clock generators Si5340A and Si5340B
- One SMA connector for external clock input
- One SMA connector for clock output

■ Memory

- DDR4 SO-DIMM SDRAM
- QDRII+ SRAM
- FLASH

Communication Ports

- Four QSFP+ connectors
- PCI Express (PCIe) x8 edge connector
- One RS422 transceiver with Expansion Header

System Monitor and Control

- Temperature sensor
- Fan control
- Power monitor

Power

- PCI Express 6-pin power connector, 12V DC Input
- PCI Express edge connector power

Mechanical Specification

- PCI Express full-height and 3/4-length

1.3 Block Diagram

Figure 1-1 shows the block diagram of the DE5a-Net board. To provide maximum flexibility for the users, all key components are connected with the Arria 10 GX FPGA device. Thus, users can configure the FPGA to implement any system design.

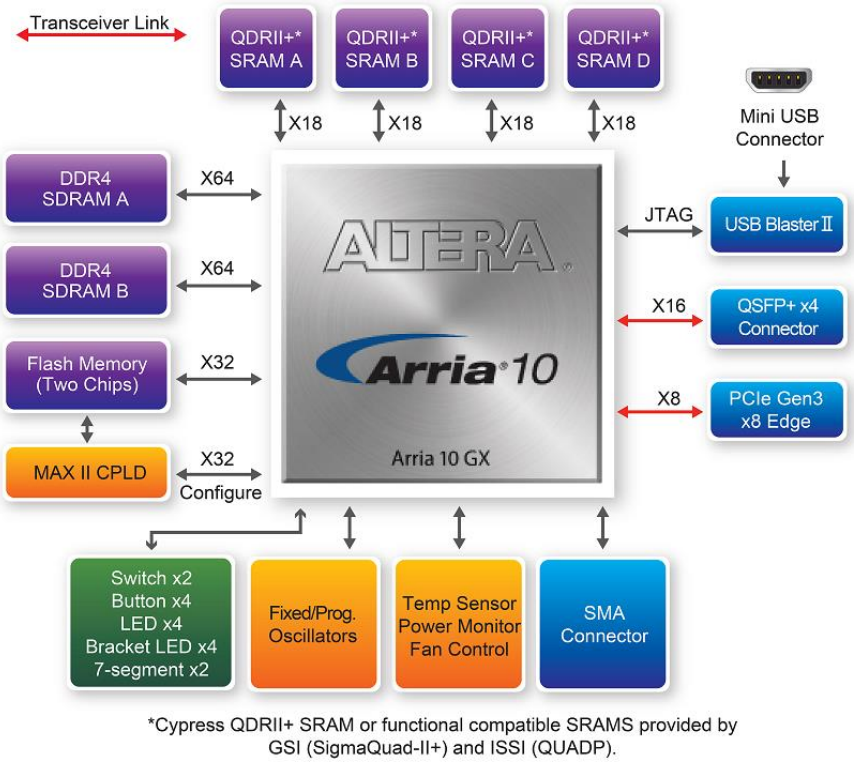

Figure 1-1 Block diagram of the DE5a-Net board

Below is more detailed information regarding the blocks in **Figure 1-1**.

■ Arria 10 GX FPGA

- 10AX115N2F45E1SG
- 1,150K logic elements (LEs)
- 67-Mbits embedded memory
- 48 transceivers (12.5Gbps)
- 3,036 18-bit x 19-bit multipliers
- 1,518 Variable-precision DSP blocks
- 4 PCI Express hard IP blocks
- 768 user I/Os

- 384 LVDS channels
- 32 phase locked loops (PLLs)

■ JTAG Header and FPGA Configuration

- On-board USB Blaster II or JTAG header for use with the Quartus Prime Programmer
- MAXII CPLD 5M2210 System Controller and Fast Passive Parallel (FPP x32) configuration

■ Memory Devices

- 32MB QDRII+ SRAM
- Up to 16GB DDR4 SO-DIMM SDRAM for each DDR4 socket
- 256MB FLASH

■ General User I/O

- 8 user controllable LEDs
- 4 user push buttons
- 2 user slide switches
- 2 seven-segment displays

■ On-Board Clock

- 50MHz oscillator
- Programming PLL providing clock for 40G QSFP+ transceiver
- Programming PLL providing clock for PCIe transceiver
- Programming PLL providing clocks for DDR4 SDRAM and QDRII+ SRAM

Four QSFP+ Ports

- Four QSFP+ connector (40 Gbps+)

PCI Express x8 Edge Connector

- Support for PCIe x8 Gen1/2/3
- Edge connector for PC motherboard with x8 or x16 PCI Express slot

Power Source

- PCI Express 6-pin DC 12V power
- PCI Express edge connector power

Temperature Range

- FPGA: 0°C ~100°C

1.4 Operating Temperature - Important

Please read the following instructions carefully to prevent damage to your DE5a-NET board.

The operating temperature range of Arria 10 GX device on DE5a-NET-DDR4 is 0°C ~100°C. When the FPGA temperature stays over 100°C for a long time, the FPGA could be damaged. It is therefore strongly recommended to use this board in an environment with sufficient airflow to dissipate the heat generated. It is also recommended to monitor the FPGA temperature continuously by adding Terasic IP introduced in **chapter 5.1** in the project. When the FPGA temperature is getting close to 100°C, please turn off the board immediately to reduce the FPGA temperature and protect the FPGA device.

Please refer to the directory /Demonstrations/Board_Protection in the DE5a-NET System CD for details about the Verilog based temperature monitor design example.

Chapter 2

Board Components

This chapter introduces all the important components on the DE5a-Net.

2.1 Board Overview

Figure 2-1 is the top and bottom view of the DE5a-Net development board. It depicts the layout of the board and indicates the location of the connectors and key components. Users can refer to this figure for relative location of the connectors and key components.

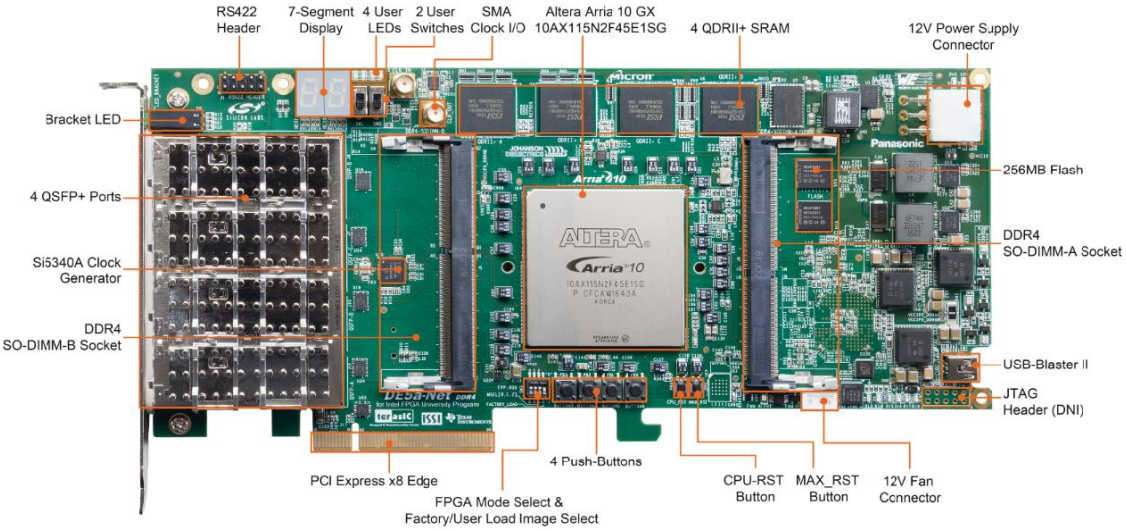

Figure 2-1 FPGA Board (Top)

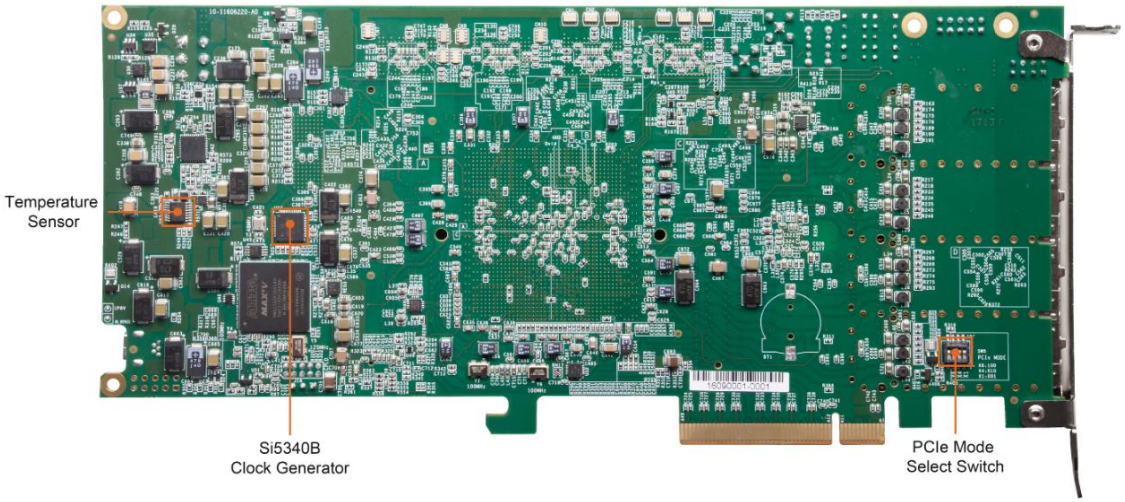

Figure 2-2 FPGA Board (Bottom)

2.2 Configuration, Status and Setup

■ Configure

The FPGA board supports two configuration methods for the Arria 10 FPGA:

- Configure the FPGA using the on-board USB-Blaster II.
- Flash memory configuration of the FPGA using stored images from the flash memory on power-up.

For programming by on-board USB-Blaster II, the following procedures show how to download a configuration bit stream into the Arria 10 GX FPGA:

- Make sure that power is provided to the FPGA board
- Connect your PC to the FPGA board using a mini-USB cable and make sure the USB-Blaster II driver is installed on PC.
- Launch Quartus Prime programmer and make sure the USB-Blaster II is detected.
- In Quartus Prime Programmer, add the configuration bit stream file (.sof), check the associated “Program/Configure” item, and click “Start” to start FPGA

programming.

Status LED

The FPGA Board development board includes board-specific status LEDs to indicate board status. Please refer to **Table 2-1** for the description of the LED indicator.

Table 2-1 Status LED

Board Reference	LED Name	Description
D6	12-V Power	Illuminates when 12-V power is active.
D5	3.3-V Power	Illuminates when 3.3-V power is active.
D16	CONF DONE	Illuminates when the FPGA is successfully configured. Driven by the MAX II CPLD 5M2210 System Controller.
D15	Loading	Illuminates when the MAX II CPLD 5M2210 System Controller is actively configuring the FPGA. Driven by the MAX II CPLD 5M2210 System Controller with the Embedded Blaster CPLD.
D17	Error	Illuminates when the MAX II CPLD 5M2210 System Controller fails to configure the FPGA. Driven by the MAX II CPLD 5M2210 System Controller.
D19	PAGE	Illuminates when FPGA is configured by the factory configuration bit stream.

Setup PCI Express Control DIP switch

The PCI Express Control DIP switch (SW5) is provided to enable or disable different configurations of the PCIe Connector. **Table 2-2** lists the switch controls and description.

Table 2-2 SW5 PCIe Control DIP Switch

Board Reference	Signal Name	Description	Default
SW5.1	PCIE_PRSNT2n_x1	On : Enable x1 presence detect Off: Disable x1 presence detect	Off
SW5.2	PCIE_PRSNT2n_x4	On : Enable x4 presence detect Off: Disable x4 presence detect	Off
SW5.3	PCIE_PRSNT2n_x8	On : Enable x8 presence detect Off: Disable x8 presence detect	On

■ Setup Configure Mode

The position 1~3 of DIP switch SW3 are used to specify the configuration mode of the FPGA. As currently only one mode is supported, please set all positions as shown in **Figure 2-3**.

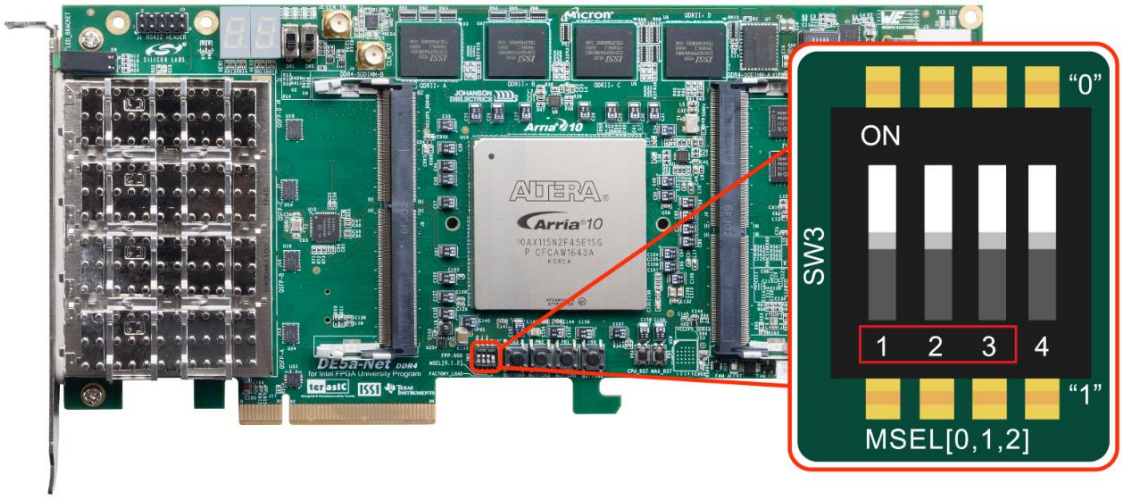

Figure 2-3 Position of DIP switch SW3 for Configure Mode

■ Select Flash Image for Configuration

The position 4 of DIP switch SW3 is used to specify the image for configuration of the FPGA. Setting Position 4 of SW3 to "1" (down position) specifies the default factory image

to be loaded, as shown in **Figure 2-4**. Setting Position 4 of SW3 to “0” (up position) specifies the DE5a-Net to load a user-defined image, as shown in **Figure 2-5**.

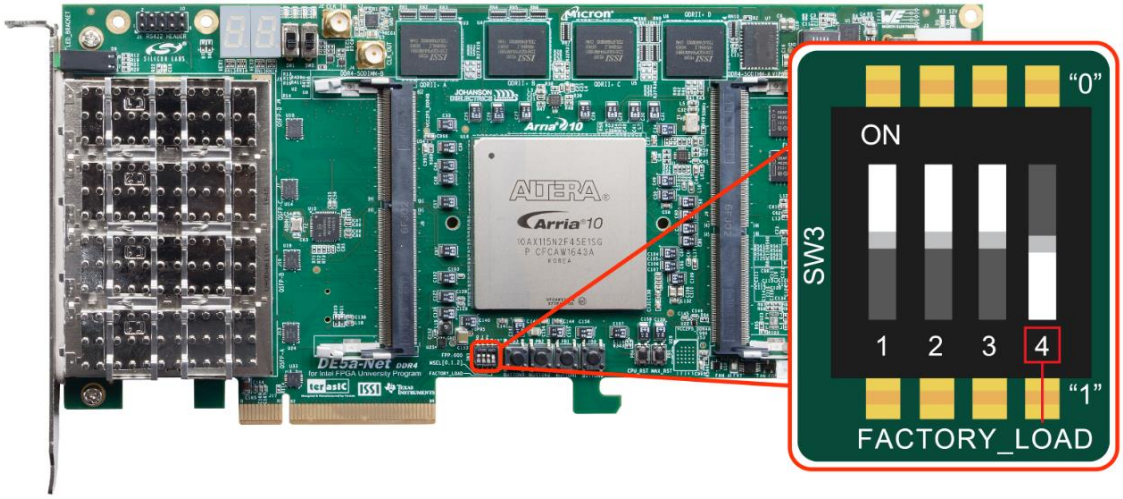

Figure 2-4 Position of DIP switch SW3 for Image Select – Factory Image Load

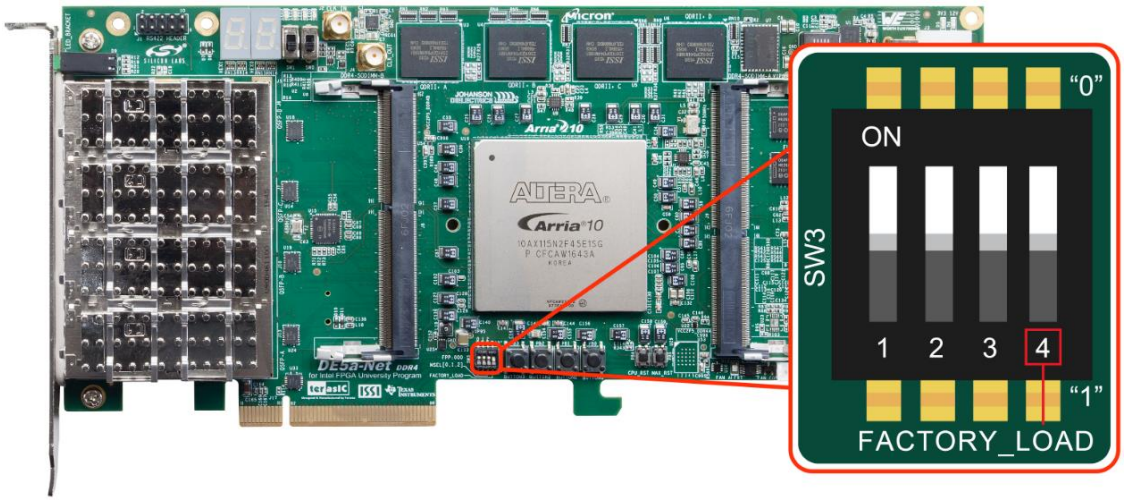

Figure 2-5 Position of DIP switch SW3 for Image Select – User Image Load

2.3 General User Input/Output

This section describes the user I/O interface to the FPGA.

■ User Defined Push-buttons

The FPGA board includes four user defined push-buttons that allow users to interact with the Arria 10 GX device. Each push-button provides a high logic level or a low logic level when it is not pressed or pressed, respectively. **Table 2-3** lists the board references, signal names and their corresponding Arria 10 GX device pin numbers.

Table 2-3 Push-button Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Arria 10 GX Pin Number
PB0	BUTTON0	High Logic Level when the button is not pressed	1.2-V	PIN_AJ13
PB1	BUTTON1		1.2-V	PIN_AE13
PB2	BUTTON2		1.2-V	PIN_AV16
PB3	BUTTON3		1.2-V	PIN_AR9

■ User-Defined Slide Switch

There are two slide switches on the FPGA board to provide additional FPGA input control. When a slide switch is in the DOWN position or the UPPER position, it provides a low logic level or a high logic level to the Arria 10 GX FPGA, respectively, as shown in **Figure 2-6**.

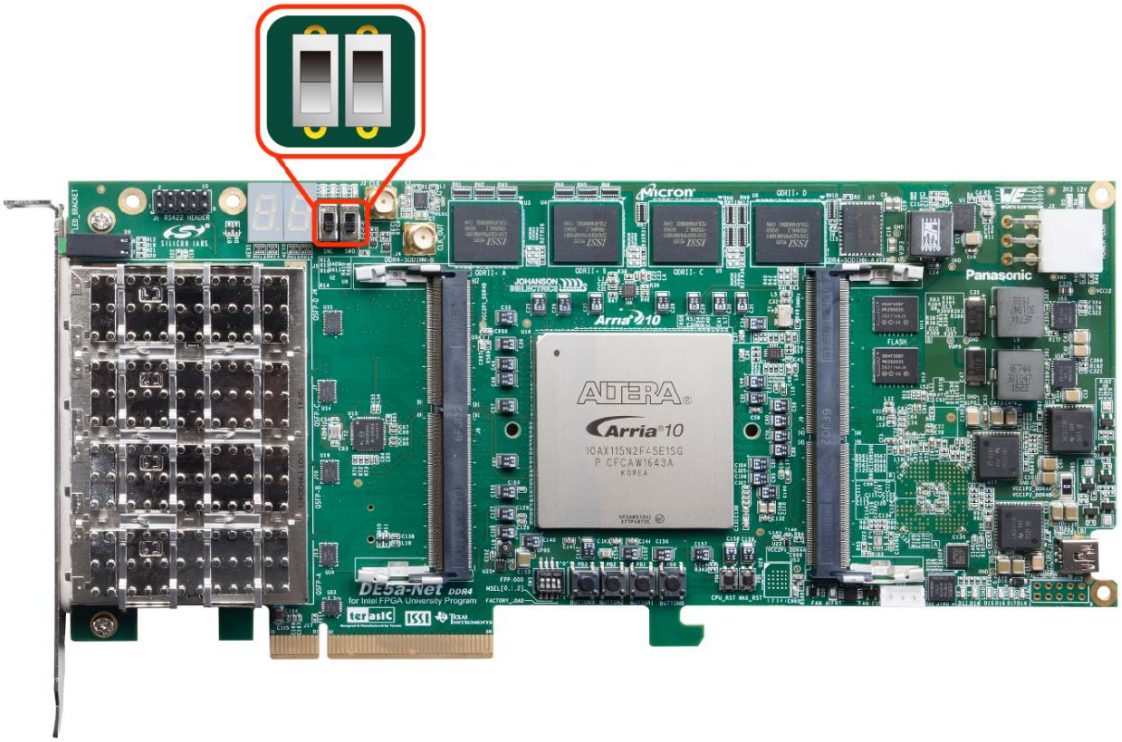

Figure 2-6 2 Slide switches

Table 2-4 lists the signal names and their corresponding Arria 10 GX device pin numbers.

Table 2-4 Slide Switch Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Arria 10 GX Pin Number
SW0	SW0	High logic level when SW in the UPPER position.	1.2-V	PIN_AY28
SW1	SW1		1.2-V	PIN_AM27

■ User-Defined LEDs

The FPGA board consists of 8 user-controllable LEDs to allow status and debugging signals to be driven to the LEDs from the designs loaded into the Arria 10 GX device. Each LED is driven directly by the Arria 10 GX FPGA. The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin names on the FPGA that are connected to the LEDs is given in **Table 2-5**.

Table 2-5 User LEDs Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Arria 10 GX Pin Number
D4	LED0	Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	1.8-V	PIN_T11
D3	LED1		1.8-V	PIN_R11
D2	LED2		1.8-V	PIN_N15
D1	LED3		1.8-V	PIN_M15
D9-1	LED_BRACKET0		1.8-V	PIN_AF10
D9-3	LED_BRACKET1		1.8-V	PIN_AF9
D9-5	LED_BRACKET2		1.8-V	PIN_Y13
D9-7	LED_BRACKET3		1.8-V	PIN_W11

■ 7-Segment Displays

The FPGA board has two 7-segment displays. As indicated in the schematic in **Figure 2-7**, the seven segments are connected to pins of the Arria 10 GX FPGA. Applying a low or high logic level to a segment will turn it on or turn it off, respectively.

Each segment in a display is identified by an index listed from 0 to 6 with the positions given in **Figure 2-8**. In addition, the decimal point is identified as DP. **Table 2-6** shows the mapping of the FPGA pin assignments to the 7-segment displays.

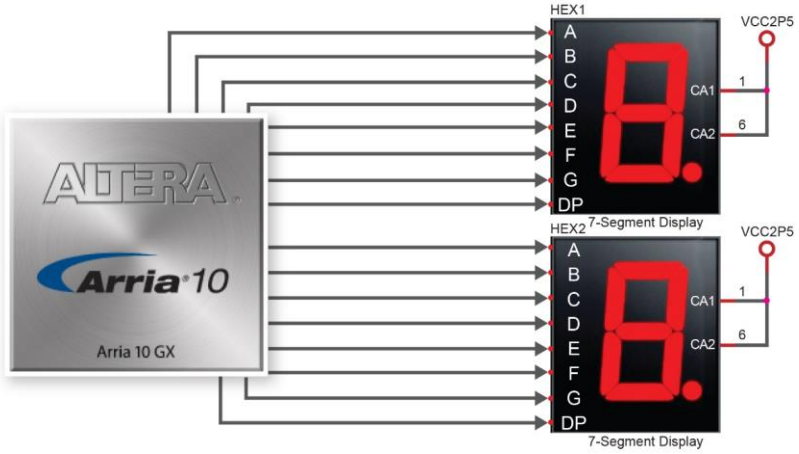

Figure 2-7 Connection between 7-segment displays and Arria 10 GX FPGA

Figure 2-8 Position and index of each segment in a 7-segment display

Table 2-6 User LEDs Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Arria 10 GX Pin Number
HEX1	HEX1_D0	User-Defined 7-Segment Display. Driving logic 0 on the I/O port turns the 7-segment signal ON. Driving logic 1 on the I/O port turns the 7-segment signal OFF.	1.2-V	PIN_AM32
HEX1	HEX1_D1		1.2-V	PIN_AN32
HEX1	HEX1_D2		1.2-V	PIN_AN31
HEX1	HEX1_D3		1.2-V	PIN_AP31
HEX1	HEX1_D4		1.2-V	PIN_BA35
HEX1	HEX1_D5		1.2-V	PIN_BD34
HEX1	HEX1_D6		1.2-V	PIN_AR31
HEX1	HEX1_DP		1.2-V	PIN_BC28
HEX0	HEX0_D0		1.2-V	PIN_AW8
HEX0	HEX0_D1		1.2-V	PIN_AY8
HEX0	HEX0_D2		1.2-V	PIN_AY9
HEX0	HEX0_D3		1.2-V	PIN_BA9
HEX0	HEX0_D4		1.2-V	PIN_BB9
HEX0	HEX0_D5		1.2-V	PIN_BD10
HEX0	HEX0_D6		1.8-V	PIN_V10
HEX0	HEX0_DP		1.8-V	PIN_AG9

2.4 Temperature Sensor and Fan Control

The FPGA board is equipped with a temperature sensor, MAX1619, which provides temperature sensing and over-temperature alert. These functions are accomplished by connecting the temperature sensor to the internal temperature sensing diode of the Arria 10 GX device. The temperature status and alarm threshold registers of the temperature sensor can be programmed by a two-wire SMBus, which is connected to the Arria 10 GX FPGA. In addition, the 7-bit POR slave address for this sensor is set to '0011000b'.**Figure 2-9** shows the connection between the temperature sensor and the Arria 10 GX FPGA.

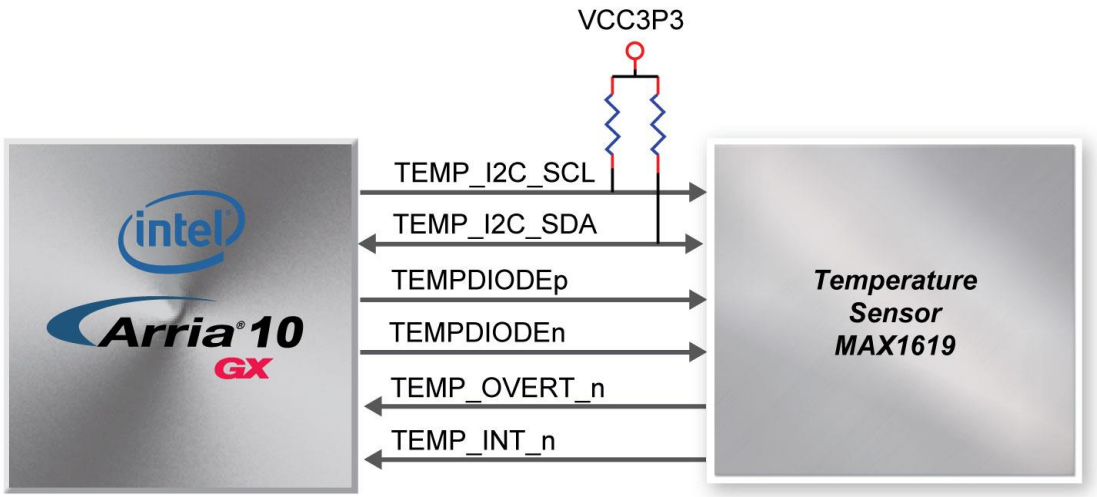

Figure 2-9 Connections between the temperature sensor and FPGA

An optional 3-pin +12V fan located on J15 of the FPGA board is intended to reduce the temperature of the FPGA. The board is equipped with a Fan-Speed regulator and monitor, MAX6650, through an I2C interface, Users regulate and monitor the speed of fan depending on the measured system temperature. **Figure2-10** shows the connection between the Fan-Speed Regulator and Monitor and the Arria 10 GX FPGA.

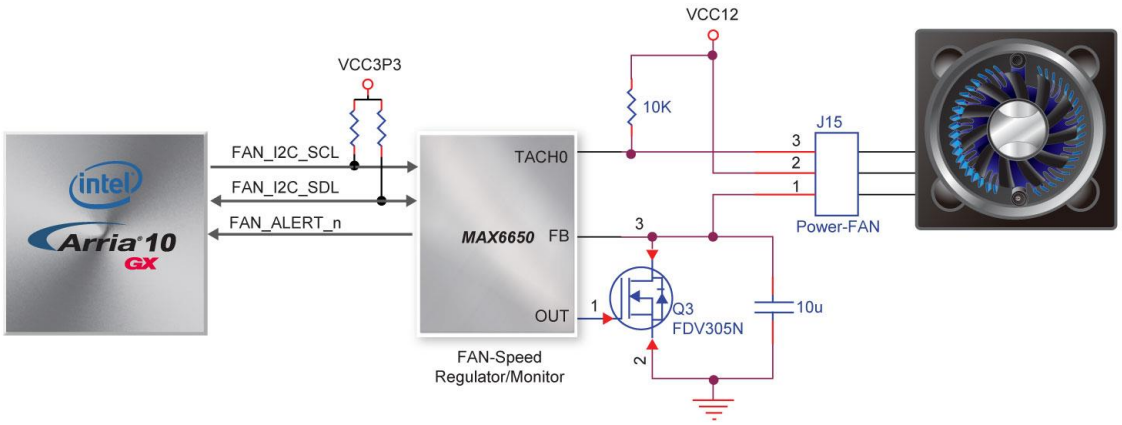

Figure 2-10 Connections between the Fan-Speed Regulator/ Monitor and the Arria 10 GX FPGA

The pin assignments for the associated interface are listed in **Table 2-7**.

Table 2-7 Temperature Sensor and Fan Speed Control Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Arria 10 GX Pin Number
TEMPDIODEp	Positive pin of temperature diode in Arria 10	-	PIN_N21
TEMPDIODEn	Negative pin of temperature diode in Arria 10	-	PIN_P21
TEMP_I2C_SCL	SMBus clock	1.2-V	PIN_AW11
TEMP_I2C_SDA	SMBus data	1.2-V	PIN_AY12
TEMP_OVERT_n	SMBus alert (interrupt)	1.2-V	PIN_AT14
TEMP_INT_n	SMBus alert (interrupt)	1.2-V	PIN_AU12
FAN_I2C_SCL	2-Wire Serial Clock	1.2-V	PIN_AJ33
FAN_I2C_SDA	2-Wire Serial-Data	1.2-V	PIN_AL32
FAN_ALERT_n	Active-low AL ERT input	1.2-V	PIN_AL31

2.5 Power Monitor

The DE5a-Net has implemented a power monitor chip to monitor the board input power voltage and current. **Figure 2-11** shows the connection between the power monitor chip and the Arria 10 GX FPGA. The power monitor chip monitors both shunt voltage drops and board input power voltage allows user to monitor the total board power consumption. Programmable calibration value, conversion times, and averaging, combined with an internal multiplier, enable direct readouts of current in amperes and power in watts. Table 2-8 shows the pin assignment of power monitor I2C bus.

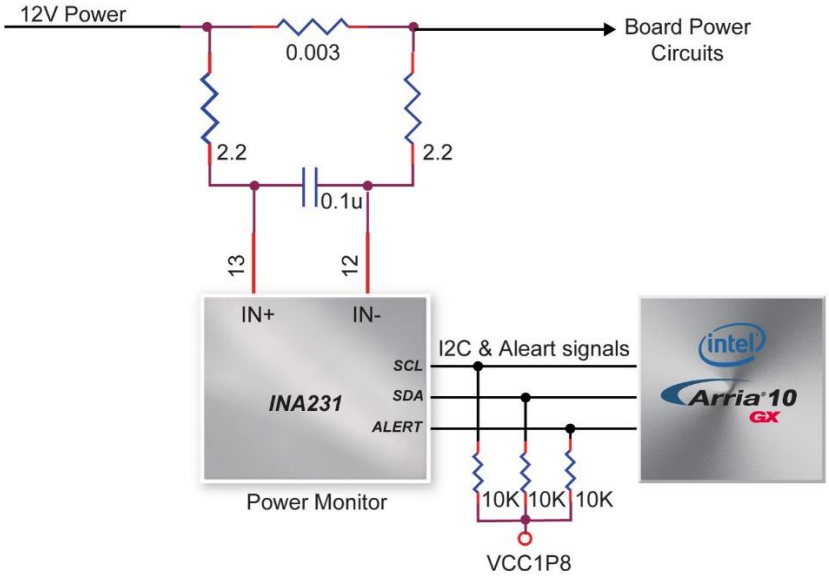

Figure 2-11 Connections between the Power Monitor and FPGA

Table 2-8 Pin Assignment of Power Monitor I2C bus

Schematic Signal Name	Description	I/O Standard	Arria 10 GX Pin Number
POWER_MONITOR_I2C_SCL	Power Monitor SCL	1.8V	PIN_AT26
POWER_MONITOR_I2C_SDA	Power Monitor SDA	1.8V	PIN_AP25
POWER_MONITOR_ALERT	Power Monitor ALERT	1.8V	PIN_BD23

2.6 Clock Circuit

The development board includes one 50 MHz and two programmable clock generators. **Figure 2-12** shows the default frequencies of on-board all external clocks going to the Arria 10 GX FPGA.

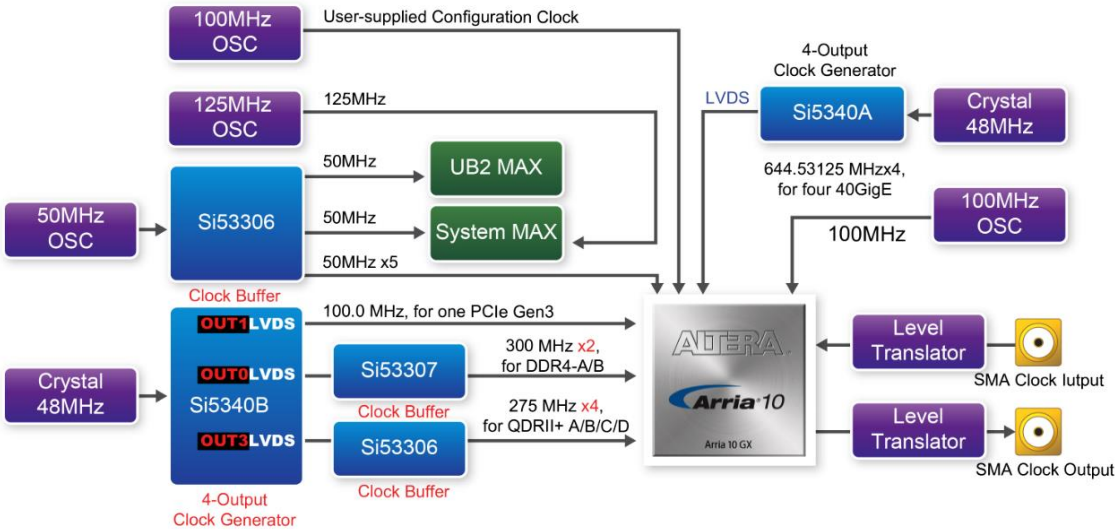

Figure 2-12 Clock circuit of the FPGA Board

A clock buffer is used to duplicate the 50 MHz oscillator, so there are five 50MHz clocks fed into different five FPGA banks. The two programming clock generators are low-jitter oscillators which are used to provide special and high-quality clock signals for high-speed transceivers and high bandwidth memory. Through I2C serial interface, the clock generator controllers in the Arria 10 GX FPGA can be used to program the Si5340A and Si5340B to generate 40G Ethernet QSFP+, PCIe and high bandwidth memory reference clocks respectively. Two SMA connectors provide external clock input and clock output respectively.

Table 2-9 lists the clock source, signal names, default frequency and their corresponding Arria 10 GX device pin numbers.

Table 2-9 Clock Source, Signal Name, Default Frequency, Pin Assignments and Functions

Source	Schematic Signal Name	Default Frequency	I/O Standard	Arria 10 GX Pin Number	Application
Y1	CLK_50_B2J	50.0 MHz	1.8V	PIN_W36	
	CLK_50_B2L		1.8V	PIN_H32	
	CLK_50_B3D		1.8V	PIN_AN7	
	CLK_50_B3F		1.8V	PIN_G12	
	CLK_50_B3H		1.8V	PIN_D21	
Y7	CLK_100_B3D	100.0MHz	1.8V	PIN_AH11	
J2	SMA_CLKIN	User Defined	1.8V	PIN_AC32	External Clock Input
J4	SMA_CLKOUT	User Defined	1.8V	PIN_AA36	Clock Output
U15	QSFPA_REFCLK_p	644.53125 MHz	LVDS	PIN_AH5	40G QSFP+ A port
	QSFPB_REFCLK_p	644.53125 MHz	LVDS	PIN_AD5	40G QSFP+ B port
	QSFPC_REFCLK_p	644.53125 MHz	LVDS	PIN_Y5	40G QSFP+ C port
	QSFPD_REFCLK_p	644.53125 MHz	LVDS	PIN_T5	40G QSFP+ D port
U44	DDR4A_REFCLK_p	300 MHz	LVDS	PIN_AV33	DDR4 reference clock for A port
	DDR4B_REFCLK_p	300 MHz	LVDS	PIN_AP14	DDR4 reference clock for B port
	QDRIIA_REFCLK_p	275 MHz	LVDS	PIN_L9	QDRII+ reference clock for A port
	QDRIIB_REFCLK_p	275 MHz	LVDS	PIN_N18	QDRII+ reference clock for B port
	QDRIIC_REFCLK_p	275 MHz	LVDS	PIN_G24	QDRII+ reference clock for C port
	QDRIID_REFCLK_p	275 MHz	LVDS	PIN_M34	QDRII+ reference clock for D port
	OB_PCIE_REFCLK_p	100 MHz	LVDS	PIN_AK40	PCIe reference clock