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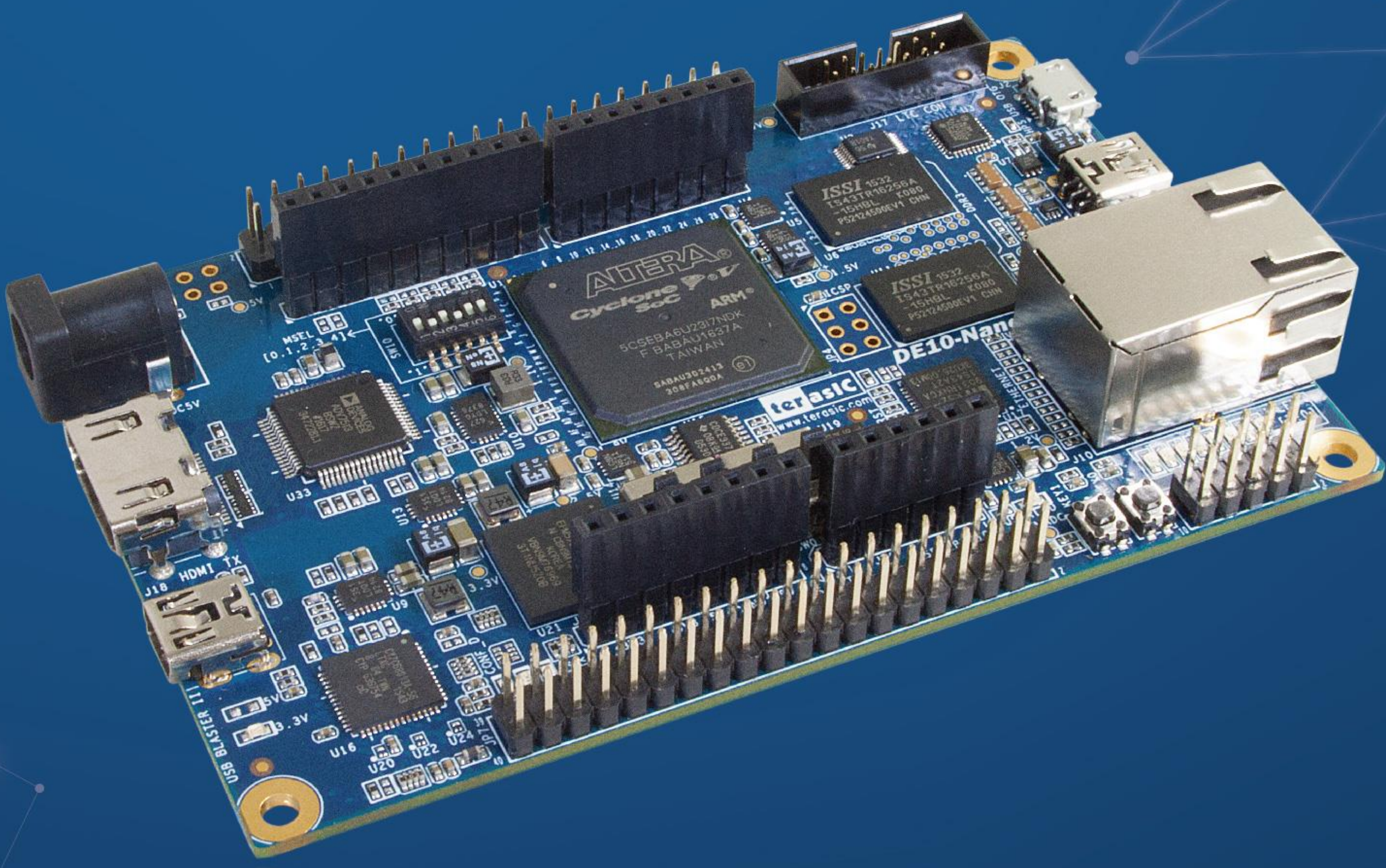
DE10-Nano

Cyclone V SoC with Dual-core ARM Cortex-A9

User Manual



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DE10-Nano

CONTENT

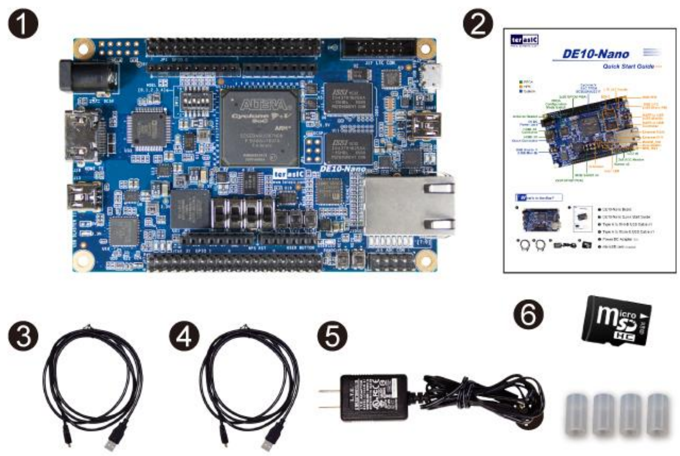
Chapter 1
DE10-Nano Development Kit

The DE10-Nano Development Kit presents a robust hardware design platform built around the Intel System-on-Chip (SoC) FPGA, which combines the latest dual-core Cortex-A9 embedded cores with industry-leading programmable logic for ultimate design flexibility. Users can now leverage the power of tremendous re-configurability paired with a high-performance, low-power processor system. Intel's SoC integrates an ARM-based hard processor system (HPS) consisting of processor, peripherals and memory interfaces tied seamlessly with the FPGA fabric using a high-bandwidth interconnect backbone. The DE10-Nano development board is equipped with high-speed DDR3 memory, analog to digital capabilities, Ethernet networking, and much more that promise many exciting applications.

The DE10-Nano Development Kit contains all the tools needed to use the board in conjunction with a computer that runs the Microsoft Windows XP or later.

1.1 Package Contents

Figure 1-1 shows a photograph of the DE10-Nano package.



❶ DE10-Nano Board
❷ DE10-Nano Quick Start Guide
❸ Type A to Mini-B USB Cable x1
❹ Type A to Micro-B USB Cable x1
❺ Power DC Adapter (5V)
❻ microSD card (installed)
❼ Four Silicon Footstands

Figure 1-1 The DE10-Nano package contents

The DE10-Nano package includes:

- The DE10-Nano development board
- DE10-Nano Quick Start Guide
- USB cable Type A to Mini-B for FPGA programming or UART control
- USB cable Type A to Micro-B for USB OTG connect to PC
- 5V DC power adapter
- microSD Card (Installed)
- Four Silicon Footstands

1.2 DE10-Nano System CD

The DE10-Nano System CD contains all the documents and supporting materials associated with DE10-Nano, including the user manual, system builder, reference designs, and device datasheets. Users can download this system CD from the link: http://de10-nano.terasic.com/cd.

1.3 Getting Help

Here are the addresses where you can get help if you encounter any problems:

Terasic Technologies

9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan

Email: support@terasic.com

Tel.: +886-3-575-0880

Website: DE10-Nano.terasic.com

Chapter 2

Introduction of the DE10-Nano Board

This chapter provides an introduction to the features and design characteristics of the board.

2.1 Layout and Components

Figure 2-1 and Figure 2-2 shows a photograph of the board. It depicts the layout of the board and indicates the location of the connectors and key components.

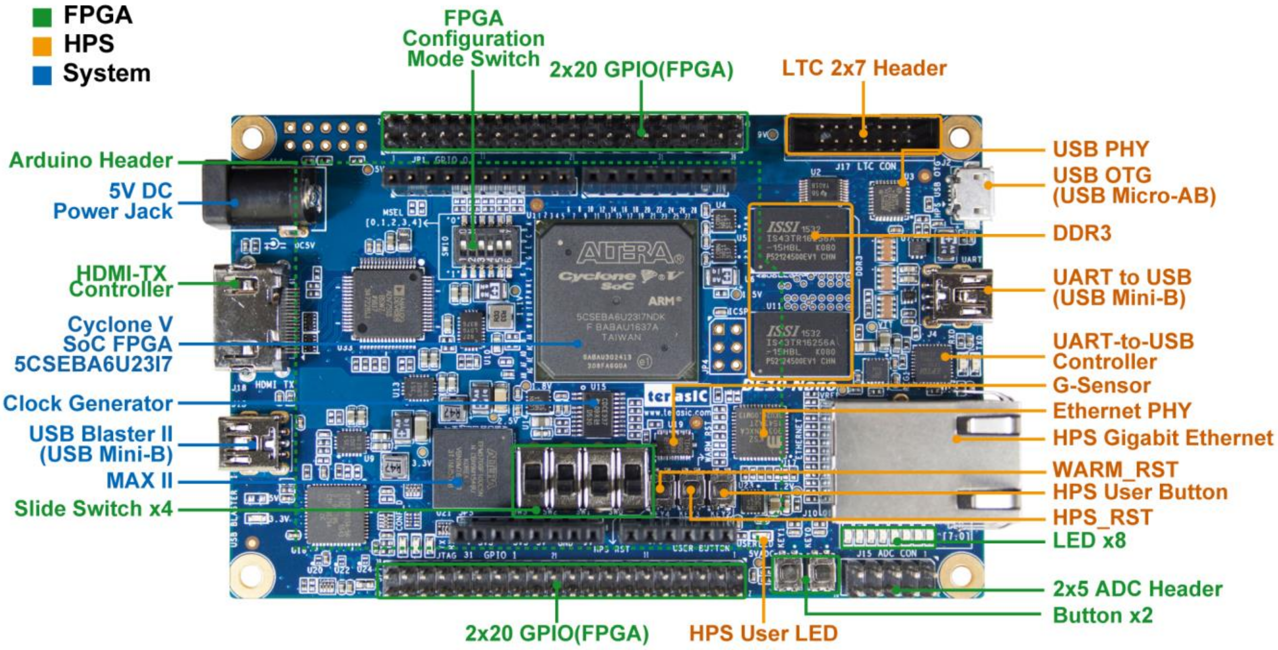


Figure 2-1 DE10-Nano development board (top view)

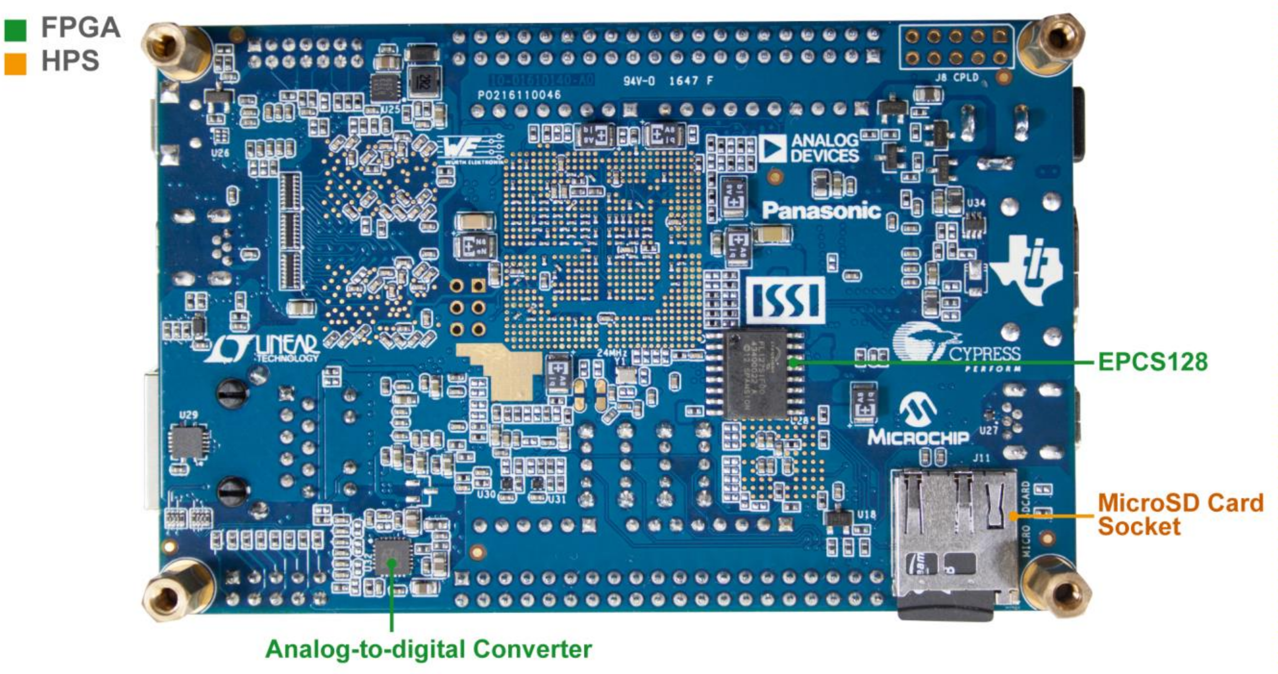


Figure 2-2 DE10-Nano development board (bottom view)

The DE10-Nano board has many features that allow users to implement a wide range of designed circuits, from simple circuits to various multimedia projects.

The following hardware is provided on the board:

■ FPGA

- Cyclone® V SE 5CSEBA6U23I7 device
- Serial configuration device – EPCS128
- USB-Blaster II onboard for programming; JTAG Mode
- 2 push-buttons
- 4 slide switches
- 8 green user LEDs
- Three 50MHz clock sources from the clock generator
- Two 40-pin expansion header
- One Arduino expansion header (Uno R3 compatibility), can connect with Arduino shields.
- One 10-pin Analog input expansion header. (shared with Arduino Analog input)
- A/D converter, 4-wire SPI interface with FPGA
- HDMI TX, compatible with DVI v1.0 and HDCP v1.4

HPS (Hard Processor System)

- 800MHz Dual-core ARM Cortex-A9 processor
- 1GB DDR3 SDRAM (32-bit data bus)
- 1 Gigabit Ethernet PHY with RJ45 connector
- port USB OTG, USB Micro-AB connector
- Micro SD card socket
- Accelerometer (I2C interface + interrupt)
- UART to USB, USB Mini-B connector
- Warm reset button and cold reset button
- One user button and one user LED
- LTC 2x7 expansion header

2.2 Block Diagram of the DE10-Nano Board

Figure 2-3 is the block diagram of the board. All the connections are established through the Cyclone V SoC FPGA device to provide maximum flexibility for users. Users can configure the FPGA to implement any system design.

Detailed information about **Figure 2-3** are listed below.

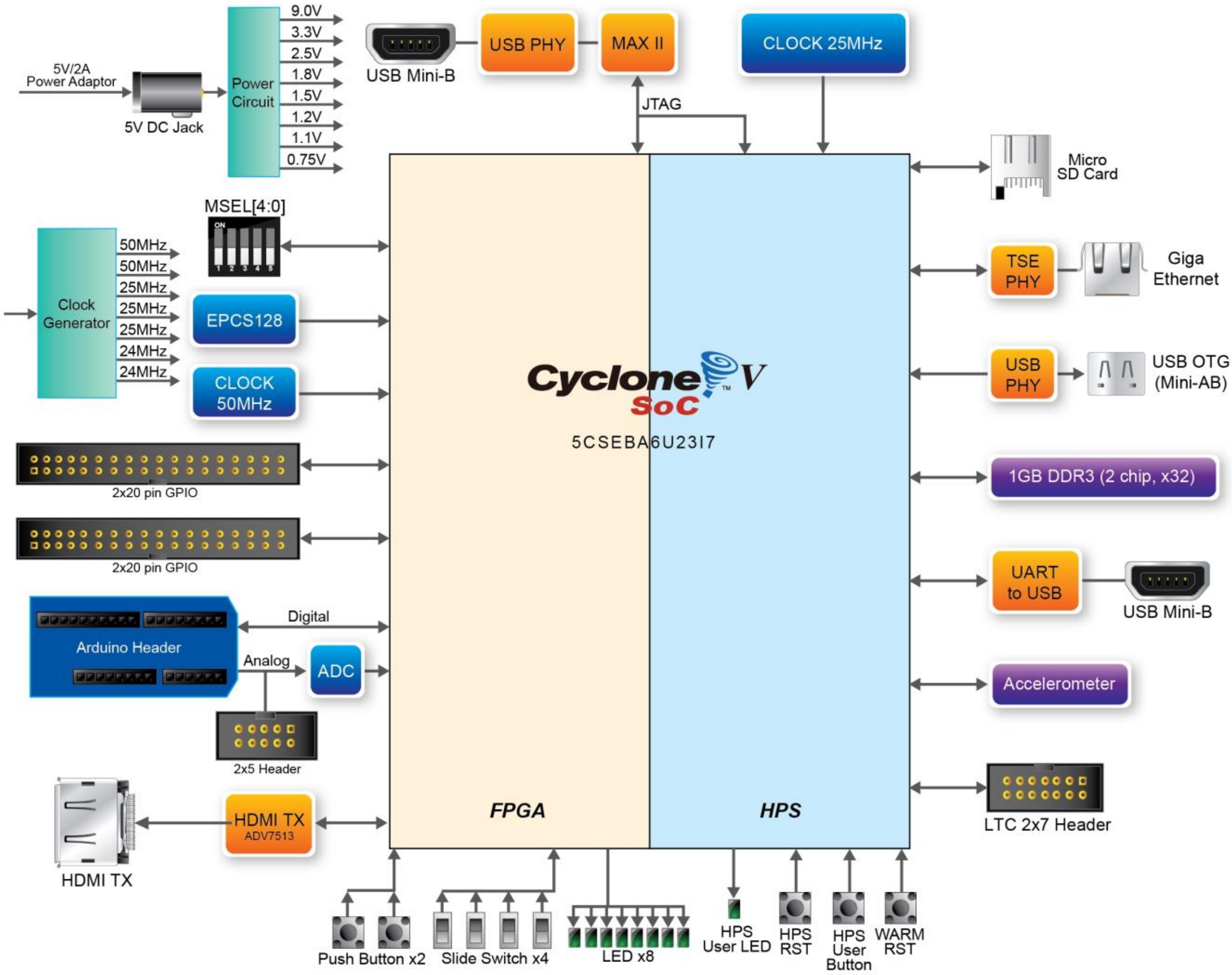


Figure 2-3 Block diagram of DE10-Nano

FPGA Device

- Cyclone V SoC 5CSEBA6U23I7 Device
- Dual-core ARM Cortex-A9 (HPS)
- 110K programmable logic elements
- 5,570 Kbits embedded memory
- 6 fractional PLLs

Configuration and Debug

- Serial configuration device – EPCS128 on FPGA
- Onboard USB-Blaster II (Mini-B USB connector)

Memory Device

- 1GB (2x256Mx16) DDR3 SDRAM on HPS
- Micro SD card socket on HPS

Communication

- One USB 2.0 OTG (ULPI interface with USB Micro-AB connector)
- UART to USB (USB Mini-B connector)
- 10/100/1000 Ethernet

Connectors

- Two 40-pin expansion headers
- Arduino expansion header
- One 10-pin ADC input header
- One LTC connector (one Serial Peripheral Interface (SPI) Master ,one I2C and one GPIO interface)

Display

- HDMI TX, compatible with DVI v1.0 and HDCP v1.4

ADC

- 12-Bit Resolution, 500Ksps Sampling Rate. SPI Interface.
- 8-Channel Analog Input. Input Range : 0V ~ 4.096V.

Switches, Buttons, and Indicators

- 3 user Keys (FPGA x2, HPS x1)
- 4 user switches (FPGA x4)
- 9 user LEDs (FPGA x8, HPS x 1)
- 2 HPS reset buttons (HPS_RESET_n and HPS_WARM_RST_n)

Sensors

- G-Sensor on HPS

Power

- 5V DC input

Chapter 3
Using the DE10-Nano Board

This chapter provides an instruction to use the board and describes the peripherals.

3.1 Settings of FPGA Configuration Mode

When the DE10-Nano board is powered on, the FPGA can be configured from EPCS or HPS.

The MSEL[4:0] pins are used to select the configuration scheme. It is implemented as a 6-pin DIP switch **SW10** on the DE10-Nano board, as shown in **Figure 3-1**.

Table 3-1 shows the relation between MSEL[4:0] and DIP switch (SW10).

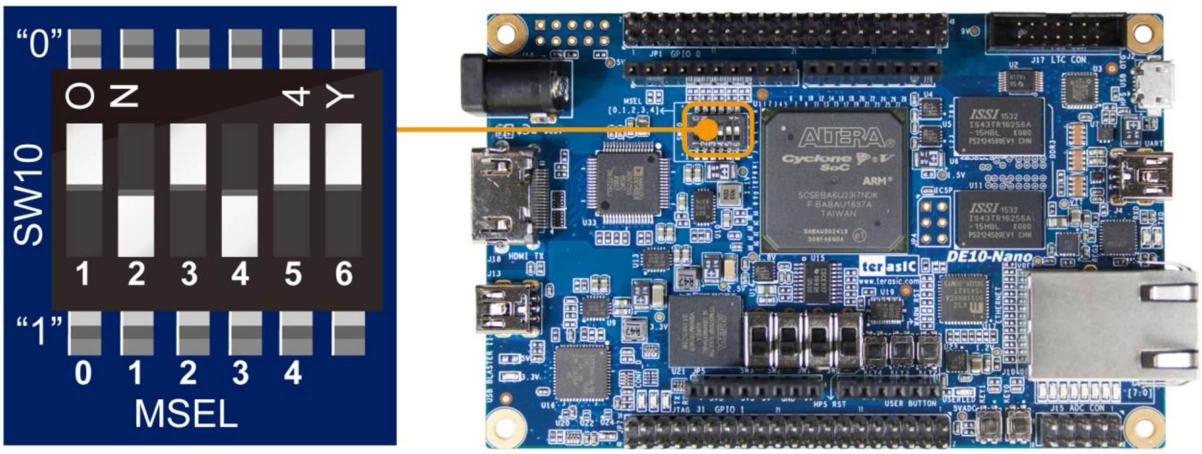


Figure 3-1 DIP switch (SW10) setting of FPPx32 mode.

Table 3-1 FPGA Configuration Mode Switch (SW10)

Board Reference	Signal Name	Description	Default
SW10.1	MSEL0	Use these pins to set the FPGA Configuration scheme	ON ("0")
SW10.2	MSEL1		OFF ("1")
SW10.3	MSEL2		ON ("0")
SW10.4	MSEL3		OFF ("1")
SW10.5	MSEL4		ON ("0")
SW10.6	N/A	N/A	N/A

Table 3-2 shows MSEL[4:0] setting for FPGA configure, and default setting is FPPx32 Mode on DE10-Nano Board.

When the board is powered on and MSEL[4:0] set to "10010", the FPGA is configured from EPCS, which is pre-programmed with the default code. If developers using the "Linux LXDE Desktop" SD Card image, the MSEL[4:0] needs to be set to "01010" before the board is powered on.

Table 3-2 MSEL Pin Settings for FPGA Configure of DE10-Nano Board

Configuration	SW10.1 MSEL0	SW10.2 MSEL1	SW10.3 MSEL2	SW10.4 MSEL3	SW10.5 MSEL4	SW10.6	Description
AS	ON	OFF	ON	ON	OFF	N/A	FPGA configured from EPCS
FPPx32(1) / Compression Enabled / Fast POR (Default)	ON	OFF	ON	OFF	ON	N/A	FPGA configured from HPS software: U-Boot, with image stored on the SD card, like LXDE Desktop (default)
FPPx16 / Compression Disabled / Fast POR	ON	ON	ON	ON	ON	N/A	FPGA configured from HPS software: U-Boot, with image stored on the SD card

(1): Please refer to the following link:

https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/cyclone-v/cv_5v4.pdf , See Table 4-1: Configuration Schemes for FPGA Configuration by the HPS

3.2 Configuration of Cyclone V SoC FPGA on DE10-Nano

There are two types of programming method supported by DE10-Nano:

1. JTAG programming: It is named after the IEEE standards Joint Test Action Group.

   The configuration bit stream is downloaded directly into the Cyclone V SoC FPGA. The FPGA will retain its current status as long as the power keeps applying to the board; the configuration information will be lost when the power is off.

2. AS programming: The other programming method is Active Serial configuration.

   The configuration bit stream is downloaded into the serial configuration device (EPCS128), which provides non-volatile storage for the bit stream. The information is retained within EPCS128 even if the DE10-Nano board is turned off. When the board is powered on, the configuration data in the EPCS128 device is automatically loaded into the Cyclone V SoC FPGA.

■ JTAG Chain on DE10-Nano Board

The FPGA device can be configured through JTAG interface on DE10-Nano board, but the JTAG chain must form a closed loop, which allows Quartus II programmer to the detect FPGA device. **Figure 3-2** illustrates the JTAG chain on DE10-Nano board.

In addition, the DE10-Nano has one external JTAG Header (J8) reserved for users to connect to JTAG chain of the DE10-Nano via external blaster. The J8 header is not installed, so users need to solder a 2.54mm 2 x 5 male pin header if it is necessary.

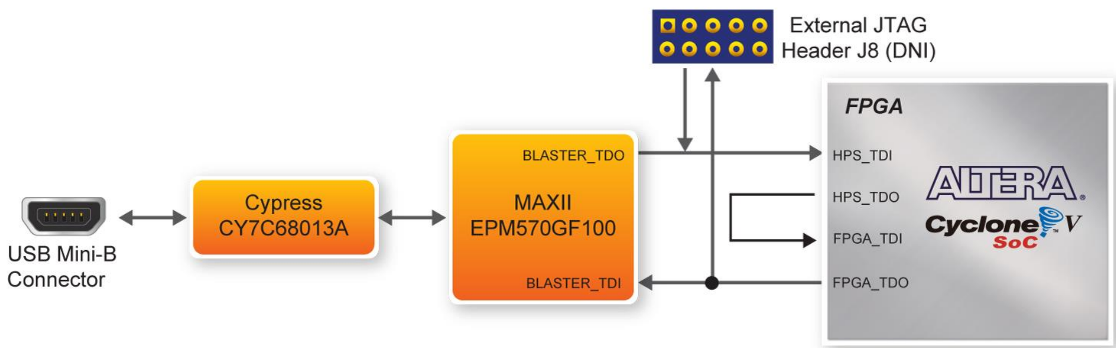


Figure 3-2 Path of the JTAG chain

■ Configure the FPGA in JTAG Mode

There are two devices (FPGA and HPS) on the JTAG chain. The following shows how the FPGA is programmed in JTAG mode step by step.

Open the Quartus II programmer, please Choose **Tools** > **Programmer**. The Programmer window opens. Please click "**Hardware Setup**", as circled in **Figure 3-3**.

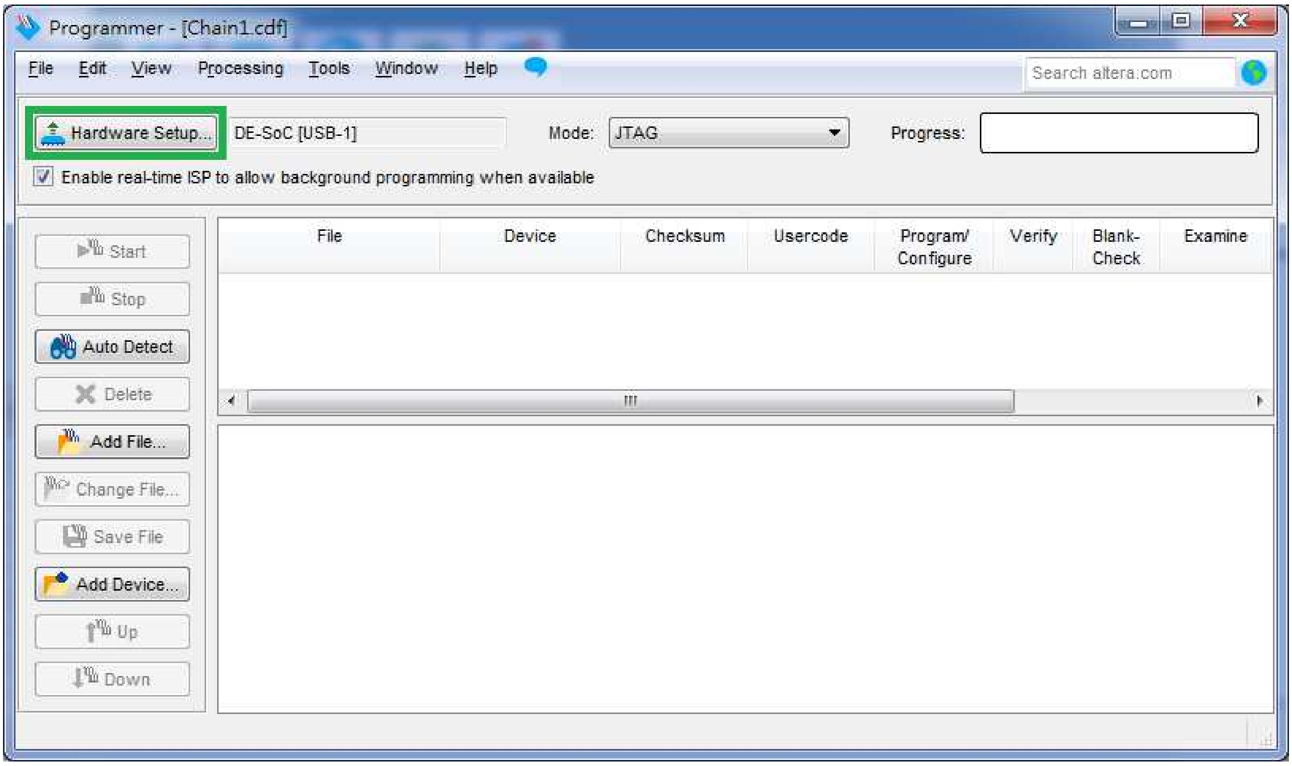


Figure 3-3 Programmer Window

If it is not already turned on, turn on the **DE-SoC [USB-1]** option under currently selected hardware and click "**Close**" to close the window. See **Figure 3-4**.

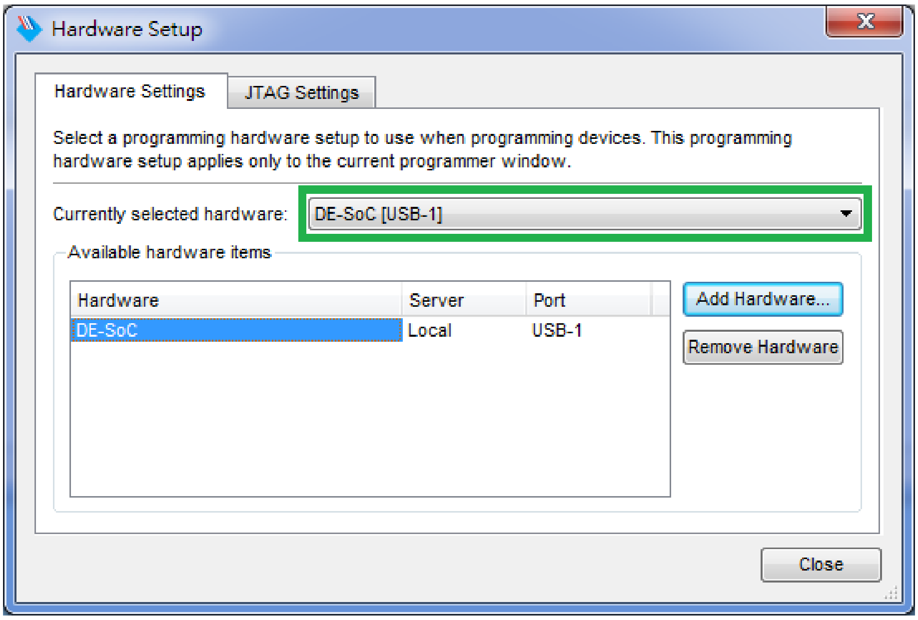


Figure 3-4 Hardware Setting

Return to the Quartus II programmer and click "**Auto Detect**", as circled in **Figure 3-5**

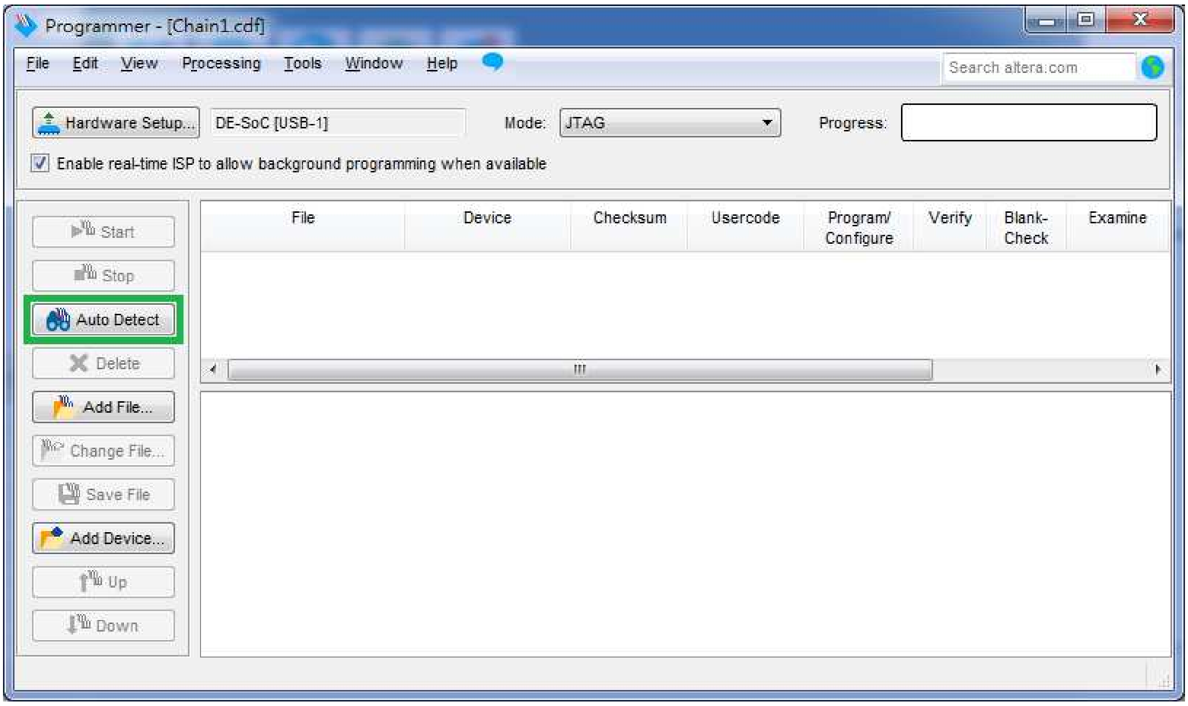


Figure 3-5 Detect FPGA device in JTAG mode

If the device is detected, the window of the selection device is opened, Please select detected device associated with the board and click "**OK**" to close the window, as circled in **Figure 3-6**.

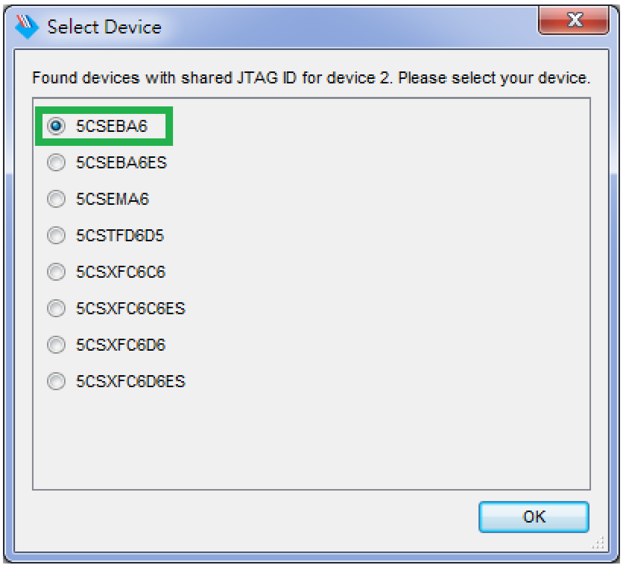


Figure 3-6 Select 5CSEBA6 device

Both FPGA and HPS are detected, as shown in **Figure 3-7**.

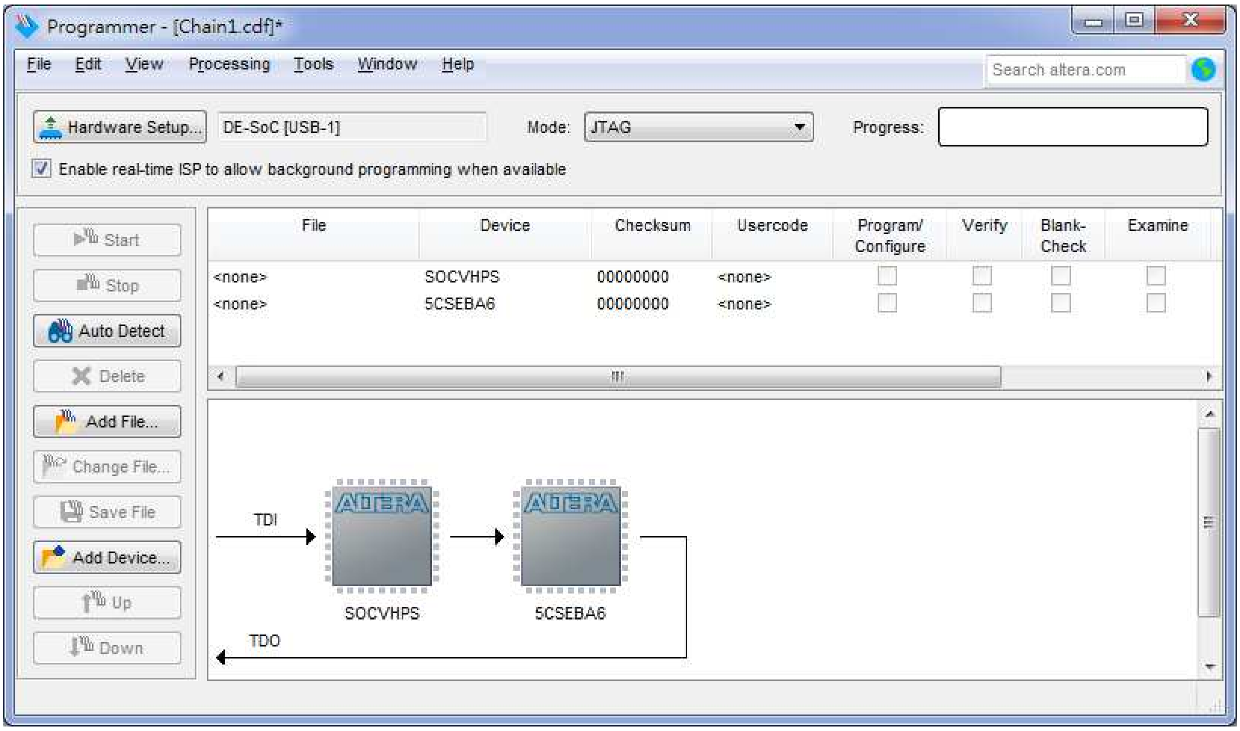


Figure 3-7 FPGA and HPS detected in Quartus programmer

Right click on the FPGA device and open the .sof file to be programmed, as highlighted in **Figure 3-8**.

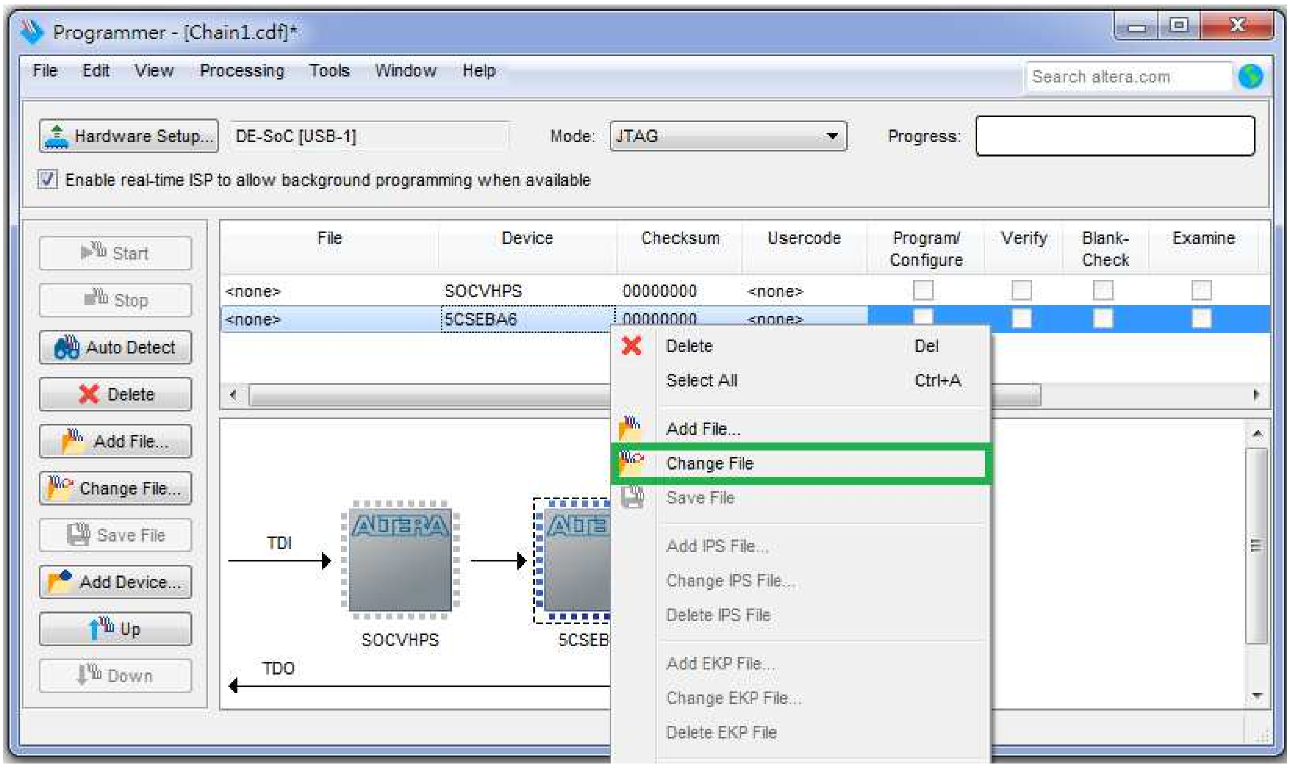


Figure 3-8 Open the .sof file to be programmed into the FPGA device

Select the .sof file to be programmed, as shown in **Figure 3-9**.

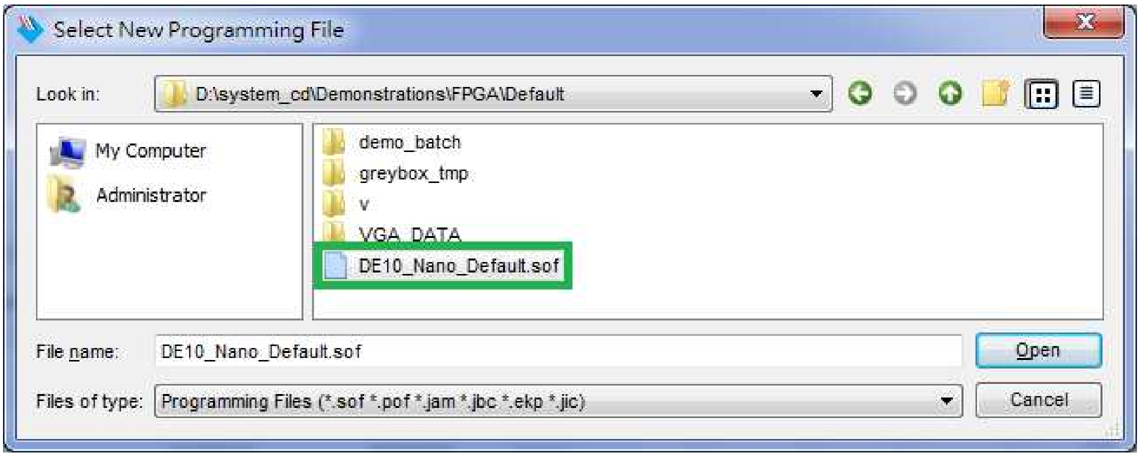


Figure 3-9 Select the .sof file to be programmed into the FPGA device

Click “Program/Configure” check box and then click “Start” button to download the .sof file into the FPGA device, as shown in **Figure 3-10**.

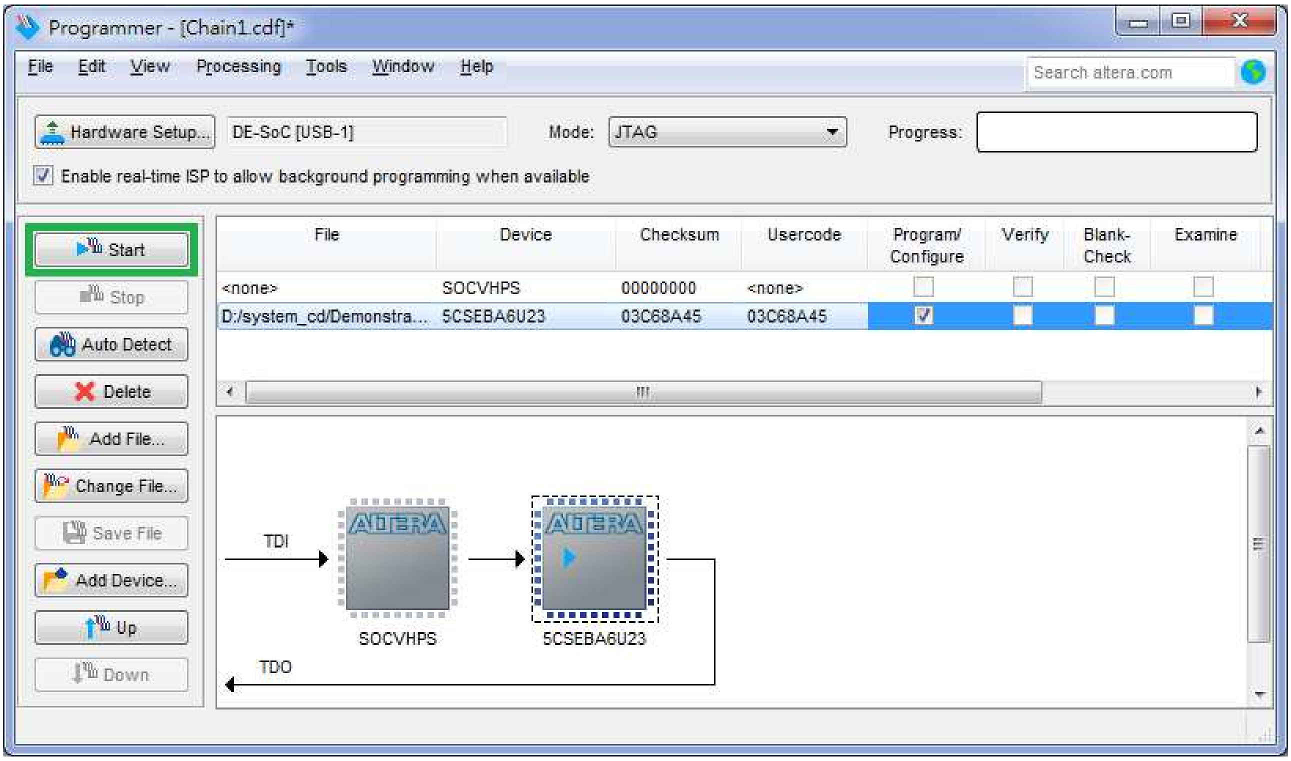


Figure 3-10 Program.sof file into the FPGA device

■ Configure the FPGA in AS Mode

- The DE10-Nano board uses a serial configuration device (EPCS128) to store configuration data for the Cyclone V SoC FPGA. This configuration data is automatically loaded from the serial configuration device chip into the FPGA when the board is powered up.
- Users need to use Serial Flash Loader (SFL) to program the serial configuration device via JTAG interface. The FPGA-based SFL is a soft intellectual property (IP) core within the FPGA that bridge the JTAG and Flash interfaces. The SFL Megafunction is available in Quartus II. **Figure 3-11** shows the programming method when adopting SFL solution.
- Please refer to Chapter 8: Steps of Programming the Serial Configuration Device for the basic programming instruction on the serial configuration device.

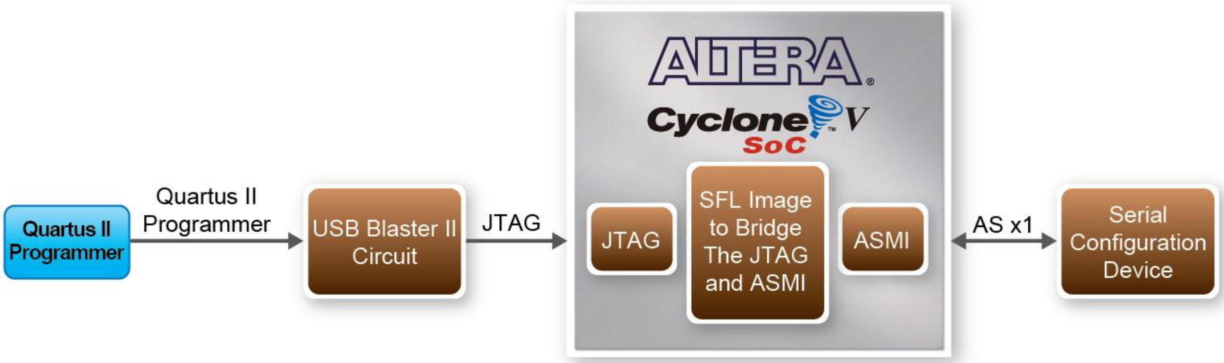


Figure 3-11 Programming a serial configuration device with SFL solution

3.3 Board Status Elements

In addition to the 9 LEDs that FPGA/HPS device can control, there are 6 indicators which can indicate the board status (See **Figure 3-12**), please refer the details in **Table 3-3**

Figure 3-12 LED Indicators on DE10-Nano

Table 3-3 LED Indicators

Board Reference	LED Name	Description
LED9	3.3-V Power	Illuminate when 3.3V power is active.
LED10	CONF_DONE	Illuminates when the FPGA is successfully configured.
LED11	JTAG_TX	Illuminate when data is transferred from JTAG to USB Host.
LED12	JTAG_RX	Illuminate when data is transferred from USB Host to JTAG.
TXD	UART TXD	Illuminate when data is transferred from FT232R to USB Host.
RXD	UART RXD	Illuminate when data is transferred from USB Host to FT232R.

3.4 Board Reset Elements

There are two HPS reset buttons on DE10-Nano, HPS (cold) reset and HPS warm reset, as shown in **Figure 3-13**. **Table 3-4** describes the purpose of these two HPS reset buttons. **Figure 3-14** is the reset tree for DE10-Nano.

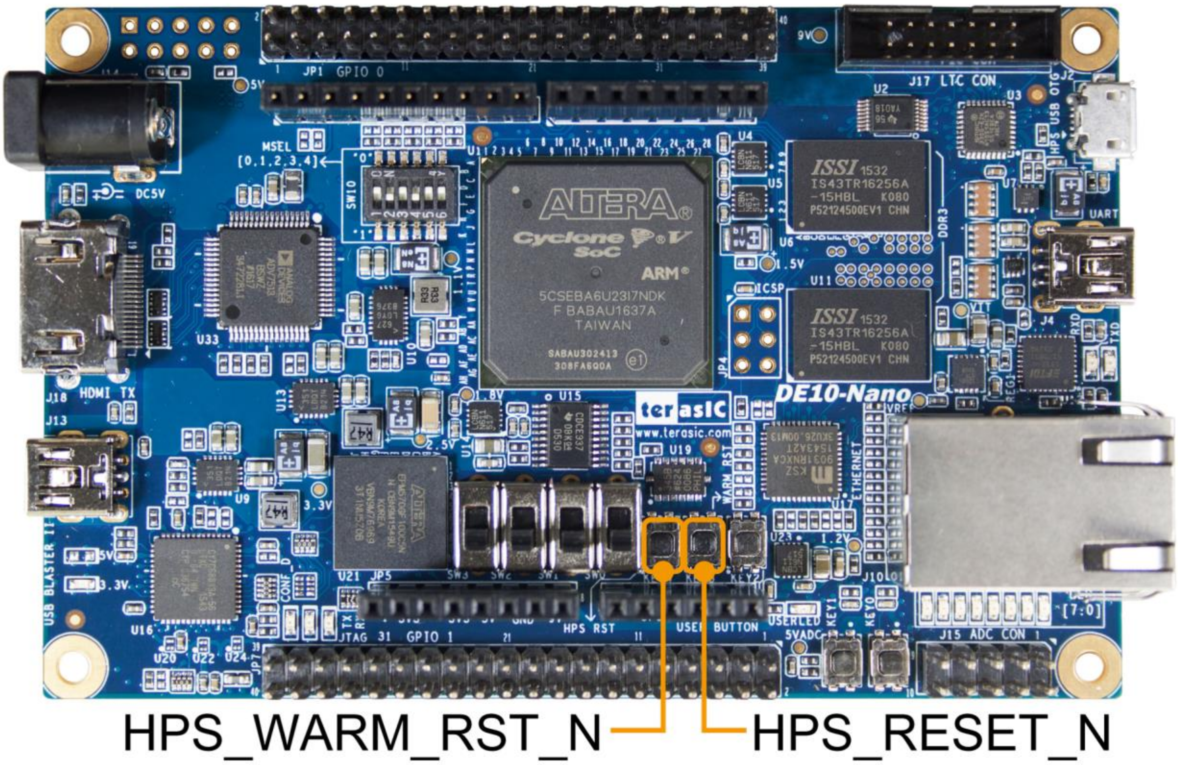


Figure 3-13 HPS cold reset and warm reset buttons on DE10-Nano

Table 3-4 Description of Two HPS Reset Buttons on DE10-Nano

Board Reference	Signal Name	Description
KEY4	HPS_RESET_N	Cold reset to the HPS, Ethernet PHY and USB host device. Active low input which resets all HPS logics that can be reset.
KEY3	HPS_WARM_RST_N	Warm reset to the HPS block. Active low input affects the system reset domain for debug purpose.

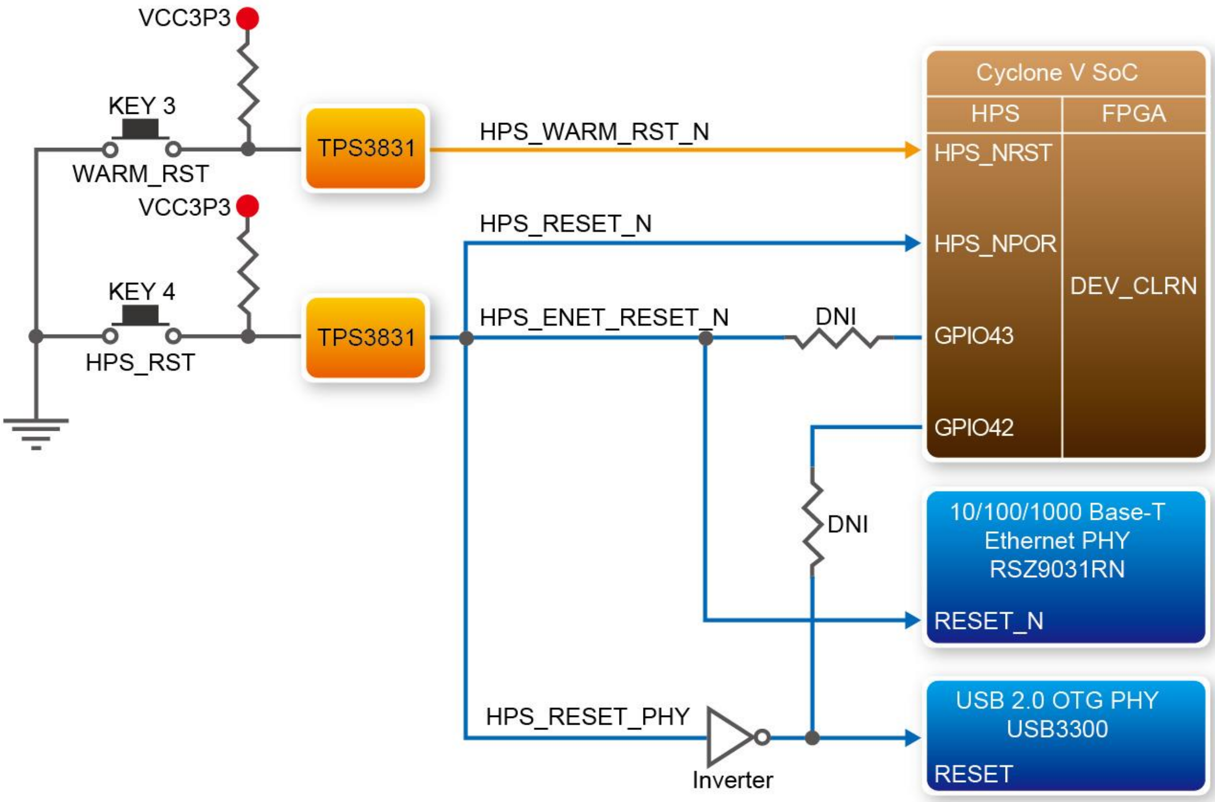


Figure 3-14 HPS reset tree on DE10-Nano board

3.5 Clock Circuitry

Figure 3-15 shows the default frequency of all external clocks to the Cyclone V SoC FPGA. A clock generator is used to distribute clock signals with low jitter. The two 50MHz clock signals connected to the FPGA are used as clock sources for user logic. Three 25MHz clock signal are connected to two HPS clock inputs, and the other one is connected to the clock input of Gigabit Ethernet Transceiver. One 24MHz clock signal is connected to the USB controller for USB Blaster II circuit and FPGA. One 24MHz clock signals are connected to the clock inputs of USB OTG PHY. The associated pin assignment for clock inputs to FPGA I/O pins is listed in **Table 3-5.**

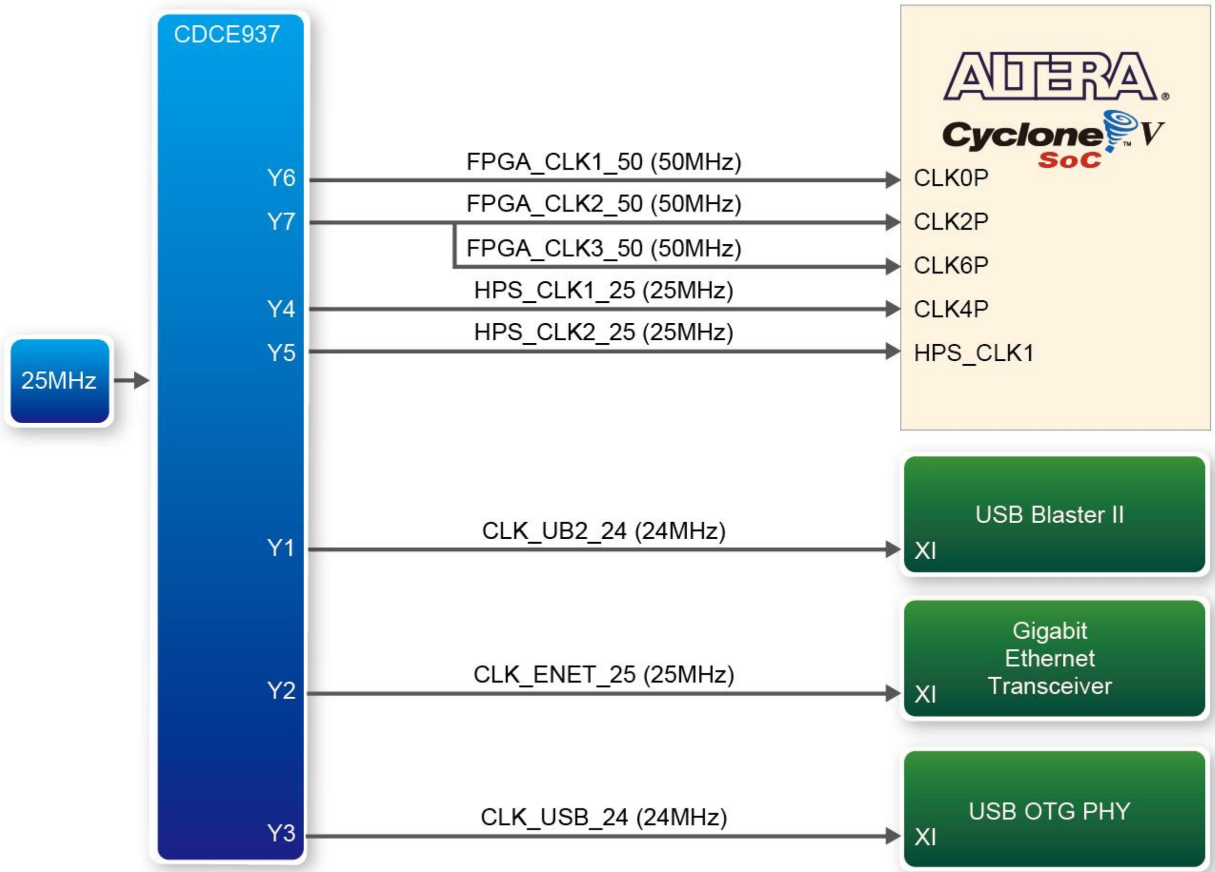


Figure 3-15 Block diagram of the clock distribution on DE10-Nano

Table 3-5 Pin Assignment of Clock Inputs

Signal Name	FPGA Pin No.	Description	I/O Standard
FPGA_CLK1_50	PIN_V11	50 MHz clock input	3.3V
FPGA_CLK2_50	PIN_Y13	50 MHz clock input	3.3V
FPGA_CLK3_50	PIN_E11	50 MHz clock input (share with FPGA_CLK1_50)	3.3V
HPS_CLK1_25	PIN_E20	25 MHz clock input	3.3V
HPS_CLK2_25	PIN_D20	25 MHz clock input	3.3V

3.6 Peripherals Connected to the FPGA

This section describes the interfaces connected to the FPGA. Users can control or monitor different interfaces with user logic from the FPGA.

3.6.1 User Push-buttons, Switches and LEDs

The board has two push-buttons connected to the FPGA, as shown in **Figure 3-16**. Schmitt trigger circuit is implemented and act as switch debounce in **Figure 3-17** for the push-buttons connected. The two push-buttons named KEY0 and KEY1 coming out of the Schmitt trigger device are connected directly to the Cyclone V SoC FPGA. The push-button generates a low logic level or high logic level when it is pressed or not, respectively. Since the push-buttons are debounced, they can be used as clock or reset inputs in a circuit.

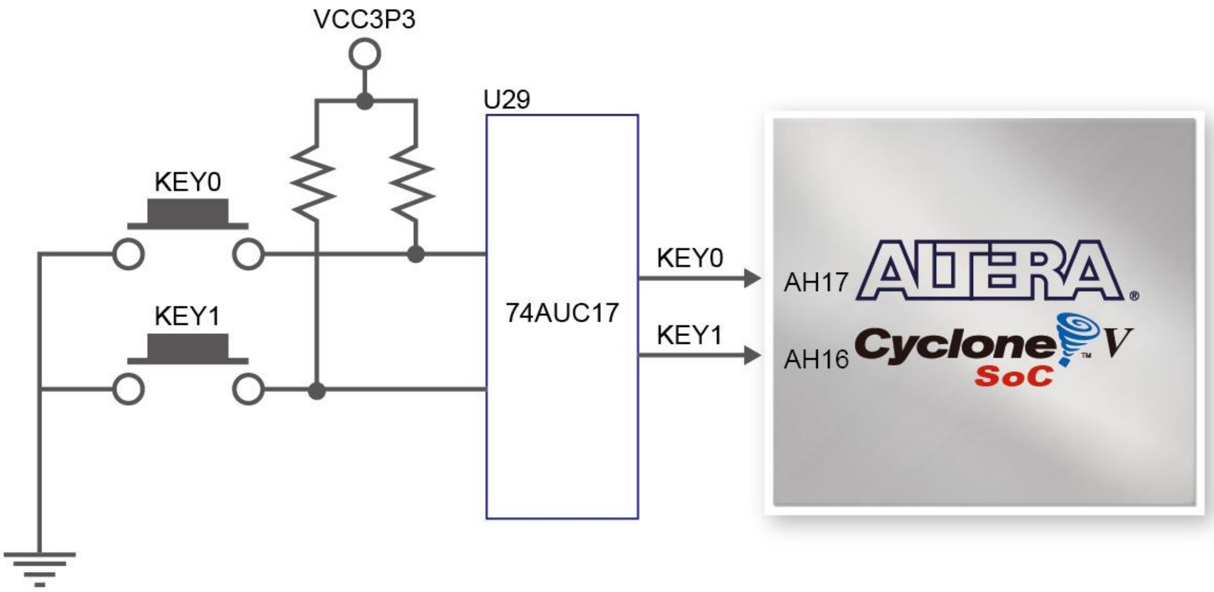


Figure 3-16 Connections between the push-buttons and the Cyclone V SoC FPGA

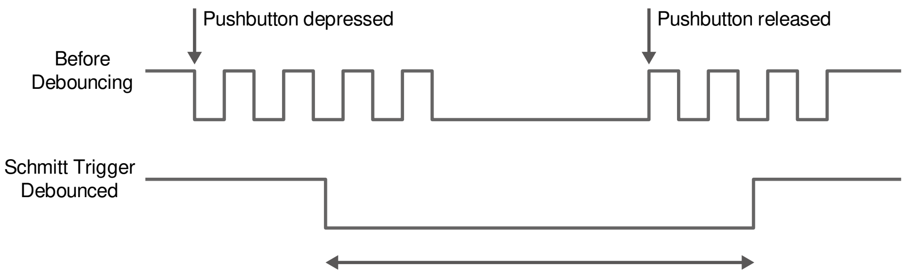


Figure 3-17 Switch debouncing