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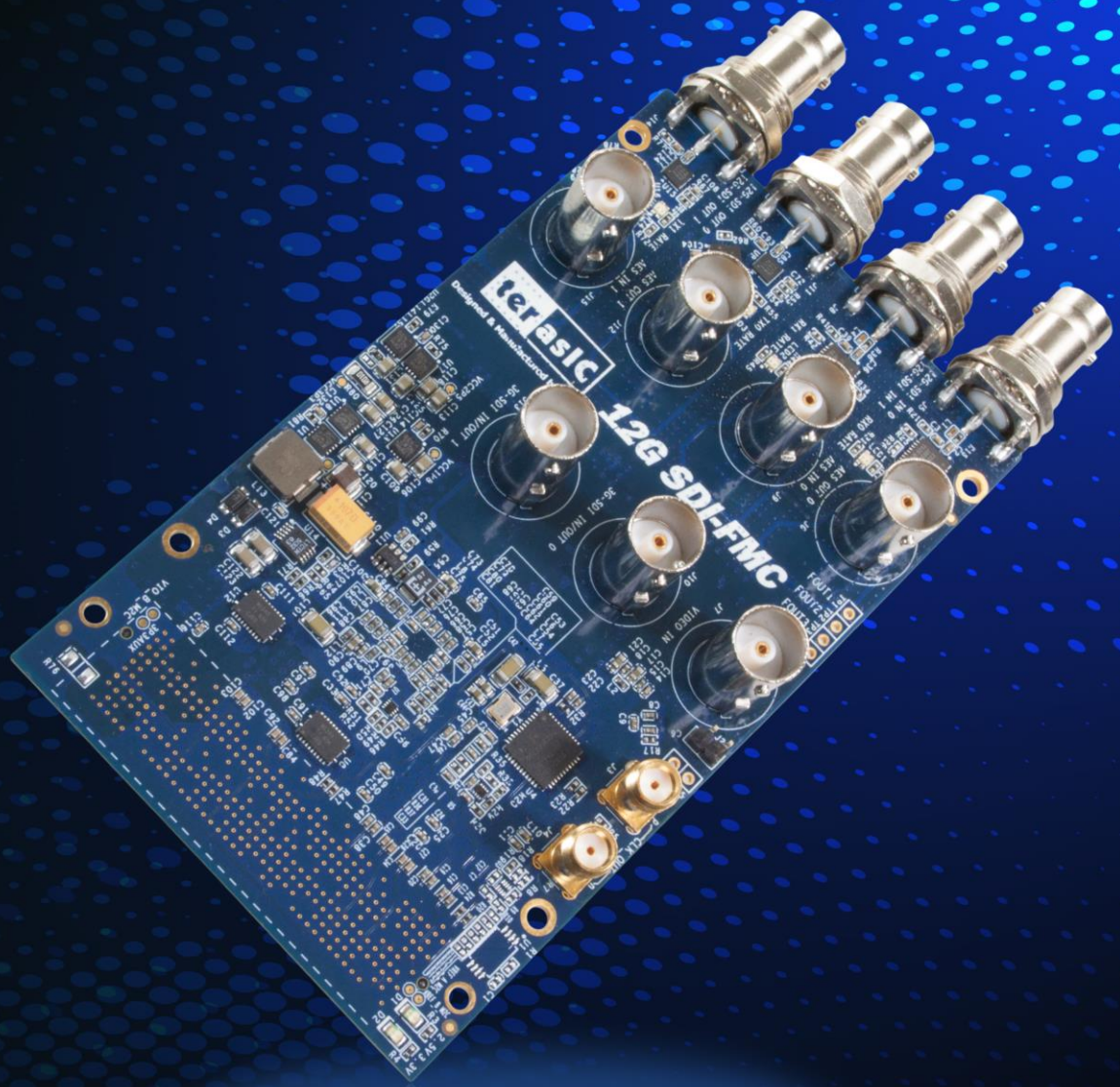
# SDI-FMC

## User Manual

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# Chapter 1

# Introduction

The Terasic SDI-FMC is a 12G SDI daughter card. It enables users to design and verify their 12G SDI product. The board includes 12G SDI, 3G SDI, AES, and Clock Generators. It uses an FMC expansion connector to interface to the FPGA boards which can support 12G SPI IP, e.g. Intel Arria 10 GX FPGA Development Kit (A10GFP) and Arria 10 SoC Development Kit (A10SoC).

## 1.1 The Package Contents

The SDI-FMC kit comes with the following items:

- SDI-FMC Daughter Card
- CD Download Guide
- Supporting Package

The system CD contains technical documents of the SDI-FMC kit, which include component datasheets, demonstrations, schematic and user manual. Users can download the CD from the link below:

http://sdi-fmc.terasic.com/cd

**Figure 1-1** shows the contents of the SDI-FMC kit.

**Figure 1-1 Contents of the SDI-FMC Kit**

## 1.2 Assemble SDI-FMC with FPGA Mainboard

In order to make the SDI-FMC daughter card and the FMC connector on the FMC card with more secure hookup, the FMC side of the SDI-FMC daughter card has reserved two screw holes, as shown in Figure 1-2. Users can use the screws, copper pillars, and nuts that come with the SDI-FMC, to secure the SDI-FMC on the FPGA mainboard, as shown in Figure 1-3. In order to use the 12G SDI high-speed transmission in normal operation, we strongly recommend that users use the screws to secure the connection between the mainboard and the SDI-FMC card.

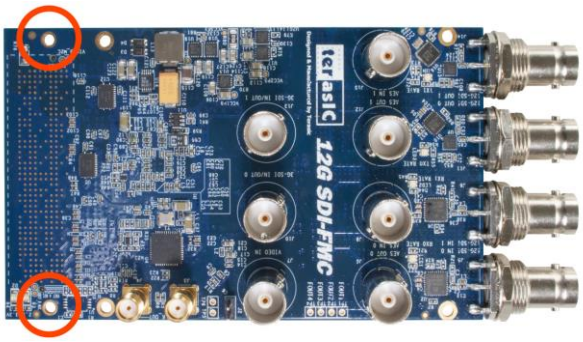


Figure 1-2 Two screw holes on the FMC side of the SDI-FMC

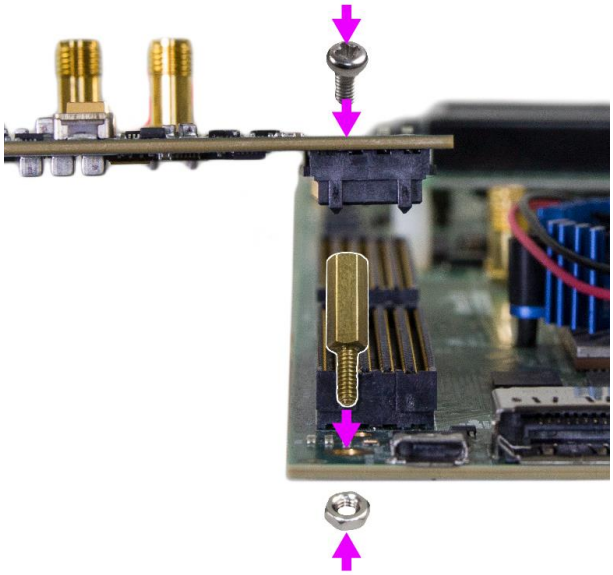

Figure 1-3 Use the screws, copper pillars, and nuts to secure the connection between the SDI-FMC and the FPGA mainboard

In addition to the screws, the SDI-FMC Kit also provides copper pillars and silicon brackets. Users can reference Figure1-4 for installation of the brackets for the SDI-FMC. Note: The height of these brackets is designed specifically for the Intel A10SoC and A10GFP. These brackets may not be suitable for other FPGA mainboards.

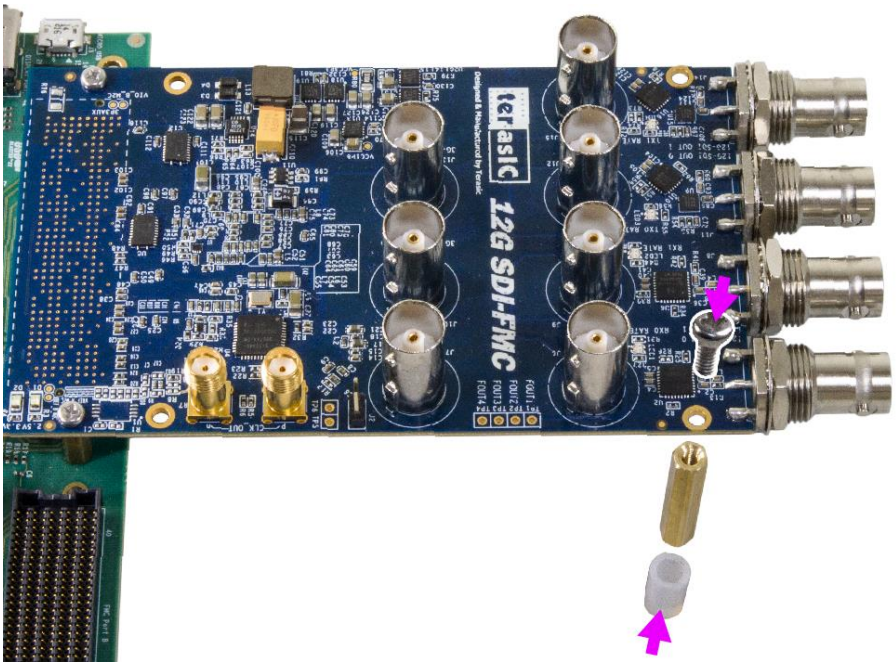


**Figure 1-4 Installation of the SDI-FMC brackets**

Figure 1-5 shows the completion of the connection assembly on the SDI-FMC and A10SoC

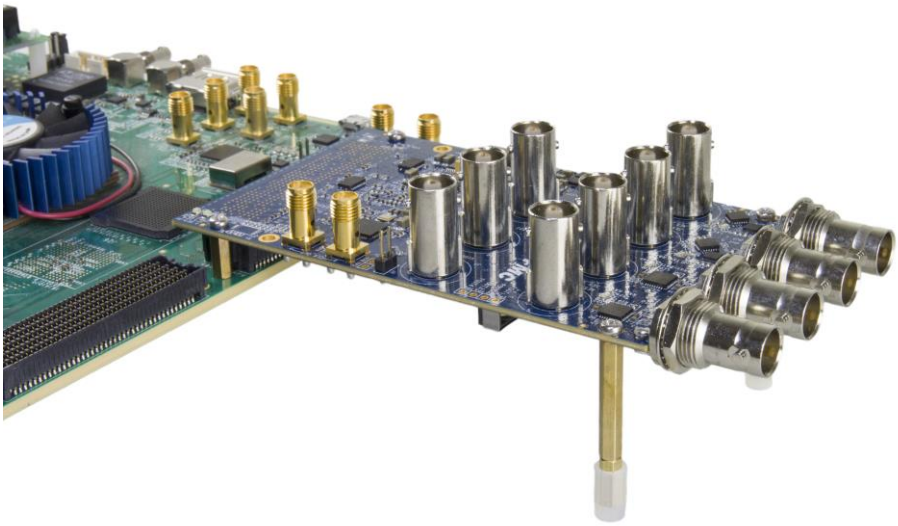

**Figure 1-5 SDI-FMC Assembled with A10SoC**

## 1.3 Connectivity

Figure 1-6 and Figure 1-7 below show the connectivity of the SDI-FMC to the A10SoC and A10GFP FPGA boards. The SDI-FMC is powered from FPGA mainboard. It is not necessary to connect a power adapter to the SDI-FMC.

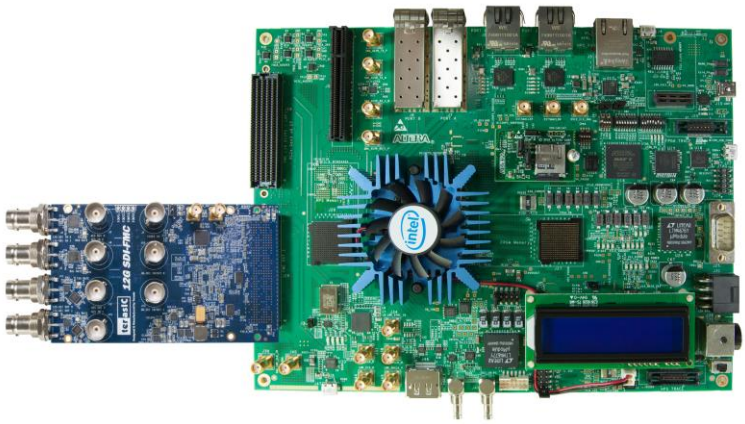

**Figure 1-6 SDI-FMC with A10SoC**

**Figure 1-7 SDI-FMC with A10GFP**

## 1.4 Getting Help

For Technical Support, Terasic's Contact Information is listed below:

- Office Hours: 9:00 a.m. to 6:00 p.m. (GMT +8)
- Telephone: +886-3-575-0880
- Email: support@terasic.com

# Chapter 2

# Architecture of SDI-FMC

This chapter lists the features and describes the architecture of SDI-FMC daughter card.

## 2.1 Features

The key features of this module are listed below:

- Two 12G SDI inputs and outputs (Connected to 4 75 Ohm BNC connector)
- Two 3G SDI inputs or outputs (Connected to 2 75 Ohm BNC connector)
- Two AES inputs and outputs (Connected to 2 75 Ohm BNC connector)
- Clock Generator
- FMC interface

## 2.2 Layout and Block Diagram

### Component and Layout

The top view of the SDI-FMC is shown in **Figure 2-1**.

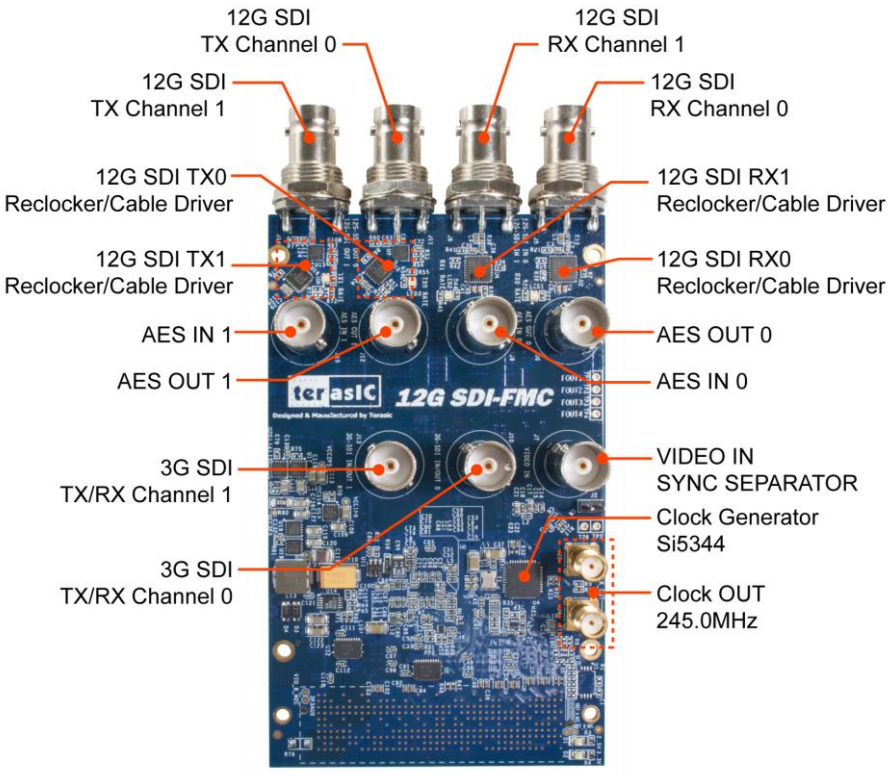


**Figure 2-1 Top view of the SDI-FMC Daughter Card**

The bottom view of the SDI-FMC is shown in Figure 2-2. It depicts the layout and indicates the locations of connectors and key components.

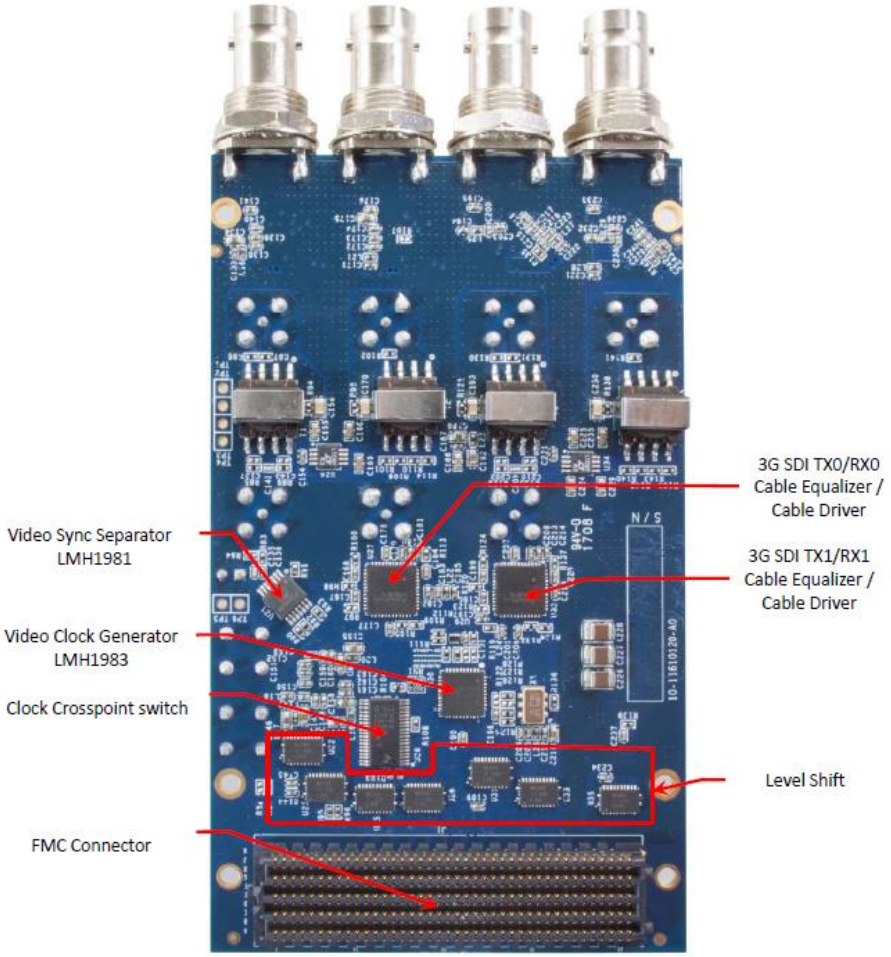


**Figure 2-2 Bottom view of the SDI-FMC Daughter Card**

## Block Diagram

Figure 2-3, Figure 2-4 and Figure 2-5 show the block diagrams of the SDI-FMC. The diagrams contain SDI, AES and clock generators three parts. Figure 2-3 shows the SDI function. There are two independent 12G SDI channels in the boards. Each channel contains one transmitter port and one receiving port connected to the BNC connectors. The six 12G SDI chips can be configured through the SPI chain. There are also two independent 3G SDI channels in the boards. Each channel can be configured as either input channel or output channel. The 3G SDI is connected to the BNC connectors. The 3G SDI chips can be configured through their SPI interface.

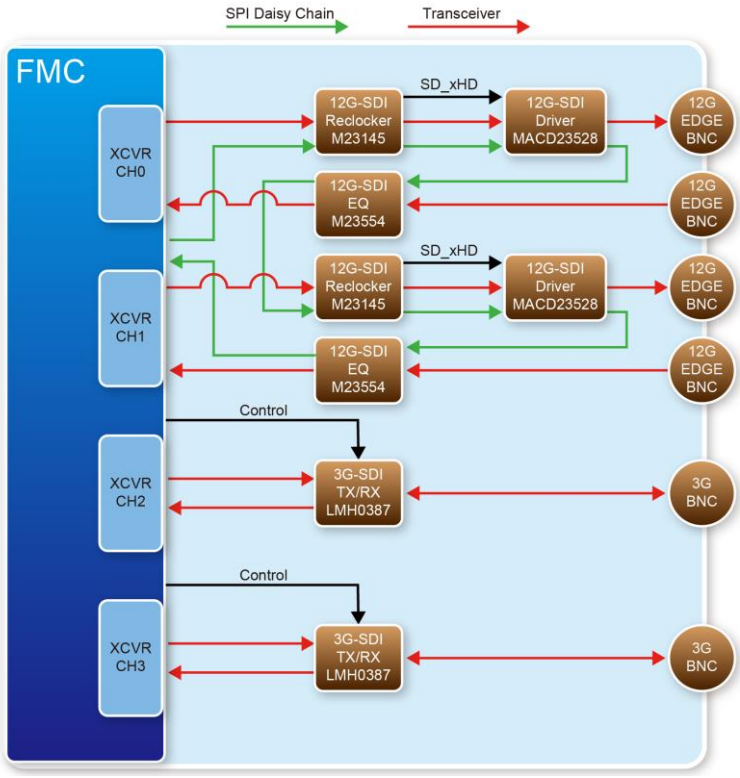


**Figure 2-3 SDI Function in the Block Diagram**

Figure 2-3Figure 2-4 shows the AES audio function. There are two independent AES channels in the boards. Each channel contains one transmitter port and one receiving port connected to the BNC connectors.

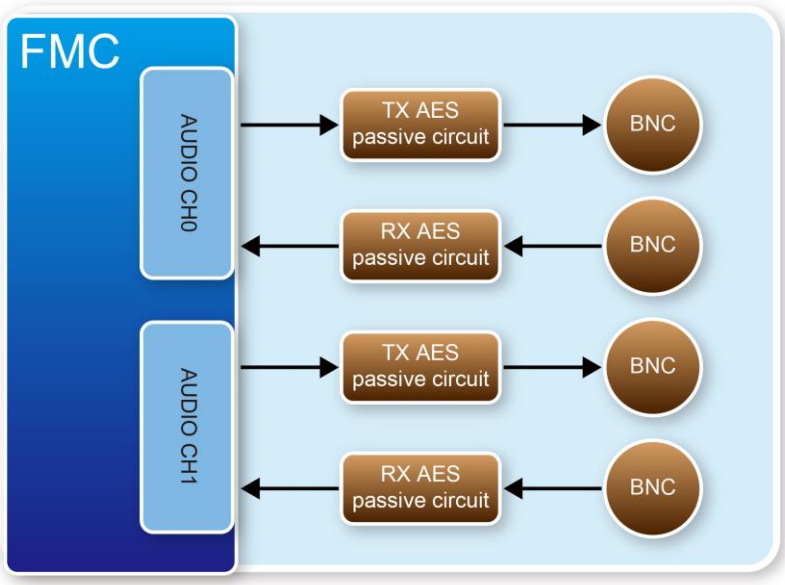

**Figure 2-4 AES Function in the Block diagram**

Figure 2-5 shows the clock functions. The Si5340, LMH1981 and LMH1983 can provide required clock sources for SDI application.

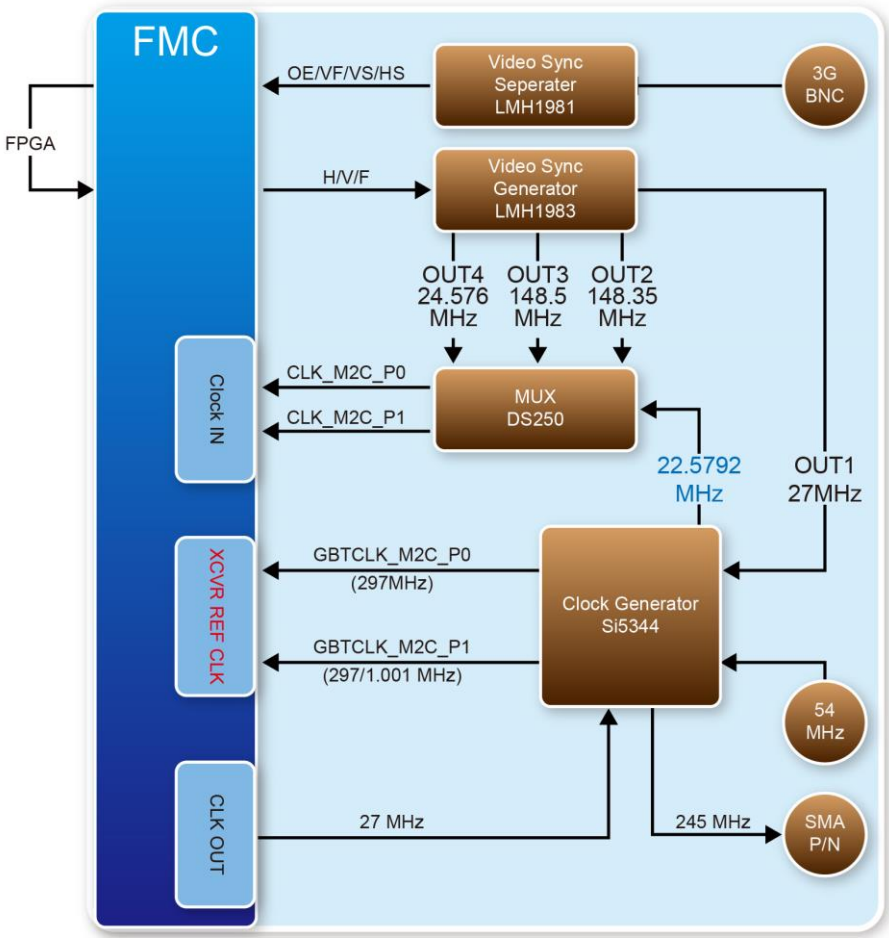


**Figure 2-5 Clock Functions in the Block diagram**

# Chapter 3

# Using the SDI-FMC

This chapter provides information on how to control the hardware of the SDI-FMC. It includes the definition of the FMC interface and how to use the 12G SDI, 3G SDI, AES and clock generator hardware in the board.

## 3.1 Pin Definition of FMC Connector

The FMC connector on the SDI-FMC daughter card connects directly to the FMC connector on the FPGA board. **Figure 3-1**, **Figure 3-2** and **Figure 3-3** illustrates the signal names of the FMC connector.

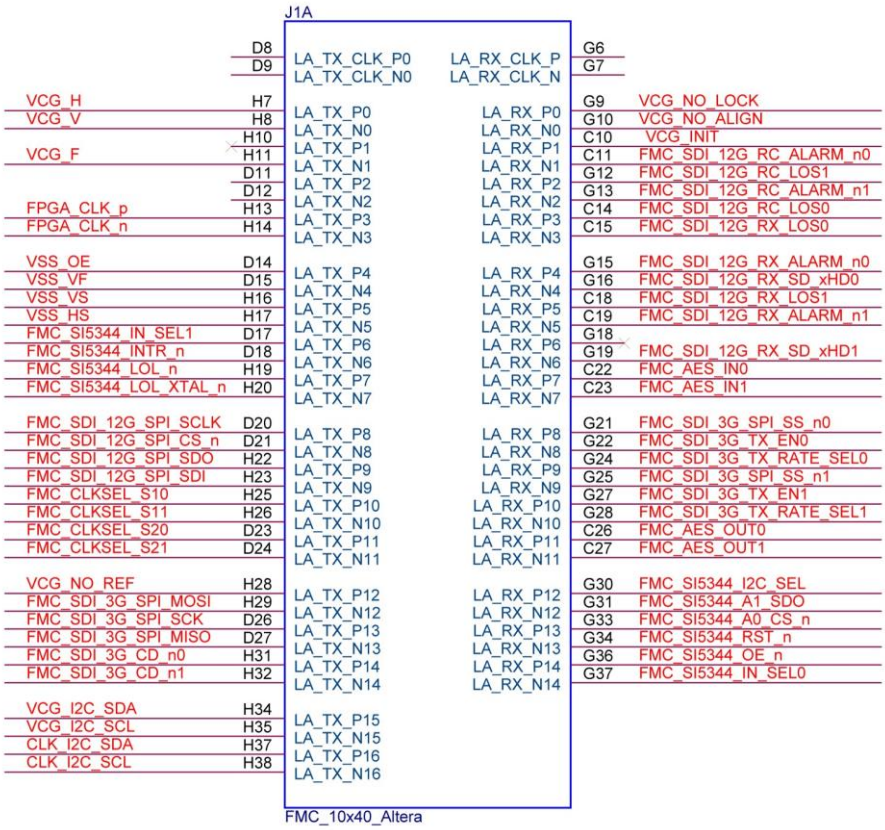


**Figure 3-1 Signal names of FMC connector part 1**

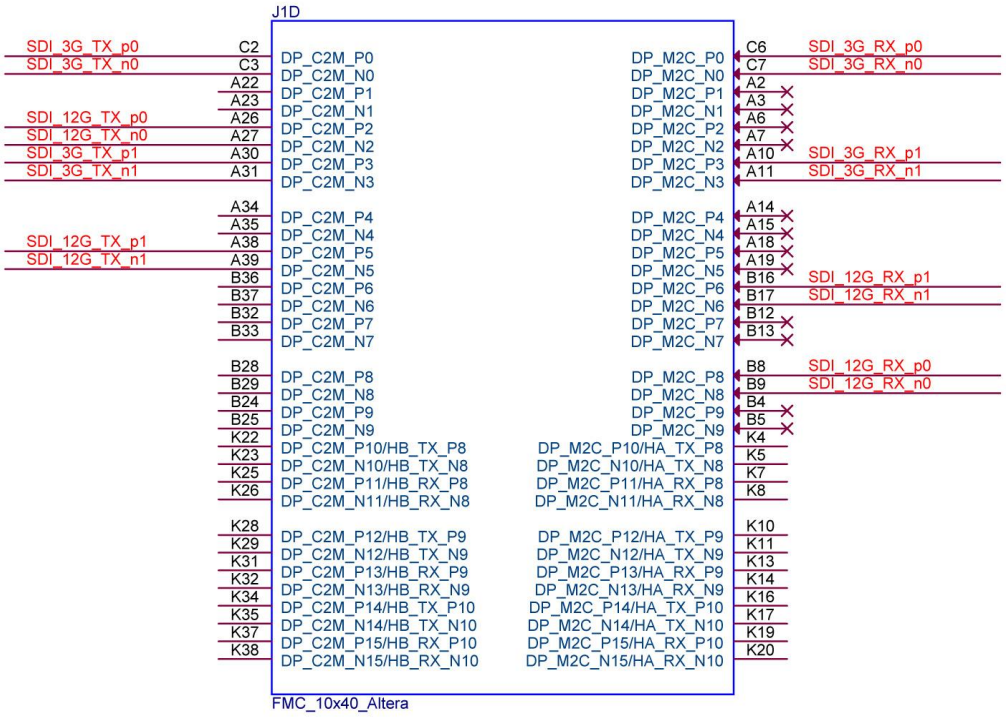


**Figure 3-2 Signal names of FMC connector part 2**

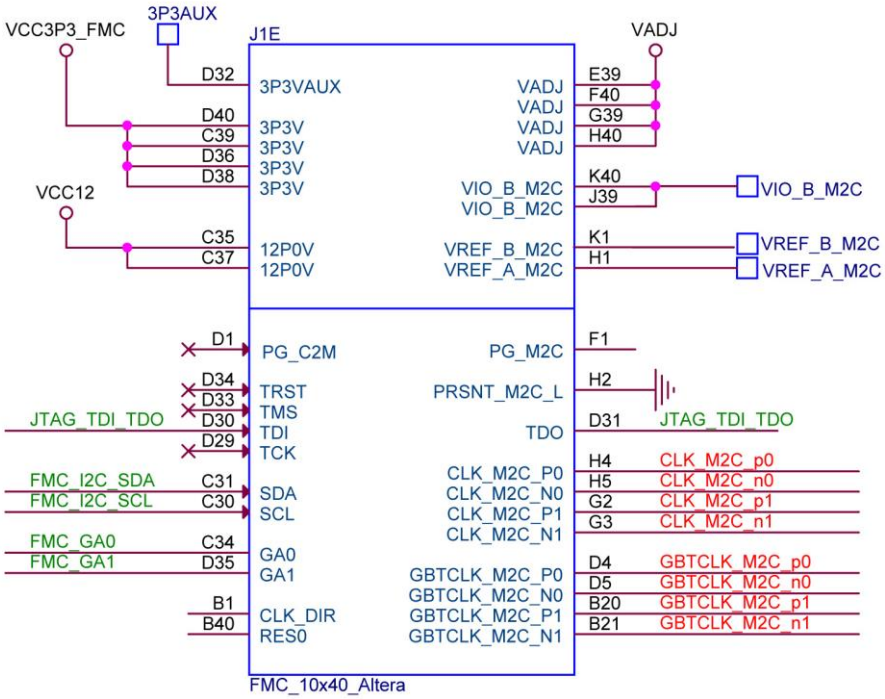


**Figure 3-3 Signal names of FMC connector part 3**

Table 3-1 shows the SDI-FMC pin assignments for the SDI-FMC pins in Quartus Prime.

**Table 3-1 SDI-FMC Pin Assignments of FMC in Quartus Prime**

| *Signal Name* | *FMC Pin No.* | *Description* | *Direction* | *IO Standard* |
|---|---|---|---|---|
| VCG_H | H7 | LMH1983 Horizontal sync reference signal | Output | VCCADJ |
| VCG_V | H8 | LMH1983 Vertical sync reference signal | Output | VCCADJ |
| VCG_F | H11 | LMH1983 Field sync (odd/even) reference signal | Output | VCCADJ |
| VCG_INIT | C10 | LMH1983 Reset signal for audio-video phase alignment (rising edge triggered) | Output | VCCADJ |
| VCG_NO_LOCK | G9 | LMH1983 Loss of lock status flag for PLLs 1-4 (active high) | Input | VCCADJ |
| VCG_NO_ALIGN | G10 | LMH1983 Loss of alignment status flag for OUTs 1–4 (active high) | Input | VCCADJ |
| VCG_NO_REF | H28 | Loss of reference status flag (active high) | Input | VCCADJ |
| VCG_I2C_SDA | H34 | LMH1983 I2C Data signal | Input/ Output | VCCADJ |
| VCG_I2C_SCL | H35 | LMH1983 I2C Clock signal | Output | VCCADJ |
| VSS_HS | H17 | LMH1981 Horizontal Sync Output | Input | VCCADJ |
| VSS_VS | H16 | LMH1981 Vertical Sync Output | Input | VCCADJ |
| VSS_VF | D15 | LMH1981 Video Format Output | Input | VCCADJ |
| VSS_OE | D14 | LMH1981 Odd/Even Field Output | Input | VCCADJ |
| FMC_CLKSEL_S10 | H25 | Select Reference Clock 0 input source, bit 0 | Output | VCCADJ |
| FMC_CLKSEL_S11 | H26 | Select Reference Clock 0 input source, bit 1 | Output | VCCADJ |
| FMC_CLKSEL_S20 | D23 | Select Reference Clock 1 input source, bit 0 | Output | VCCADJ |
| FMC_CLKSEL_S21 | D24 | Select Reference Clock 1 input source, bit 1 | Output | VCCADJ |
| CLK_I2C_SDA | H37 | Serial Data Signal | Input/ Output | VCCADJ |
| CLK_I2C_SCL | H38 | Serial Clock Signal | Output | VCCADJ |
| FMC_SI5344_I2C_SEL | G30 | Serial interface select, | Output | VCCADJ |

| | | | | |
|---|---|---|---|---|
| | | FMC_SI5344_I2C_SEL = 0 is SPI Mode.<br>FMC_SI5344_I2C_SEL = 1 is I2C mode.<br>Please setting high for I2C Interface. | | |
| FMC_SI5344_A1_SDO | G31 | I2C Interface Address Select 1 | Input/ Output | VCCADJ |
| FMC_SI5344_A0_CS_n | G33 | I2C Interface Address Select 0 | Output | VCCADJ |
| FMC_SI5344_RST_n | G34 | Si5344 Device Reset.<br>Active low input that performs power-on reset (POR) of the device.<br>Clock outputs are disabled during reset. | Output | VCCADJ |
| FMC_SI5344_OE_n | G36 | Si5344 Device Output Enable.<br>Disables all outputs when held high. | Output | VCCADJ |
| FMC_SI5344_IN_SEL0 | G37 | Input Reference Select, bit0. | Output | VCCADJ |
| FMC_SI5344_IN_SEL1 | D17 | Input Reference Select, bit1. | Output | VCCADJ |
| FMC_SI5344_INTR_n | D18 | Interrupt output.<br>This pin is asserted low when a change in device status has occurred. | Input | VCCADJ |
| FMC_SI5344_LOL_n | H19 | Loss Of Lock<br>This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). | Input | VCCADJ |
| FMC_SI5344_LOL_XTAL_n | H20 | Loss Of Signal on XA/XB Pins.<br>This pin indicates a loss of signal at the XA/XB pins when low. | Input | VCCADJ |
| FMC_SDI_12G_SPI_SCLK | D20 | SDI 12G SPI interface, Slave clock input signal. | Output | VCCADJ |
| FMC_SDI_12G_SPI_CS_n | D21 | SDI 12G SPI interface, Chip select signal, Low active. | Output | VCCADJ |
| FMC_SDI_12G_SPI_SDI | H23 | SDI 12G SPI interface, | Output | VCCADJ |

| | | | | |
|---|---|---|---|---|
| | | Slave data input signal | | |
| FMC_SDI_12G_SPI_SDO | H22 | SDI 12G SPI interface, Slave data output signal | Input | VCCADJ |
| FMC_SDI_12G_RX_LOS0 | C15 | SDI 12G RX 0 LOS signal,<br>Signal Detect Complement<br>H: No input signal is present or the cable length is above the MUTEREF threshold<br>L: Input signal is present and cable length is below the MUTEREF threshold | Input | VCCADJ |
| FMC_SDI_12G_RX_ALARM_n0 | G15 | SDI 12G RX 0 ALARM signal,<br>Active low (open drain)<br>H: Normal operation<br>L: Alarm asserted | Input | VCCADJ |
| FMC_SDI_12G_RX_SD_xHD0 | G16 | SDI 12G RX 0 SD Data Rate<br>H: SD data rate detected<br>L: HD/3G/6G/12G data rate detected | Input | VCCADJ |
| FMC_SDI_12G_RX_LOS1 | C18 | SDI 12G RX 1 LOS signal,<br>Signal Detect Complement<br>H: No input signal is present or the cable length is above the MUTEREF threshold<br>L: Input signal is present and cable length is below the MUTEREF threshold | Input | VCCADJ |
| FMC_SDI_12G_RX_ALARM_n1 | C19 | SDI 12G RX 0 ALARM signal,<br>Active low (open drain)<br>H: Normal operation<br>L: Alarm asserted | Input | VCCADJ |
| FMC_SDI_12G_RX_SD_xHD1 | G19 | SDI 12G RX 1 SD Data Rate<br>H: SD data rate | Input | VCCADJ |

| | | | | |
|---|---|---|---|---|
| | | detected<br>L: HD/3G/6G/12G data rate detected | | |
| FMC_SDI_12G_RC_LOS0 | C14 | SDI 12G TX 0 Reclocker LOS signal, Signal Detect Complement<br>H: No input signal is present or the cable length is above the MUTEREF threshold<br>L: Input signal is present and cable length is below the MUTEREF threshold | Input | VCCADJ |
| FMC_SDI_12G_RC_ALARM_n0 | C11 | SDI 12G TX 0 Reclocker ALARM signal,<br>Active low (open drain)<br>H: Normal operation<br>L: Alarm asserted | Input | VCCADJ |
| FMC_SDI_12G_RC_LOS1 | C12 | SDI 12G TX 1 Reclocker LOS signal, Signal Detect Complement<br>H: No input signal is present or the cable length is above the MUTEREF threshold<br>L: Input signal is present and cable length is below the MUTEREF threshold | Input | VCCADJ |
| FMC_SDI_12G_RC_ALARM_n1 | C13 | SDI 12G TX 1 Reclocker ALARM signal,<br>Active low (open drain)<br>H: Normal operation<br>L: Alarm asserted | Input | VCCADJ |
| FMC_SDI_3G_SPI_MISO | D27 | SDI 3G SPI Interface Data.<br>Master Input, Slave Output. | Input | VCCADJ |
| FMC_SDI_3G_SPI_MOSI | H29 | SDI 3G SPI Interface Data.<br>Master Output, Slave Input. | Output | VCCADJ |

| | | | | |
|---|---|---|---|---|
| FMC_SDI_3G_SPI_SCK | D26 | SDI 3G SPI Interface, Serial clock. | Output | VCCADJ |
| FMC_SDI_3G_SPI_SS_n0 | G21 | SDI 3G SPI Interface, Slave Select for device 0. Low active. | Output | VCCADJ |
| FMC_SDI_3G_SPI_SS_n1 | G25 | SDI 3G SPI Interface, Slave Select for device 1. Low active. | Output | VCCADJ |
| FMC_SDI_3G_CD_n0 | H31 | SDI 3G Channel 0 Carrier detect,<br>H = No input signal detected.<br>L = Input signal detected. | Input | VCCADJ |
| FMC_SDI_3G_CD_n1 | H32 | SDI 3G Channel 1 Carrier detect,<br>H = No input signal detected.<br>L = Input signal detected. | Input | VCCADJ |
| FMC_SDI_3G_TX_EN0 | G22 | SDI 3G Channel 0 Transmitter output driver enable. Internal pullup.<br>H = output driver is enabled.<br>L = output driver is powered off. | Output | VCCADJ |
| FMC_SDI_3G_TX_EN1 | G27 | SDI 3G Channel 1 Transmitter output driver enable. Internal pullup.<br>H = output driver is enabled.<br>L = output driver is powered off. | Output | VCCADJ |
| FMC_SDI_3G_TX_RATE_SEL0 | G24 | SDI 3G Channel 0 output slew rate control. Internal pulldown.<br>H = Output rise/fall time complies with SMPTE 259M (SD).<br>L = Output rise/fall time complies with SMPTE 424M / 292M (3G/HD). | Output | VCCADJ |
| FMC_SDI_3G_TX_RATE_SEL1 | G28 | SDI 3G Channel 1 output slew rate control. | Output | VCCADJ |

| | | | | |
|---|---|---|---|---|
| | | Internal pulldown.<br>H = Output rise/fall time complies with SMPTE 259M (SD).<br>L = Output rise/fall time complies with SMPTE 424M / 292M (3G/HD). | | |
| FPGA_CLK_p | H13 | For Si5344 input reference clock 1. | Output | VCCADJ |
| FPGA_CLK_n | H14 | For Si5344 input reference clock 1. | Output | VCCADJ |
| FMC_AES_IN0 | C22 | AES Channel 0 input. | Input | VCCADJ |
| FMC_AES_IN1 | C23 | AES Channel 1 input. | Input | VCCADJ |
| FMC_AES_OUT0 | C26 | AES Channel 0 output. | Output | VCCADJ |
| FMC_AES_OUT1 | C27 | AES Channel 0 output. | Output | VCCADJ |
| CLK_M2C_p0 | H4 | Reference Clock 0 for FPGA. | Input | VCCADJ |
| CLK_M2C_n0 | H5 | Reference Clock 0 for FPGA. | Input | VCCADJ |
| CLK_M2C_p1 | G2 | Reference Clock 1 for FPGA. | Input | VCCADJ |
| CLK_M2C_n1 | G3 | Reference Clock 1 for FPGA. | Input | VCCADJ |
| GBTCLK_M2C_p0 | D4 | Transceiver Reference clock 0, 297MHz input. | Input | VCCADJ |
| GBTCLK_M2C_n0 | D5 | Transceiver Reference clock 0, 297MHz input. | Input | VCCADJ |
| GBTCLK_M2C_p1 | B20 | Transceiver Reference clock 0, 297.0/1.001MHz input. | Input | VCCADJ |
| GBTCLK_M2C_n1 | B21 | Transceiver Reference clock 0, 297.0/1.001MHz input. | Input | VCCADJ |
| SDI_12G_TX_p0 | A26 | SDI 12G Transmitter Channel 0 | Output | VCCADJ |
| SDI_12G_TX_n0 | A27 | SDI 12G Transmitter Channel 0 | Output | VCCADJ |
| SDI_12G_TX_p1 | A38 | SDI 12G Transmitter Channel 1 | Output | VCCADJ |
| SDI_12G_TX_n1 | A39 | SDI 12G Transmitter Channel 1 | Output | VCCADJ |
| SDI_12G_RX_p0 | B8 | SDI 12G Receiver Channel 0 | Input | VCCADJ |
| SDI_12G_RX_n0 | B9 | SDI 12G Receiver Channel 0 | Input | VCCADJ |

| | | | | |
|---|---|---|---|---|
| SDI_12G_RX_p1 | B16 | SDI 12G Receiver Channel 1 | Input | VCCADJ |
| SDI_12G_RX_n1 | B17 | SDI 12G Receiver Channel 1 | Input | VCCADJ |
| SDI_3G_TX_p0 | C2 | SDI 3G Transmitter Channel 0 | Output | VCCADJ |
| SDI_3G_TX_n0 | C3 | SDI 3G Transmitter Channel 0 | Output | VCCADJ |
| SDI_3G_TX_p1 | A30 | SDI 3G Transmitter Channel 1 | Output | VCCADJ |
| SDI_3G_TX_n1 | A31 | SDI 3G Transmitter Channel 1 | Output | VCCADJ |
| SDI_3G_RX_p0 | C6 | SDI 3G Receiver Channel 0 | Input | VCCADJ |
| SDI_3G_RX_n0 | C7 | SDI 3G Receiver Channel 0 | Input | VCCADJ |
| SDI_3G_RX_p1 | A10 | SDI 3G Receiver Channel 1 | Input | VCCADJ |
| SDI_3G_RX_n1 | A11 | SDI 3G Receiver Channel 1 | Input | VCCADJ |

## 3.2 Using the 12G SDI

Figure 3-4 shows the system block diagram of the 12G SDI. The M23145 Reclocker chips and MACD23528 Cable Driver chips are used to transmit the 12G SDI signal and the M23554 Cable Equalizer chips are used to receive the 12G SDI signal. The M23145 and M23554 are directly connected to the FPGA transceiver pins. The BNC connecters are used as an interface to connect the external 12G SDI signals. Besides the 12G SDI signal, these chips also support the 6G/3G/HD/SD SDI signals.

The six 12G-SDI chips are connected through an SPI daisy chain (seeing green line in Figure 3-4). Developers can communicate with these chips through the SPI interface. Due to the NDA limitation (for detail information about how to control the 12G SDI chips) please contact the chip vender **MACOM** Company.

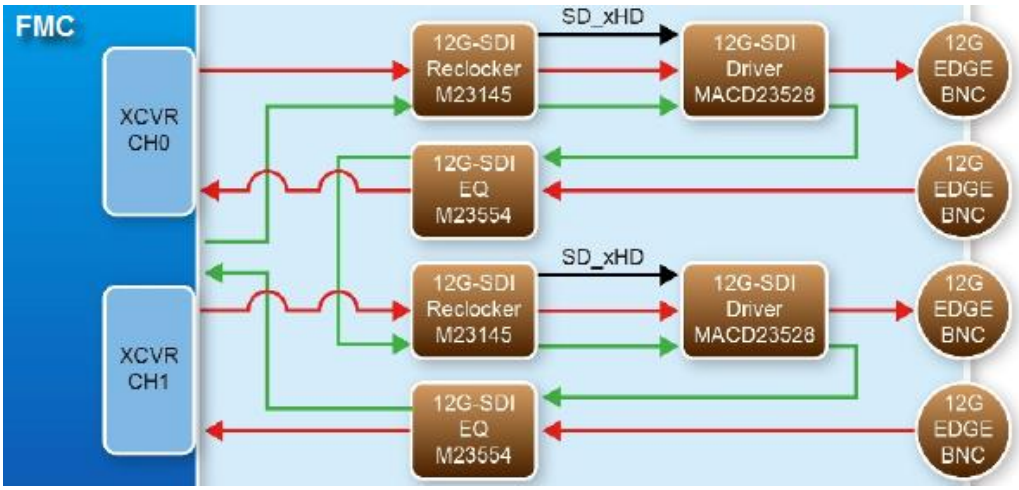


**Figure 3-4 12G SDI System Block Diagram**

## 3.3 Using the 3G SDI

Figure 3-5 shows the system block diagram of the 3G SDI. The LMH0387 chips are used to either transmit or receive a 3G SDI signal. The LMH0387 is directly connected to the FPGA transceiver pins. The BNC connecters are used as an interface to connect external 3G SDI signals. The LMH0387 chips can be configured either in the input mode as an equalizer to receiver data over coaxial cable, or in the output mode as a cable driver to transmit data over coaxial cable. Developers can configure the chips through the chips' SPI interface. For detailed information about how to control the SDI chips, please refer to the chips' datasheet included in the SDI-FMC CD-ROM.

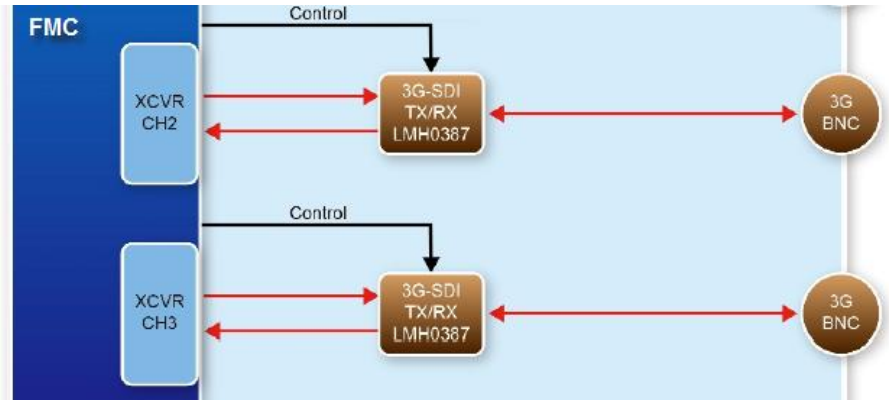


**Figure 3-5 3G SDI System Blok Diagram**

## 3.4 Using the AES

Figure 3-6 shows the system block diagram of the AES. There are two AES channels on the SDI-FMC Board. Each contains one TX channel and one RX Channel.

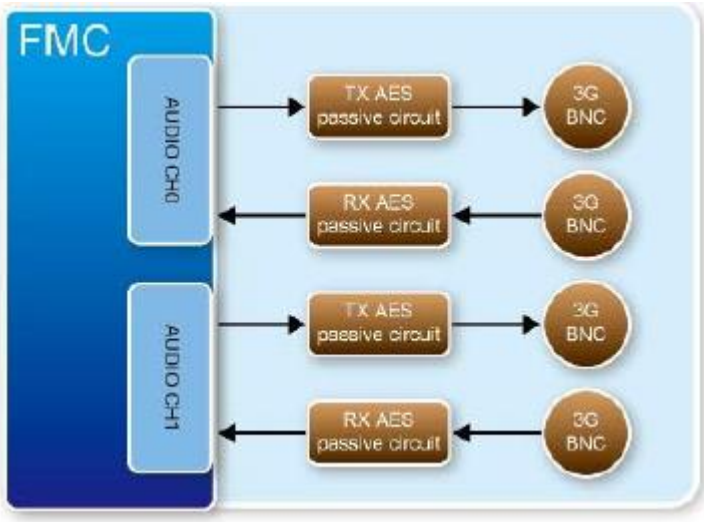


**Figure 3-6 AES System Blok Diagram**

The AES3 RX channel delivers a 75-Ω load termination with a return loss of 25 dB or more. The signal is inputted through a 75-Ω BNC and terminated with a 75-Ω resistor to ground. The unbalanced signal is then balanced through an isolation transformer. The differential signal output from the transformer is biased and input to a RS422 transceiver. The output of the RS422 transceiver is a single-ended LVCMOS signal which is driven to the host board through the HSMC connector.

Figure 3-7 shows the AES3 RX Channel block diagram.

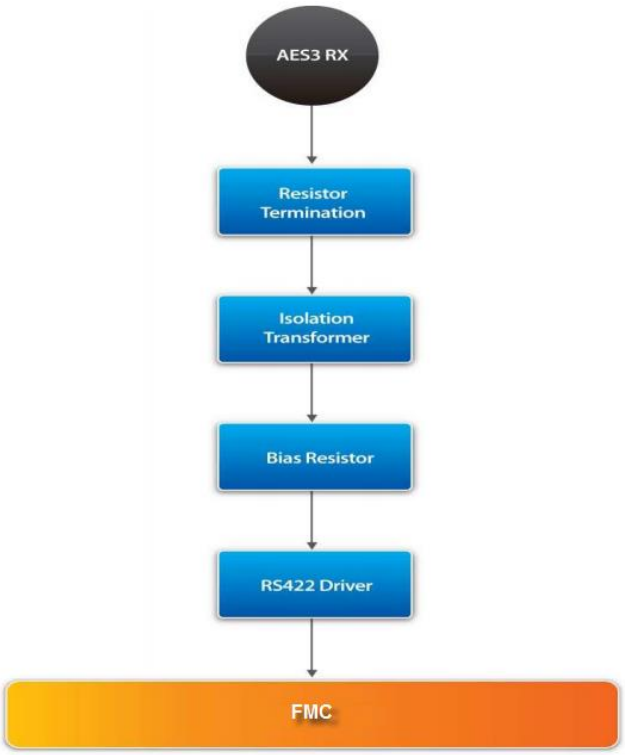


**Figure 3-7 AES RX Channel Block Diagram**

The AES3 TX channel is designed to have a balanced signal driver next to or on the isolation transformer. The output of the RS422 transceiver has an RX network to limit the output slew rate, thus limiting the bandwidth of AES3 output. The AES3 channel is designed to support 192-kHz to 24-kHz sample rates. The output is unbalanced with a source impedance of 75 Ω and a return loss of 25 dB or more. The peak-to-peak output voltage is 1.0V centered around the ground the transmitter.

Figure 3-8 shows the AES3 TX Channel block diagram.

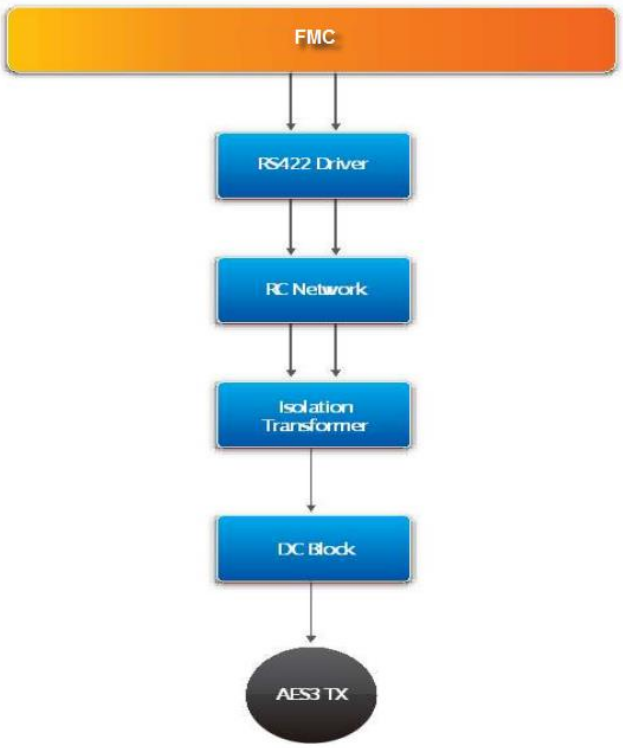


**Figure 3-8 AES TX Channel Block Diagram**

## 3.5 Using the Clock Generators

Figure 3-9 shows the block diagram of clock generators on the SDI-FMC. The SI5344 is designed to generate 270.0 and 270.0/1.001 clocks for the transceiver based SDI IP in FPGA. The LMH1983 provides 27MHz as a reference clock for Si5344 chip. In the demonstration project, Terasic provides the Si5344 and LMH1983 configure IP so developers can easily configure these clock generator chips to generate the required clock frequency/ies.