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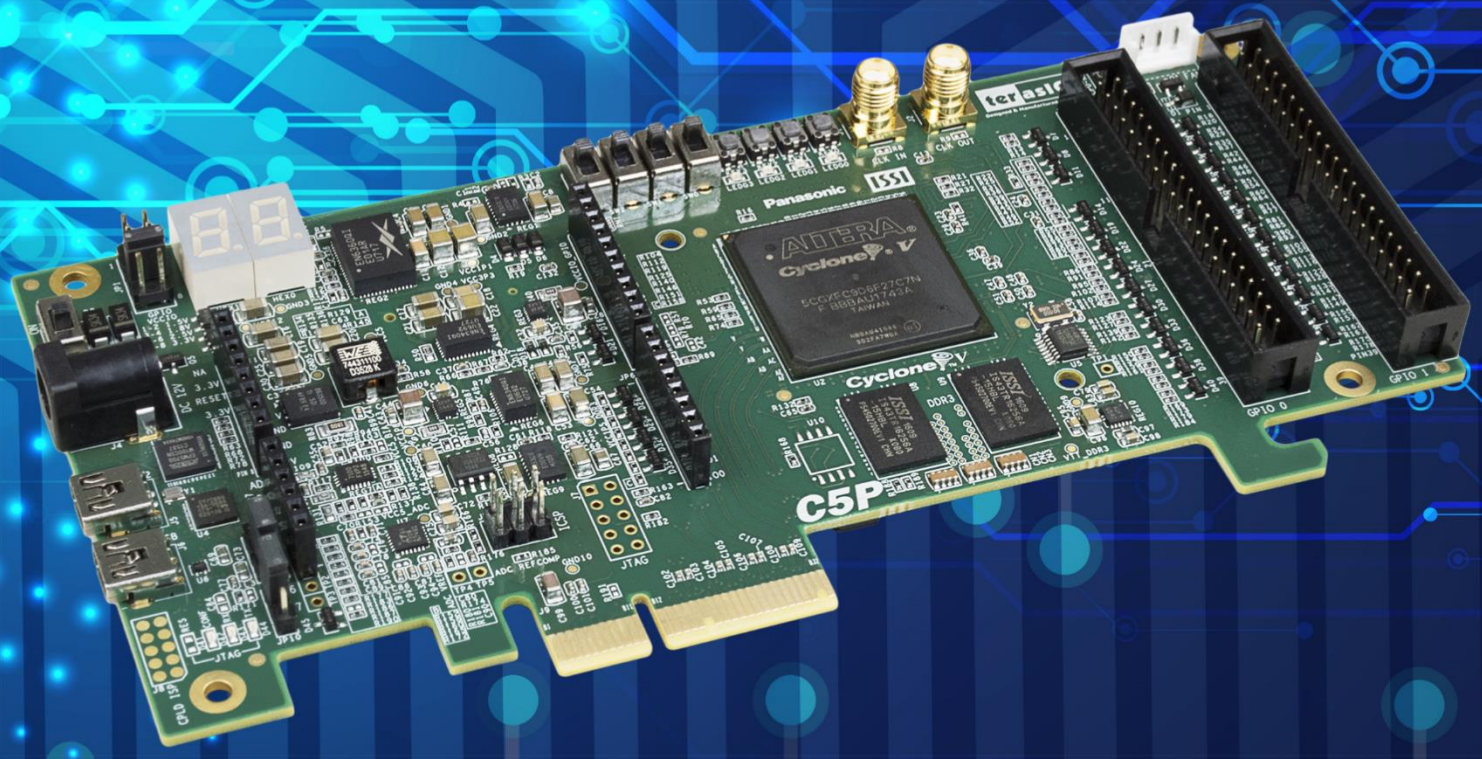
C5P

User Manual



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Contents

Chapter 1

C5P Development Kit

The C5P Development Kit presents a robust hardware design platform built around the Intel Cyclone V FPGA, it also provides a powerful platform of reconfigurable power with high performance and low power processing system. The C5P Development Kit is equipped with PCIe Gen1x4, high-speed DDR3 memory, GPIO, Arduino and much more that promises many exciting applications.

The C5P Development Board is equipped with PCIe Gen1X4 interface, it is low development cost, and can support users who develop mainstream applications and OpenCL applications based on PCIe, as well as a wide range of high-speed connectivity applications.

The C5P Development Board contains all the tools needed to use the board in conjunction with a computer that runs the Microsoft Windows 7 or later.

1.1 Package Contents

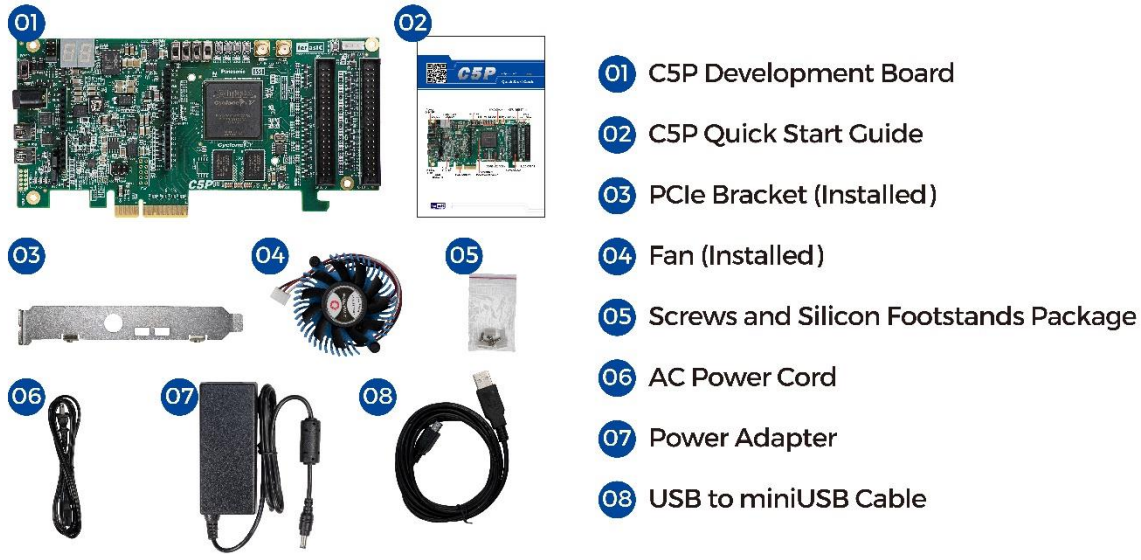

Figure 1-1 C5P package contents

■ C5P package includes

1. C5P Development Board
2. C5P Quick Start Guide
3. PCIe Bracket (Installed)
4. Fan (Installed)
5. Screw and Silicon Footstands Package
6. AC Power Cord
7. Power Adapter
8. USB to mini-USB Cable

1.2 C5P System CD

The C5P System CD contains all the documents and supporting materials associated with C5P, including the user manual, system builder, reference designs, and device datasheets. Users can download this system CD from the link c5p.terasic.com.

1.3 Getting Help

Here are the addresses where you can get help if you encounter any problems:

- Terasic Inc.
- 9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan
- Email：support@terasic.com.cn
- Tel.：+886-3-575-0880
- Website：c5p.terasic.com

Chapter 2

Introduction of the C5P board

This chapter provides an introduction to the features and design characteristics of the C5P board.

2.1 Layout and Components

Figure 2-1 and **Figure 2-2** shows a photograph of the board. It depicts the layout of the board and indicates the location of the connectors and key components.

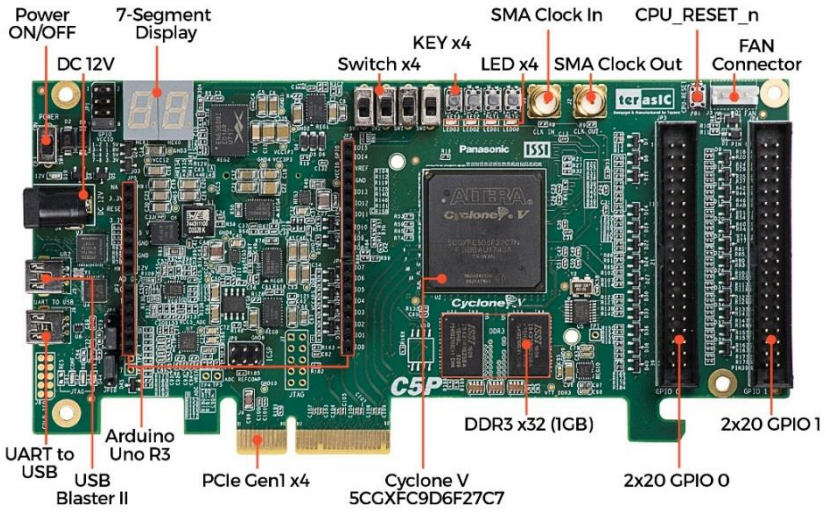

Figure 2-1 C5P development board (top view)

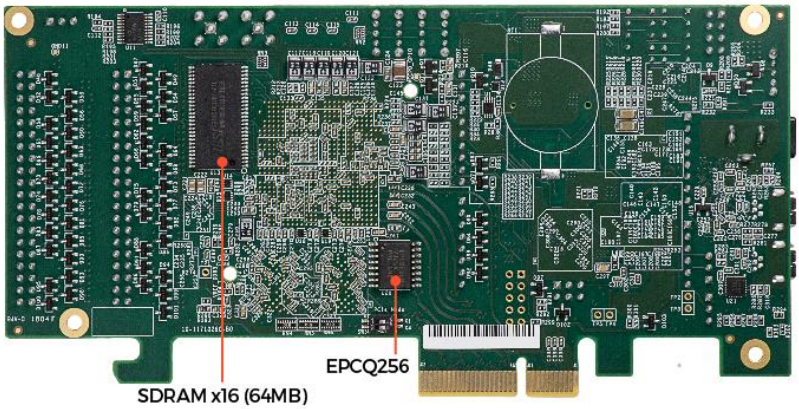

Figure 2-2 C5P development board (bottom view)

The C5P board has many features that allow users to implement a wide range of designed circuits, from simple circuits to various multimedia projects:

- Intel FPGA Cyclone® V GX 5CGXFC9D6F27C7N device
- Serial configuration device– EPCQ256
- USB-Blaster II onboard for programming; JTAG Mode
- UART to USB (USB Mini-B connector)
- PCIe Gen1x4
- 1GB DDR3 SDRAM (32-bit data bus)
- 64MB SDRAM (16-bit data bus)
- 4 push-buttons
- 4 slide switches
- 4 green LED
- Two 7-segment displays
- Four 50MHz clock sources from the clock generator
- One Arduino header
- Two 40 pin GPIO header

2.2 Block Diagram of the C5P Board

Figure 2-3 is the block diagram of the board. All the connections are established through the Cyclone V FPGA device to provide maximum flexibility for users. Users can configure the FPGA to implement any system design.

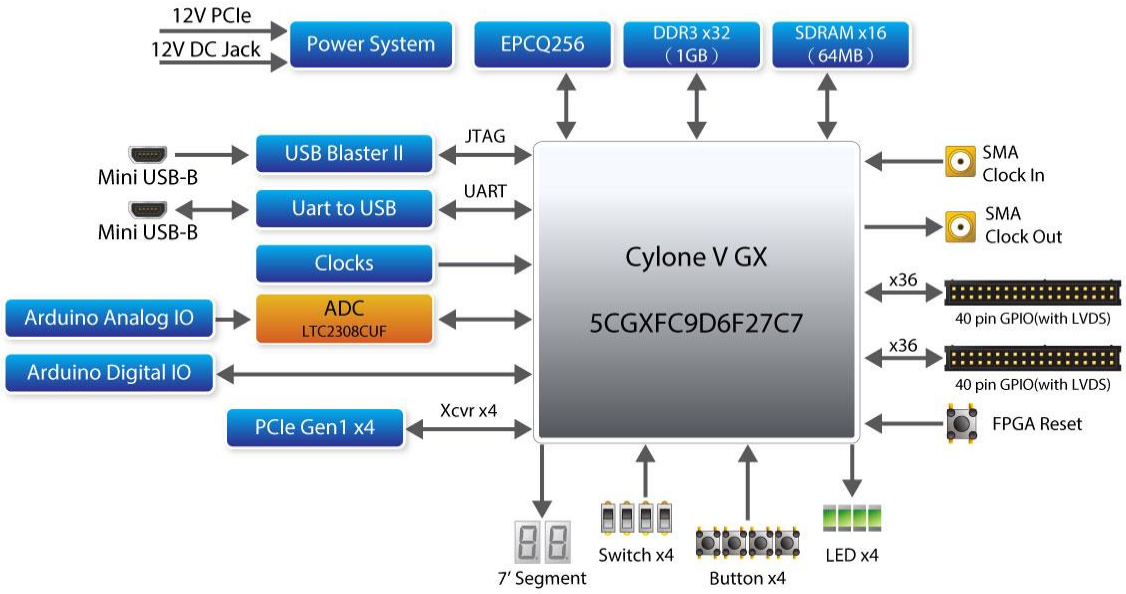

Figure 2-3 Block diagram of C5P board

Detailed information about **Figure 2-3** are listed below.

FPGA Device

- Cyclone V 5CGXFC9D6F27C7N device
  - 301K programmable logic elements
  - 13,917 Kbit/s embedded memory
  - 8 fractional PLLs
  - 2 hard memory controllers
  - Nine 3.125G Transceivers

Configuration and Debug

- Quad Serial Configuration device – EPCQ256
- Onboard USB-Blaster II (Mini-B USB connector)

Memory Device

- 64MB (32Mx16) SDRAM
- 1GB (2x256Mx16) DDR3 SDRAM

Communication

- UART to USB（USB Mini-B connector）
- PCIe Gen1x4

Connectors

- Two 40 Pin GPIO header，features of each GPIO connector
  - 36 General GPIO Pins
  - Support to configureas 8 LVDS TX and LVDS RX
  - With diode protection
  - Configurable I/O standards (voltage levels: 3.3/2.5/1.8/1.5V)
- One Arduino Uno Revision 3 header
  - Analog ADC
    - Interface: SPI
    - Fast through put rate：500Ksps
    - Channel number: 8
    - Resolution: 12-bit
    - Analog input range：0 ~ 4.096 V
  - Digital IO
    - With diode protection

- SMA IN/OUT 3.3V Single-end input and output

Switches/ Buttons/ Indicators

- 5 user Keys (4 general keys, 1 CPU_RESET_n)
- 4 user switches
- 4 LED
- Two 7-segment displays

Power

- 12V DC Input
- PCIe 12V Input

Cooling System

- 12V Fan with 5000 Rotational Speed

Chapter 3

Using the C5P Board

This chapter provides how to instructions to use the board and describes the peripherals.

3.1 Configuring the Cyclone V FPGA

There are two types of programming method supported by C5P:

1. JTAG programming：It is named after the IEEE standards Joint Test Action Group. The configuration bitstream is downloaded directly into the Cyclone V FPGA. The FPGA will retain its current status as long as power is applied to the board; the configuration information will be lost when the power is off.
2. AS programming：The other programming method is Active Serial configuration. The configuration bitstream is downloaded into the Intel FPGA EPCQ256 device, which provides non-volatile storage for the bit stream. The information is retained within EPCQ256 even if the C5P board is turned off. When the board is powered on, the configuration data in the EPCQ256 device is automatically loaded into the Cyclone V FPGA.

■ JTAG Chain on C5P Board

The FPGA device can be configured through JTAG interface on the C5P board, but the JTAG chain must form a closed loop, which allows a Quartus II programmer to the detect FPGA device.

Figure 3-1 illustrates the JTAG chain on C5P board.

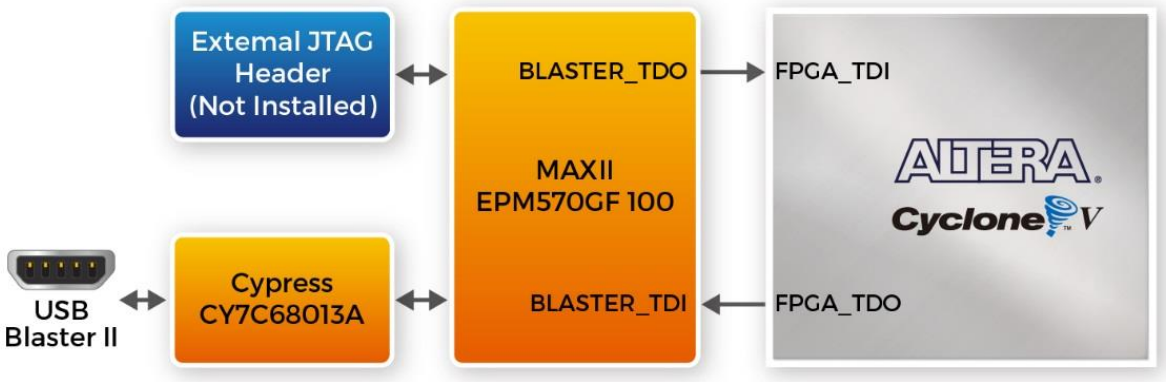

Figure 3-1 Path of the JTAG chain

■ Configure the FPGA in JTAG Mode

There is one FPGA device on the JTAG chain. The following shows how the FPGA is programmed in JTAG mode step by step.

1. Open the Quartus II programmer under Quartus Prime Tools and click “Auto Detect”, as circled in **Figure 3-2**.

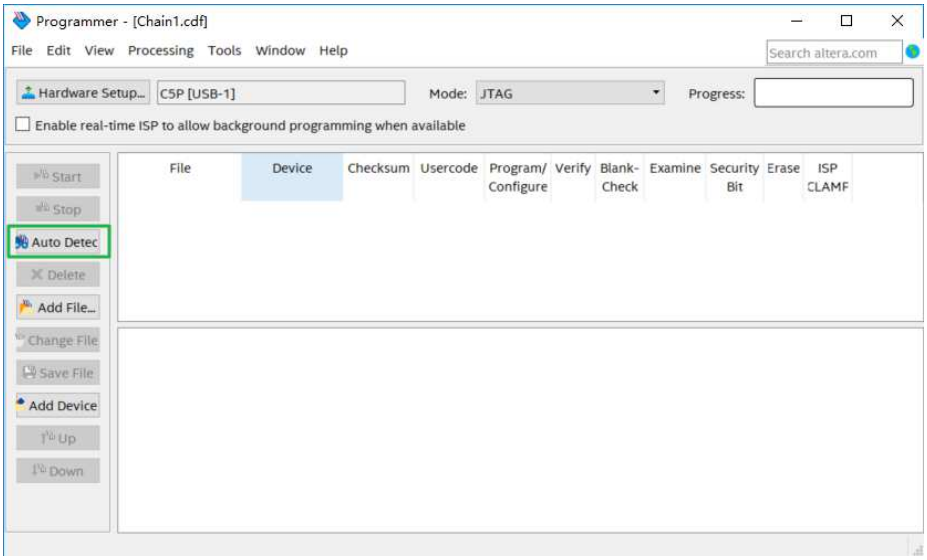

Figure 3-2 Detect FPGA device in JTAG mode

2. Select detected device associated with the board, as circled in **Figure 3-3**.

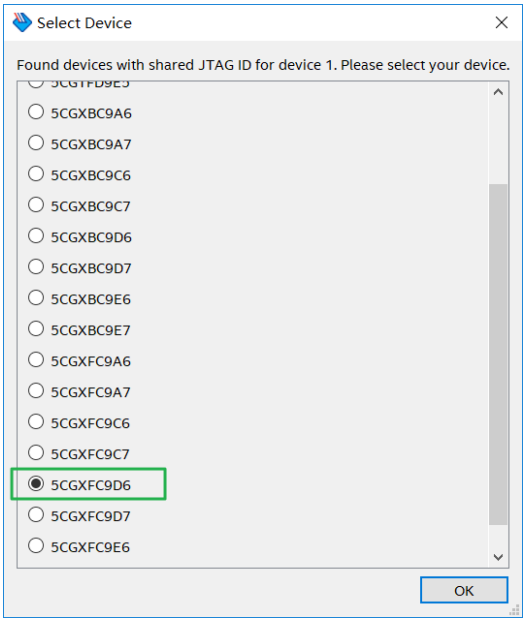

Figure 3-3 Select 5CGXFC9D6

3. The FPGA is detected, as shown in **Figure 3-4**.

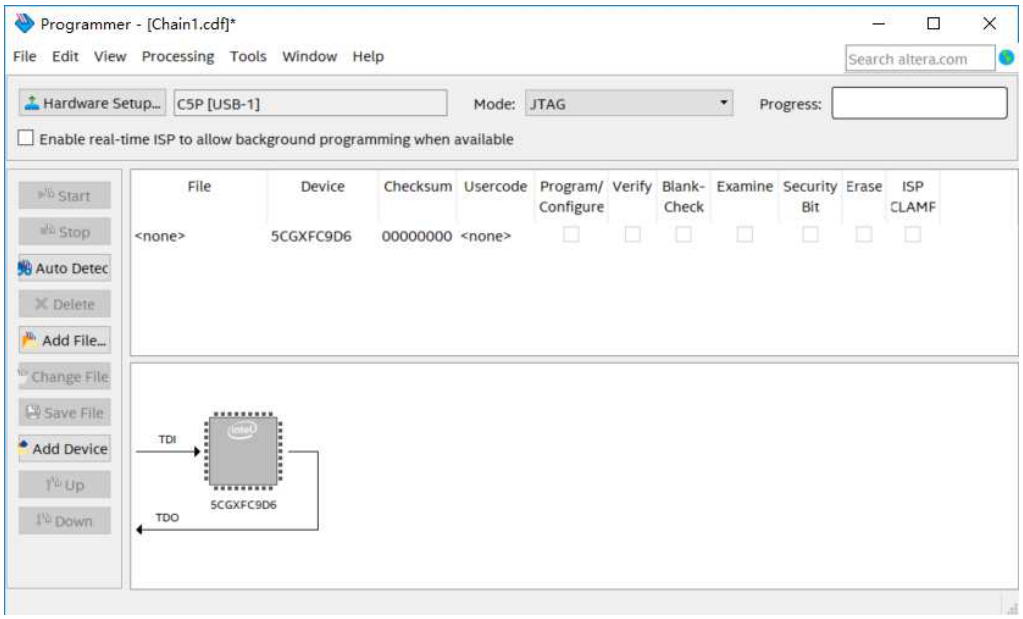

Figure 3-4 FPGA detected in Quartus programmer

4. Right click on the FPGA device and select Change File to open the .sof file to be programmed, as highlighted in **Figure 3-5**.

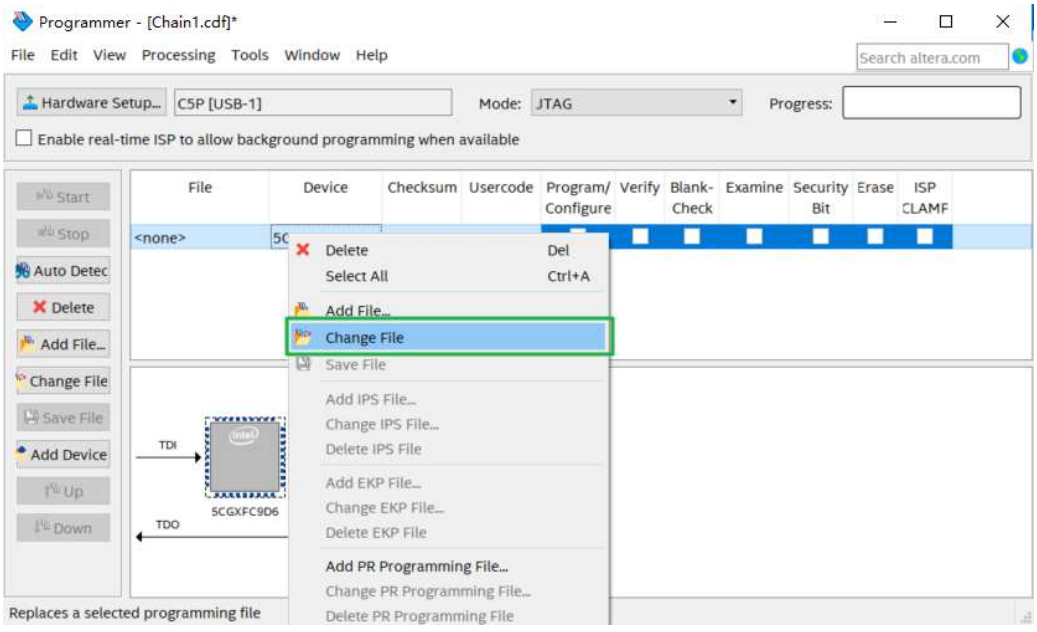

Figure 3-5 Open the .sof file to be programmed into the FPGA device

5. Select the .sof file to be programmed, as shown in **Figure 3-6**.

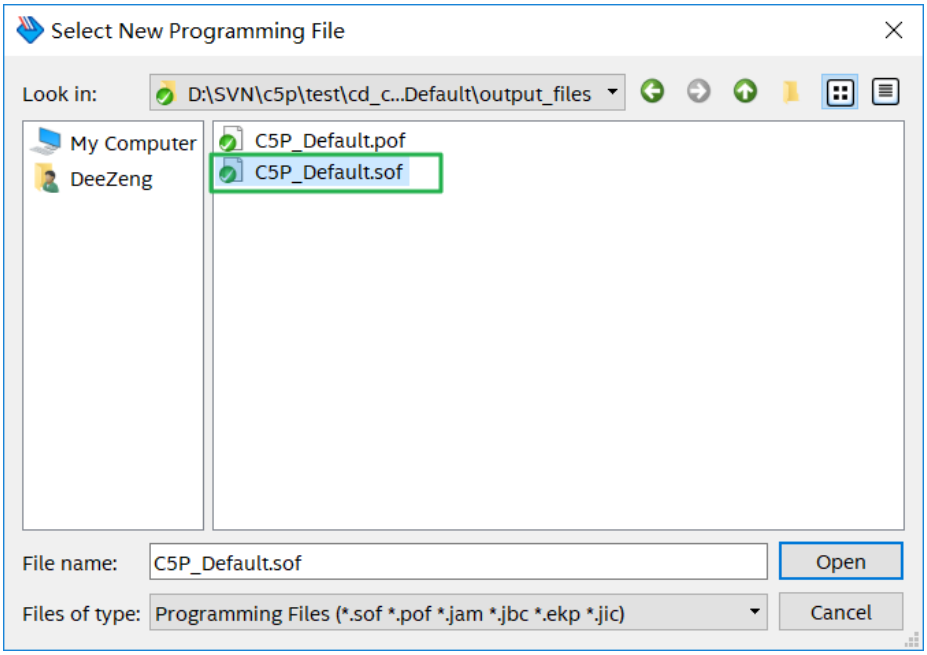

Figure 3-6 Select the .sof file to be programmed into the FPGA device

6. Click “Program/Configure” check box and then click “Start” button to download the .sof file into the FPGA device, as shown in **Figure 3-7**.

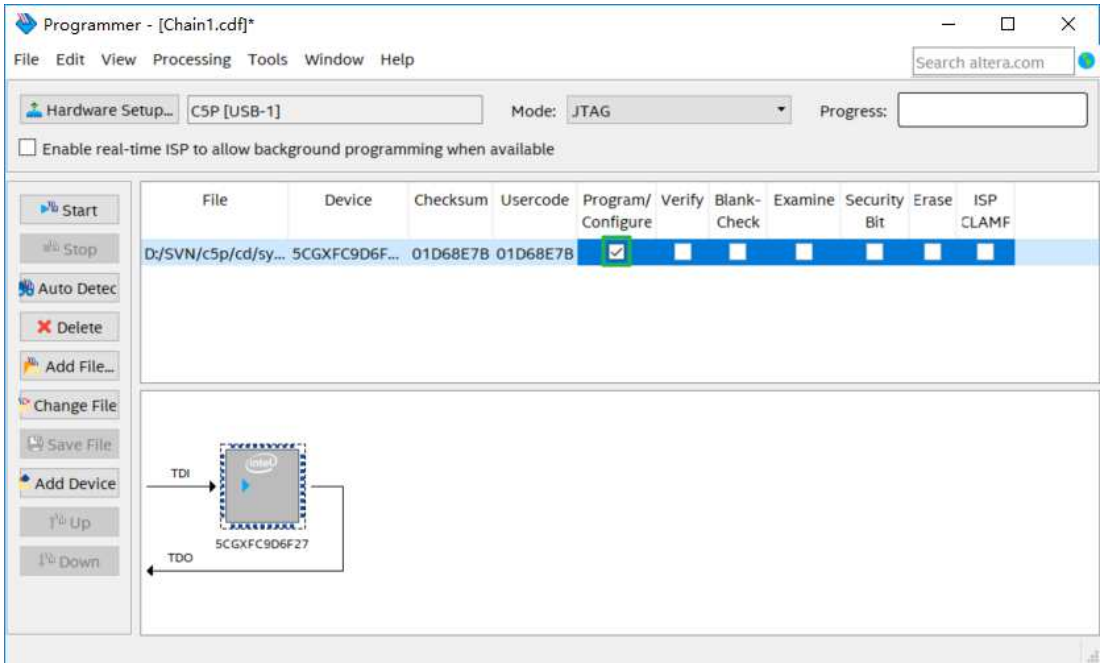

Figure 3-7 Program .sof file into the FPGA device

■ Configure the FPGA in AS Mode

- The C5P board uses the EPCSQ256 device to store configuration data for the Cyclone V FPGA. This configuration data is automatically loaded from the quad serial configuration device chip into the FPGA when the board is powered up

- Users need to use Serial Flash Loader (SFL) to program the EPCQ256 device via JTAG interface.
- The FPGA-based SFL is a soft intellectual property (IP) core within the FPGA that bridges the JTAG and Flash interfaces. The SFL Megafunction is available in Quartus Prime. **Figure 3-8** shows the programming method when adopting SFL solution.
- Please refer to Chapter 6 Program the EPCQ for the basic programming instructions on the serial configuration device.

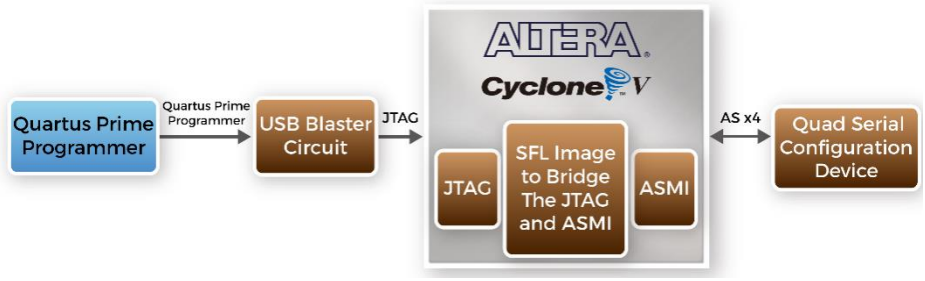

Figure 3-8 Programming a quad serial configuration device with SFL solution

3.2 Board Status Elements

In addition to the 4 LEDs that the FPGA device can control, there are 4 indicators which can indicate the board status, as shown in **Figure 3-9**, please refer the details in **Table 3-1**.

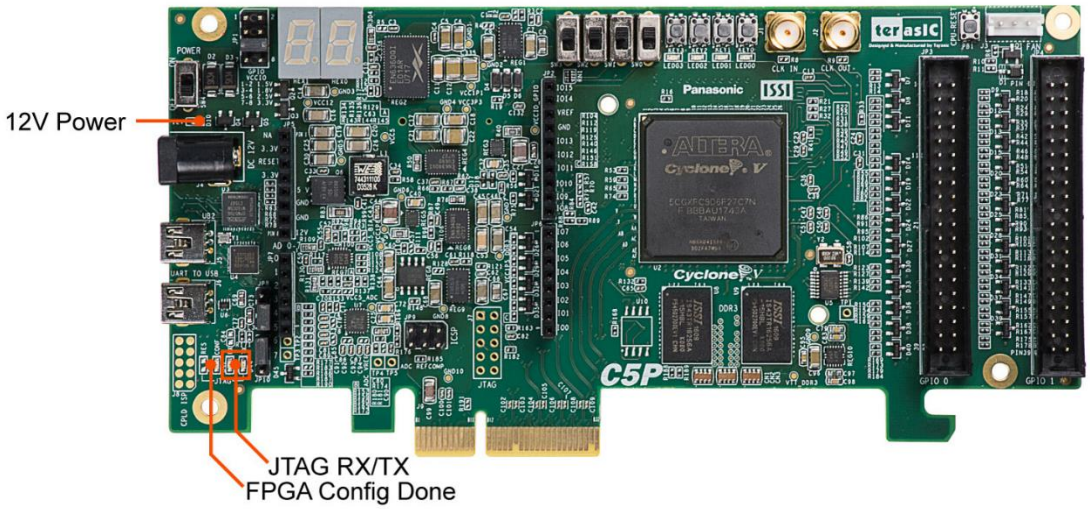

Figure 3-9 LED Indicators on C5P

Table 3-1 LED Indicators

LED Name	Signal Name	Description
D3	12V Power	Illuminates when 12V power is active
D43	JTAG_RX	Illuminates when USB Blaster II receives data
D44	JTAG_TX	Illuminates when USB Blaster II transmits data
D42	CONF_DONE	Illuminates when FPGA is configured successfully

3.3 Clock Circuitry

Figure 3-10 shows the default frequency of all external clocks to the Cyclone V FPGA. The 50MHz is generated by a crystal oscillator. The 50MHz clock signals connected to the FPGA are used as clock sources for user logic. The board also includes two SMA connectors which can be used to connect an external clock source to the board or to drive a clock signal in/out through the SMA connector. All these clock inputs are connected to the phase locked loops (PLL) clock input pins of the FPGA to allow users to use these clocks as a source clock for the PLL circuit.

The associated pin assignment for clock inputs to FPGA I/O pins is listed in **Table 3-2**.

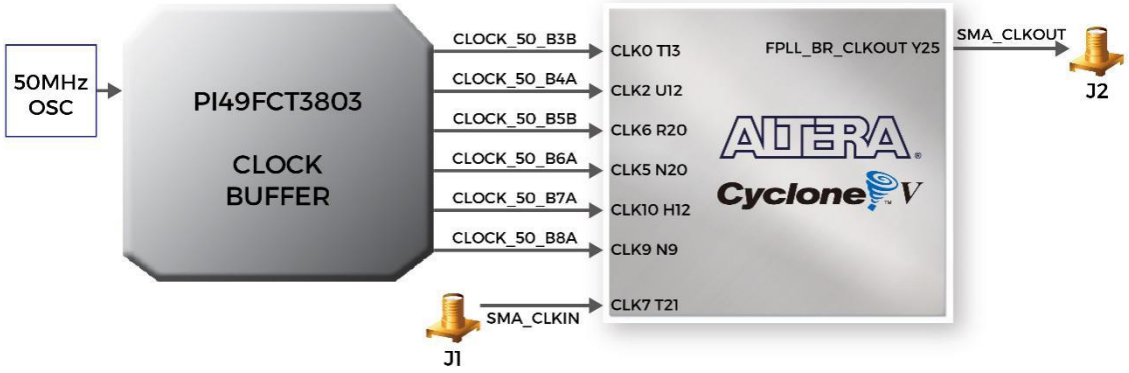

Figure 3-10 Block diagram of the clock distribution on C5P

Table 3-2 Pin Assignment of Clock Inputs

Signal Name	FPGA Pin No.	Direction	Description	I/O Standard
CLOCK_50_B3B	PIN_T13	Input	50MHz clock input (Bank 3B)	1.5 V
CLOCK_50_B4A	PIN_U12	Input	50MHz clock input (Bank 4A)	1.5 V
CLOCK_50_B5B	PIN_R20	Input	50MHz clock input (Bank 5B)	3.3-V LVTTL
CLOCK_50_B6A	PIN_N20	Input	50MHz clock input (Bank 6A)	3.3-V LVTTL
CLOCK_50_B7A	PIN_H12	Input	50MHz clock input (Bank 7A)	3.3-V LVTTL

CLOCK_50_B8A	PIN_N9	Input	50MHz clock input (Bank 8A)	3.3-V LVTTL
SMA_CLKIN	PIN_T21	Input	Externa（SMA) clock input	3.3-V LVTTL
SMA_CLKOUT	PIN_Y25	Output	Externa (SMA) clock output	3.3-V LVTTL

3.4 Peripherals Connected to the FPGA

This section describes the interfaces connected to the FPGA. Users can control or monitor different interfaces with user logic from the FPGA.

3.4.1 User Push-buttons, Switches and LEDs

The board has four push-buttons connected to the FPGA, as shown in **Figure 3-11**. Schmitt trigger circuit is implemented and acts as a switch debounce in **Figure 3-12** for the push-buttons connector. The four push-buttons are named KEY0, KEY1, KEY2, and KEY3; they are coming out of the Schmitt trigger device and are connected directly to the Cyclone V FPGA. The push-button generates a high logic level when it is not pressed and provides a low logic level when pressed. Since the push-buttons are debounced, they can be used as reset inputs in a circuit.

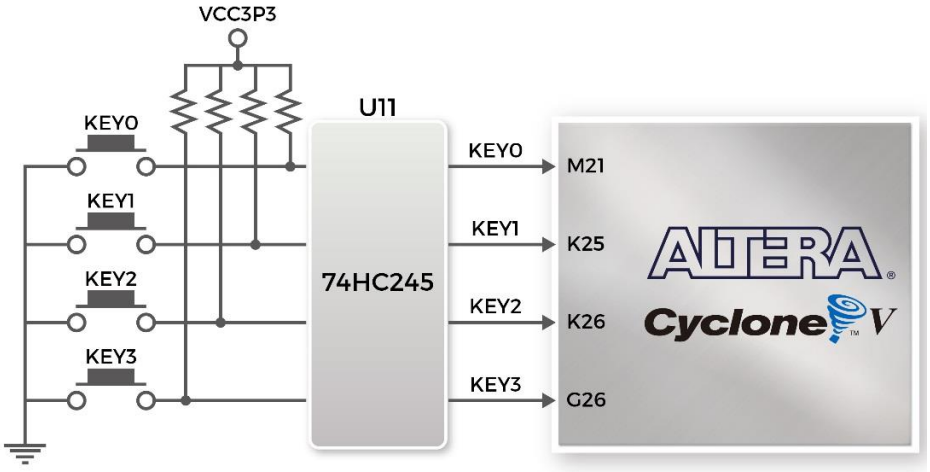

Figure 3-11 Connections between the push-buttons and the Cyclone V FPGA

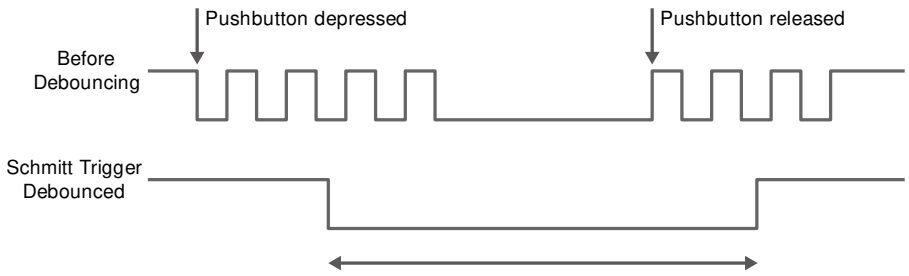

Figure 3-12 Switch debouncing

There are four slide switches connected to the FPGA, as shown in **Figure 3-13**. These switches are not debounced and are to be used as level-sensitive data inputs to a circuit. Each switch is connected directly and individually to the FPGA. When the switch is set to the DOWN position (towards the edge of the board), it generates a low logic level to the FPGA. When the switch is set to the UP position, a high logic level is generated to the FPGA.

.

Figure 3-13 Connections between the slide switches and Cyclone V FPGA

There are also four user-controllable LEDs connected to the FPGA. Each LED is driven directly and individually by the Cyclone V FPGA; driving its associated pin to a high logic level or low level to turn the LED on or off, respectively. **Figure 3-14** shows the connections between LEDs and Cyclone V FPGA. **Table 3-3**、**Table 3-4** and **Table 3-5** list the pin assignment of user push-buttons, switches, and LEDs.

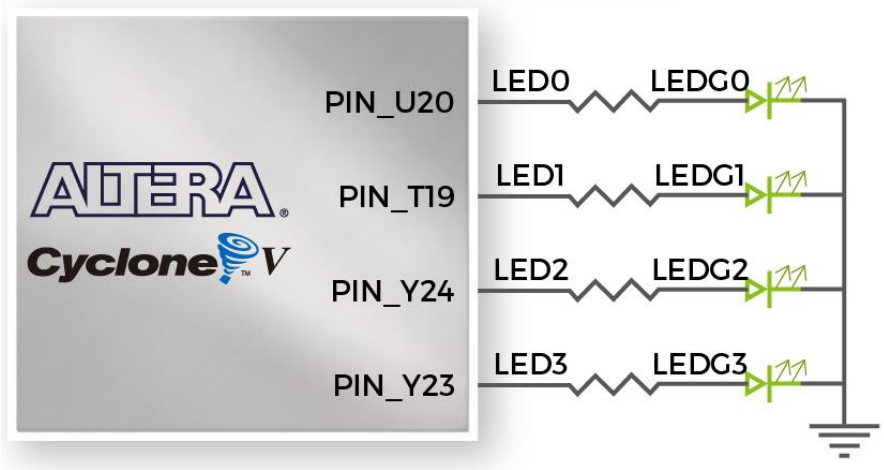

Figure 3-14 Connections between the LEDs and the Cyclone V FPGA

Table 3-3 Pin Assignment of Slide Switches

Switch Name	FPGA Pin No.	Direction	Description	I/O Standard
SW[0]	PIN_G20	Input	Slide Switch [0]	3.3-V LVTTL
SW[1]	PIN_F21	Input	Slide Switch [1]	3.3-V LVTTL
SW[2]	PIN_E21	Input	Slide Switch [2]	3.3-V LVTTL
SW[3]	PIN_H19	Input	Slide Switch [3]	3.3-V LVTTL

Table 3-4 Pin Assignment of Push-buttons

Key Name	FPGA Pin No.	Direction	Description	I/O Standard
CPU_RESET_n	PIN_AB24	Input	Generate a high logic level when it is not pressed	3.3-V LVTTL
KEY[0]	PIN_M21	Input	Generate a high logic level when it is not pressed. Four push-buttons (KEY0, KEY1, KEY2 and KEY3) are debounced.	3.3-V LVTTL
KEY[1]	PIN_K25	Input		3.3-V LVTTL
KEY[2]	PIN_K26	Input		3.3-V LVTTL
KEY[3]	PIN_G26	Input		3.3-V LVTTL

Table 3-5 LED Pin Assignment of LEDs

LED Name	FPGA Pin No.	Direction	Description	I/O Standard
LED[0]	PIN_U20	Output	Drive high logic 1 to I/O pin to turn the LED on. Drive lowh logic 0 to I/O pin to turn the LED off.	3.3-V LVTTL
LED[1]	PIN_T19	Output		3.3-V LVTTL
LED[2]	PIN_Y24	Output		3.3-V LVTTL
LED[3]	PIN_Y23	Output		3.3-V LVTTL

3.4.2 7-Segment Displays

C5P board has two 7-segment displays. **Figure 3-15** shows the connection of seven segments (common anode) to pins on Cyclone V FPGA。The segment can be turned on or off by applying a low logic level or high logic level from the FPGA, respectively. Each segment in a display is indexed from 0 to 6, with corresponding positions given in **Figure 3-15**. **Table 3-6** shows the pin assignment of FPGA to the 7-segment displays.

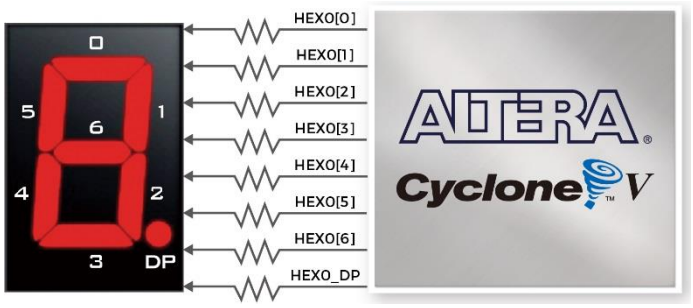

Figure 3-15 Connections between the 7-segment displays and Cyclone V FPGA

Table 3-6 Pin Assignment of 7-segment Displays

HEX Name	FPGA Pin No.	Direction	Description	I/O Standard
HEX0_DP	PIN_AA6	Input	Seven Segment Digit 0 DP	3.3-V LVTTL
HEX0[0]	PIN_T8	Input	Seven Segment Digit 0[0]	3.3-V LVTTL
HEX0[1]	PIN_P26	Input	Seven Segment Digit 0[1]	3.3-V

				LVTTL
HEX0[2]	PIN_V8	Input	Seven Segment Digit 0[2]	3.3-V LVTTL
HEX0[3]	PIN_U7	Input	Seven Segment Digit 0[3]	3.3-V LVTTL
HEX0[4]	PIN_U25	Input	Seven Segment Digit 0[4]	3.3-V LVTTL
HEX0[5]	PIN_W8	Input	Seven Segment Digit 0[5]	3.3-V LVTTL
HEX0[6]	PIN_U26	Input	Seven Segment Digit 0[6]	3.3-V LVTTL
HEX1_DP	PIN_V25	Input	Seven Segment Digit 1 DP	3.3-V LVTTL
HEX1[0]	PIN_T7	Input	Seven Segment Digit 1[0]	3.3-V LVTTL
HEX1[1]	PIN_W20	Input	Seven Segment Digit 1[1]	3.3-V LVTTL
HEX1[2]	PIN_AB6	Input	Seven Segment Digit 1[2]	3.3-V LVTTL
HEX1[3]	PIN_AC22	Input	Seven Segment Digit 1[3]	3.3-V LVTTL
HEX1[4]	PIN_Y9	Input	Seven Segment Digit 1[4]	3.3-V LVTTL
HEX1[5]	PIN_W21	Input	Seven Segment Digit 1[5]	3.3-V LVTTL
HEX1[6]	PIN_N25	Input	Seven Segment Digit 1[6]	3.3-V LVTTL

3.4.3 SDRAM Memory

The C5P features 64MB of SDRAM with a single 64MB (32Mx16) SDRAM chip. The chip consists of 16-bit data line, control line, and address line connected to the FPGA. This chip uses the 3.3V LVCMOS signaling standard. Connections between the FPGA and SDRAM are shown in **Figure 3-16**, and the pin assignment is listed in **Table 3-7**.

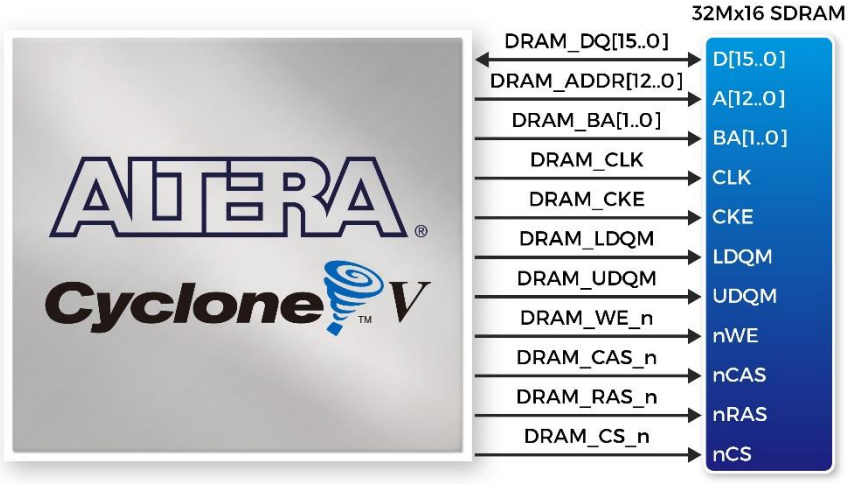

Figure 3-16 Connections between the FPGA and SDRAM

Table 3-7 Pin Assignment of SDRAM

Signal Name	FPGA Pin No.	Direction	Description	I/O Standard
DRAM_CLK	PIN_F26	Output	SDRAM Clock	3.3-V LVTTL
DRAM_CKE	PIN_E25	Output	SDRAM Clock Enable	3.3-V LVTTL
DRAM_ADDR[0]	PIN_D26	Output	SDRAM Address[0]	3.3-V LVTTL
DRAM_ADDR[1]	PIN_H20	Output	SDRAM Address[1]	3.3-V LVTTL
DRAM_ADDR[2]	PIN_F23	Output	SDRAM Address[2]	3.3-V LVTTL
DRAM_ADDR[3]	PIN_G22	Output	SDRAM Address[3]	3.3-V LVTTL
DRAM_ADDR[4]	PIN_B25	Output	SDRAM Address[4]	3.3-V LVTTL
DRAM_ADDR[5]	PIN_D22	Output	SDRAM Address[5]	3.3-V LVTTL
DRAM_ADDR[6]	PIN_C25	Output	SDRAM Address[6]	3.3-V LVTTL
DRAM_ADDR[7]	PIN_E23	Output	SDRAM Address[7]	3.3-V LVTTL
DRAM_ADDR[8]	PIN_B26	Output	SDRAM Address[8]	3.3-V LVTTL
DRAM_ADDR[9]	PIN_E24	Output	SDRAM Address[9]	3.3-V LVTTL
DRAM_ADDR[10]	PIN_D25	Output	SDRAM Address[10]	3.3-V LVTTL
DRAM_ADDR[11]	PIN_M26	Output	SDRAM Address[11]	3.3-V LVTTL
DRAM_ADDR[12]	PIN_M25	Output	SDRAM Address[12]	3.3-V LVTTL
DRAM_BA[0]	PIN_J20	Output	SDRAM Bank Address[0]	3.3-V LVTTL
DRAM_BA[1]	PIN_H22	Output	SDRAM Bank Address[1]	3.3-V LVTTL
DRAM_DQ[0]	PIN_L24	Output	SDRAM Data[0]	3.3-V LVTTL
DRAM_DQ[1]	PIN_M24	Output	SDRAM Data[1]	3.3-V LVTTL
DRAM_DQ[2]	PIN_N23	Output	SDRAM Data[2]	3.3-V LVTTL
DRAM_DQ[3]	PIN_K23	Output	SDRAM Data[3]	3.3-V LVTTL

DRAM_DQ[4]	PIN_H24	Output	SDRAM Data[4]	3.3-V LVTTL
DRAM_DQ[5]	PIN_J23	Output	SDRAM Data[5]	3.3-V LVTTL
DRAM_DQ[6]	PIN_K24	Output	SDRAM Data[6]	3.3-V LVTTL
DRAM_DQ[7]	PIN_L22	Output	SDRAM Data[7]	3.3-V LVTTL
DRAM_DQ[8]	PIN_G25	Output	SDRAM Data[8]	3.3-V LVTTL
DRAM_DQ[9]	PIN_G24	Output	SDRAM Data[9]	3.3-V LVTTL
DRAM_DQ[10]	PIN_H25	Output	SDRAM Data[10]	3.3-V LVTTL
DRAM_DQ[11]	PIN_J21	Output	SDRAM Data[11]	3.3-V LVTTL
DRAM_DQ[12]	PIN_L23	Output	SDRAM Data[12]	3.3-V LVTTL
DRAM_DQ[13]	PIN_K21	Output	SDRAM Data[13]	3.3-V LVTTL
DRAM_DQ[14]	PIN_N24	Output	SDRAM Data[14]	3.3-V LVTTL
DRAM_DQ[15]	PIN_M22	Output	SDRAM Data[15]	3.3-V LVTTL
DRAM_LDQM	PIN_H23	Output	DQ[7:0] SDRAM Data Mask	3.3-V LVTTL
DRAM_UDQM	PIN_F24	Output	DQ[15:8] SDRAM Data Mask	3.3-V LVTTL
DRAM_CS_n	PIN_F22	Output	SDRAM Chip Select	3.3-V LVTTL
DRAM_WE_n	PIN_J25	Output	SDRAM Write Enable	3.3-V LVTTL
DRAM_CAS_n	PIN_J26	Output	SDRAM Column Address Strobe	3.3-V LVTTL
DRAM_RAS_n	PIN_E26	Output	SDRAM Row Address Strobe	3.3-V LVTTL

3.4.4 DDR3 Memory

C5P supports 1GB of DDR3 SDRAM comprising of two x16 bit DDR3 devices. The signals are connected to the dedicated Hard Memory Controller for FPGA I/O banks and the target speed is 400MHz. **Figure 3-17** shows the connections between the DDR3 and Cyclone V FPGA. **Table 3-8** lists the pin assignment of the DDR3 and its description with I/O standard.

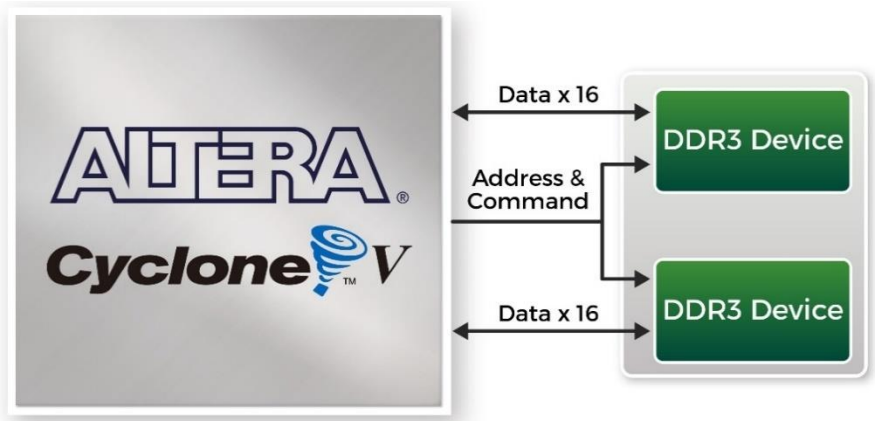

Figure 3-17 Connections between FPGA and DDR3

Table 3-8 Pin Assignment of DDR3 Memory

Signal Name	FPGA Pin No.	Direction	Description	I/O Standard
DDR3_ADDR[0]	PIN_AE6	Output	DDR3 Address[0]	SSTL-15 Class I
DDR3_ADDR[1]	PIN_AF6	Output	DDR3 Address[1]	SSTL-15 Class I
DDR3_ADDR[2]	PIN_AF7	Output	DDR3 Address[2]	SSTL-15 Class I
DDR3_ADDR[3]	PIN_AF8	Output	DDR3 Address[3]	SSTL-15 Class I
DDR3_ADDR[4]	PIN_U10	Output	DDR3 Address[4]	SSTL-15 Class I
DDR3_ADDR[5]	PIN_U11	Output	DDR3 Address[5]	SSTL-15 Class I
DDR3_ADDR[6]	PIN_AE9	Output	DDR3 Address[6]	SSTL-15 Class I
DDR3_ADDR[7]	PIN_AF9	Output	DDR3 Address[7]	SSTL-15 Class I
DDR3_ADDR[8]	PIN_AB12	Output	DDR3 Address[8]	SSTL-15 Class I
DDR3_ADDR[9]	PIN_AB11	Output	DDR3 Address[9]	SSTL-15 Class I
DDR3_ADDR[10]	PIN_AC9	Output	DDR3 Address[10]	SSTL-15 Class I
DDR3_ADDR[11]	PIN_AC8	Output	DDR3 Address[11]	SSTL-15 Class I
DDR3_ADDR[12]	PIN_AB10	Output	DDR3 Address[12]	SSTL-15 Class I
DDR3_ADDR[13]	PIN_AC10	Output	DDR3 Address[13]	SSTL-15 Class I
DDR3_ADDR[14]	PIN_W11	Output	DDR3 Address[14]	SSTL-15 Class I
DDR3_BA[0]	PIN_V10	Output	DDR3 Bank Address[0]	SSTL-15 Class I
DDR3_BA[1]	PIN_AD8	Output	DDR3 Bank Address[1]	SSTL-15 Class I
DDR3_BA[2]	PIN_AE8	Output	DDR3 Bank Address[2]	SSTL-15 Class I
DDR3_CK_p	PIN_N10	Output	DDR3 Clock p	Differential 1.5-V SSTL Class I
DDR3_CK_n	PIN_P10	Output	DDR3 Clock n	Differential 1.5-V SSTL Class I
DDR3_CKE	PIN_AF14	Output	DDR3 Clock Enable	SSTL-15 Class I
DDR3_DQS_p[0]	PIN_V13	Output	DDR3 Data Strobe p[0]	Differential 1.5-V SSTL Class I
DDR3_DQS_p[1]	PIN_U14	Output	DDR3 Data Strobe p[1]	Differential 1.5-V SSTL Class I
DDR3_DQS_p[2]	PIN_V15	Output	DDR3 Data Strobe p[2]	Differential 1.5-V SSTL Class I
DDR3_DQS_p[3]	PIN_W16	Output	DDR3 Data Strobe p[3]	Differential 1.5-V SSTL Class I
DDR3_DQS_n[0]	PIN_W13	Output	DDR3 Data Strobe n[0]	Differential 1.5-V

				SSTL Class I
DDR3_DQS_n[1]	PIN_V14	Output	DDR3 Data Strobe n[1]	Differential 1.5-V SSTL Class I
DDR3_DQS_n[2]	PIN_W15	Output	DDR3 Data Strobe n[2]	Differential 1.5-V SSTL Class I
DDR3_DQS_n[3]	PIN_W17	Output	DDR3 Data Strobe n[3]	Differential 1.5-V SSTL Class I
DDR3_DQ[0]	PIN_AA14	Output	DDR3 Data[0]	SSTL-15 Class I
DDR3_DQ[1]	PIN_Y14	Output	DDR3 Data[1]	SSTL-15 Class I
DDR3_DQ[2]	PIN_AD11	Output	DDR3 Data[2]	SSTL-15 Class I
DDR3_DQ[3]	PIN_AD12	Output	DDR3 Data[3]	SSTL-15 Class I
DDR3_DQ[4]	PIN_Y13	Output	DDR3 Data[4]	SSTL-15 Class I
DDR3_DQ[5]	PIN_W12	Output	DDR3 Data[5]	SSTL-15 Class I
DDR3_DQ[6]	PIN_AD10	Output	DDR3 Data[6]	SSTL-15 Class I
DDR3_DQ[7]	PIN_AF12	Output	DDR3 Data[7]	SSTL-15 Class I
DDR3_DQ[8]	PIN_AC15	Output	DDR3 Data[8]	SSTL-15 Class I
DDR3_DQ[9]	PIN_AB15	Output	DDR3 Data[9]	SSTL-15 Class I
DDR3_DQ[10]	PIN_AC14	Output	DDR3 Data[10]	SSTL-15 Class I
DDR3_DQ[11]	PIN_AF13	Output	DDR3 Data[11]	SSTL-15 Class I
DDR3_DQ[12]	PIN_AB16	Output	DDR3 Data[12]	SSTL-15 Class I
DDR3_DQ[13]	PIN_AA16	Output	DDR3 Data[13]	SSTL-15 Class I
DDR3_DQ[14]	PIN_AE14	Output	DDR3 Data[14]	SSTL-15 Class I
DDR3_DQ[15]	PIN_AF18	Output	DDR3 Data[15]	SSTL-15 Class I
DDR3_DQ[16]	PIN_AD16	Output	DDR3 Data[16]	SSTL-15 Class I
DDR3_DQ[17]	PIN_AD17	Output	DDR3 Data[17]	SSTL-15 Class I
DDR3_DQ[18]	PIN_AC18	Output	DDR3 Data[18]	SSTL-15 Class I
DDR3_DQ[19]	PIN_AF19	Output	DDR3 Data[19]	SSTL-15 Class I
DDR3_DQ[20]	PIN_AC17	Output	DDR3 Data[20]	SSTL-15 Class I
DDR3_DQ[21]	PIN_AB17	Output	DDR3 Data[21]	SSTL-15 Class I
DDR3_DQ[22]	PIN_AF21	Output	DDR3 Data[22]	SSTL-15 Class I
DDR3_DQ[23]	PIN_AE21	Output	DDR3 Data[23]	SSTL-15 Class I
DDR3_DQ[24]	PIN_AE15	Output	DDR3 Data[24]	SSTL-15 Class I
DDR3_DQ[25]	PIN_AE16	Output	DDR3 Data[25]	SSTL-15 Class I
DDR3_DQ[26]	PIN_AC20	Output	DDR3 Data[26]	SSTL-15 Class I
DDR3_DQ[27]	PIN_AD21	Output	DDR3 Data[27]	SSTL-15 Class I
DDR3_DQ[28]	PIN_AF16	Output	DDR3 Data[28]	SSTL-15 Class I
DDR3_DQ[29]	PIN_AF17	Output	DDR3 Data[29]	SSTL-15 Class I

DDR3_DQ[30]	PIN_AD23	Output	DDR3 Data[30]	SSTL-15 Class I
DDR3_DQ[31]	PIN_AF23	Output	DDR3 Data[31]	SSTL-15 Class I
DDR3_DM[0]	PIN_AF11	Output	DDR3 Data Mask[0]	SSTL-15 Class I
DDR3_DM[1]	PIN_AE18	Output	DDR3 Data Mask[1]	SSTL-15 Class I
DDR3_DM[2]	PIN_AE20	Output	DDR3 Data Mask[2]	SSTL-15 Class I
DDR3_DM[3]	PIN_AE24	Output	DDR3 Data Mask[3]	SSTL-15 Class I
DDR3_CS_n	PIN_R11	Output	DDR3 Chip Select	SSTL-15 Class I
DDR3_WE_n	PIN_T9	Output	DDR3 Write Enable	SSTL-15 Class I
DDR3_CAS_n	PIN_W10	Output	DDR3 Column Address Strobe	SSTL-15 Class I
DDR3_RAS_n	PIN_Y10	Output	DDR3 Row Address Strobe	SSTL-15 Class I
DDR3_RESET_n	PIN_AE19	Output	DDR3 Reset	SSTL-15 Class I
DDR3_ODT	PIN_AD13	Output	DDR3 On-die Termination	SSTL-15 Class I
DDR3_RZQ	PIN_AE11	Input	External reference ball for output drive calibration	1.5 V

3.4.5 UART to USB

The C5P board has one UART interface. The physical interface is implemented by UART-USB onboard bridge from a CP2102N chip to the host with a USB Mini-B connector. More information about the chip is available on the manufacturer's website, or in the directory \Datasheets\UART TO USB of C5P system CD. **Figure 3-18** shows the connections between the FPGA, CP2102N chip, and the USB Mini-B connector. **Table 3-9** lists the pin assignment of UART interface connected to the FPGA.

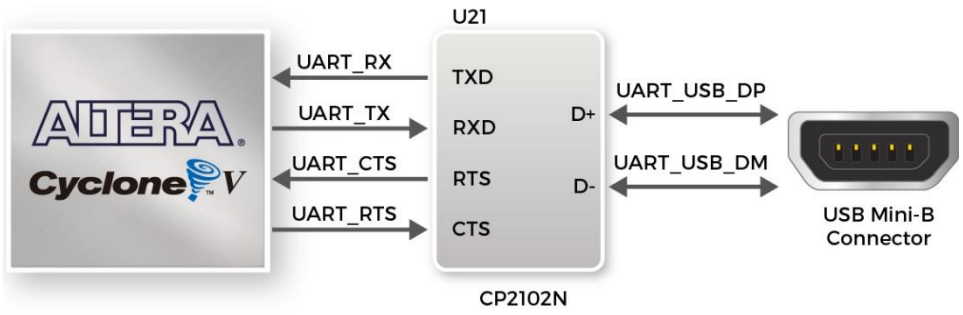

Figure 3-18 Connections between the FPGA, CP2102N chip and USB Mini-B connector