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MAX 10 NEEK

FPGA Development Kit

User Manual

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CONTENTS

Chapter 1

MAX 10 NEEK Development Kit

The MAX 10 NEEK from Terasic is a full featured embedded evaluation kit based upon the MAX10 family of Altera FPGAs. It offers a comprehensive design environment with everything embedded developers need to create a processing based system. The MAX 10 NEEK delivers an integrated platform that includes hardware, design tools, intellectual property and reference designs for developing a wide range of audio, video and many other exciting applications.

The fully integrated kit allows developers to rapidly customize their processor and IP to suit their specific needs, rather than constraining their software around the fixed feature set of the processor. The all-in-one embedded solution, the MAX 10 NEEK, combines a 5-point LCD touch panel and digital image module that provides developers an ideal platform for multimedia applications, making the best use of the parallel nature of FPGAs.

1.1 Package Contents

Figure 1-1 shows a photograph of the MAX 10 NEEK package.

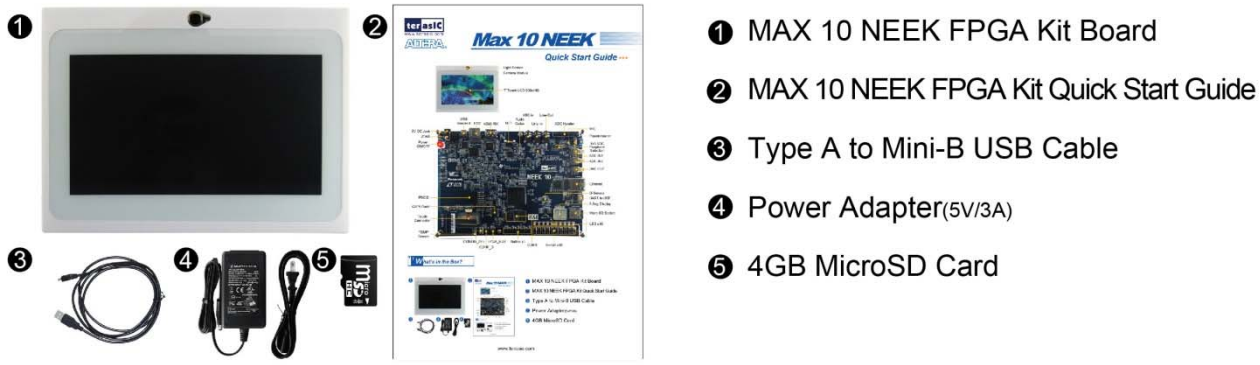

Figure 1-1 The MAX 10 NEEK package contents

The MAX 10 NEEK package includes:

- The MAX 10 NEEK development board
- MAX 10 NEEK Quick Start Guide
- One USB cables (Type A to Mini-B) for USB control and FPGA programming and control
- 5V DC power adapter
- Power Cable

1.2 MAX 10 NEEK System CD

The MAX 10 NEEK System CD contains all the documents and supporting materials associated with MAX 10 NEEK, including the user manual, system builder, reference designs, and device datasheets. Users can download this system CD from the link: http://cd-max10-neek.terasic.com.

1.3 Getting Help

Here are the addresses where you can get help if you encounter any problems:

- Altera Corporation
- 101 Innovation Drive San Jose, California, 95134 USA

Email: university@altera.com

- Terasic Technologies
- 9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan

Email: support@terasic.com

Tel.: +886-3-575-0880

Website: max10-neek.terasic.com

Chapter 2

Introduction of the MAX 10 NEEK Board

2.1 Layout and Components

Figure 2-1 shows a photograph of the board. It depicts the layout of the board and indicates the location of the connectors and key components.

Figure 2-1 MAX 10 NEEK development board (top view)

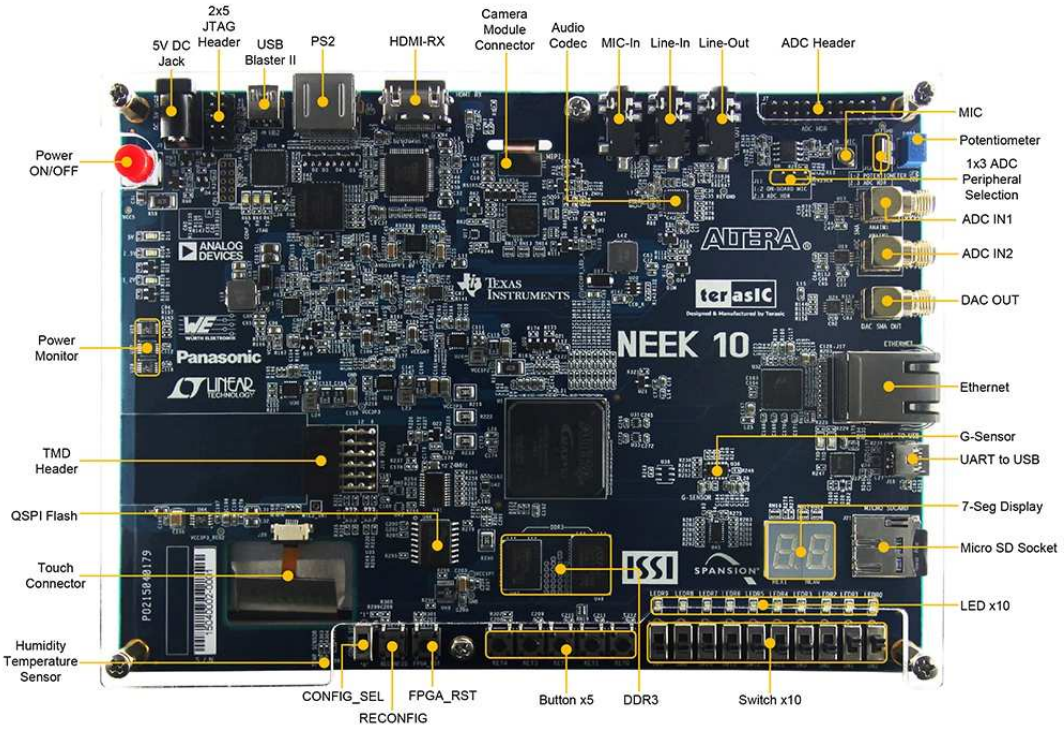

Figure 2-2 MAX 10 NEEK development board (bottom view)

The MAX 10 NEEK board has many features that allow users to implement a wide range of designed circuits, from simple circuits to various multimedia projects.

The following hardware is provided on the board:

- Altera MAX® 10 10M50DAF484C6G device
- USB-Blaster II onboard for programming; JTAG Mode
- 256MB DDR3 SDRAM (64Mx16 and 128Mx8)
- 64MB QSPI Flash
- Micro SD card socket
- Five push-buttons
- Ten slide switches
- Ten red user LEDs
- Two 7-segment displays
- Three 50MHz clock sources from the clock generator
- 24-bit CD-quality audio CODEC with line-in, line-out jacks
- On-board microphone
- HDMI RX, incorporates HDM v1.4a features, including 3D video supporting
- 800x480 7.0 inch Color LCD with 5-point Capacitive-touch
- Gigabit Ethernet PHY with RJ45 connector
- UART to USB, USB Mini-B connector
- 8M pixel MIPI CS2 color camera input

- One ambient light sensor
- One humidity and temperature sensor
- One accelerometer
- One external 16 bit digital-to-analog converter (DAC) device with SMA output
- Potentiometer input to ADC
- Two MAX 10 FPGA ADC SMA inputs
- One 2x10 ADC header with 16 analog inputs connected to MAX10 ADCs

2.2 Block Diagram of the MAX 10 NEEK Board

Figure 2-3 is the block diagram of the board. All the connections are established through the MAX 10 FPGA device to provide maximum flexibility for users. Users can configure the FPGA to implement any system design.

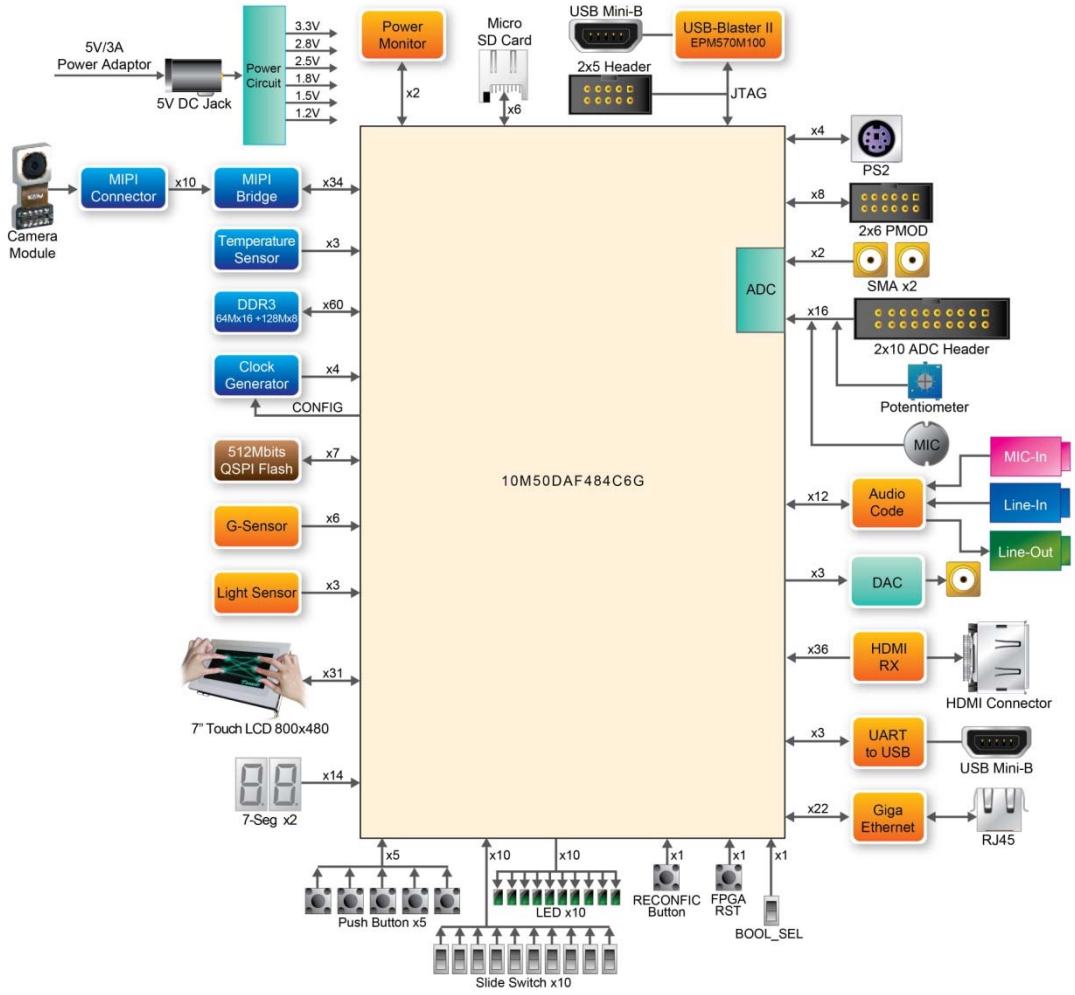

Figure 2-3 Block diagram of MAX 10 NEEK

FPGA Device

- MAX 10 10M50DAF484C6G Device
- Integrated dual ADCs, each ADC supports 1 dedicated analog input and 8 dual function pins
- 50K programmable logic elements
- 1,638 Kbits embedded memory
- 5,888 Kbits user flash memory
- 4 PLLs

Configuration and Debug

- On-board USB-Blaster II (mini USB type B connector)
- Optional JTAG direct via 10-pin header
- One slide switch for dual boot image selection

Memory Device

- 256MB DDR3 SDRAM (64Mx16 and 128Mx8)
- 512Mb QSPI Flash
- Micro SD card socket

Communication and Expansion Header

- Gigabit Ethernet PHY with RJ45 connector
- UART to USB, USB Mini-B connector
- PS/2 mouse/keyboard connector
- 2x6 TMD (Terasic Mini Digital) Expansion Header

Display

- 800x480 7.0 inch Color LCD with 5-point Capacitive-touch

Audio

- 24-bit CD-quality audio CODEC with line-in, line-out jacks

Video Input

- HDMI RX, incorporates HDM v1.4a features, including 3D video supporting
- 8M pixel MIPI CS2 color camera input

Analog

- Two MAX 10 FPGA ADC SMA inputs
- Potentiometer input to ADC
- On-Board MIC input to ADC
- 2x10 ADC header with 16 analog inputs connected to MAX10 ADCs
- One DAC SMA output

Switches, Buttons, and Indicators

- Five push-buttons
- Ten slide switches
- Ten red user LEDs
- Two 7-segment displays

Sensors

- Ambient light sensor
- Humidity and temperature sensor
- Accelerometer
- Power monitor

Power

- 5V/3A DC input

Chapter 3

Using the MAX 10 NEEK Board

This chapter provides an instruction to use the board and describes the peripherals.

3.1 Configuration of MAX 10 FPGA on MAX 10 NEEK

There are two types of configuration method supported by MAX 10 NEEK:

1. JTAG configuration: configuration using JTAG ports.

JTAG configuration scheme allows you to directly configure the device core through JTAG pins - TDI, TDO, TMS, and TCK pins. The Quartus II software automatically generates .sof that are used for JTAG configuration with a download cable in the Quartus II software programmer..

2. Internal configuration: configuration using internal flash.

Before internal configuration, you need to program the configuration data into the configuration flash memory (CFM) which provides non-volatile storage for the bit stream. The information is retained within CFM even if the MAX 10 NEEK board is turned off. When the board is powered on, the configuration data in the CFM is automatically loaded into the MAX 10 FPGA.

■ JTAG Chain on MAX 10 NEEK Board

The FPGA device can be configured through JTAG interface on MAX 10 NEEK board, but the JTAG chain must form a closed loop, which allows Quartus II programmer to the detect FPGA device. **Figure 3-1** illustrates the JTAG chain on MAX 10 NEEK board

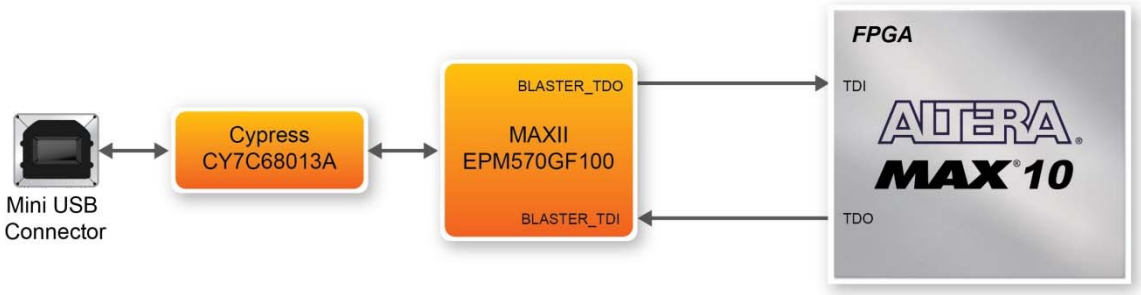

Figure 3-1 Path of the JTAG chain

■ Configure the FPGA in JTAG Mode

The following shows how the FPGA is programmed in JTAG mode step by step.

1. Open the Quartus II programmer and click "Auto Detect", as circled in Figure 3-2

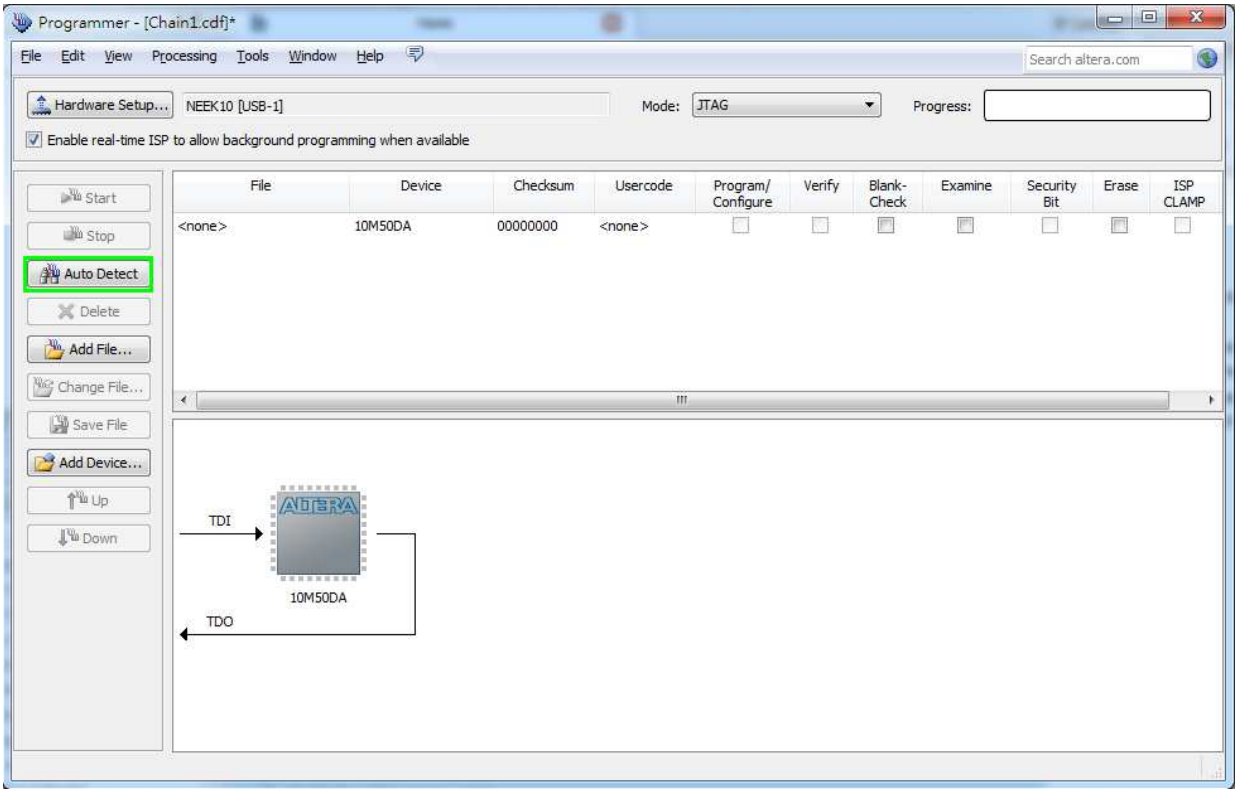

Figure 3-2 Detect FPGA device in JTAG mode

2. Select detected device associated with the board, as circled in Figure 3-3.

Figure 3-3 Select 10M50DAES device

3. FPGA is detected, as shown in **Figure 3-4**.

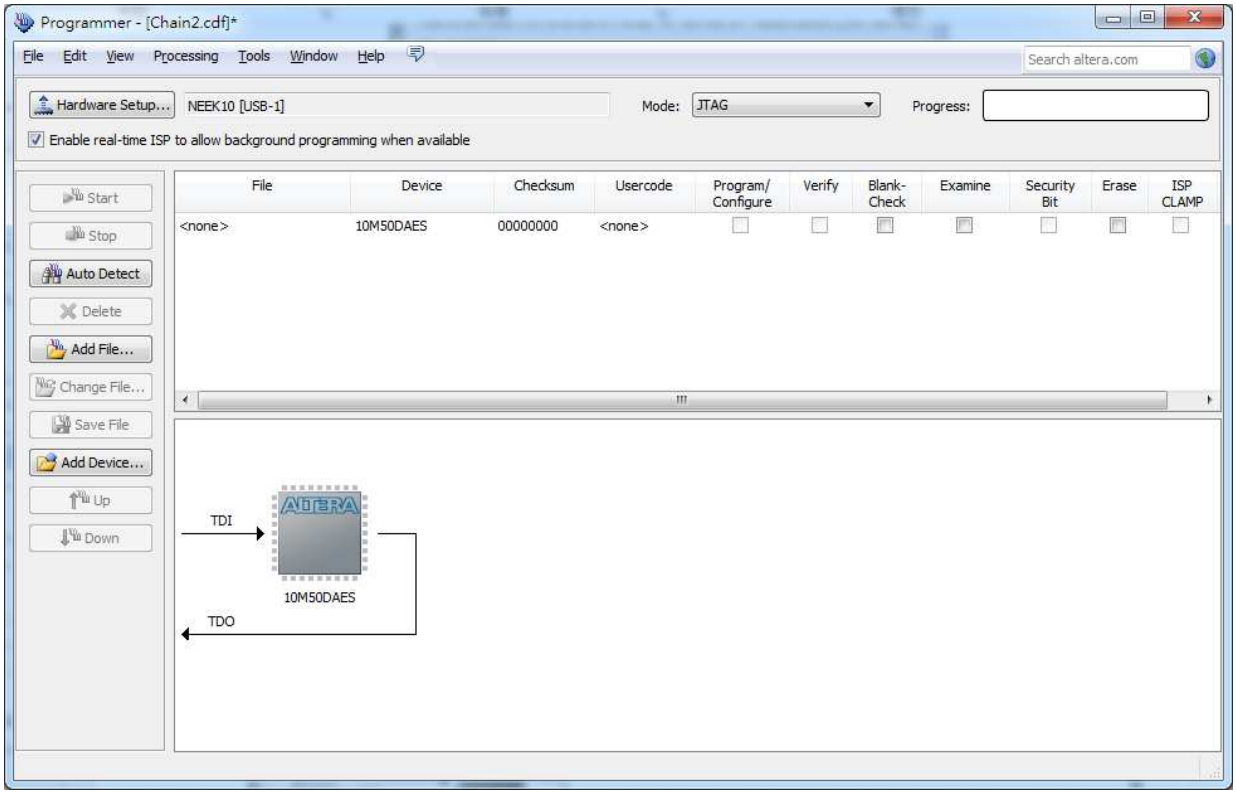

Figure 3-4 FPGA detected in Quartus programmer

4. Right click on the FPGA device and open the .sof file to be programmed, as highlighted in **Figure 3-5**

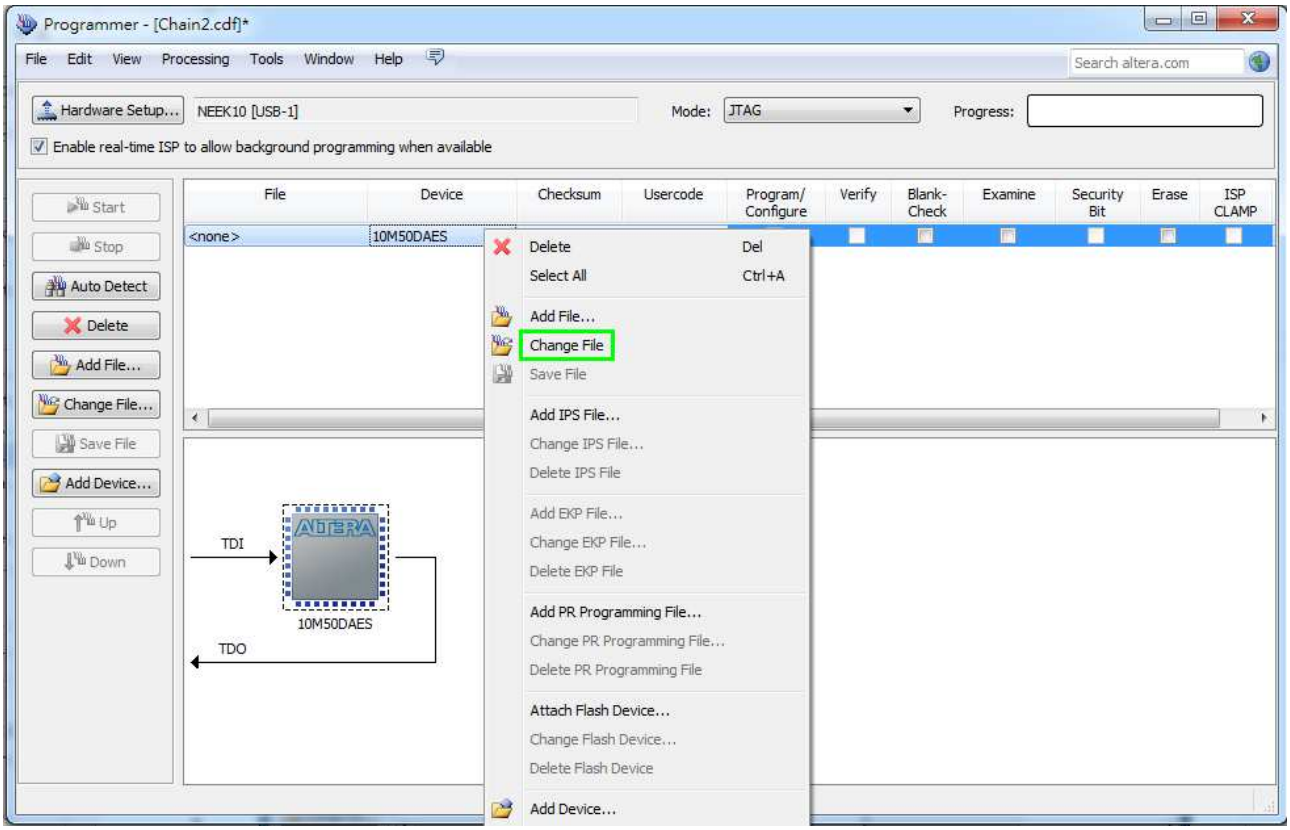

Figure 3-5 Open the .sof file to be programmed into the FPGA device

5. Select the .sof file to be programmed, as shown in **Figure 3-6**.

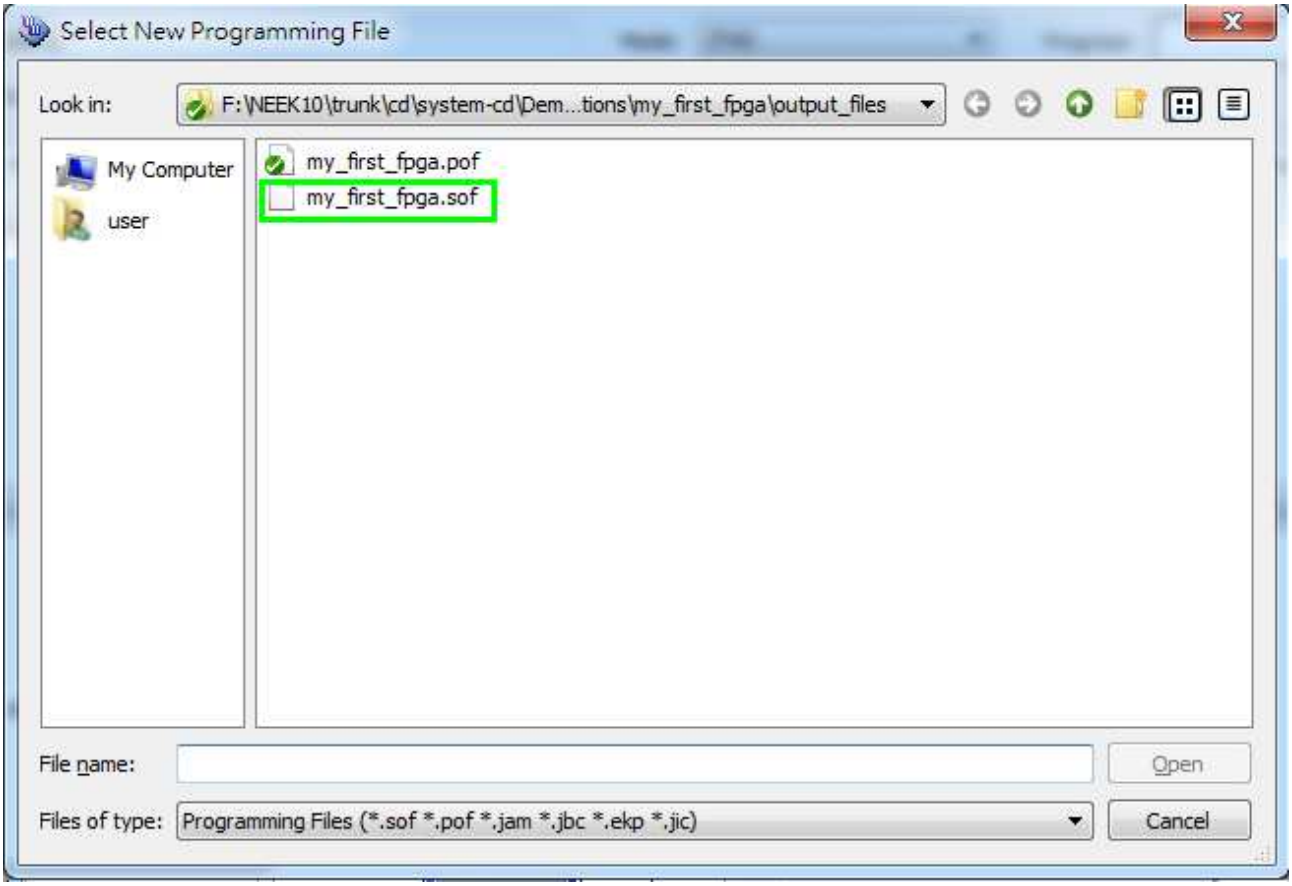

Figure 3-6 Select the .sof file to be programmed into the FPGA device

6. Click “Program/Configure” check box and then click “Start” button to download the .sof file into the FPGA device, as shown in **Figure 3-7**.

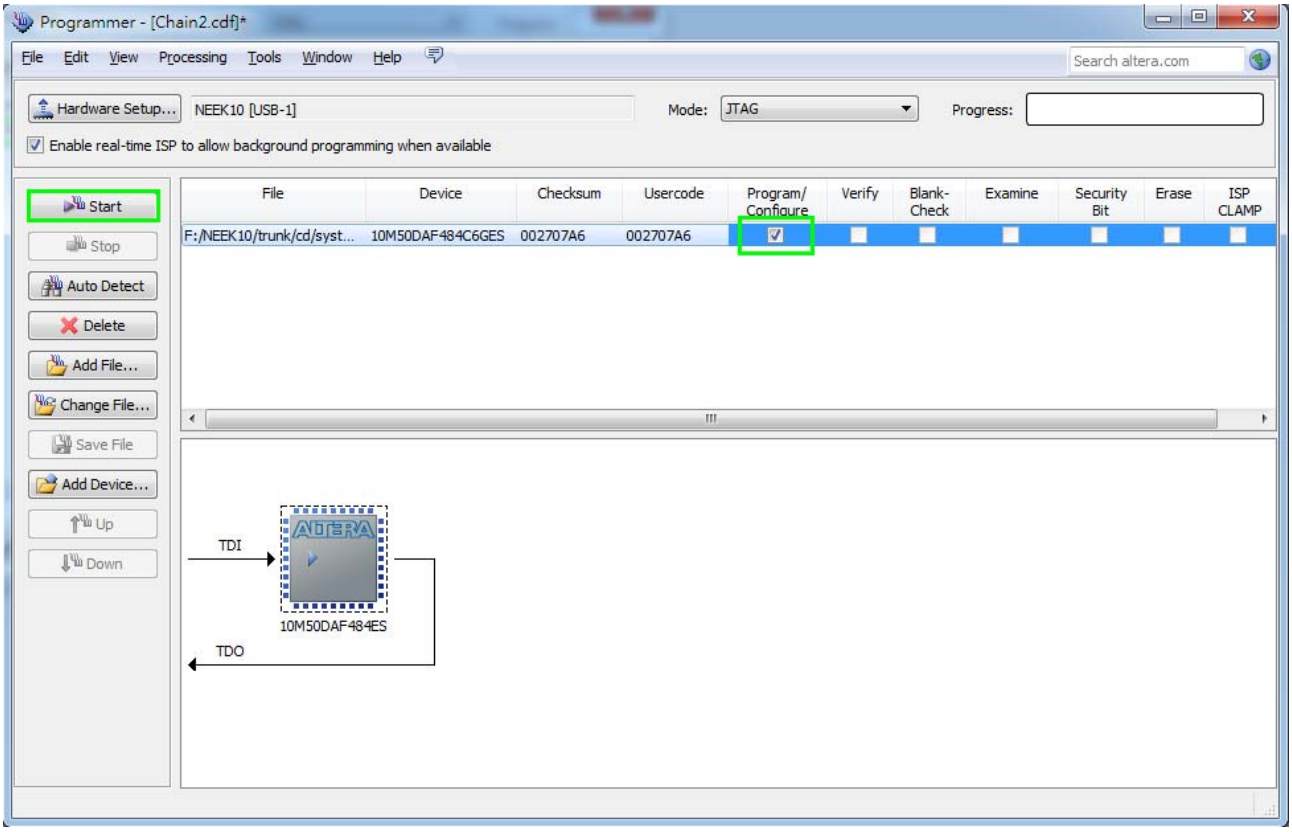

Figure 3-7 Program .sof file into the FPGA device

■ Internal Configuration

- The configuration data to be written to CFM will be part of the programmer object file (.pof). This configuration data is automatically loaded from the CFM into the MAX 10 devices when the board is powered up.
- Please refer to Chapter 8: Programming the Configuration Flash Memory (CFM) for the basic programming instruction on the configuration flash memory (CFM).

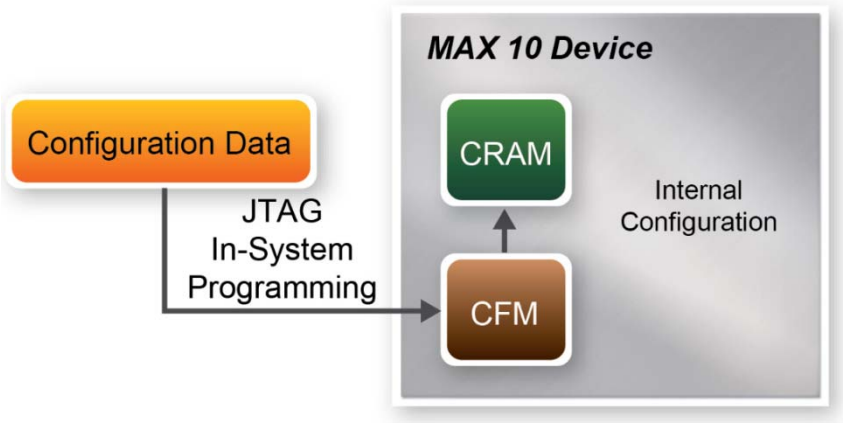

Figure 3-8 High-Level Overview of Internal Configuration for MAX 10 Devices

3.2 Board Status Elements

In addition to the 10 LEDs that FPGA device can control, there are 4 indicators which can indicate the board status (See **Figure 3-9)**, please refer the details in **Table 3-1**

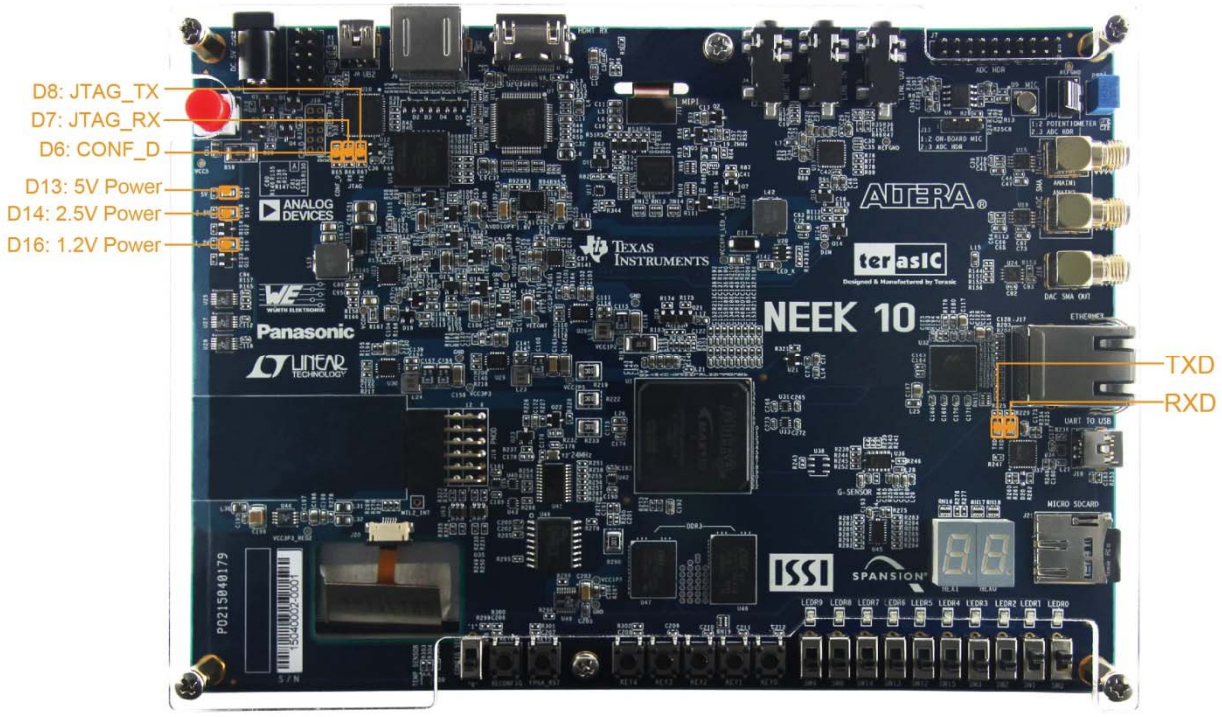

Figure 3-9 LED Indicators on MAX 10 NEEK

Table 3-1 LED Indicators

Board Reference	*LED Name*	*Description*
D13	5V Power	Illuminate when 5V power is active.
D14	2.5V Power	Illuminate when 2.5V power is active.
D16	1.2V Power	Illuminate when 1.2V power is active.
D6	CONF_DONE	Illuminate when configuration data is loaded into MAX 10 device without error.
D7	JTAG_RX	Illuminate during data is uploaded from MAX 10 device to PC through UB2.
D8	JTAG_TX	Illuminate during configuration data is loaded into MAX 10 device from UB2.
TXD	TXD	Illuminate during transmitting data via USB.
RXD	RXD	Illuminate during receiving data via USB.

3.3 Clock Circuitry

Figure 3-10 shows the default frequency of all external clocks to the MAX 10 FPGA. A clock generator is used to distribute clock signals with low jitter. The three 50MHz clock signals connected to the FPGA are used as clock sources for user logic. One 25MHz clock signal is connected to the clock input of Gigabit Ethernet Transceiver. One 24MHz clock signal is connected to the clock inputs of USB microcontroller of USB Blaster II. One 28.63636MHz clock signal is connected to the clock input of HDMI Receiver chip. The other 50MHz clock signal is connected to MAX CPLD of USB Blaster II. One 10MHz clock signal is connected to the PLL1 and PLL3 of FPGA, the outputs of these two PLLs can drive ADC clock. The associated pin assignment for clock inputs to FPGA I/O pins is listed in Table 3-2.

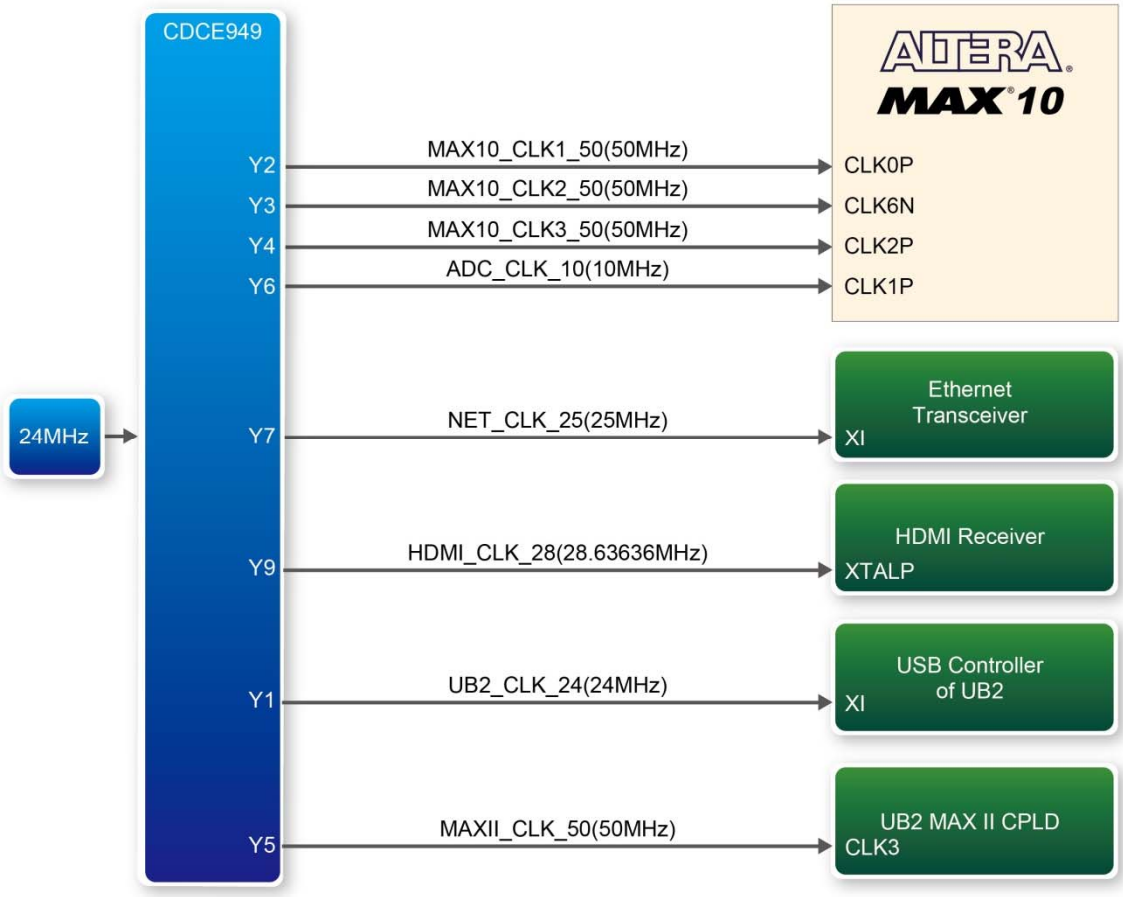

Figure 3-10 Block diagram of the clock distribution on MAX 10 NEEK

Table 3-2 Pin Assignment of Clock Inputs

Signal Name	FPGA Pin No.	Description	I/O Standard
MAX10_CLK1_50	PIN_N5	50 MHz clock input	2.5V
MAX10_CLK2_50	PIN_V9	50 MHz clock input	3.3V
MAX10_CLK3_50	PIN_N14	50 MHz clock input	1.5V
ADC_CLK_10	PIN_M9	10 MHz clock input	3.3V

3.4 Peripherals Connected to the FPGA

This section describes the interfaces connected to the FPGA. User can control or monitor different interfaces with user logic from the FPGA.

3.4.1 User Push-buttons, Switches, LEDs

The board has five push-buttons connected to the FPGA, as shown in Figure 3-11. MAX 10 devices support Schmitt trigger input on all I/O pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signal with slow edge rate and act as switch debounce in Figure 3-12 for the push-buttons connected.

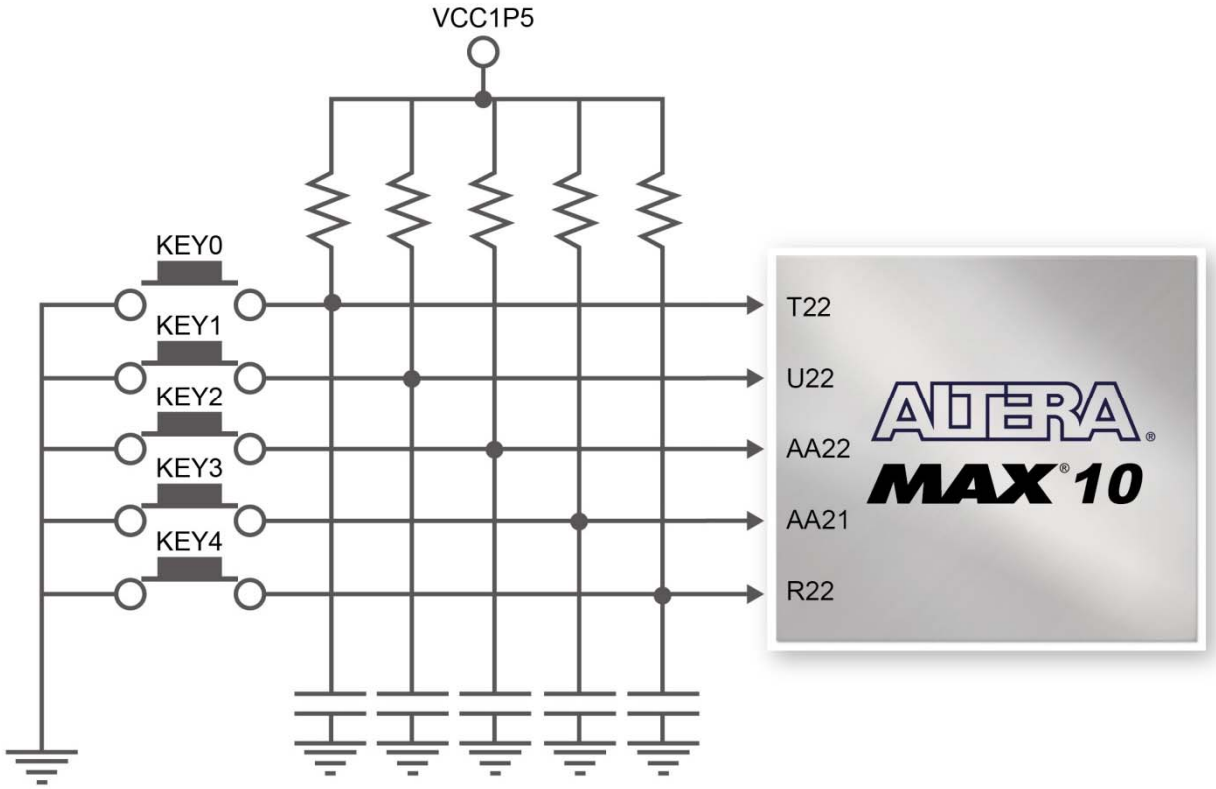

Figure 3-11 Connections between the push-buttons and the MAX 10 FPGA

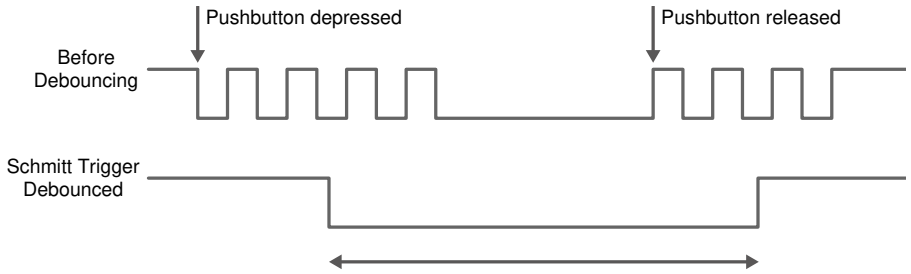

Figure 3-12 Switch debouncing

There are two ten switches connected to the FPGA, as shown in **Figure 3-13**. These switches are used as level-sensitive data inputs to a circuit. Each switch is connected directly and individually to the FPGA. When the switch is set to the DOWN position (towards the edge of the board), it generates a low logic level to the FPGA. When the switch is set to the UP position, a high logic level is generated to the FPGA.

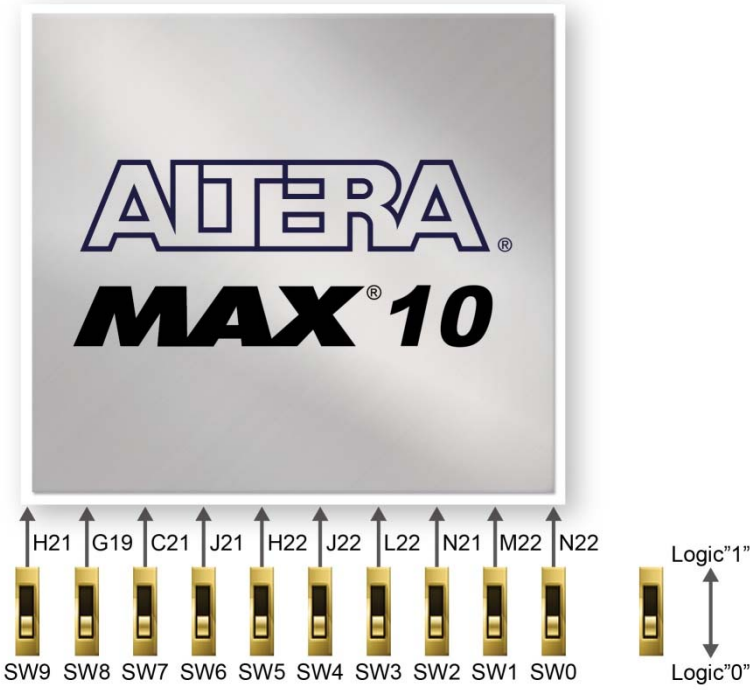

Figure 3-13 Connections between the slide switches and the MAX 10 FPGA

There are also ten user-controllable LEDs connected to the FPGA. Each LED is driven directly and individually by the MAX 10 FPGA; driving its associated pin to a high logic level or low level to turn the LED on or off, respectively. **Figure 3-14** shows the connections between LEDs and MAX 10 FPGA. **Table 3-3**, **Figure 3-14** and **Table 3-9** list the pin assignment of user push-buttons, switches, and LEDs.

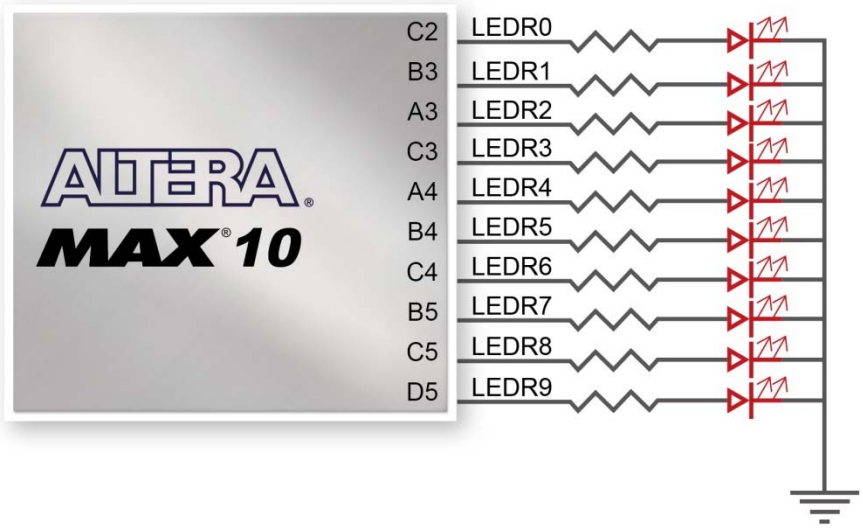

Figure 3-14 Connections between the LEDs and the MAX 10 FPGA

Table 3-3 Pin Assignment of Push-buttons

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
KEY[0]	PIN_T22	Push-button[0]	1.5V
KEY[1]	PIN_U22	Push-button[1]	1.5V
KEY[2]	PIN_AA22	Push-button[2]	1.5V
KEY[3]	PIN_AA21	Push-button[3]	1.5V
KEY[4]	PIN_R22	Push-button[4]	1.5V

Table 3-4 Pin Assignment of Slide Switches

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
SW[0]	PIN_N22	Slide Switch[0]	1.5V
SW[1]	PIN_M22	Slide Switch[1]	1.5V
SW[2]	PIN_N21	Slide Switch[2]	1.5V
SW[3]	PIN_L22	Slide Switch[3]	1.5V
SW[4]	PIN_J22	Slide Switch[4]	1.5V
SW[5]	PIN_H22	Slide Switch[5]	1.5V
SW[6]	PIN_J21	Slide Switch[6]	1.5V
SW[7]	PIN_C21	Slide Switch[7]	1.5V
SW[8]	PIN_G19	Slide Switch[8]	1.5V
SW[9]	PIN_H21	Slide Switch[9]	1.5V

Table 3-5 Pin Assignment of LEDs

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
LEDR[0]	PIN_C2	LEDR [0]	3.3V
LEDR[1]	PIN_B3	LEDR [1]	3.3V
LEDR[2]	PIN_A3	LEDR [2]	3.3V

LEDR[3]	PIN_C3	LEDR [3]	3.3V
LEDR[4]	PIN_A4	LEDR [4]	3.3V
LEDR[5]	PIN_B4	LEDR [5]	3.3V
LEDR[6]	PIN_C4	LEDR [6]	3.3V
LEDR[7]	PIN_B5	LEDR [7]	3.3V
LEDR[8]	PIN_C5	LEDR [8]	3.3V
LEDR[9]	PIN_D5	LEDR [9]	3.3V

3.4.2 7-segment Displays

The MAX 10 NEEK has two 7-segment displays. These displays are paired to display numbers in various sizes. Figure 3-15 shows the connection of seven segments (common anode) to pins on MAX 10 FPGA. The segment can be turned on or off by applying a low logic level or high logic level from the FPGA, respectively.

Each segment in a display is indexed from 0 to 6, with corresponding positions given in Figure 3-15. Table 3-4 shows the pin assignment of FPGA to the 7-segment displays.

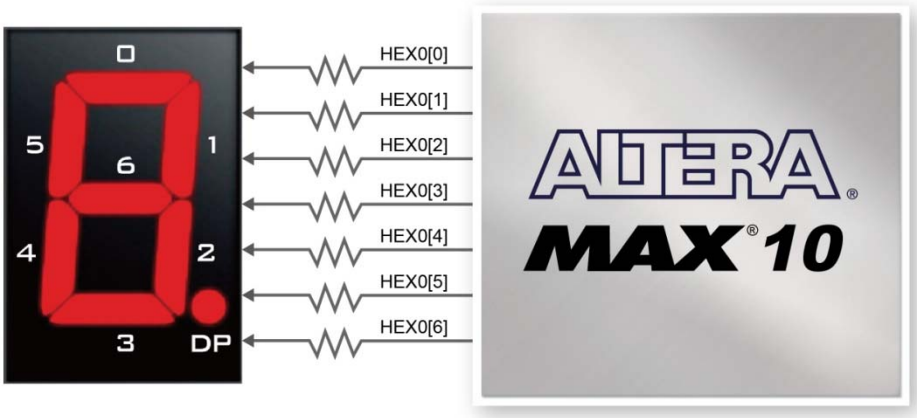

Figure 3-15 Connections between the 7-segment display HEX0 and the MAX 10 FPGA

Table 3-4 Pin Assignment of 7-segment Displays

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
HEX0[0]	PIN_D6	Seven Segment Digit 0[0]	3.3V
HEX0[1]	PIN_A5	Seven Segment Digit 0[1]	3.3V
HEX0[2]	PIN_C6	Seven Segment Digit 0[2]	3.3V
HEX0[3]	PIN_A6	Seven Segment Digit 0[3]	3.3V
HEX0[4]	PIN_F7	Seven Segment Digit 0[4]	3.3V
HEX0[5]	PIN_D7	Seven Segment Digit 0[5]	3.3V

HEX0[6]	PIN_B7	Seven Segment Digit 0[6]	3.3V
HEX1[0]	PIN_C7	Seven Segment Digit 1[0]	3.3V
HEX1[1]	PIN_C8	Seven Segment Digit 1[1]	3.3V
HEX1[2]	PIN_D8	Seven Segment Digit 1[2]	3.3V
HEX1[3]	PIN_D10	Seven Segment Digit 1[3]	3.3V
HEX1[4]	PIN_E10	Seven Segment Digit 1[4]	3.3V
HEX1[5]	PIN_H11	Seven Segment Digit 1[5]	3.3V
HEX1[6]	PIN_E6	Seven Segment Digit 1[6]	3.3V

3.4.3 Power Monitor

The MAX 10 NEEK has implemented three power monitor chips to monitor the FPGA core power and VCCIO power voltage and current. Figure 3-16 shows the connection between the power monitor chip and the MAX 10 FPGA. Through the I2C serial interface, the power monitor can be configured to measure remote voltage and remote current. Programmable calibration value, conversion times, and averaging, combined with an internal multiplier, enable direct readouts of current in amperes and power in watts. Table 3-5 shows the pin assignment of power monitor I2C bus.

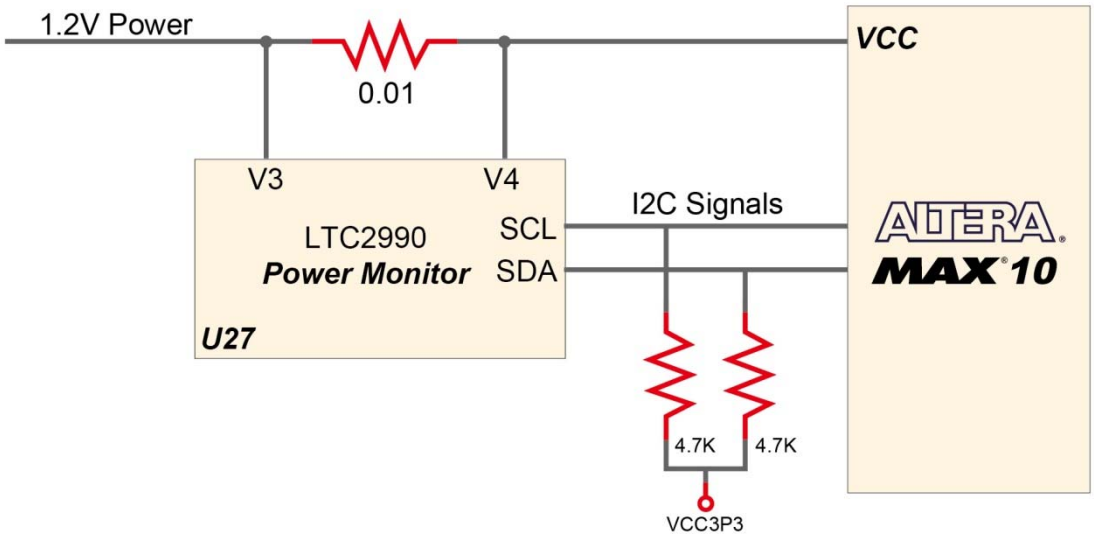

Figure 3-16 Connections between the power monitor chip and the MAX 10 FPGA

Table 3-5 Pin Assignment of Power Monitor I2C bus

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
PM_I2C_SCL	PIN_E8	Power Monitor SCL	3.3V
PM_I2C_SDA	PIN_E9	Power Monitor SDA	3.3V

3.4.4 2x6 TMD Expansion Header

The board has one 2x6 TMD (Terasic Mini Digital) expansion header. The TMD header has 8 digital GPIO user pins connected to the MAX 10 FPGA, two 3.3V power pins and two ground pins. There are two Transient Voltage Suppressor diode arrays used to implement ESD protection for 8 GPIO user pins..

Figure 3-17 shows the connection between the TMD header and MAX 10 FPGA. Table 3-9 shows the pin assignment of 2x6 TMD header.

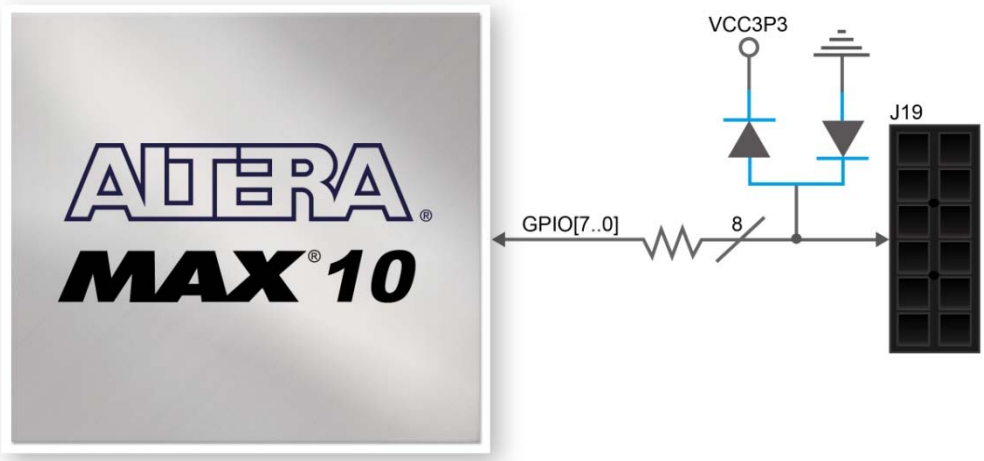

Figure 3-17 Connections between the 2x6 TMD header and MAX 10 FPGA

Table 3-6 Pin Assignment of 2x6 TMD Header

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
GPIO[0]	PIN_Y17	GPIO Connection [0]	3.3V
GPIO[1]	PIN_AA17	GPIO Connection [1]	3.3V
GPIO[2]	PIN_V16	GPIO Connection [2]	3.3V
GPIO[3]	PIN_W15	GPIO Connection [3]	3.3V
GPIO[4]	PIN_AB16	GPIO Connection [4]	3.3V
GPIO[5]	PIN_AA16	GPIO Connection [5]	3.3V
GPIO[6]	PIN_Y16	GPIO Connection [6]	3.3V
GPIO[7]	PIN_W16	GPIO Connection [7]	3.3V

3.4.5 24-bit Audio CODEC

The MAX 10 NEEK offers high-quality 24-bit audio via the Texas Instruments TLV320AIC3254 audio CODEC (Encoder/Decoder). This chip on MAX 10 NEEK supports, line-in, line-out and microphone-in ports with adjustable sample rate from 8kHz to 192kHz. The connection of the audio

circuitry to the FPGA is shown in Figure 3-18, and the associated pin assignment to the FPGA is listed in Table 3-7. More information about the TLV320AIC3254 CODEC is available in its datasheet, which can be found on the manufacturer's website, or in the directory \MAX10_NEEK_datasheets\Audio CODEC of DECA System CD.

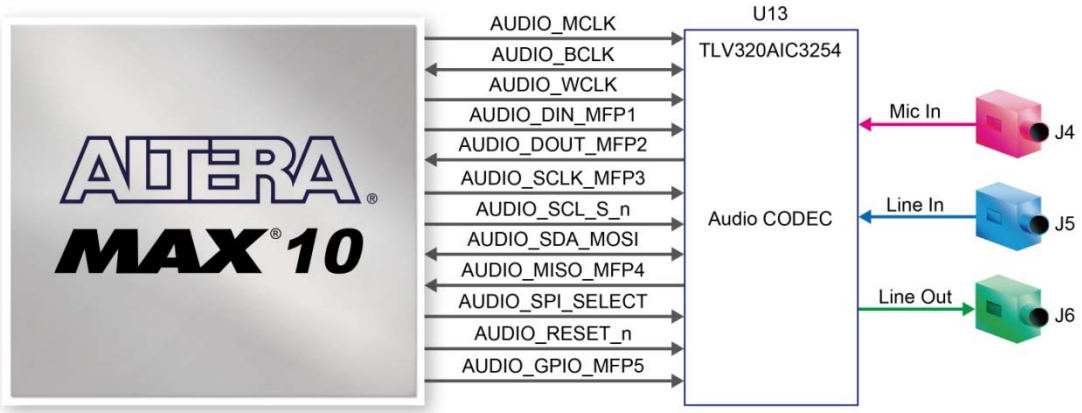

Figure 3-18 Connections between the FPGA and audio CODEC

Table 3-7 Pin Assignment of Audio CODEC

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
AUDIO_MCLK	PIN_J11	Master output Clock	2.5V
AUDIO_BCLK	PIN_J12	Audio serial data bus (primary) bit clock	2.5V
AUDIO_WCLK	PIN_H12	Audio serial data bus (primary) word clock	2.5V
AUDIO_DIN_MFP1	PIN_J13	Audio serial data bus data output/digital microphone output	2.5V
AUDIO_DOUT_MFP2	PIN_H13	Audio serial data bus data input/general purpose input	2.5V
AUDIO_SCLK_MFP3	PIN_H14	SPI serial Clock/headphone-detect output	2.5V
AUDIO_SCL_SS_n	PIN_F15	I2C Clock/SPI interface mode chip-select signal	2.5V
AUDIO_SDA_MOSI	PIN_F16	I2C Data/SPI interface mode serial data output	2.5V
AUDIO_MISO_MFP4	PIN_E13	Serial data input/General purpose input	2.5V
AUDIO_SPI_SELECT	PIN_E14	Control mode select pin	2.5V
AUDIO_RESET_n	PIN_D13	Reset signal	2.5V
AUDIO_GPIO_MFP5	PIN_D14	General Purpose digital IO/CLKOUT input	2.5V

3.4.6 Two Analog Input SMA Connectors

The MAX 10 NEEK board implements two analog input SMA connectors. The analog inputs are amplified and translated by Texas Instruments INA159 gain of 0.2 level translation difference amplifier, then the amplifier's outputs are fed to dedicated single-ended analog input pins for MAX 10 build-in ADC1 and ADC2 respectively. With the amplifiers, the analog input of two SMAs