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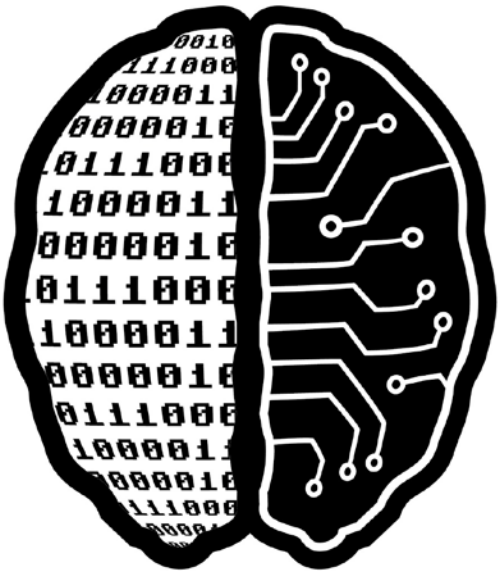

parallella

Parallella-1.x

Reference Manual

Revision History

Version	Comments
0.13.2.13	Initial release
1.13.6.24	Updated PEC_POWER Pin outs Part Numbers Added + Document Links Changed flash to 128Mb Replaced 5V DC/USB power mux with pin header Changed power sub-system Epiphany now uses 1.8V IO voltage Added UART 2-pin header Changed license to creative common
1.13.7.27	Added UART interface back to PEC_POWER Added test points for SYS_5V and 1P0V Added 2-pin header for 5V mounting hole
14.04.15	Removed second USB port “PC connection” as supported feature No longer supporting the USB-OTG (only host mode)
14.09.09	Removed reference to reset button Remove reference to 2nd USB port Added numerous tables, design details

Related Documents

Epiphany Architecture Reference Manual:

http://www.adapteva.com/docs/epiphany_arch_ref.pdf

Epiphany SDK Reference Manual:

http://www.adapteva.com/docs/epiphany_sdk_ref.pdf

Epiphany-III Datasheet:

http://www.adapteva.com/docs/e16g301_datasheet.pdf

Epiphany-IV Datasheet:

http://www.adapteva.com/docs/e64g401_datasheet.pdf

Software Repositories:

Parallella Hardware and Software Repository

https://github.com/parallella

Epiphany SDK Software Repository

https://github.com/adapteva

SD Card Images:

ftp://ftp.parallella.org

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1 Overview

The Parallella board is a high performance computing platform based on a dual-core ARM-A9 Zynq System-On-Chip and Adapteva's Epiphany multicore coprocessor. Current commercially available models:

Model	P1600	P1601	P1602
Mnemonic	"Microserver"	"Desktop"	"Embedded"
Host Processor	Xilinx Zynq Dual-core ARM A9 XC7Z010		Xilinx Zynq Dual-core ARM A9 XC7Z020
Coprocessor	Epiphany 16-core CPU E16G301		
Memory	1 GB DDR3		
Ethernet	Gigabit Ethernet		
Boot Flash	128Mb QSPI Flash		
Power	5V DC		
Storage	Micro-SD		
USB	No	USB 2.0 Host Port	
HDMI	No	Micro HDMI	
GPIO Pins	0	24	48
eLink Connectors	0	2	2
FPGA Logic	28K Logic Cells 80 DSP Slices	28K Logic Cells 80 DSP Slices	80K Logic Cells 220 DSP slices
Weight	1.3 oz (36 grams)	1.4 oz (38 grams)	
Size	3.5" x 2.1" x 0.625" (90mmx55mmx18mm)		
SKU	P1600-DKxx	P1601-DKxx	P1602-DKxx
HTS Code (Schedule B)	8471.41.0150	8471.41.0150	8471.41.0150

Table 1: Parallella Feature Summary

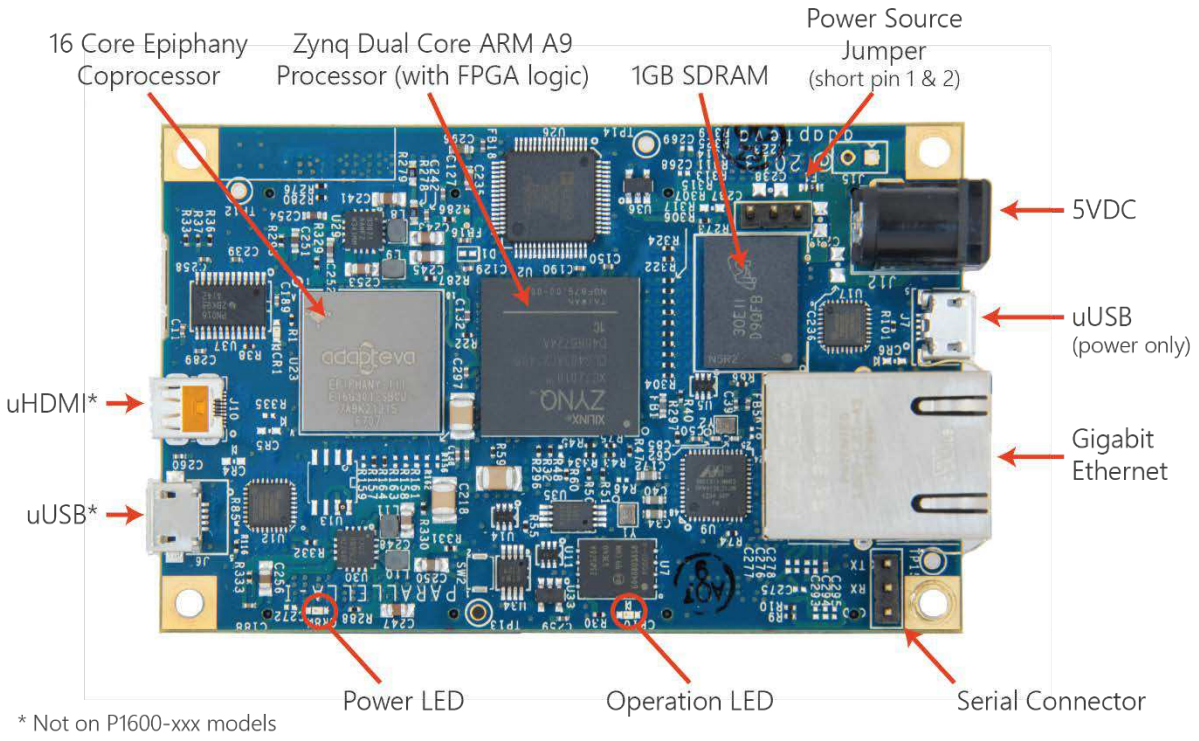


Figure 1: The Parallella Board (top view)

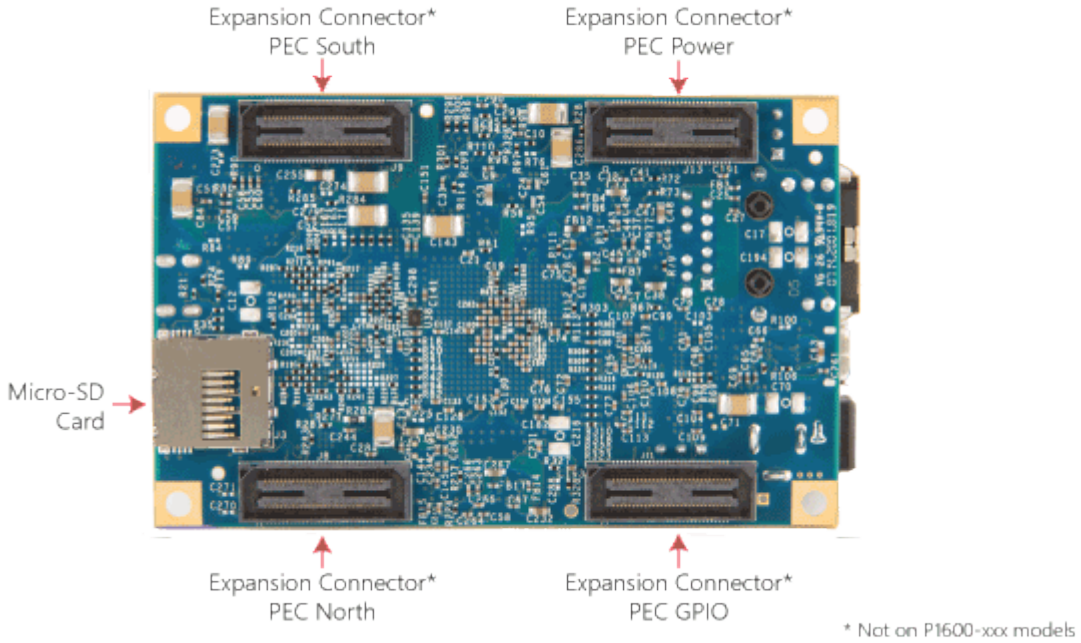


Figure 2: The Parallella Board (bottom view)

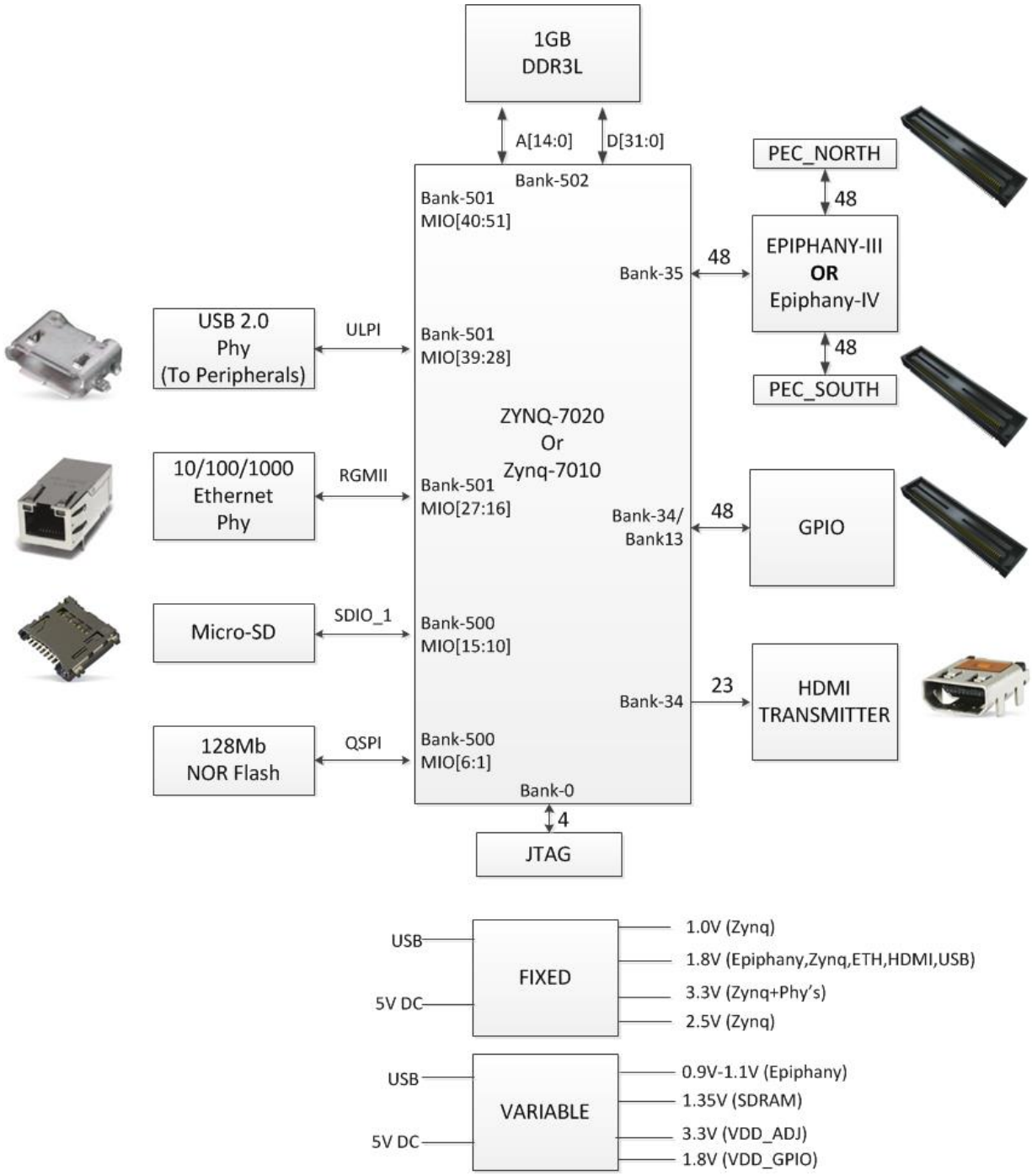


Figure 3: Zynq Connectivity Diagram

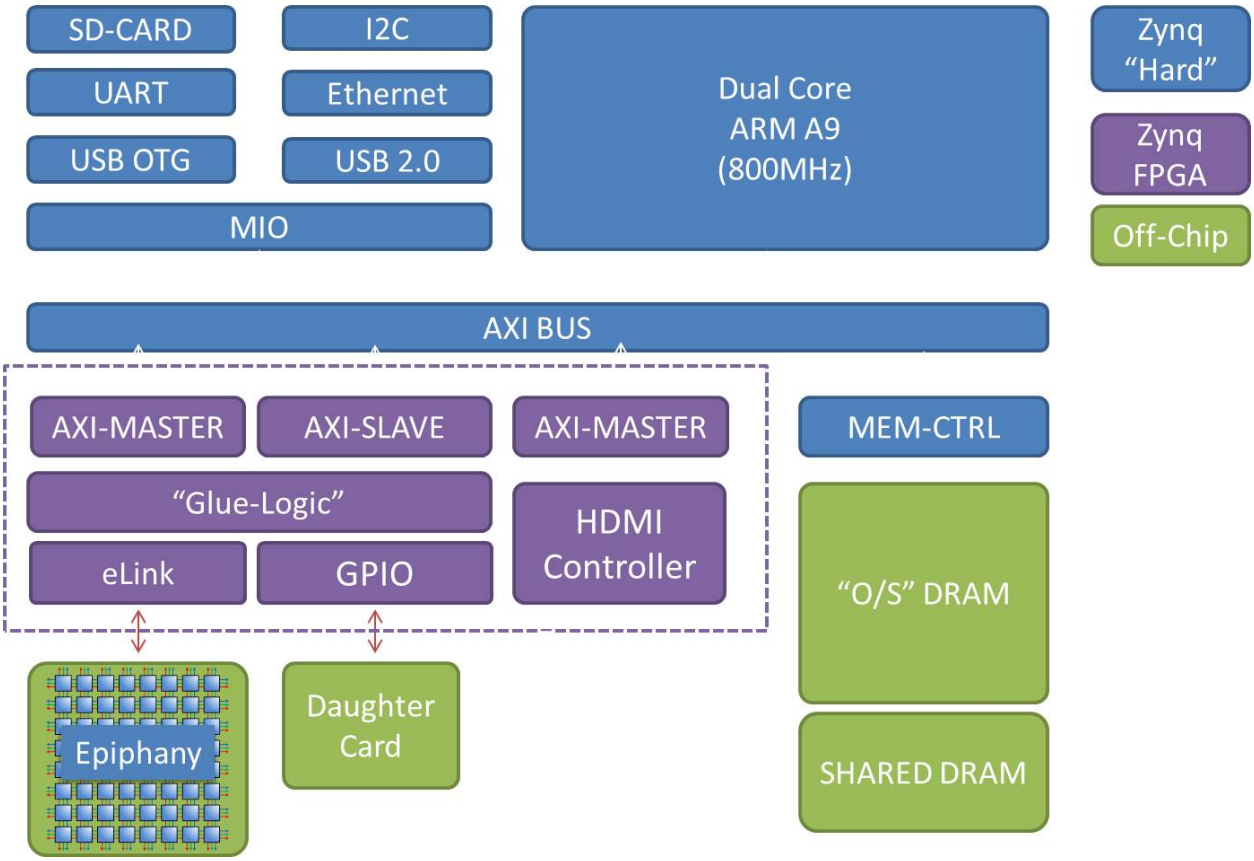
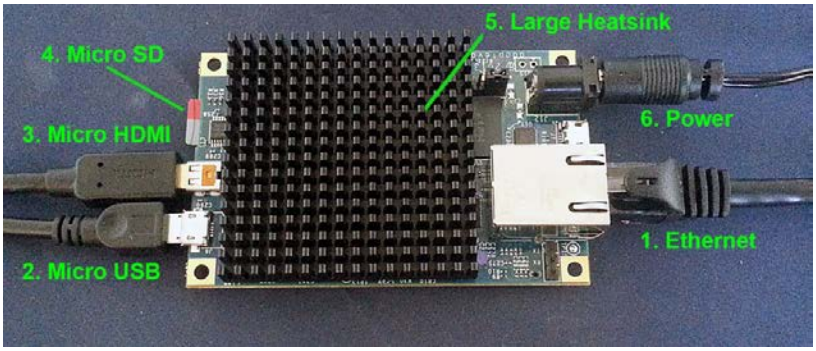


Figure 4: Parallella High Level Architecture

2 Quick Start Guide

This section is a summary of the quick start guide is found at www.parallella.org/quick-start



Step1: Ensure that you have the required accessories

- A high quality 2000mA rated 5V DC power supply with 5.5mm OD / 2.1mm ID center positive polarity plug.
- An ethernet cable
- A fan (required for boards sold before July 10th, 2014, recommended for all others)
- A micro HDMI to HDMI cable (not needed for headless option)
- A USB male Micro-B to female Standard-A cable (not needed for headless option)

Step 2: Create a bootable micro-SD card

Burn a fresh Micro-SD card using the latest distribution.

- Instructions for creating an SD card

Note: Burn a fresh SD card even if you were shipped a pre-programmed micro-SD card!

Step 3: Familiarize yourself with known issues

- The board does get hot so you have to take precautions to cool the board properly. Before letting the board run for hours, you must ensure that the board doesn't overheat. (preferably by using the 'xtemp' utility.)
- Boards used without a fan must be placed vertically.
- The Parallella is sensitive to static discharge and must be handled appropriately.
- If you were shipped a board before March 1st, 2014, then you must use a conforming powered USB hub.
- If you were shipped a board before July 10th, 2014 then you must use a fan with the board. (we do still recommend a fan for all customers, especially if you are going to push the performance of the board)

Step 4. Connect peripherals, fit the heat-sink and apply power

- Connect the cables as indicated by #1-4 in the picture above
- Attach a heatsink to the Zynq device (#5 in right hand picture) OR install the new large heatsink onto the Parallella board
- Make sure a fan is directed at the board if required. A fan is required when using the small heatsink (right hand picture above). With the large heatsink (left hand picture above) the board will function in normal conditions without requiring a fan, depending on your usage. Monitor the temperature using a utility such as xtemp, and keep the chip temp below 70 degrees Celsius.
- Apply power (#6 in picture)

Step 5: Build and run a program

The system will boot and a login screen will appear.

Login with the username `linaro` and password `linaro`.

3 Feature Descriptions

3.1 Introduction

The Parallella-1.x board uses the components listed in the table below.

Device	Part Number (and datasheet link)
CPU	Zynq™-7000 AP SoC
Epiphany	E16G301 and E64G401
Eth PHY	88E1318
USB PHY	USB3320C-EZK-TR
HDMI PHY	ADV7513BSWZ
SDRAM	MT41K256M32SLD
Flash	N25Q128A13EF840E
PMIC #1	ISL9307
PMIC #2	ISL9305

Table 2: Parallella IC summary

3.2 CPU

The central processor on the Parallella board is the Zynq™-7000 AP SoC. The Zynq represents a new class of processor product which combines an industry-standard ARM® dual-core Cortex™-A9 MPCore™ processing system with Xilinx 28nm programmable logic. The Zynq SoC includes the following set of features:

Dual-core ARM® Cortex™-A9 CPU:

- Coherent multiprocessor support
- ARMv7-A architecture
- 32 KB Level 1 4-way set-associative instruction/data caches (independent for each CPU)
- 512 KB 8-way set-associative Level 2 cache shared between CPUs
- TrustZone® security
- Jazelle® RCT execution Environment Architecture
- NEON™ media-processing engine
- Single and double precision Vector Floating Point Unit (VFPU)
- CoreSight™ and Program Trace Macrocell (PTM)
- Three watchdog timers, one global timer, two triple-timer counters

I/O Peripherals and Interfaces:

- 10/100/1000 tri-speed Ethernet MAC peripherals GMII, RGMII, and SGMII interfaces
- Two USB 2.0 OTG peripherals
- Two full CAN 2.0B compliant CAN bus interfaces
- Two SD/SDIO 2.0/MMC3.31 compliant controllers
- Two full-duplex SPI ports with three peripheral chip selects
- Two high-speed UARTs (up to 1 Mb/s)
- Two master and slave I2C interfaces
- 8-Channel DMA Controller with scatter/gather capability
- JTAG port for ARM debugging and FPGA programming
- 12 bit ADC input
- On-chip voltage and temperature sensing

Programmable Logic:

- LVCMOS, LVDS, and SSTL signaling with 1.2V to 3.3V IO
- Easily accessible from ARM cores through AXI bus(master or slave)
- Up to 125 programmable IO pins (Z-7020)
- Up to 85K programmable logics cells (Z-7020)
- Up to 560 KB distributed RAM (Z-7020)
- Up to 220 DSP slice and (Z-7020)

The Parallella board can be built with two different pin compatible Zynq devices: Zynq Z-7010 or the Zynq Z-7020. The major differences between the Z-7010 and Z-7020 are summarized in Table 4:

	Z-7010	Z-7020
Programmable Logic Cells	28K	85K
Look-Up Tables	17,600	53,200
Flip-flops	35,200	106,400
Extensible Block RAM	240KB	560KB
Programmable DSP Slices	80	220
Bank-13 IO Pins	No	Yes

Table 3: Zynq Feature Summary

3.3 Epiphany Coprocessor

The Parallella-16 includes the E16G301 device with 16 CPU cores and the Parallella-64 includes the E64G401 device with 64 CPU cores. Both devices have the following basic features:

Epiphany Core (eCore):

- 32-bit dual-issue superscalar RISC architecture
- Quad-bank 32KB local single cycle access memory
- Floating point instruction set (IEEE754)
- 64-entry register file
- Dual channel DMA engine
- Two 32-bit timers
- Nested interrupt controller
- Memory protection unit
- Debug unit

Network-On-Chip (eMesh):

- Three separate networks:
    - rMesh for read transactions
    - xMesh for off-chip write transactions
    - cMesh for on-chip write transactions
- "API-less" network that processes regular load/store transactions
- All transactions are complete and atomic 104 bit transactions (32 bit address, 64 bit data, and 8 control bits)
- Round robin arbitration at every mesh node
- Mesh network extends off chip enabling glue-less multi-chip design

Chip-To-Chip Links (eLink):

- North, east, west, south links for connecting to other Epiphany chips, FPGAs, or ASICs
- Source synchronous LVDS links with transmit clock aligned in the middle of the data eye
- Dual data rate communication (positive and negative edge transfers)
- Max transfer of 2 bytes transferred in and out simultaneously per link per clock cycle
- Automatic bursting for sequential 64-bit write transactions

3.4 SDRAM

1GB 32-bit wide DDR3L SDRAM

3.5 Flash

128Mb QSPI Flash Memory for boot code

3.6 Gigabit Ethernet

10/100/1000 Ethernet, RJ45 connector with magnetics.

3.7 USB 2.0 Host Port

Connects to peripheral devices such as mice, keyboard, camera, etc.

3.8 Micro SD

Primary boot source and main Parallella board storage medium.

3.9 HDMI Port

A high quality connection to modern DVI/HDMI monitors and TVs through a micro-HDMI connector.

3.10 LED Indicators

- A green LED controlled by the Zynq GPIO pin.
- A red LED controlled by the Epiphany flag pin
- Two LEDs on the RJ45. The left LED indicates link speed. (amber=1Gb, green=100Mb, off=10Mb). The right indicates that there is activity on the port.

3.11 Serial Port

A three-pin header for 3.3V UART output from the Zynq.

3.12 I2C

A 5V I2C interface is available through the PEC_POWER connector.

3.13 Audio

Audio is available through the HDMI connector and through the SPDIF pin on the PEC_POWER connector.

3.14 Analog Input

A differential analog input is available on the PEC_POWER connector that is sampled by the Zynq built in Analog to Digital Converter.

3.15 JTAG Debugging

FPGA programming and debugging of programs running on the Zynq is possible through the JTAG pins on the PEC_POWER connector.

3.16 Powering the board

The Parallella should be powered through a stable 5V/2A power supply. The following methods are available for connecting a 5V supply. Current consumption for the Parallella board can be as low as 0.3A but can reach 1.5A when fully loaded.

Recommended Methods (choose one only):

- **J12:** 5.5mm OD / 2.1mm ID center positive barrel connector (place jumper on J14 in 1-2 position)
- **J7:** micro-USB connector (place jumper on J14 in 2-3 position)

Experimental (at your own risk):

- **PTH1:** Mounting hole. Need to install/solder and short J15
- **J13:** Pins 1 and 2 of the PEC_POWER connector

3.17 Parallella On-Board Power Management

The on-board power rails are regulated by the Intersil PMICs ISL9307 and ISL9305 as shown in the following Figure.

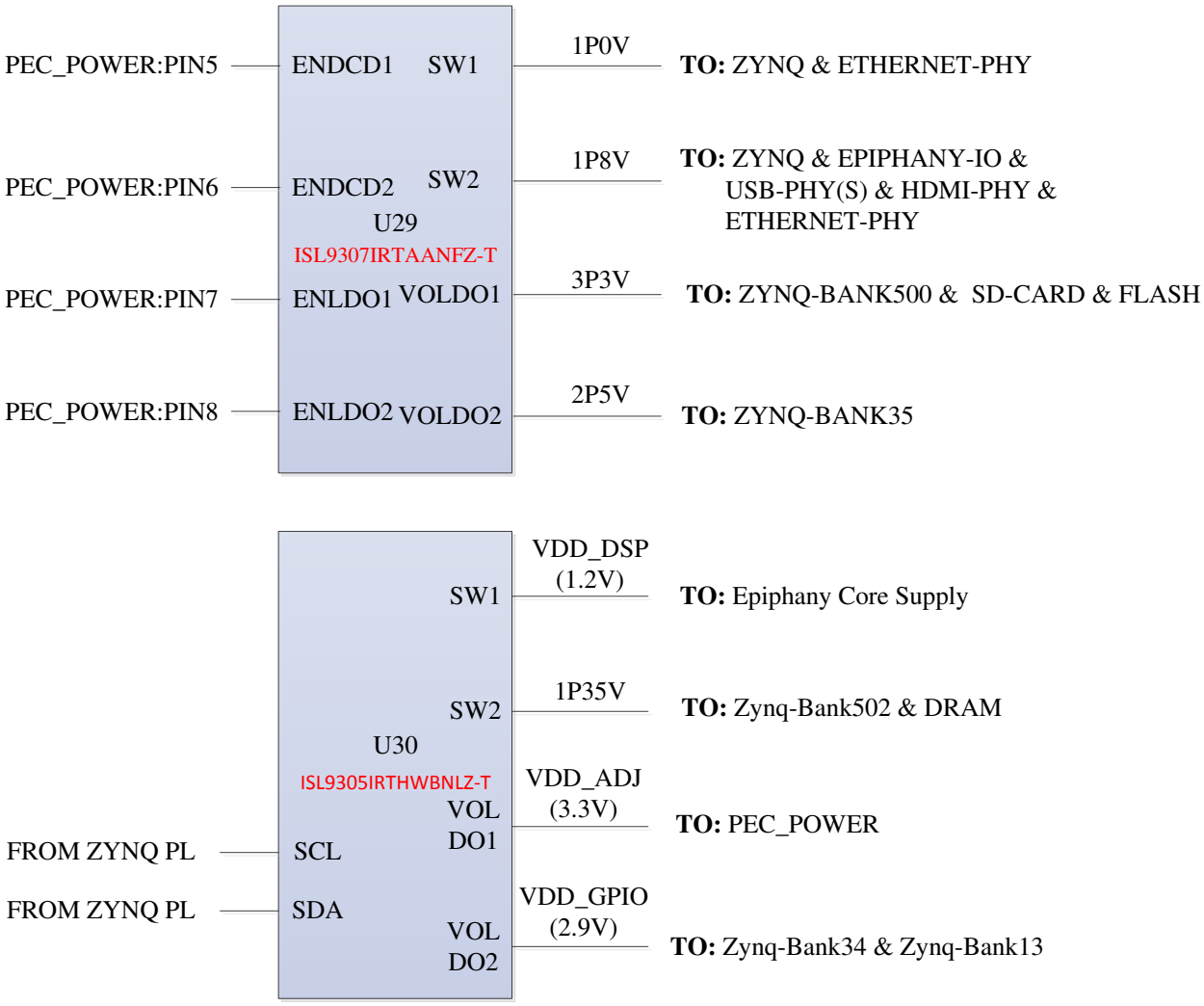


Figure 5: Power Management

All four voltage rail outputs on the ISL9305 can be set by programming the appropriate registers within the chip using the I2C interface. The Parallella on-board flash contains the appropriate programming sequence to set the VDD_DSP rail to 1.0V and the VDD_GPIO rail to 2.5V automatically at boot time.

3.18 Parallella Supply Outputs

The Parallella can power expansion/daughter cards directly using the PEC_POWER connector.

The following voltages are available at the PEC_POWER connector:

- 5V
- 3.3V
- 2.5V
- VADJ
- VAD_GPIO
- 1.8V
- 1.35V
- 1.0V (Zynq)
- 1.0V (Epiphany)

The two on-board PMICs can deliver 1.5A on each step-down converter output and 300MA on each general purpose LDO output. The amount of current drawn by the Parallella board will depend on the level of activity on the board and the amount of current left over for the expansion card is yet to be characterized.

NOTE: At this time, the PEC_POWER feature should be considered experimental. The safest power solution for expansion cards is to: 1.) Have a completely independent power sub system or 2.) To use the 5V PEC_POWER rail.

Each one of the Parallella rails can also be powered directly from the PEC_POWER connector instead of from the on board power management ICs. Each rail to be driven from an external connector would first need to be powered down appropriately to avoid damaging the circuitry. To disable one of the ISL7307 outputs, pull down the corresponding REG_EN* signal available on the PEC_POWER connector. To disable one of the ISL9305 outputs, program the appropriate registers using the I2C interface.

NOTE: There WILL be permanent damage to the board the power rails are driven incorrectly. Please exercise extreme caution!

3.19 Parallella Expansion Connectors

The Parallella board has four expansions connectors placed on the opposite edges of the bottom side of the board shown in Figure 2. For exact connector and placement information, please refer to the Parallella mechanical drawings. The following figure shows the expansion connector placements as seen from the bottom side of the board.

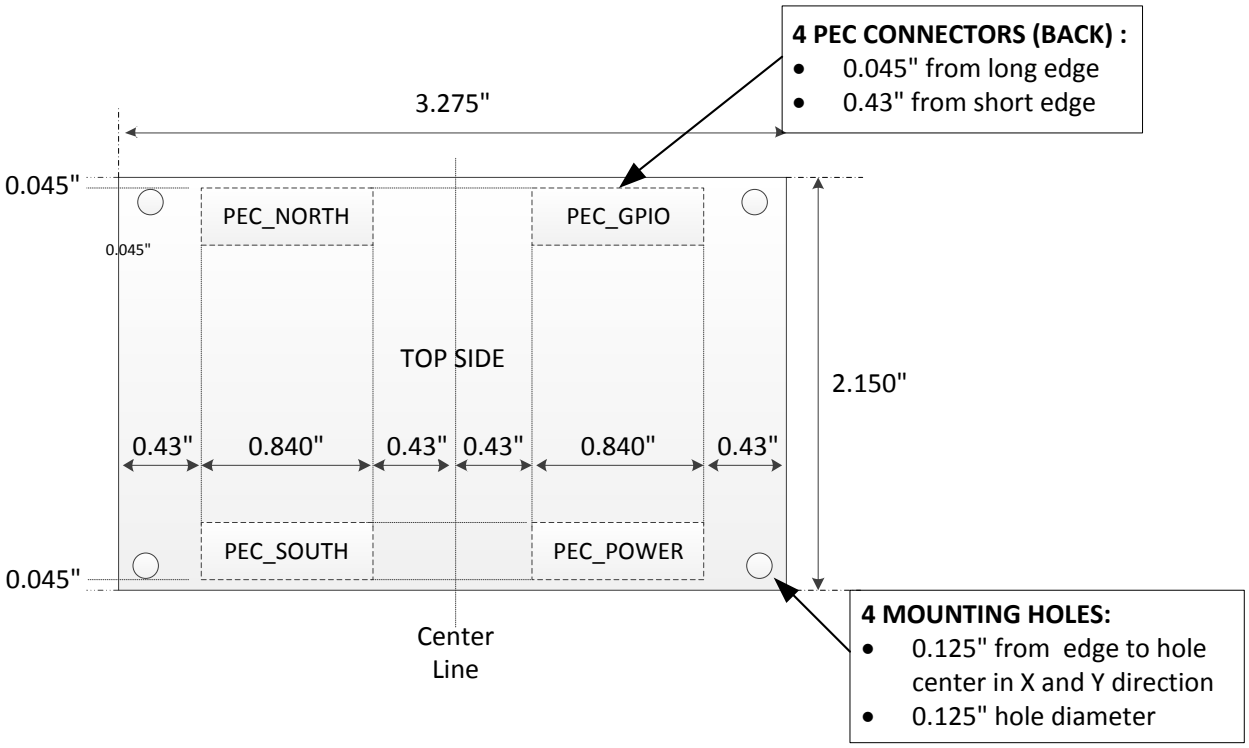


Figure 6: PEC Placement Diagram

The Parallella Expansion Connectors uses the 60 pin BSH-030-01-FDA high speed connector from Samtec. The corresponding mating connector to be placed on the expansion card is BTH-030-01-FDA. The complete data sheets can be found at:

https://www.samtec.com/technical-specifications/Default.aspx?SeriesMaster=BSH

A complete characterization report for the Samtec connectors can be found at:

http://www.samtec.com/Documents/WebFiles/TestRpt/172630_report_rev_2_qua.pdf

Connector	Functions
PEC_POWER	Power and control signal expansion connector
PEC_FPGA	Zynq programmable logic expansion connector
PEC_NORTH	Epiphany north link expansion connector
PEC_SOUTH	Epiphany south link expansion connector

Figure 7: Parallella Expansion Connectors (PEC)

The four symmetrically placed connectors allow for robust mating of expansion cards and the Parallella board using matching BTH-030-01-FDA connectors. As shown in Figure 5, it is possible to connect a single full length credit card sized expansion cards or two half-length expansion cards. The left side shows two half-length expansion boards (pink/green transparent) connected to the backside of the Parallella board

and the right side shows a full length (blue transparent) expansion board connected to the backside of the Parallella board.

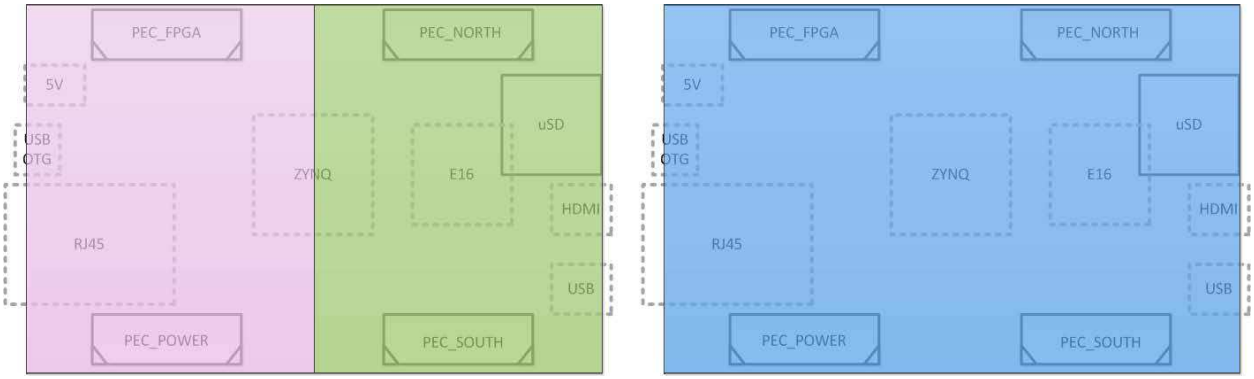


Figure 8: Daughter Card Configurations

3.20 Mounting Holes

The board has four symmetrically placed mounting holes, one in each corner. The mounting holes have a diameter of 0.125”.

Three of the mounting holes are connected to ground while the fourth mounting hole is floating by default. This floating mounting hole can be connected to the 5V supply as a build or solder option, allowing power to be easily applied to a stack of Parallella boards without the need for extensive 5V DC cabling.

4 Parallella System Architecture

4.1 Zynq Memory Map

The following Table shows the hard-coded memory architecture of the Zynq architecture most relevant to the Parallella architecture. For a complete description of the Zynq of the memory architecture, please refer to the Architecture Reference manual for the Zynq.

Address Start	Address End	Size	Function	Note
0x0010_0000	0x3FFF_FFFF	1GB	DRAM	Accessible to all interconnect masters
0x4000_0000	0x7FFF_FFFF	1GB	PL	Custom logic address range
0x8000_0000	0xBFFF_FFFF	1GB	PL	Epiphany address range
0xFC00_0000	0xFCFF_FFFF	16MB	FLASH	Quad-SPI linear address for linear mode
0xFFFC_0000	0xFFFF_FFFF	252KB	OCM	OCM upper address range

Figure 9: Zynq Memory Map

The ARM communicates with programmable logic, GPIO connected to the programmable logic, and the Epiphany by accessing the memory ranges shown in the table.

The Epiphany 32-bit memory space is mapped into the Zynq memory space allowing for easy sharing of data and resources between the ARM and the Epiphany. The Epiphany address range is a matter of convention and depends on the appropriate AXI master and slave interfaces being implemented within the programmable logic on the Zynq.

4.2 Epiphany Memory Map

The Epiphany chip is situated within a 1GB section within the Zynq host processor memory map. The offset within the 1GB space occupied by an Epiphany coprocessor is set by the ROWID and COLID pins on the Epiphany chip. The ROWID and COLID can be individually set on boards through the PEC_POWER connector enabling direct board to board connection through the PEC_NORTH and PEC_SOUTH connectors. By default the address locations of the Epiphany cores on Parallella-16 are as shown in the Table below.

Core Number	Start Address	End Address	Size
(32,8)	80800000	80807FFF	32KB
(32,9)	80900000	80907FFF	32KB
(32,10)	80A00000	80A07FFF	32KB
(32,11)	80B00000	80B07FFF	32KB
(33,8)	84800000	84807FFF	32KB
(33,9)	84900000	84907FFF	32KB
(33,10)	84A00000	84A07FFF	32KB
(33,11)	84B00000	84B07FFF	32KB
(34,8)	88800000	88807FFF	32KB
(34,9)	88900000	88907FFF	32KB
(34,10)	88A00000	88A07FFF	32KB
(34,11)	88B00000	88B07FFF	32KB
(35,8)	8C800000	8C807FFF	32KB
(35,9)	8C900000	8C907FFF	32KB
(35,10)	8CA00000	8CA07FFF	32KB
(35,11)	8CB00000	9CB07FFF	32KB

Figure 10: Epiphany Memory Map

4.3 Epiphany Specific FPGA Resources

Developers that want leverage the Epiphany co-processors should use the Parallella programmable logic reference design with minimal changes for best results. The following registers must be accessible by the Epiphany drivers from the ARM for correct operation.

Register	Address	Bits	Details
ESYSCONFIG	0x808f0f00	[0]	Enable transaction timeout on read from Zynq
		[2:1]	00: Filter disable 01: Inclusive range. Block transactions inside REG_FILTERL and REG_FILTERH range) 10: Exclusive range. Block transactions outside REG_FILTERL and REG_FILTERH range) 11: Reserved
		[3]	Epiphany eLink enable 0:→ 1.) Forces RESET_N to zero, 2.) turns off the epiphany input clock cclk 3.) and turns off the elink TX/RX in the FPGA 1:→ 1.) Turns on epiphany clock, 2.) forces RESET_N to one (“out of reset”) 3.) Turns on elink RX/TX in the FPGA
		[27:4]	Reserved
		[31:28]	Epiphany transaction control mode
ESYSRESET	0x808f0f04		A write transaction to this register asserts a reset signal to Epiphany and the eLink logic within the Zynq.