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Freescale Semiconductor
Data Sheet: Technical Data

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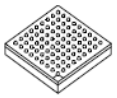
P2040

P2040 QorIQ Integrated Processor Hardware Specifications



FCPBGA–780
23 mm x 23 mm

The P2040 QorIQ integrated communication processor combines four Power Architecture® processor cores with high performance data path acceleration logic and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and aerospace applications.

This chip can be used for combined control, data path, and application layer processing in routers, switches, base station controllers, and general-purpose embedded computing. Its high level of integration offers significant performance benefits compared to multiple discrete devices, while also greatly simplifying board design.

This chip includes the following functions and features:

- Four e500mc Power Architecture cores
  - Three levels of instructions: User, supervisor, and hypervisor
  - Independent boot and reset
  - Secure boot capability
- CoreNet fabric supporting coherent and non-coherent transactions amongst CoreNet endpoints
- One 1 MB CoreNet platform cache with ECC
- CoreNet bridges between the CoreNet fabric the I/Os, data path accelerators, and high and low speed peripheral interfaces
- Five 1-Gigabit Ethernet controllers
  - 2.5 Gbps SGMII interfaces
  - RGMII interfaces
- One 64-bit DDR3 and DDR3L SDRAM memory controller with ECC
- Multicore programmable interrupt controller
- Four I^2C controllers
- Four 2-pin UARTs or two 4-pin UARTs
- Two 4-channel DMA engines
- Enhanced local bus controller (eLBC)
- Three PCI Express 2.0 controllers/ports
- Two serial RapidIO® controllers/ports (sRIO port) supporting version 1.3 with features 2.1
- Two serial ATA (SATA 2.0) controllers
- Enhanced secure digital host controller (SD/MMC)
- Enhanced serial peripheral interface (eSPI)
- 2× high-speed USB 2.0 controllers with integrated PHYs

Table of Contents

This figure shows the major functional units within the chip.

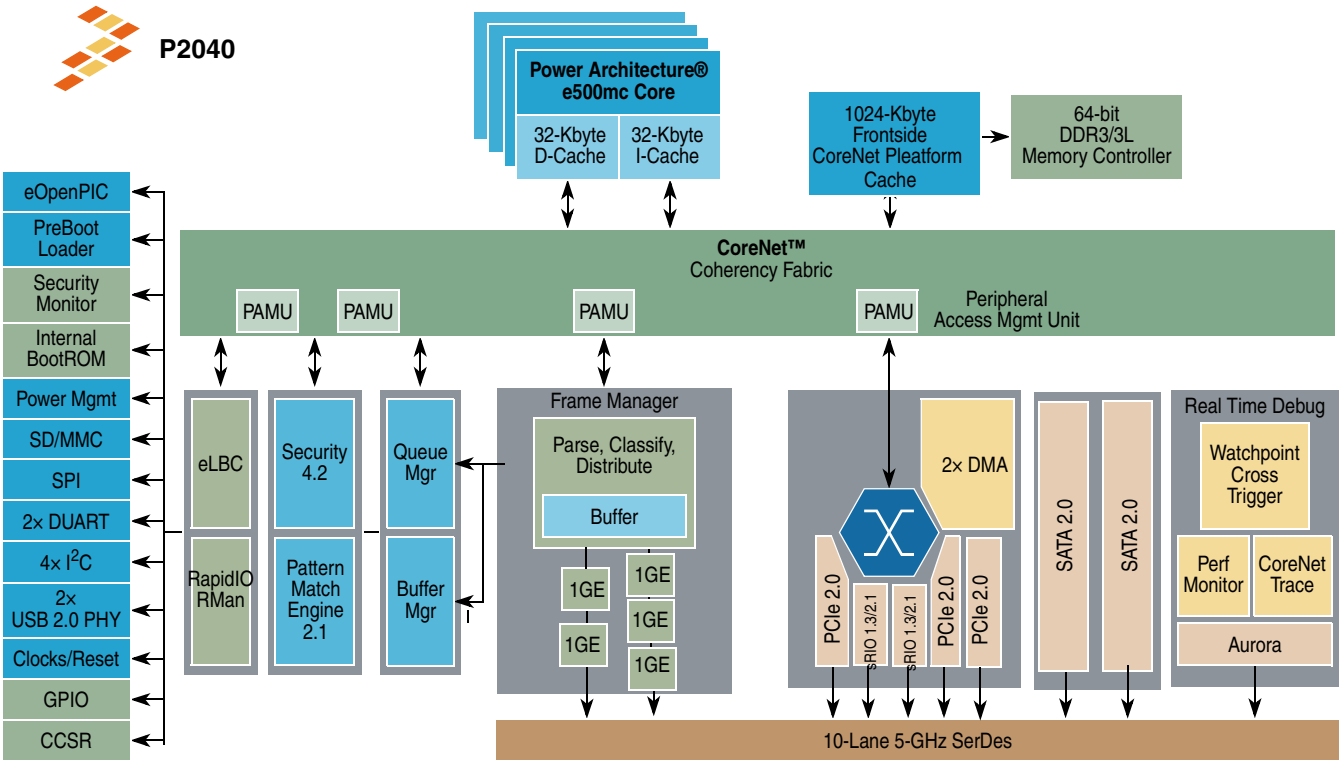


Figure 1. Block Diagram

1 Pin Assignments and Reset States

This section provides a top view of the ball layout diagram and four detailed views by quadrant. It also provides a pinout listing by bus.

1.1 780 FC-PBGA Ball Layout Diagrams

These figures show the FC-PBGA ball map diagrams.

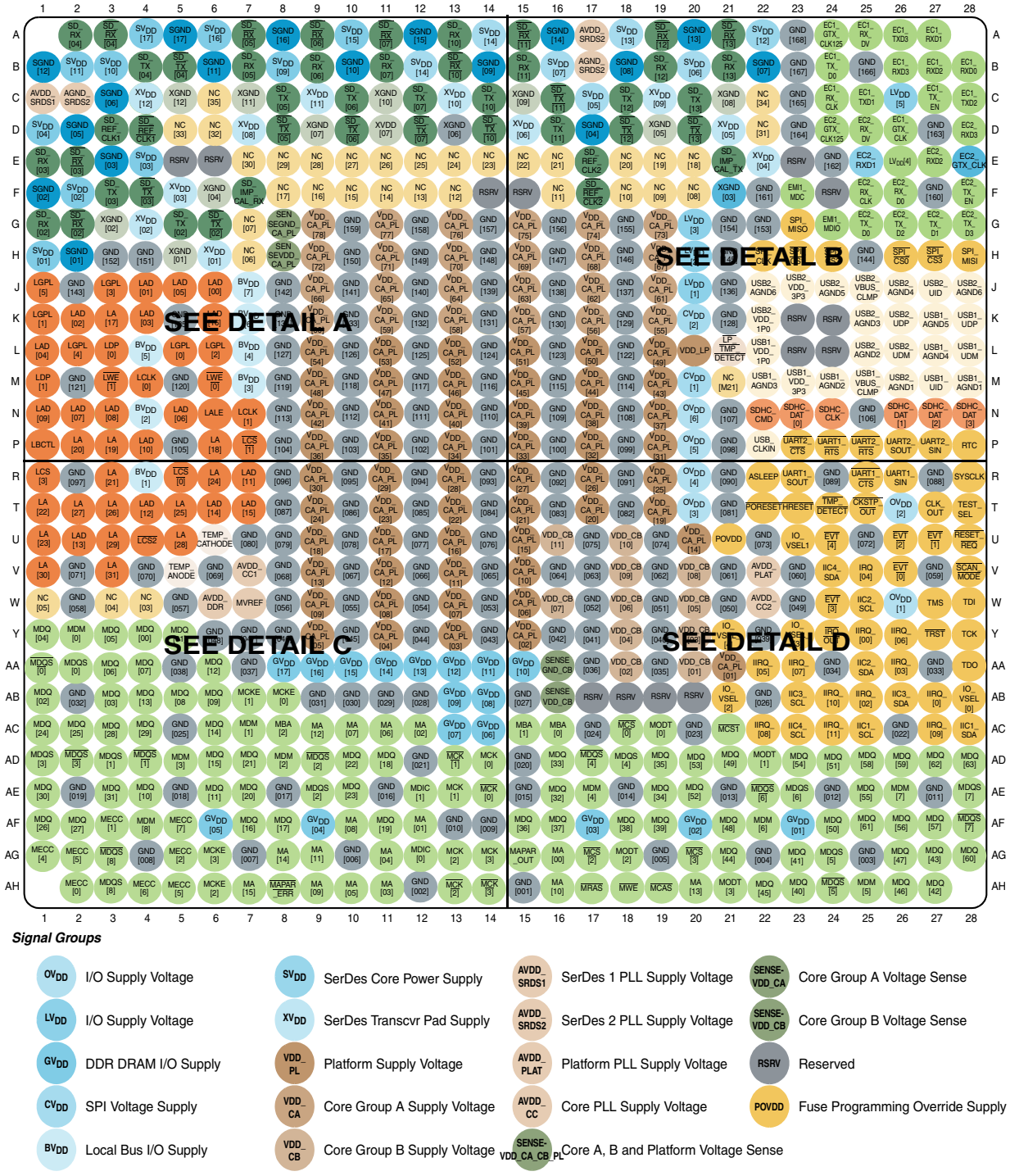


Figure 2. 780 BGA Ball Map Diagram (Top View)

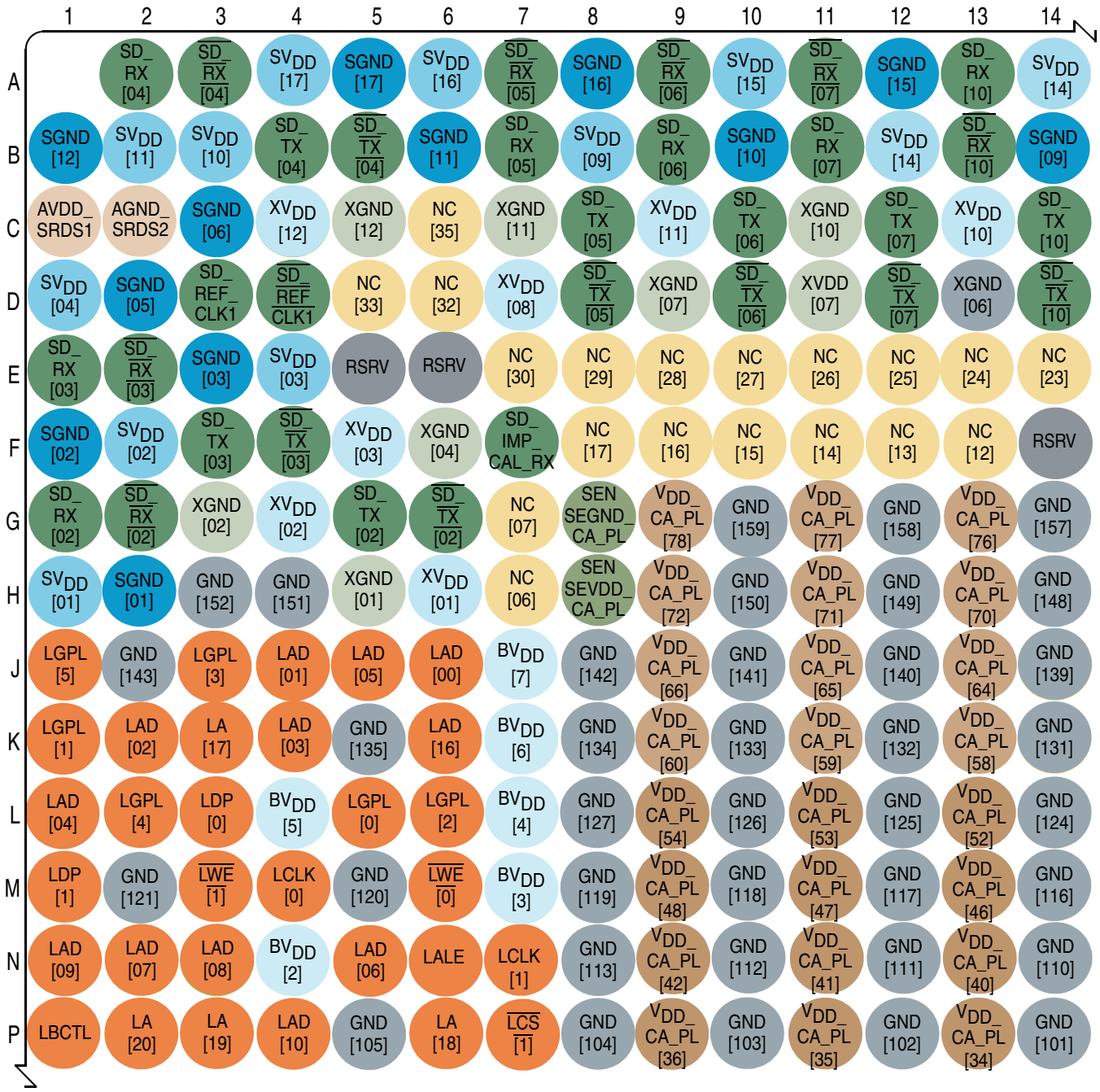


Figure 3. 780 BGA Ball Map Diagram (Detail View A)

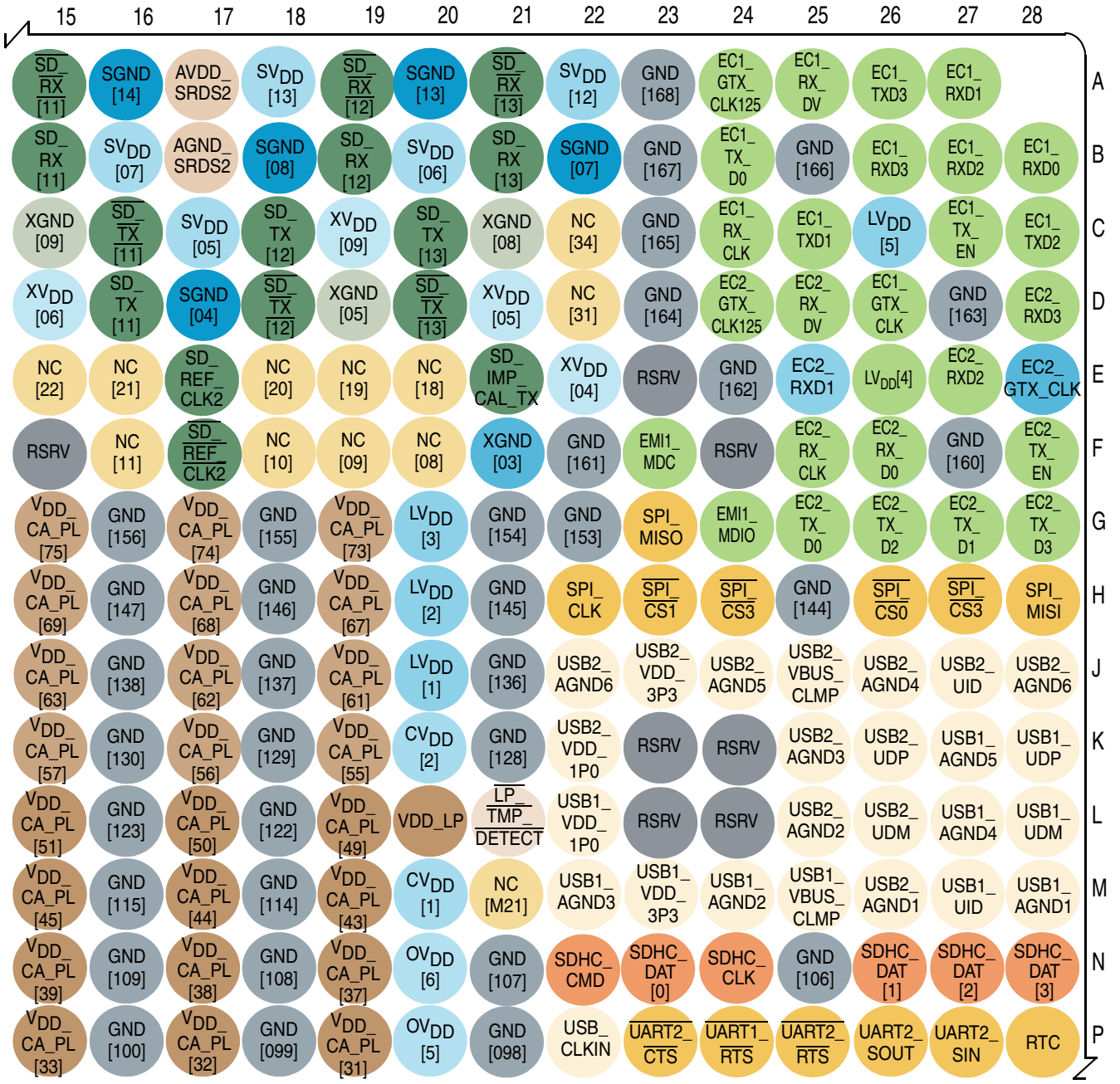


Figure 4. 780 BGA Ball Map Diagram (Detail View B)

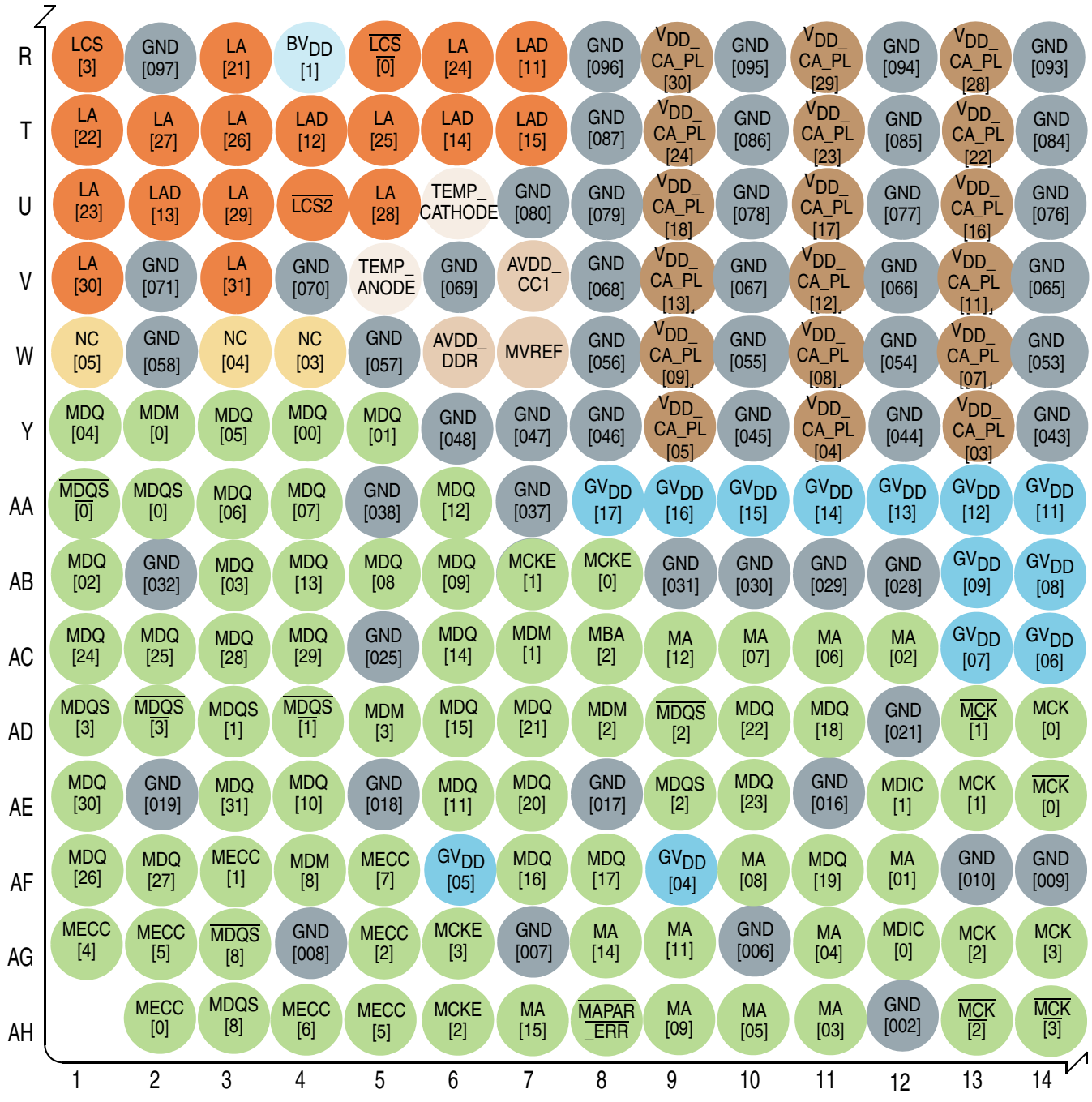


Figure 5. 780 BGA Ball Map Diagram (Detail View C)

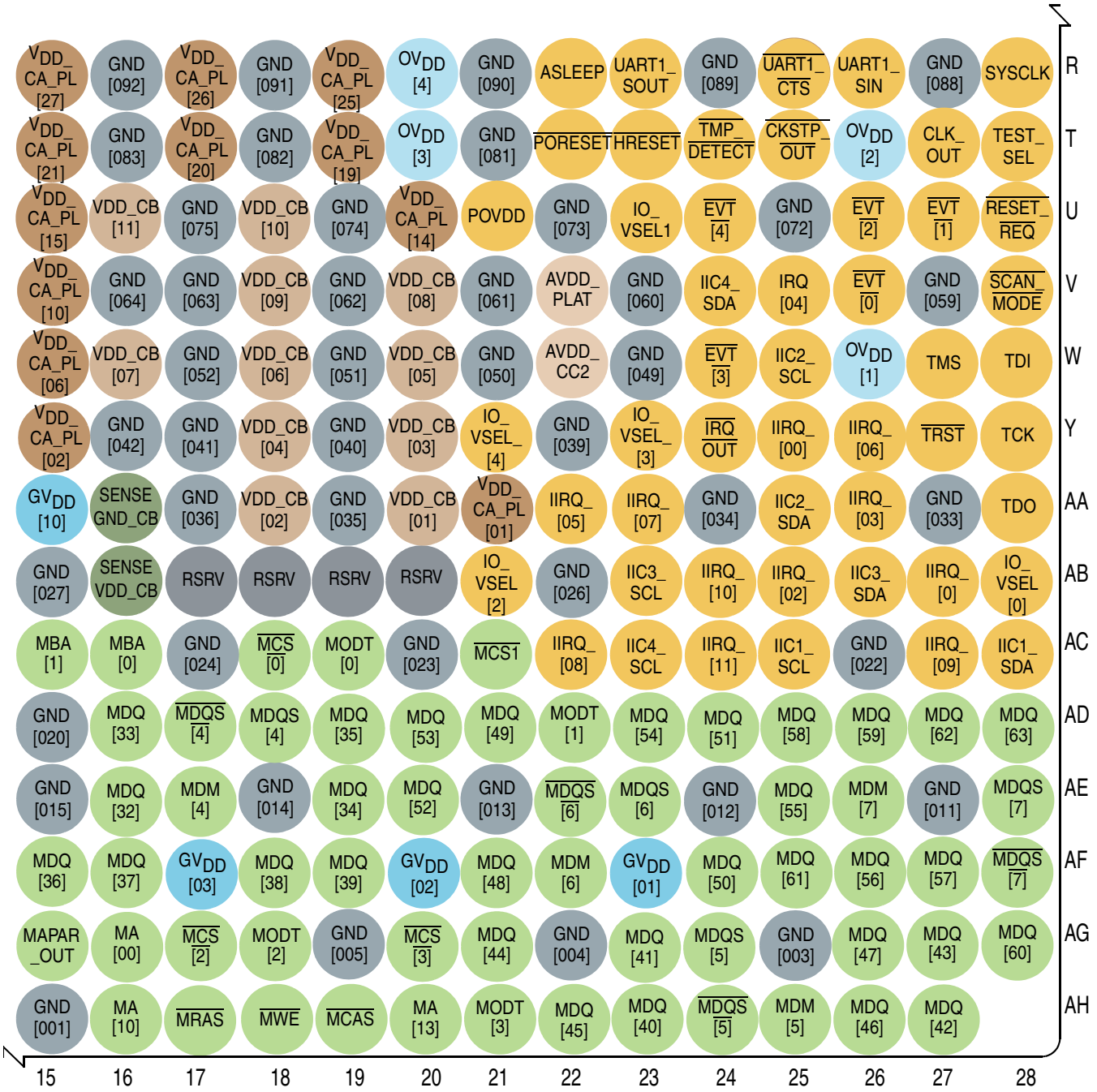


Figure 6. 780 BGA Ball Map Diagram (Detail View D)

1.2 Pinout List

This table provides the pinout listing for the 780 FC-PBGA package by bus. Pins for multiplexed signals appear in the bus group for their default status and have a corresponding note stating that they have multiple functionality depending on the mode in which they are configured.

Table 1. Pin List by Bus

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
DDR SDRAM Memory Interface					
MDQ00	Data	Y4	I/O	GV_{DD}	—
MDQ01	Data	Y5	I/O	GV_{DD}	—
MDQ02	Data	AB1	I/O	GV_{DD}	—
MDQ03	Data	AB3	I/O	GV_{DD}	—
MDQ04	Data	Y1	I/O	GV_{DD}	—
MDQ05	Data	Y3	I/O	GV_{DD}	—
MDQ06	Data	AA3	I/O	GV_{DD}	—
MDQ07	Data	AA4	I/O	GV_{DD}	—
MDQ08	Data	AB5	I/O	GV_{DD}	—
MDQ09	Data	AB6	I/O	GV_{DD}	—
MDQ10	Data	AE4	I/O	GV_{DD}	—
MDQ11	Data	AE6	I/O	GV_{DD}	—
MDQ12	Data	AA6	I/O	GV_{DD}	—
MDQ13	Data	AB4	I/O	GV_{DD}	—
MDQ14	Data	AC6	I/O	GV_{DD}	—
MDQ15	Data	AD6	I/O	GV_{DD}	—
MDQ16	Data	AF7	I/O	GV_{DD}	—
MDQ17	Data	AF8	I/O	GV_{DD}	—
MDQ18	Data	AD11	I/O	GV_{DD}	—
MDQ19	Data	AF11	I/O	GV_{DD}	—
MDQ20	Data	AE7	I/O	GV_{DD}	—
MDQ21	Data	AD7	I/O	GV_{DD}	—
MDQ22	Data	AD10	I/O	GV_{DD}	—
MDQ23	Data	AE10	I/O	GV_{DD}	—
MDQ24	Data	AC1	I/O	GV_{DD}	—
MDQ25	Data	AC2	I/O	GV_{DD}	—
MDQ26	Data	AF1	I/O	GV_{DD}	—
MDQ27	Data	AF2	I/O	GV_{DD}	—
MDQ28	Data	AC3	I/O	GV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
MDQ29	Data	AC4	I/O	GV_{DD}	—
MDQ30	Data	AE1	I/O	GV_{DD}	—
MDQ31	Data	AE3	I/O	GV_{DD}	—
MDQ32	Data	AE16	I/O	GV_{DD}	—
MDQ33	Data	AD16	I/O	GV_{DD}	—
MDQ34	Data	AE19	I/O	GV_{DD}	—
MDQ35	Data	AD19	I/O	GV_{DD}	—
MDQ36	Data	AF15	I/O	GV_{DD}	—
MDQ37	Data	AF16	I/O	GV_{DD}	—
MDQ38	Data	AF18	I/O	GV_{DD}	—
MDQ39	Data	AF19	I/O	GV_{DD}	—
MDQ40	Data	AH23	I/O	GV_{DD}	—
MDQ41	Data	AG23	I/O	GV_{DD}	—
MDQ42	Data	AH27	I/O	GV_{DD}	—
MDQ43	Data	AG27	I/O	GV_{DD}	—
MDQ44	Data	AG21	I/O	GV_{DD}	—
MDQ45	Data	AH22	I/O	GV_{DD}	—
MDQ46	Data	AH26	I/O	GV_{DD}	—
MDQ47	Data	AG26	I/O	GV_{DD}	—
MDQ48	Data	AF21	I/O	GV_{DD}	—
MDQ49	Data	AD21	I/O	GV_{DD}	—
MDQ50	Data	AF24	I/O	GV_{DD}	—
MDQ51	Data	AD24	I/O	GV_{DD}	—
MDQ52	Data	AE20	I/O	GV_{DD}	—
MDQ53	Data	AD20	I/O	GV_{DD}	—
MDQ54	Data	AD23	I/O	GV_{DD}	—
MDQ55	Data	AE25	I/O	GV_{DD}	—
MDQ56	Data	AF26	I/O	GV_{DD}	—
MDQ57	Data	AF27	I/O	GV_{DD}	—
MDQ58	Data	AD25	I/O	GV_{DD}	—
MDQ59	Data	AD26	I/O	GV_{DD}	—
MDQ60	Data	AG28	I/O	GV_{DD}	—
MDQ61	Data	AF25	I/O	GV_{DD}	—
MDQ62	Data	AD27	I/O	GV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
MDQ63	Data	AD28	I/O	GV_{DD}	—
MECC0	Error Correcting Code	AH2	I/O	GV_{DD}	—
MECC1	Error Correcting Code	AF3	I/O	GV_{DD}	—
MECC2	Error Correcting Code	AG5	I/O	GV_{DD}	—
MECC3	Error Correcting Code	AH5	I/O	GV_{DD}	—
MECC4	Error Correcting Code	AG1	I/O	GV_{DD}	—
MECC5	Error Correcting Code	AG2	I/O	GV_{DD}	—
MECC6	Error Correcting Code	AH4	I/O	GV_{DD}	—
MECC7	Error Correcting Code	AF5	I/O	GV_{DD}	—
$\overline{\text{MAPAR\_ERR}}$	Address Parity Error	AH8	I	GV_{DD}	4
MAPAR_OUT	Address Parity Out	AG15	O	GV_{DD}	—
MDM0	Data Mask	Y2	O	GV_{DD}	—
MDM1	Data Mask	AC7	O	GV_{DD}	—
MDM2	Data Mask	AD8	O	GV_{DD}	—
MDM3	Data Mask	AD5	O	GV_{DD}	—
MDM4	Data Mask	AE17	O	GV_{DD}	—
MDM5	Data Mask	AH25	O	GV_{DD}	—
MDM6	Data Mask	AF22	O	GV_{DD}	—
MDM7	Data Mask	AE26	O	GV_{DD}	—
MDM8	Data Mask	AF4	O	GV_{DD}	—
MDQS0	Data Strobe	AA2	I/O	GV_{DD}	—
MDQS1	Data Strobe	AD3	I/O	GV_{DD}	—
MDQS2	Data Strobe	AE9	I/O	GV_{DD}	—
MDQS3	Data Strobe	AD1	I/O	GV_{DD}	—
MDQS4	Data Strobe	AD18	I/O	GV_{DD}	—
MDQS5	Data Strobe	AG24	I/O	GV_{DD}	—
MDQS6	Data Strobe	AE23	I/O	GV_{DD}	—
MDQS7	Data Strobe	AE28	I/O	GV_{DD}	—
MDQS8	Data Strobe	AH3	I/O	GV_{DD}	—
$\overline{\text{MDQS0}}$	Data Strobe	AA1	I/O	GV_{DD}	—
$\overline{\text{MDQS1}}$	Data Strobe	AD4	I/O	GV_{DD}	—
$\overline{\text{MDQS2}}$	Data Strobe	AD9	I/O	GV_{DD}	—
$\overline{\text{MDQS3}}$	Data Strobe	AD2	I/O	GV_{DD}	—
$\overline{\text{MDQS4}}$	Data Strobe	AD17	I/O	GV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{MDQS5}}$	Data Strobe	AH24	I/O	GV_{DD}	—
$\overline{\text{MDQS6}}$	Data Strobe	AE22	I/O	GV_{DD}	—
$\overline{\text{MDQS7}}$	Data Strobe	AF28	I/O	GV_{DD}	—
$\overline{\text{MDQS8}}$	Data Strobe	AG3	I/O	GV_{DD}	—
MBA0	Bank Select	AC16	O	GV_{DD}	—
MBA1	Bank Select	AC15	O	GV_{DD}	—
MBA2	Bank Select	AC8	O	GV_{DD}	—
MA00	Address	AG16	O	GV_{DD}	—
MA01	Address	AF12	O	GV_{DD}	—
MA02	Address	AC12	O	GV_{DD}	—
MA03	Address	AH11	O	GV_{DD}	—
MA04	Address	AG11	O	GV_{DD}	—
MA05	Address	AH10	O	GV_{DD}	—
MA06	Address	AC11	O	GV_{DD}	—
MA07	Address	AC10	O	GV_{DD}	—
MA08	Address	AF10	O	GV_{DD}	—
MA09	Address	AH9	O	GV_{DD}	—
MA10	Address	AH16	O	GV_{DD}	—
MA11	Address	AG9	O	GV_{DD}	—
MA12	Address	AC9	O	GV_{DD}	—
MA13	Address	AH20	O	GV_{DD}	—
MA14	Address	AG8	O	GV_{DD}	—
MA15	Address	AH7	O	GV_{DD}	—
$\overline{\text{MWE}}$	Write Enable	AH18	O	GV_{DD}	—
$\overline{\text{MRAS}}$	Row Address Strobe	AH17	O	GV_{DD}	—
$\overline{\text{MCAS}}$	Column Address Strobe	AH19	O	GV_{DD}	—
$\overline{\text{MCS0}}$	Chip Select	AC18	O	GV_{DD}	—
$\overline{\text{MCS1}}$	Chip Select	AC21	O	GV_{DD}	—
$\overline{\text{MCS2}}$	Chip Select	AG17	O	GV_{DD}	—
$\overline{\text{MCS3}}$	Chip Select	AG20	O	GV_{DD}	—
MCKE0	Clock Enable	AB8	O	GV_{DD}	—
MCKE1	Clock Enable	AB7	O	GV_{DD}	—
MCKE2	Clock Enable	AH6	O	GV_{DD}	—
MCKE3	Clock Enable	AG6	O	GV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
MCK0	Clock	AD14	O	GV_{DD}	—
MCK1	Clock	AE13	O	GV_{DD}	—
MCK2	Clock	AG13	O	GV_{DD}	—
MCK3	Clock	AG14	O	GV_{DD}	—
$\overline{\text{MCK0}}$	Clock Complements	AE14	O	GV_{DD}	—
$\overline{\text{MCK1}}$	Clock Complements	AD13	O	GV_{DD}	—
$\overline{\text{MCK2}}$	Clock Complements	AH13	O	GV_{DD}	—
$\overline{\text{MCK3}}$	Clock Complements	AH14	O	GV_{DD}	—
MODT0	On Die Termination	AC19	O	GV_{DD}	—
MODT1	On Die Termination	AD22	O	GV_{DD}	—
MODT2	On Die Termination	AG18	O	GV_{DD}	—
MODT3	On Die Termination	AH21	O	GV_{DD}	—
MDIC0	Driver Impedance Calibration	AG12	I/O	GV_{DD}	16
MDIC1	Driver Impedance Calibration	AE12	I/O	GV_{DD}	16
Local Bus Controller Interface					
LAD00	Muxed Data/Address	J6	I/O	BV_{DD}	3
LAD01	Muxed Data/Address	J4	I/O	BV_{DD}	3
LAD02	Muxed Data/Address	K2	I/O	BV_{DD}	3
LAD03	Muxed Data/Address	K4	I/O	BV_{DD}	3
LAD04	Muxed Data/Address	L1	I/O	BV_{DD}	3
LAD05	Muxed Data/Address	J5	I/O	BV_{DD}	3
LAD06	Muxed Data/Address	N5	I/O	BV_{DD}	3
LAD07	Muxed Data/Address	N2	I/O	BV_{DD}	3
LAD08	Muxed Data/Address	N3	I/O	BV_{DD}	3
LAD09	Muxed Data/Address	N1	I/O	BV_{DD}	3
LAD10	Muxed Data/Address	P4	I/O	BV_{DD}	3
LAD11	Muxed Data/Address	R7	I/O	BV_{DD}	3
LAD12	Muxed Data/Address	T4	I/O	BV_{DD}	3
LAD13	Muxed Data/Address	U2	I/O	BV_{DD}	3
LAD14	Muxed Data/Address	T6	I/O	BV_{DD}	3
LAD15	Muxed Data/Address	T7	I/O	BV_{DD}	3
LA16	Address	K6	I/O	BV_{DD}	31
LA17	Address	K3	I/O	BV_{DD}	31
LA18	Address	P6	I/O	BV_{DD}	31

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
LA19	Address	P3	I/O	BV_{DD}	31
LA20	Address	P2	I/O	BV_{DD}	31
LA21	Address	R3	I/O	BV_{DD}	31
LA22	Address	T1	I/O	BV_{DD}	31
LA23	Address	U1	I/O	BV_{DD}	3
LA24	Address	R6	I/O	BV_{DD}	3
LA25	Address	T5	I/O	BV_{DD}	31
LA26	Address	T3	I/O	BV_{DD}	3, 29
LA27	Address	T2	O	BV_{DD}	—
LA28	Address	U5	I/O	BV_{DD}	—
LA29	Address	U3	I/O	BV_{DD}	—
LA30	Address	V1	I/O	BV_{DD}	—
LA31	Address	V3	I/O	BV_{DD}	—
LDP0	Data Parity	L3	I/O	BV_{DD}	—
LDP1	Data Parity	M1	I/O	BV_{DD}	—
$\overline{\text{LCS0}}$	Chip Selects	R5	O	BV_{DD}	5
$\overline{\text{LCS1}}$	Chip Selects	P7	O	BV_{DD}	5
$\overline{\text{LCS2}}$	Chip Selects	U4	O	BV_{DD}	5
$\overline{\text{LCS3}}$	Chip Selects	R1	O	BV_{DD}	5
$\overline{\text{LWE0}}$	Write Enable	M6	O	BV_{DD}	—
$\overline{\text{LWE1}}$	Write Enable	M3	O	BV_{DD}	—
LBCTL	Buffer Control	P1	O	BV_{DD}	—
LALE	Address Latch Enable	N6	I/O	BV_{DD}	—
LGPL0/LFCLE	UPM General Purpose Line 0/ LFCLE—FCM	L5	O	BV_{DD}	3, 4
LGPL1/LFALE	UPM General Purpose Line 1/ LFALE—FCM	K1	O	BV_{DD}	3, 4
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM General Purpose Line 2/ LOE_B—Output Enable	L6	O	BV_{DD}	3, 4
LGPL3/$\overline{\text{LFWP}}$	UPM General Purpose LIne 3/ LFWP_B—FCM	J3	O	BV_{DD}	3, 4
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	UPM General Purpose Line 4/ LGTA_B—FCM	L2	I/O	BV_{DD}	36
LGPL5	UPM General Purpose Line 5 / Amux	J1	O	BV_{DD}	3, 4
LCLK0	Local Bus Clock	M4	O	BV_{DD}	—
LCLK1	Local Bus Clock	N7	O	BV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
DMA					
DMA1_DREQ0/IIC4_SCL/EVT5/M1SRCID1/LB_SRCID1/GPIO18	DMA1 Channel 0 Request	AC23	I	OV_{DD}	24
DMA1_DACK0/IIC3_SCL/GPIO16/SDHC_CD/ M1DVAL/LB_DVAL	DMA1 Channel 0 Acknowledge	AB23	O	OV_{DD}	2, 14
DMA1_DDONE0/IIC3_SDA/GPIO17/M1SRCID0/LB_SRCID0/SDHC_WP	DMA1 Channel 0 Done	AB26	O	OV_{DD}	2, 14
DMA2_DREQ0/IRQ03/GPIO21	DMA2 Channel 0 Request	AA26	I	OV_{DD}	24
DMA2_DACK0/IRQ04/GPIO22	DMA2 Channel 0 Acknowledge	V25	O	OV_{DD}	24
DMA2_DDONE0/IRQ05/GPIO23	DMA2 Channel 0 Done	AA22	O	OV_{DD}	24
USB Host Port 1					
USB1_UDP	USB1 PHY Data Plus	K28	I/O	$USB\_V_{DD}\_3P3$	—
USB1_UDM	USB1 PHY Data Minus	L28	I/O	$USB\_V_{DD}\_3P3$	—
USB1_VBUS_CLMP	USB1 PHY VBUS Divided Signals	M25	I	$USB\_V_{DD}\_3P3$	34
USB1_UID	USB1 PHY ID Detect	M27	I	$USB\_V_{DD}\_3P3$	—
USB_CLKIN	USB PHY Clock Input	P22	I	OV_{DD}	—
USB1_DRVVBUS/GPIO24/IRQ6	USB1 5V Supply Enable	Y26	O	OV_{DD}	—
USB1_PWRFAULT/GPIO25/IRQ7	USB Power Fault	AA23	I	OV_{DD}	—
USB Host Port 2					
USB2_UDP	USB2 PHY Data Plus	K26	I/O	$USB\_V_{DD}\_3P3$	—
USB2_UDM	USB2 PHY Data Minus	L26	I/O	$USB\_V_{DD}\_3P3$	—
USB2_VBUS_CLMP	USB2 PHY VBUS Divided Signals	J25	I	$USB\_V_{DD}\_3P3$	34
USB2_UID	USB2 PHY ID Detect	J27	I	$USB\_V_{DD}\_3P3$	—
USB2_DRVVBUS/GPIO26/IRQ8	USB2 5V Supply Enable	AC22	I/O	OV_{DD}	—
USB2_PWRFAULT/GPIO27/IRQ9	USB2 Power Fault	AC27	I/O	OV_{DD}	—
Programmable Interrupt Controller					
IRQ00	External Interrupts	Y25	I	OV_{DD}	—
IRQ01	External Interrupts	AB27	I	OV_{DD}	—
IRQ02	External Interrupts	AB25	I	OV_{DD}	—
IRQ03/GPIO21/DMA2_DREQ0	External Interrupts	AA26	I	OV_{DD}	24
IRQ04/GPIO22/DMA2_DACK0	External Interrupts	V25	I	OV_{DD}	24

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
IRQ05/GPIO23/DMA2_DDONE0	External Interrupts	AA22	I	OV_{DD}	24
IRQ06/GPIO24/USB1_DRVVBUS	External Interrupts	Y26	I	OV_{DD}	24
IRQ07/GPIO25/USB1_PWRFAULT	External Interrupts	AA23	I	OV_{DD}	24
IRQ08/GPIO26/USB2_DRVVBUS	External Interrupts	AC22	I	OV_{DD}	24
IRQ09/GPIO27/USB2_PWRFAULT	External Interrupts	AC27	I	OV_{DD}	24
IRQ10/GPIO28/EVT7	External Interrupts	AB24	I	OV_{DD}	24
IRQ11/GPIO29/EVT8	External Interrupts	AC24	I	OV_{DD}	24
IRQ_OUT/EVT9	Interrupt Output	Y24	O	OV_{DD}	1, 2, 24
Trust					
TMP_DETECT	Tamper Detect	T24	I	OV_{DD}	25
LP_TMP_DETECT	Low Power Tamper Detect	L21	I	V_{DD_LP}	25
eSDHC					
SDHC_CMD	Command/Response	N22	I/O	CV_{DD}	—
SDHC_DAT0	Data	N23	I/O	CV_{DD}	—
SDHC_DAT1	Data	N26	I/O	CV_{DD}	—
SDHC_DAT2	Data	N27	I/O	CV_{DD}	—
SDHC_DAT3	Data	N28	I/O	CV_{DD}	—
SDHC_DAT4/SPI_CS0/GPIO00	Data	H26	I/O	CV_{DD}	24, 28
SDHC_DAT5/SPI_CS1/GPIO01	Data	H23	I/O	CV_{DD}	24, 28
SDHC_DAT6/SPI_CS2/GPIO02	Data	H27	I/O	CV_{DD}	24, 28
SDHC_DAT7/SPI_CS3/GPIO03	Data	H24	I/O	CV_{DD}	24, 28
SDHC_CLK	Host to Card Clock	N24	O	OV_{DD}	—
SDHC_CD/IIC3_SCL/GPIO16/ M1DVAL/LB_DVAL/DMA1_DACK0	Card Detection	AB23	I/O	OV_{DD}	24, 28
SDHC_WP/IIC3_SDA/GPIO17/ M1SRCID0/LB_SRCID0/DMA1_DDONE0	Card Write Protection	AB26	I	OV_{DD}	24, 28
eSPI					
SPI_MOSI	Master Out Slave In	H28	I/O	CV_{DD}	—
SPI_MISO	Master In Slave Out	G23	I	CV_{DD}	—
SPI_CLK	eSPI Clock	H22	O	CV_{DD}	—
SPI_CS0/SDHC_DAT4/GPIO00	eSPI Chip Select	H26	O	CV_{DD}	24
SPI_CS1/SDHC_DAT5/GPIO01	eSPI Chip Select	H23	O	CV_{DD}	24
SPI_CS2/SDHC_DAT6/GPIO02	eSPI Chip Select	H27	O	CV_{DD}	24
SPI_CS3/SDHC_DAT7/GPIO03	eSPI Chip Select	H24	O	CV_{DD}	24

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
IEEE 1588					
TSEC_1588_CLK_IN/EC1_RXD2	Clock In	B27	I	LV_{DD}	—
TSEC_1588_TRIG_IN1/EC1_RXD0	Trigger In 1	B28	I	LV_{DD}	—
TSEC_1588_TRIG_IN2/EC1_RXD1	Trigger In 2	A27	I	LV_{DD}	—
TSEC_1588_ALARM_OUT1/EC1_TXD0	Alarm Out 1	B24	O	LV_{DD}	—
TSEC_1588_ALARM_OUT2/ EC1_TXD1/GPIO30	Alarm Out 2	C25	O	LV_{DD}	23
TSEC_1588_CLK_OUT/EC1_RXD3	Clock Out	B26	O	LV_{DD}	—
TSEC_1588_PULSE_OUT1/EC1_TXD2	Pulse Out1	C28	O	LV_{DD}	—
TSEC_1588_PULSE_OUT2/EC1_TXD3/GPIO31	Pulse Out2	A26	O	LV_{DD}	23
Ethernet Management Interface 1					
EMI1_MDC	Management Data Clock	F23	O	LV_{DD}	—
EMI1_MDIO	Management Data In/Out	G24	I/O	LV_{DD}	—
Ethernet Reference Clock					
EC1_GTX_CLK125/EC_XTRNL_TX_STMP2	Reference Clock (RGMII)	A24	I	LV_{DD}	25
EC2_GTX_CLK125	Reference Clock (RGMII)	D24	I	LV_{DD}	25
Ethernet External Timestamping					
EC_XTRNL_TX_STMP1/EC1_TX_EN	External Timestamp Transmit 1	C27	I	LV_{DD}	—
EC_XTRNL_RX_STMP1/EC1_RX_DV	External Timestamp Receive 1	A25	I	LV_{DD}	—
EC_XTRNL_TX_STMP2/EC1_GTX_CLK125	External Timestamp Transmit 2	A24	I	LV_{DD}	—
EC_XTRNL_RX_STMP2/EC1_RX_CLK	External Timestamp Receive 2	C24	I	LV_{DD}	—
Three-Speed Ethernet Controller 1					
EC1_TXD3/TSEC_1588_PULSE_OUT2/GPIO31	Transmit Data	A26	O	LV_{DD}	—
EC1_TXD2/TSEC_1588_PULSE_OUT1	Transmit Data	C28	O	LV_{DD}	—
EC1_TXD1/TSEC_1588_ALARM_OUT2/GPIO30	Transmit Data	C25	O	LV_{DD}	—
EC1_TXD0/TSEC_1588_ALARM_OUT1	Transmit Data	B24	O	LV_{DD}	—
EC1_TX_EN/EC_XTRNL_TX_STMP1	Transmit Enable	C27	O	LV_{DD}	15
EC1_GTX_CLK	Transmit Clock Out (RGMII)	D26	O	LV_{DD}	24
EC1_RXD3/TSEC_1588_CLK_OUT	Receive Data	B26	I	LV_{DD}	25
EC1_RXD2/TSEC_1588_CLK_IN	Receive Data	B27	I	LV_{DD}	25

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
EC1_RXD1/TSEC_1588_TRIG_IN2	Receive Data	A27	I	LV_{DD}	25
EC1_RXD0/TSEC_1588_TRIG_IN1	Receive Data	B28	I	LV_{DD}	25
EC1_RX_DV/EC_XTRNL_RX_STMP1	Receive Data Valid	A25	I	LV_{DD}	25
EC1_RX_CLK/EC_XTRNL_RX_STMP2	Receive Clock	C24	I	LV_{DD}	25
Three-Speed Ethernet Controller 2					
EC2_TXD3	Transmit Data	G28	O	LV_{DD}	—
EC2_TXD2	Transmit Data	G26	O	LV_{DD}	—
EC2_TXD1	Transmit Data	G27	O	LV_{DD}	—
EC2_TXD0	Transmit Data	G25	O	LV_{DD}	—
EC2_TX_EN	Transmit Enable	F28	O	LV_{DD}	15
EC2_GTX_CLK	Transmit Clock Out (RGMII)	E28	O	LV_{DD}	24
EC2_RXD3	Receive Data	D28	I	LV_{DD}	25
EC2_RXD2	Receive Data	E27	I	LV_{DD}	25
EC2_RXD1	Receive Data	E25	I	LV_{DD}	24, 25
EC2_RXD0	Receive Data	F26	I	LV_{DD}	24, 25
EC2_RX_DV	Receive Data Valid	D25	I	LV_{DD}	25
EC2_RX_CLK	Receive Clock	F25	I	LV_{DD}	25
UART					
UART1_SOUT/GPIO8	Transmit Data	R23	O	OV_{DD}	24
UART2_SOUT/GPIO9	Transmit Data	P26	O	OV_{DD}	24
UART1_SIN/GPIO10	Receive Data	R26	I	OV_{DD}	24
UART2_SIN/GPIO11	Receive Data	P27	I	OV_{DD}	24
$\overline{\text{UART1\_RTS}}$/UART3_SOUT/GPIO12	Ready to Send	P24	O	OV_{DD}	24
$\overline{\text{UART2\_RTS}}$/UART4_SOUT/GPIO13	Ready to Send	P25	O	OV_{DD}	24
$\overline{\text{UART1\_CTS}}$/UART3_SIN/GPIO14	Clear to Send	R25	I	OV_{DD}	24
$\overline{\text{UART2\_CTS}}$/UART4_SIN/GPIO15	Clear to Send	P23	I	OV_{DD}	24
I^2C Interface					
IIC1_SCL	Serial Clock	AC25	I/O	OV_{DD}	2, 14
IIC1_SDA	Serial Data	AC28	I/O	OV_{DD}	2, 14
IIC2_SCL	Serial Clock	W25	I/O	OV_{DD}	2, 14
IIC2_SDA	Serial Data	AA25	I/O	OV_{DD}	2, 14
IIC3_SCL/GPIO16/M1DVAL/LB_DVAL/ $\overline{\text{DMA1\_DACK0}}$/SDHC_CD	Serial Clock	AB23	I/O	OV_{DD}	2, 14

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
IIC3_SDA/GPIO17/M1SRCID0/LB_SRCID0/ DMA1_DDONE0/SDHC_WP	Serial Data	AB26	I/O	OV_{DD}	2, 14
IIC4_SCL/EVT5/M1SRCID1/LB_SRCID1/ GPIO18/DMA1_DREQ0	Serial Clock	AC23	I/O	OV_{DD}	2, 14
IIC4_SDA/EVT6/M1SRCID2/ LB_SRCID2/GPIO19	Serial Data	V24	I/O	OV_{DD}	2, 14
SerDes (x10) PCI Express, Serial RapidIO, Aurora, 10GE, 1GE					
SD_TX13	Transmit Data (positive)	C20	O	XV_{DD}	—
SD_TX12	Transmit Data (positive)	C18	O	XV_{DD}	—
SD_TX11	Transmit Data (positive)	D16	O	XV_{DD}	—
SD_TX10	Transmit Data (positive)	C14	O	XV_{DD}	—
SD_TX07	Transmit Data (positive)	C12	O	XV_{DD}	—
SD_TX06	Transmit Data (positive)	C10	O	XV_{DD}	—
SD_TX05	Transmit Data (positive)	C8	O	XV_{DD}	—
SD_TX04	Transmit Data (positive)	B4	O	XV_{DD}	—
SD_TX03	Transmit Data (positive)	F3	O	XV_{DD}	—
SD_TX02	Transmit Data (positive)	G5	O	XV_{DD}	—
SD_TX13	Transmit Data (negative)	D20	O	XV_{DD}	—
SD_TX12	Transmit Data (negative)	D18	O	XV_{DD}	—
SD_TX11	Transmit Data (negative)	C16	O	XV_{DD}	—
SD_TX10	Transmit Data (negative)	D14	O	XV_{DD}	—
SD_TX07	Transmit Data (negative)	D12	O	XV_{DD}	—
SD_TX06	Transmit Data (negative)	D10	O	XV_{DD}	—
SD_TX05	Transmit Data (negative)	D8	O	XV_{DD}	—
SD_TX04	Transmit Data (negative)	B5	O	XV_{DD}	—
SD_TX03	Transmit Data (negative)	F4	O	XV_{DD}	—
SD_TX02	Transmit Data (negative)	G6	O	XV_{DD}	—
SD_RX13	Receive Data (positive)	B21	I	XV_{DD}	—
SD_RX12	Receive Data (positive)	B19	I	XV_{DD}	—
SD_RX11	Receive Data (positive)	B15	I	XV_{DD}	—
SD_RX10	Receive Data (positive)	A13	I	XV_{DD}	—
SD_RX07	Receive Data (positive)	B11	I	XV_{DD}	—
SD_RX06	Receive Data (positive)	B9	I	XV_{DD}	—
SD_RX05	Receive Data (positive)	B7	I	XV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
SD_RX04	Receive Data (positive)	A2	I	XV_{DD}	—
SD_RX03	Receive Data (positive)	E1	I	XV_{DD}	—
SD_RX02	Receive Data (positive)	G1	I	XV_{DD}	—
$\overline{\text{SD\_RX13}}$	Receive Data (negative)	A21	I	XV_{DD}	—
$\overline{\text{SD\_RX12}}$	Receive Data (negative)	A19	I	XV_{DD}	—
$\overline{\text{SD\_RX11}}$	Receive Data (negative)	A15	I	XV_{DD}	—
$\overline{\text{SD\_RX10}}$	Receive Data (negative)	B13	I	XV_{DD}	—
$\overline{\text{SD\_RX07}}$	Receive Data (negative)	A11	I	XV_{DD}	—
$\overline{\text{SD\_RX06}}$	Receive Data (negative)	A9	I	XV_{DD}	—
$\overline{\text{SD\_RX05}}$	Receive Data (negative)	A7	I	XV_{DD}	—
$\overline{\text{SD\_RX04}}$	Receive Data (negative)	A3	I	XV_{DD}	—
$\overline{\text{SD\_RX03}}$	Receive Data (negative)	E2	I	XV_{DD}	—
$\overline{\text{SD\_RX02}}$	Receive Data (negative)	G2	I	XV_{DD}	—
SD_REF_CLK1	SerDes Bank 1 PLL Reference Clock	D3	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK1}}$	SerDes Bank 1 PLL Reference Clock Complement	D4	I	XV_{DD}	—
SD_REF_CLK2	SerDes Bank 2 PLL Reference Clock	E17	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK2}}$	SerDes Bank 2 PLL Reference Clock Complement	F17	I	XV_{DD}	—
General-Purpose Input/Output					
GPIO00/$\overline{\text{SPI\_CS0}}$/SDHC_DATA4	General Purpose Input/Output	H26	I/O	CV_{DD}	—
GPIO01/$\overline{\text{SPI\_CS1}}$/SDHC_DATA5	General Purpose Input/Output	H23	I/O	CV_{DD}	—
GPIO02/$\overline{\text{SPI\_CS2}}$/SDHC_DATA6	General Purpose Input/Output	H27	I/O	CV_{DD}	—
GPIO03$\overline{\text{SPI_CS3}}$/SDHC_DATA7	General Purpose Input/Output	H24	I/O	CV_{DD}	—
GPIO08/UART1_SOUT	General Purpose Input/Output	R23	I/O	OV_{DD}	—
GPIO09/UART2_SOUT	General Purpose Input/Output	P26	I/O	OV_{DD}	—
GPIO10/UART1_SIN	General Purpose Input/Output	R26	I/O	OV_{DD}	—
GPIO11/UART2_SIN	General Purpose Input/Output	P27	I/O	OV_{DD}	—
GPIO12/$\overline{\text{UART1\_RTS}}$/UART3_SOUT	General Purpose Input/Output	P24	I/O	OV_{DD}	—
GPIO13/$\overline{\text{UART2\_RTS}}$/UART4_SOUT	General Purpose Input/Output	P25	I/O	OV_{DD}	—
GPIO14/$\overline{\text{UART1\_CTS}}$/UART3_SIN	General Purpose Input/Output	R25	I/O	OV_{DD}	—
GPIO15/$\overline{\text{UART2\_CTS}}$/UART4_SIN	General Purpose Input/Output	P23	I/O	OV_{DD}	—
GPIO16/IIC3_SCL/M1DVAL/LB_DVAL/ $\overline{\text{DMA1\_DACK0}}$/$\overline{\text{SDHC\_CD}}$	General Purpose Input/Output	AB23	I/O	OV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GPIO17/IIC3_SDA/M1SRCID0/LB_SRCID0 / DMA1_DDONE0/SDHC_WP	General Purpose Input/Output	AB26	I/O	OV_{DD}	—
GPIO18/IIC4_SCL/EVT5/M1SRCID1/ LB_SRCID1/DMA1_DREQ0	General Purpose Input/Output	AC23	I/O	OV_{DD}	—
GPIO19/IIC4_SDA/EVT6/M1SRCID2/ LB_SRCID2	General Purpose Input/Output	V24	I/O	OV_{DD}	—
GPIO21/IRQ3/DMA2_DREQ0	General Purpose Input/Output	AA26	I/O	OV_{DD}	—
GPIO22/IRQ4/DMA2_DACK0	General Purpose Input/Output	V25	I/O	OV_{DD}	—
GPIO23/IRQ5/DMA2_DDONE0	General Purpose Input/Output	AA22	I/O	OV_{DD}	—
GPIO24/IRQ6/USB1_DRVVBUS	General Purpose Input/Output	Y26	I/O	OV_{DD}	—
GPIO25/IRQ7/USB1_PWRFAULT	General Purpose Input/Output	AA23	I/O	OV_{DD}	—
GPIO26/IRQ8/USB2_DRVVBUS	General Purpose Input/Output	AC22	I/O	OV_{DD}	—
GPIO27/IRQ9/USB2_PWRFAULT	General Purpose Input/Output	AC27	I/O	OV_{DD}	—
GPIO28/IRQ10/EVT7	General Purpose Input/Output	AB24	I/O	OV_{DD}	—
GPIO29/IRQ11/EVT8	General Purpose Input/Output	AC24	I/O	OV_{DD}	—
GPIO30/EC1_TXD1/TSEC_1588_ALARM_ OUT2	General Purpose Input/Output	C25	I/O	LV_{DD}	23
GPIO31/EC1_TXD3/TSEC_1588_PULSE_ OUT2	General Purpose Input/Output	A26	I/O	LV_{DD}	23
System Control					
PORESET	Power On Reset	T22	I	OV_{DD}	—
HRESET	Hard Reset	T23	I/O	OV_{DD}	1, 2
RESET_REQ	Reset Request	U28	O	OV_{DD}	31
CKSTP_OUT	Checkstop Out	T25	O	OV_{DD}	1, 2
Debug					
EVT0	Event 0	V26	I/O	OV_{DD}	18
EVT1	Event 1	U27	I/O	OV_{DD}	—
EVT2	Event 2	U26	I/O	OV_{DD}	—
EVT3	Event 3	W24	I/O	OV_{DD}	—
EVT4	Event 4	U24	I/O	OV_{DD}	—
EVT5/IIC4_SCL/M1SRCID1/LB_SRCID1/ GPIO18/DMA1_DREQ0	Event 5	AC23	I/O	OV_{DD}	—
EVT6/IIC4_SDA/M1SRCID2/ LB_SRCID2/GPIO19	Event 6	V24	I/O	OV_{DD}	—
EVT7GPIO28/IRQ10	Event 7	AB24	I/O	OV_{DD}	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
EVT8/GPIO29/IRQ11	Event 8	AC24	I/O	OV_{DD}	—
EVT9/IRQ_OUT	Event 9	Y24	I/O	OV_{DD}	—
M1DVAL/LB_DVAL/IIC3_SCL/GPIO16/ SDHC_CD/DMA1_DACK0	Debug Data Valid	AB23	O	OV_{DD}	—
MSRCID0/LB_SRCID0/IIC3_SDA/GPIO17/ DMA_DDONE0/SDHC_WP	Debug Source ID 0	AB26	O	OV_{DD}	4, 31
MSRCID1/LB_MSRCID1/EVT5/IIC4_SCL/ LB_SRCID1/GPIO18/DMA1_DREQ0	Debug Source ID 1	AC23	O	OV_{DD}	—
MSRCID2/LB_SRCID2/EVT6/IIC4_SDA/ LB_SRCID2/GPIO19	Debug Source ID 2	V24	O	OV_{DD}	—
CLK_OUT	Clock Out	T27	O	OV_{DD}	6
Clock					
RTC	Real Time Clock	P28	I	OV_{DD}	—
SYSCLK	System Clock	R28	I	OV_{DD}	—
JTAG					
TCK	Test Clock	Y28	I	OV_{DD}	—
TDI	Test Data In	W28	I	OV_{DD}	7
TDO	Test Data Out	AA28	O	OV_{DD}	6
TMS	Test Mode Select	W27	I	OV_{DD}	7
TRST	Test Reset	Y27	I	OV_{DD}	7
DFT					
SCAN_MODE	Scan Mode	V28	I	OV_{DD}	35
TEST_SEL	Test Mode Select	T28	I	OV_{DD}	12, 26
Power Management					
ASLEEP	Asleep	R22	O	OV_{DD}	31
Input /Output Voltage Select					
IO_VSEL0	I/O Voltage Select	AB28	I	OV_{DD}	27
IO_VSEL1	I/O Voltage Select	U23	I	OV_{DD}	27
IO_VSEL2	I/O Voltage Select	AB21	I	OV_{DD}	27
IO_VSEL3	I/O Voltage Select	Y23	I	OV_{DD}	27
IO_VSEL4	I/O Voltage Select	Y21	I	OV_{DD}	27
Power and Ground Signals					
GND168	Ground	A23	—	—	—
GND167	Ground	B23	—	—	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND166	Ground	B25	—	—	—
GND165	Ground	C23	—	—	—
GND164	Ground	D23	—	—	—
GND163	Ground	D27	—	—	—
GND162	Ground	E24	—	—	—
GND161	Ground	F22	—	—	—
GND160	Ground	F27	—	—	—
GND159	Ground	G10	—	—	—
GND158	Ground	G12	—	—	—
GND157	Ground	G14	—	—	—
GND156	Ground	G16	—	—	—
GND155	Ground	G18	—	—	—
GND154	Ground	G21	—	—	—
GND153	Ground	G22	—	—	—
GND152	Ground	H3	—	—	—
GND151	Ground	H4	—	—	—
GND150	Ground	H10	—	—	—
GND149	Ground	H12	—	—	—
GND148	Ground	H14	—	—	—
GND147	Ground	H16	—	—	—
GND146	Ground	H18	—	—	—
GND145	Ground	H21	—	—	—
GND144	Ground	H25	—	—	—
GND143	Ground	J2	—	—	—
GND142	Ground	J8	—	—	—
GND141	Ground	J10	—	—	—
GND140	Ground	J12	—	—	—
GND139	Ground	J14	—	—	—
GND138	Ground	J16	—	—	—
GND137	Ground	J18	—	—	—
GND136	Ground	J21	—	—	—
GND135	Ground	K5	—	—	—
GND134	Ground	K8	—	—	—
GND133	Ground	K10	—	—	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND132	Ground	K12	—	—	—
GND131	Ground	K14	—	—	—
GND130	Ground	K16	—	—	—
GND129	Ground	K18	—	—	—
GND128	Ground	K21	—	—	—
GND127	Ground	L8	—	—	—
GND126	Ground	L10	—	—	—
GND125	Ground	L12	—	—	—
GND124	Ground	L14	—	—	—
GND123	Ground	L16	—	—	—
GND122	Ground	L18	—	—	—
GND121	Ground	M2	—	—	—
GND120	Ground	M5	—	—	—
GND119	Ground	M8	—	—	—
GND118	Ground	M10	—	—	—
GND117	Ground	M12	—	—	—
GND116	Ground	M14	—	—	—
GND115	Ground	M16	—	—	—
GND114	Ground	M18	—	—	—
GND113	Ground	N8	—	—	—
GND112	Ground	N10	—	—	—
GND111	Ground	N12	—	—	—
GND110	Ground	N14	—	—	—
GND109	Ground	N16	—	—	—
GND108	Ground	N18	—	—	—
GND107	Ground	N21	—	—	—
GND106	Ground	N25	—	—	—
GND105	Ground	P5	—	—	—
GND104	Ground	P8	—	—	—
GND103	Ground	P10	—	—	—
GND102	Ground	P12	—	—	—
GND101	Ground	P14	—	—	—
GND100	Ground	P16	—	—	—
GND099	Ground	P18	—	—	—

Table 1. Pin List by Bus (continued)

Signal	Signal Description	Package Pin Number	Pin Type	Power Supply	Note
GND098	Ground	P21	—	—	—
GND097	Ground	R2	—	—	—
GND096	Ground	R8	—	—	—
GND095	Ground	R10	—	—	—
GND094	Ground	R12	—	—	—
GND093	Ground	R14	—	—	—
GND092	Ground	R16	—	—	—
GND091	Ground	R18	—	—	—
GND090	Ground	R21	—	—	—
GND089	Ground	R24	—	—	—
GND088	Ground	R27	—	—	—
GND087	Ground	T8	—	—	—
GND086	Ground	T10	—	—	—
GND085	Ground	T12	—	—	—
GND084	Ground	T14	—	—	—
GND083	Ground	T16	—	—	—
GND082	Ground	T18	—	—	—
GND081	Ground	T21	—	—	—
GND080	Ground	U7	—	—	—
GND079	Ground	U8	—	—	—
GND078	Ground	U10	—	—	—
GND077	Ground	U12	—	—	—
GND076	Ground	U14	—	—	—
GND075	Ground	U17	—	—	—
GND074	Ground	U19	—	—	—
GND073	Ground	U22	—	—	—
GND072	Ground	U25	—	—	—
GND071	Ground	V2	—	—	—
GND070	Ground	V4	—	—	—
GND069	Ground	V6	—	—	—
GND068	Ground	V8	—	—	—
GND067	Ground	V10	—	—	—
GND066	Ground	V12	—	—	—
GND065	Ground	V14	—	—	—