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Freescale Semiconductor
Data Sheet: Technical Data

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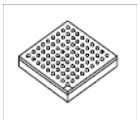
P5021

P5021 QorIQ Integrated Processor Data Sheet



FC-PBGA–1295
37.5 mm × 37.5 mm

The P5021 QorIQ integrated communication processor combines two Power Architecture® processor cores with high-performance data path acceleration logic and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and aerospace applications.

This chip can be used for combined control, data path, and application layer processing in routers, switches, base station controllers, and general-purpose embedded computing. Its high level of integration offers significant performance benefits compared to multiple discrete devices while also greatly simplifying board design.

The chip includes the following function and features:

- Two e5500 Power Architecture cores
  - Each core has a backside 512 KB L2 cache with ECC
  - Three levels of instructions: user, supervisor, and hypervisor
  - Independent boot and reset
  - Secure boot capability
- CoreNet fabric supporting coherent and non-coherent transactions amongst CoreNet endpoints
- Frontside 2 MB CoreNet platform cache with ECC
- CoreNet bridges between the CoreNet fabric the I/Os, datapath accelerators, and high and low speed peripheral interfaces
- Two 10-Gigabit Ethernet (XAUI) controllers
- Ten 1-Gigabit Ethernet controllers
  - SGMII, 2.5Gb/s SGMII and RGMII interfaces
- Two 64-bit DDR3/3L SDRAM memory controllers with ECC
- Multicore programmable interrupt controller (PIC)
- Four I^2C controllers
- Four 2-pin UARTs or two 4-pin UARTs
- Two 4-channel DMA engines
- Enhanced local bus controller (eLBC)
- Three PCI Express 2.0 controllers/ports
- Two serial ATA (SATA) 2.0 controllers
- Enhanced secure digital host controller (SD/MMC)
- Enhanced serial peripheral interface (eSPI)
- Two high-speed USB 2.0 controllers with integrated PHYs
- RAID 5 and 6 storage accelerator with support for end-to-end data protection information
- Data Path Acceleration Architecture (DPAA) incorporating acceleration for the following functions:
  - Frame Manager (FMan) for packet parsing, classification, and distribution
  - Queue Manager (QMan) for scheduling, packet sequencing and congestion management
  - Hardware Buffer Manager (BMan) for buffer allocation and deallocation
  - Encryption/Decryption
- 1295 FC-PBGA package

This figure shows the major functional units within the chip.

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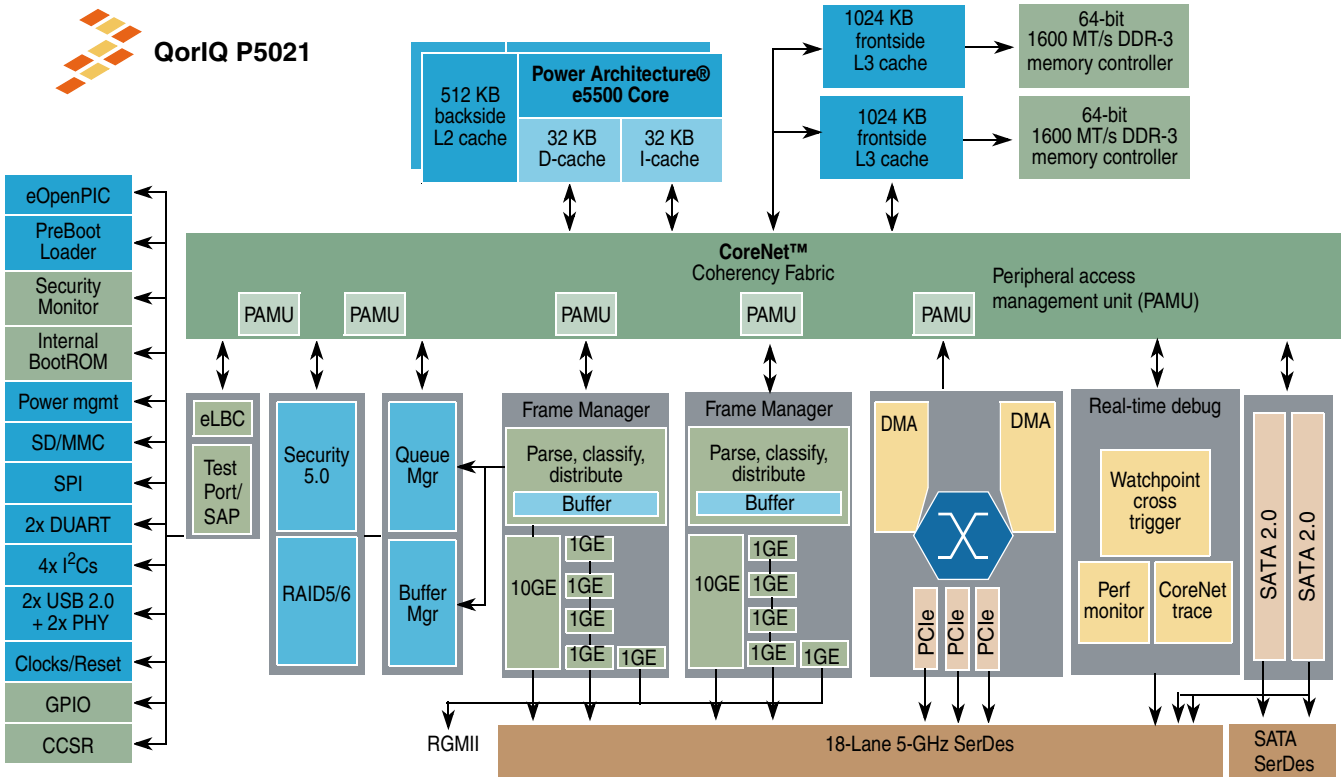
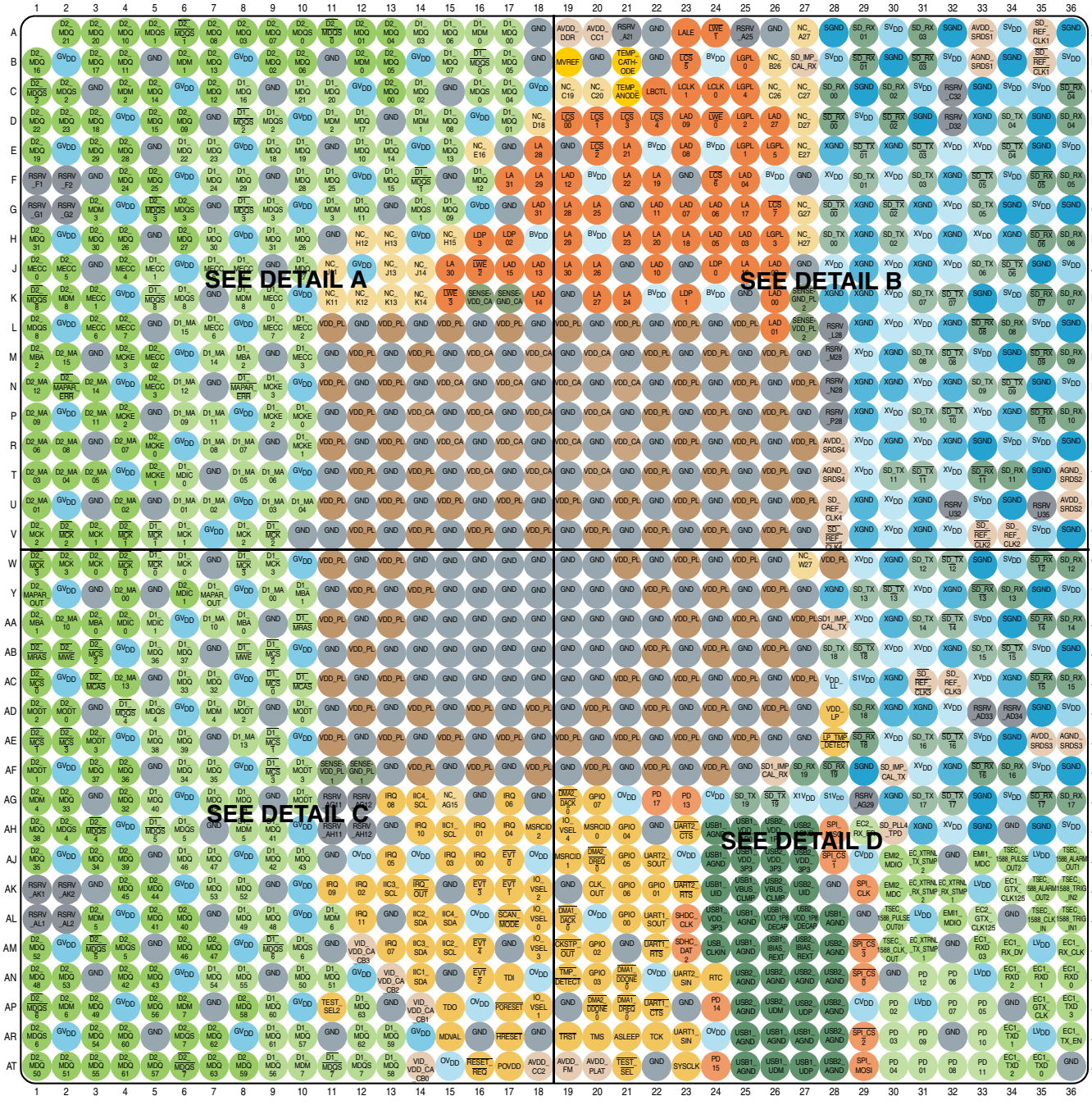


Figure 1. P5021 block diagram

1 Pin assignments and reset states

1.1 1295 FC-PBGA ball layout diagrams

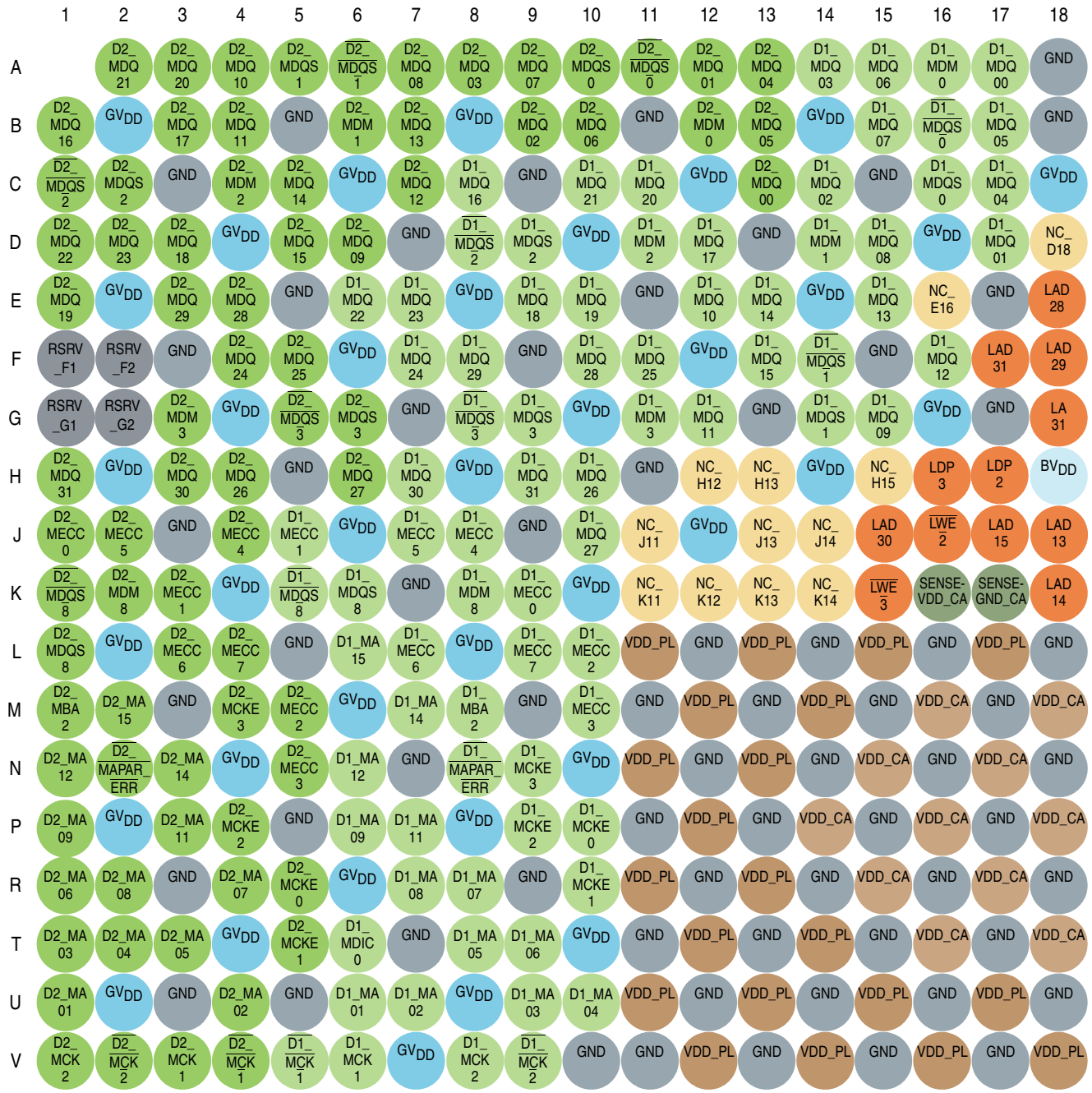
These figures show the FC-PBGA ball map diagrams.



Signal Groups

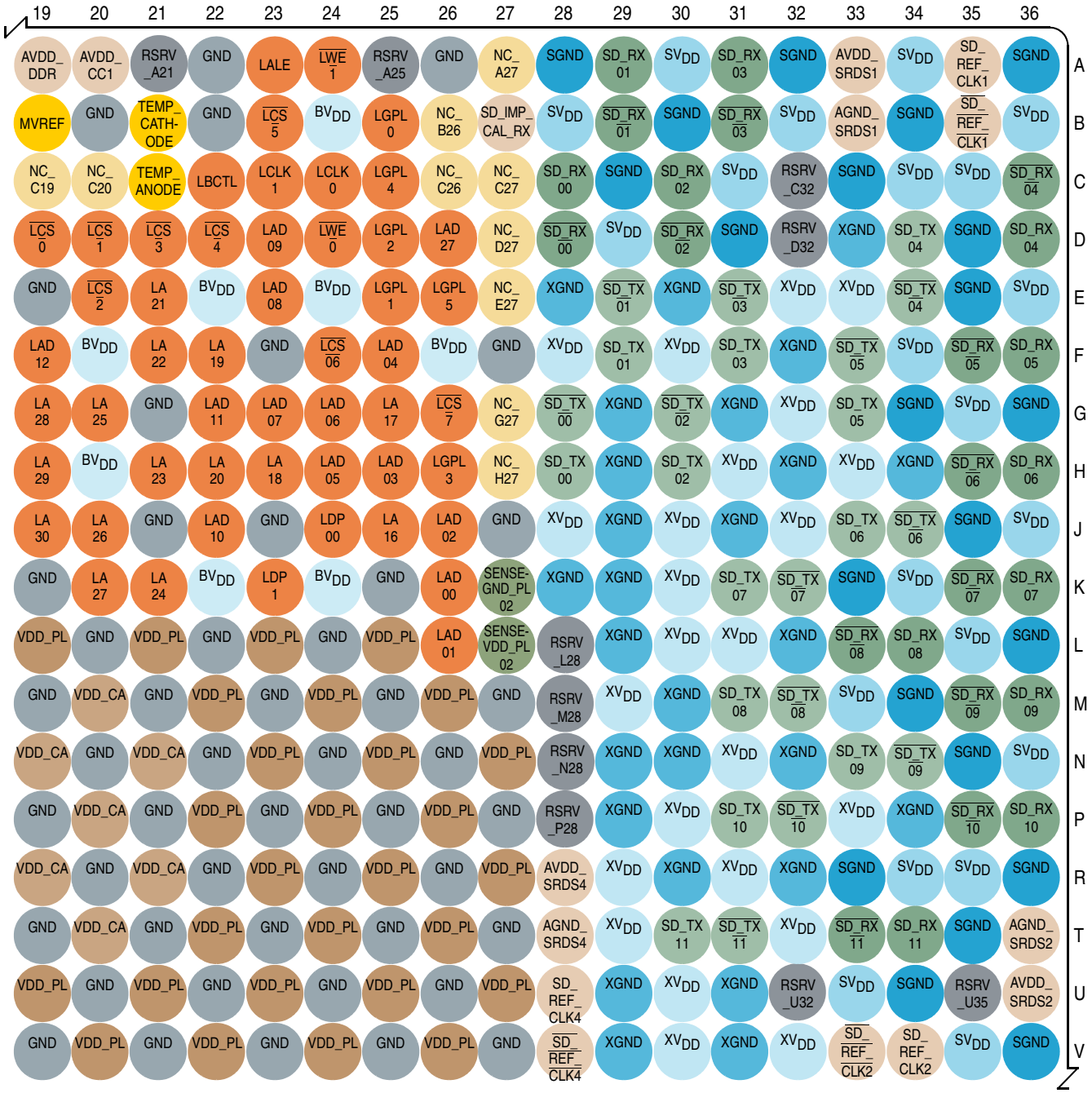
OV_{DD}	I/O Supply Voltage	SV_{DD}	SerDes Core Power Supply	$AVDD\_SRDS1$	SerDes 1 PLL Supply Voltage	$SENSE\text{-}VDD$	Core Group A Voltage Sense
LV_{DD}	I/O Supply Voltage	XV_{DD}	SerDes Transcvr Pad Supply	$AVDD\_SRDS2$	SerDes 2 PLL Supply Voltage	$SENSE\text{-}VDD\_CB$	Core Group B Voltage Sense
GV_{DD}	DDR DRAM I/O Supply	VDD_PL	Platform Supply Voltage	$AVDD\_PLAT$	Platform PLL Supply Voltage	RSRV	Reserved
CV_{DD}	SPI Voltage Supply	VDD_CA	Core Group A Supply Voltage	$AVDD\_CC$	Core PLL Supply Voltage	POVDD	Fuse Programming Override Supply
BV_{DD}	Local Bus I/O Supply			$SENSE\text{-}VDD\_PL$	Platform Voltage Sense		

Figure 2. 1295 BGA ball map diagram (top view)



DETAIL A

Figure 3. 1295 BGA ball map diagram (detail view A)



DETAIL B

Figure 4. 1295 BGA ball map diagram (detail view B)

DETAIL C

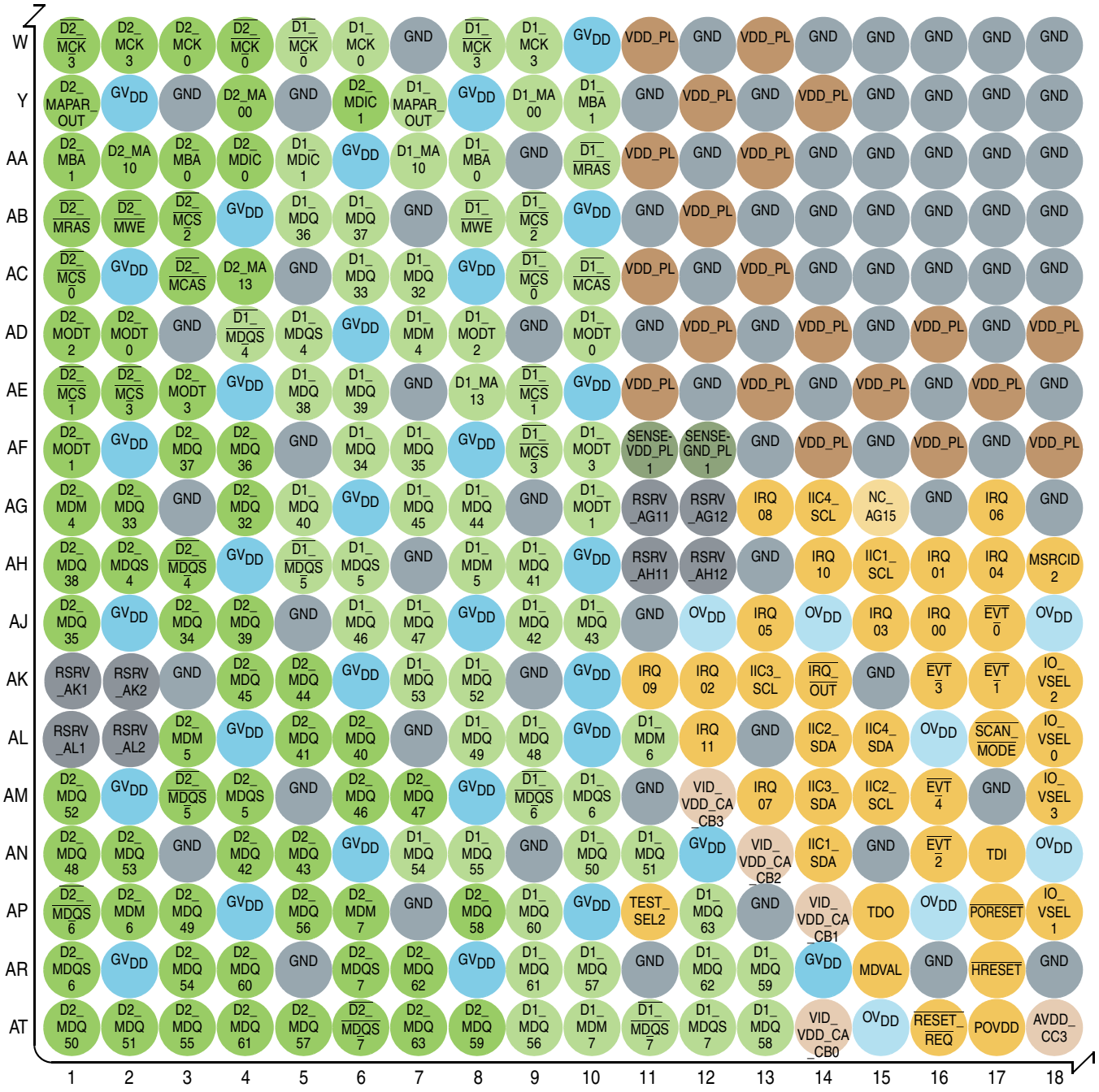


Figure 5. 1295 BGA ball map diagram (detail view C)

DETAIL D

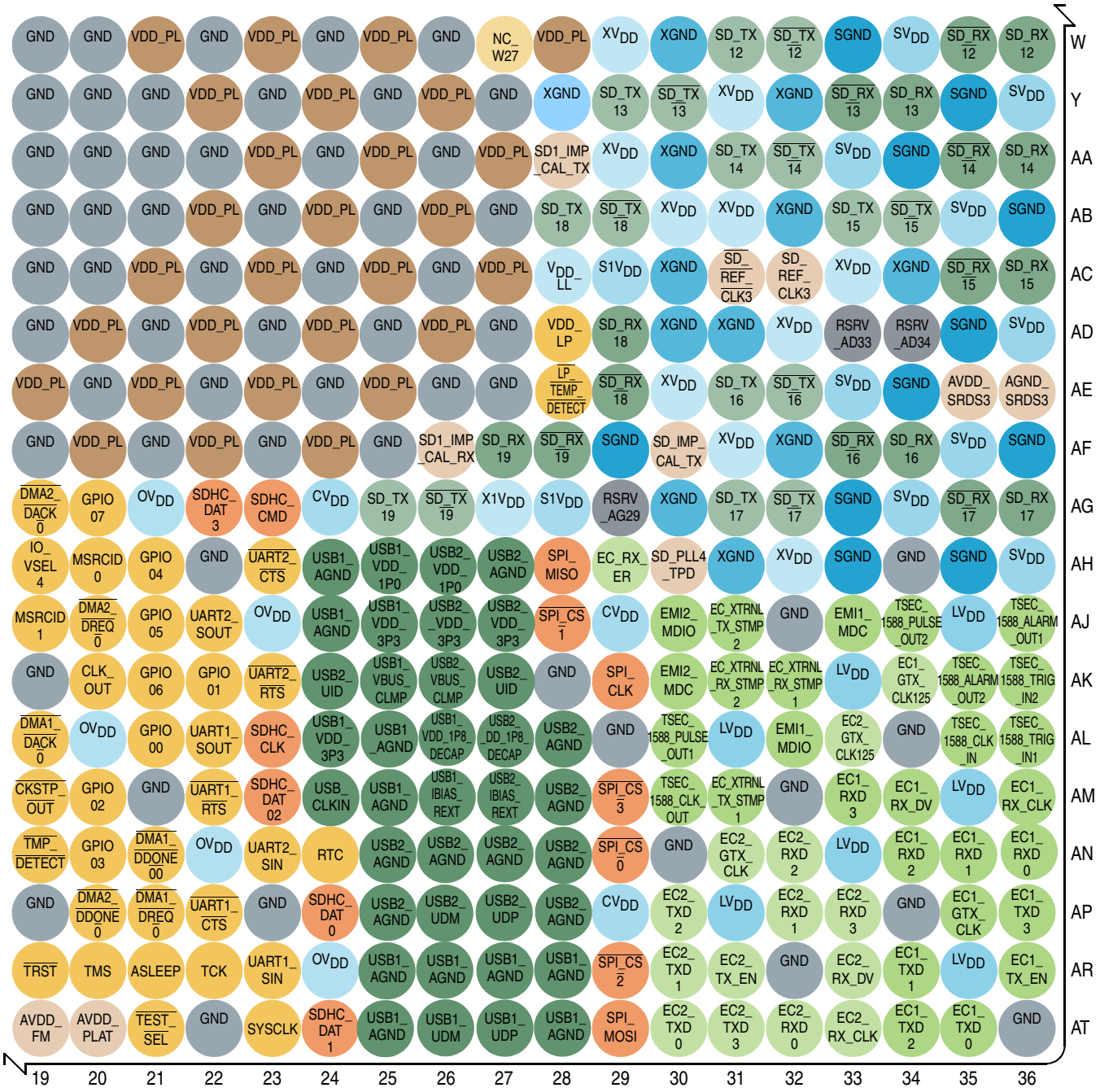


Figure 6. 1295 BGA ball map diagram (detail view D)

1.2 Pinout list

This table provides the pinout listing for the 1295 FC-PBGA package by bus.

Table 1. Pins listed by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory interface 1					
D1_MDQ00	Data	A17	I/O	GV_{DD}	—
D1_MDQ01	Data	D17	I/O	GV_{DD}	—
D1_MDQ02	Data	C14	I/O	GV_{DD}	—
D1_MDQ03	Data	A14	I/O	GV_{DD}	—
D1_MDQ04	Data	C17	I/O	GV_{DD}	—
D1_MDQ05	Data	B17	I/O	GV_{DD}	—
D1_MDQ06	Data	A15	I/O	GV_{DD}	—
D1_MDQ07	Data	B15	I/O	GV_{DD}	—
D1_MDQ08	Data	D15	I/O	GV_{DD}	—
D1_MDQ09	Data	G15	I/O	GV_{DD}	—
D1_MDQ10	Data	E12	I/O	GV_{DD}	—
D1_MDQ11	Data	G12	I/O	GV_{DD}	—
D1_MDQ12	Data	F16	I/O	GV_{DD}	—
D1_MDQ13	Data	E15	I/O	GV_{DD}	—
D1_MDQ14	Data	E13	I/O	GV_{DD}	—
D1_MDQ15	Data	F13	I/O	GV_{DD}	—
D1_MDQ16	Data	C8	I/O	GV_{DD}	—
D1_MDQ17	Data	D12	I/O	GV_{DD}	—
D1_MDQ18	Data	E9	I/O	GV_{DD}	—
D1_MDQ19	Data	E10	I/O	GV_{DD}	—
D1_MDQ20	Data	C11	I/O	GV_{DD}	—
D1_MDQ21	Data	C10	I/O	GV_{DD}	—
D1_MDQ22	Data	E6	I/O	GV_{DD}	—
D1_MDQ23	Data	E7	I/O	GV_{DD}	—
D1_MDQ24	Data	F7	I/O	GV_{DD}	—
D1_MDQ25	Data	F11	I/O	GV_{DD}	—
D1_MDQ26	Data	H10	I/O	GV_{DD}	—
D1_MDQ27	Data	J10	I/O	GV_{DD}	—
D1_MDQ28	Data	F10	I/O	GV_{DD}	—
D1_MDQ29	Data	F8	I/O	GV_{DD}	—
D1_MDQ30	Data	H7	I/O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ31	Data	H9	I/O	GV_{DD}	—
D1_MDQ32	Data	AC7	I/O	GV_{DD}	—
D1_MDQ33	Data	AC6	I/O	GV_{DD}	—
D1_MDQ34	Data	AF6	I/O	GV_{DD}	—
D1_MDQ35	Data	AF7	I/O	GV_{DD}	—
D1_MDQ36	Data	AB5	I/O	GV_{DD}	—
D1_MDQ37	Data	AB6	I/O	GV_{DD}	—
D1_MDQ38	Data	AE5	I/O	GV_{DD}	—
D1_MDQ39	Data	AE6	I/O	GV_{DD}	—
D1_MDQ40	Data	AG5	I/O	GV_{DD}	—
D1_MDQ41	Data	AH9	I/O	GV_{DD}	—
D1_MDQ42	Data	AJ9	I/O	GV_{DD}	—
D1_MDQ43	Data	AJ10	I/O	GV_{DD}	—
D1_MDQ44	Data	AG8	I/O	GV_{DD}	—
D1_MDQ45	Data	AG7	I/O	GV_{DD}	—
D1_MDQ46	Data	AJ6	I/O	GV_{DD}	—
D1_MDQ47	Data	AJ7	I/O	GV_{DD}	—
D1_MDQ48	Data	AL9	I/O	GV_{DD}	—
D1_MDQ49	Data	AL8	I/O	GV_{DD}	—
D1_MDQ50	Data	AN10	I/O	GV_{DD}	—
D1_MDQ51	Data	AN11	I/O	GV_{DD}	—
D1_MDQ52	Data	AK8	I/O	GV_{DD}	—
D1_MDQ53	Data	AK7	I/O	GV_{DD}	—
D1_MDQ54	Data	AN7	I/O	GV_{DD}	—
D1_MDQ55	Data	AN8	I/O	GV_{DD}	—
D1_MDQ56	Data	AT9	I/O	GV_{DD}	—
D1_MDQ57	Data	AR10	I/O	GV_{DD}	—
D1_MDQ58	Data	AT13	I/O	GV_{DD}	—
D1_MDQ59	Data	AR13	I/O	GV_{DD}	—
D1_MDQ60	Data	AP9	I/O	GV_{DD}	—
D1_MDQ61	Data	AR9	I/O	GV_{DD}	—
D1_MDQ62	Data	AR12	I/O	GV_{DD}	—
D1_MDQ63	Data	AP12	I/O	GV_{DD}	—
D1_MECC0	Error Correcting Code	K9	I/O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MECC1	Error Correcting Code	J5	I/O	GV_{DD}	—
D1_MECC2	Error Correcting Code	L10	I/O	GV_{DD}	—
D1_MECC3	Error Correcting Code	M10	I/O	GV_{DD}	—
D1_MECC4	Error Correcting Code	J8	I/O	GV_{DD}	—
D1_MECC5	Error Correcting Code	J7	I/O	GV_{DD}	—
D1_MECC6	Error Correcting Code	L7	I/O	GV_{DD}	—
D1_MECC7	Error Correcting Code	L9	I/O	GV_{DD}	—
$\overline{\text{D1\_MAPAR\_ERR}}$	Address Parity Error	N8	I	GV_{DD}	40
D1_MAPAR_OUT	Address Parity Out	Y7	O	GV_{DD}	—
D1_MDM0	Data Mask	A16	O	GV_{DD}	—
D1_MDM1	Data Mask	D14	O	GV_{DD}	—
D1_MDM2	Data Mask	D11	O	GV_{DD}	—
D1_MDM3	Data Mask	G11	O	GV_{DD}	—
D1_MDM4	Data Mask	AD7	O	GV_{DD}	—
D1_MDM5	Data Mask	AH8	O	GV_{DD}	—
D1_MDM6	Data Mask	AL11	O	GV_{DD}	—
D1_MDM7	Data Mask	AT10	O	GV_{DD}	—
D1_MDM8	Data Mask	K8	O	GV_{DD}	—
D1_MDQS0	Data Strobe	C16	I/O	GV_{DD}	—
D1_MDQS1	Data Strobe	G14	I/O	GV_{DD}	—
D1_MDQS2	Data Strobe	D9	I/O	GV_{DD}	—
D1_MDQS3	Data Strobe	G9	I/O	GV_{DD}	—
D1_MDQS4	Data Strobe	AD5	I/O	GV_{DD}	—
D1_MDQS5	Data Strobe	AH6	I/O	GV_{DD}	—
D1_MDQS6	Data Strobe	AM10	I/O	GV_{DD}	—
D1_MDQS7	Data Strobe	AT12	I/O	GV_{DD}	—
D1_MDQS8	Data Strobe	K6	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS0}}$	Data Strobe	B16	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS1}}$	Data Strobe	F14	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS2}}$	Data Strobe	D8	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS3}}$	Data Strobe	G8	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS4}}$	Data Strobe	AD4	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS5}}$	Data Strobe	AH5	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS6}}$	Data Strobe	AM9	I/O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQS7	Data Strobe	AT11	I/O	GV_{DD}	—
D1_MDQS8	Data Strobe	K5	I/O	GV_{DD}	—
D1_MBA0	Bank Select	AA8	O	GV_{DD}	—
D1_MBA1	Bank Select	Y10	O	GV_{DD}	—
D1_MBA2	Bank Select	M8	O	GV_{DD}	—
D1_MA00	Address	Y9	O	GV_{DD}	—
D1_MA01	Address	U6	O	GV_{DD}	—
D1_MA02	Address	U7	O	GV_{DD}	—
D1_MA03	Address	U9	O	GV_{DD}	—
D1_MA04	Address	U10	O	GV_{DD}	—
D1_MA05	Address	T8	O	GV_{DD}	—
D1_MA06	Address	T9	O	GV_{DD}	—
D1_MA07	Address	R8	O	GV_{DD}	—
D1_MA08	Address	R7	O	GV_{DD}	—
D1_MA09	Address	P6	O	GV_{DD}	—
D1_MA10	Address	AA7	O	GV_{DD}	—
D1_MA11	Address	P7	O	GV_{DD}	—
D1_MA12	Address	N6	O	GV_{DD}	—
D1_MA13	Address	AE8	O	GV_{DD}	—
D1_MA14	Address	M7	O	GV_{DD}	—
D1_MA15	Address	L6	O	GV_{DD}	—
D1_MWE	Write Enable	AB8	O	GV_{DD}	—
D1_MRAS	Row Address Strobe	AA10	O	GV_{DD}	—
D1_MCAS	Column Address Strobe	AC10	O	GV_{DD}	—
D1_MCS0	Chip Select	AC9	O	GV_{DD}	—
D1_MCS1	Chip Select	AE9	O	GV_{DD}	—
D1_MCS2	Chip Select	AB9	O	GV_{DD}	—
D1_MCS3	Chip Select	AF9	O	GV_{DD}	—
D1_MCKE0	Clock Enable	P10	O	GV_{DD}	—
D1_MCKE1	Clock Enable	R10	O	GV_{DD}	—
D1_MCKE2	Clock Enable	P9	O	GV_{DD}	—
D1_MCKE3	Clock Enable	N9	O	GV_{DD}	—
D1_MCK0	Clock	W6	O	GV_{DD}	—
D1_MCK1	Clock	V6	O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MCK2	Clock	V8	O	GV_{DD}	—
D1_MCK3	Clock	W9	O	GV_{DD}	—
$\overline{\text{D1\_MCK0}}$	Clock Complements	W5	O	GV_{DD}	—
$\overline{\text{D1\_MCK1}}$	Clock Complements	V5	O	GV_{DD}	—
$\overline{\text{D1\_MCK2}}$	Clock Complements	V9	O	GV_{DD}	—
$\overline{\text{D1\_MCK3}}$	Clock Complements	W8	O	GV_{DD}	—
D1_MODT0	On Die Termination	AD10	O	GV_{DD}	—
D1_MODT1	On Die Termination	AG10	O	GV_{DD}	—
D1_MODT2	On Die Termination	AD8	O	GV_{DD}	—
D1_MODT3	On Die Termination	AF10	O	GV_{DD}	—
D1_MDIC0	Driver Impedance Calibration	T6	I/O	GV_{DD}	16
D1_MDIC1	Driver Impedance Calibration	AA5	I/O	GV_{DD}	16
DDR SDRAM Memory interface 2					
D2_MDQ00	Data	C13	I/O	GV_{DD}	—
D2_MDQ01	Data	A12	I/O	GV_{DD}	—
D2_MDQ02	Data	B9	I/O	GV_{DD}	—
D2_MDQ03	Data	A8	I/O	GV_{DD}	—
D2_MDQ04	Data	A13	I/O	GV_{DD}	—
D2_MDQ05	Data	B13	I/O	GV_{DD}	—
D2_MDQ06	Data	B10	I/O	GV_{DD}	—
D2_MDQ07	Data	A9	I/O	GV_{DD}	—
D2_MDQ08	Data	A7	I/O	GV_{DD}	—
D2_MDQ09	Data	D6	I/O	GV_{DD}	—
D2_MDQ10	Data	A4	I/O	GV_{DD}	—
D2_MDQ11	Data	B4	I/O	GV_{DD}	—
D2_MDQ12	Data	C7	I/O	GV_{DD}	—
D2_MDQ13	Data	B7	I/O	GV_{DD}	—
D2_MDQ14	Data	C5	I/O	GV_{DD}	—
D2_MDQ15	Data	D5	I/O	GV_{DD}	—
D2_MDQ16	Data	B1	I/O	GV_{DD}	—
D2_MDQ17	Data	B3	I/O	GV_{DD}	—
D2_MDQ18	Data	D3	I/O	GV_{DD}	—
D2_MDQ19	Data	E1	I/O	GV_{DD}	—
D2_MDQ20	Data	A3	I/O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MDQ21	Data	A2	I/O	GV_{DD}	—
D2_MDQ22	Data	D1	I/O	GV_{DD}	—
D2_MDQ23	Data	D2	I/O	GV_{DD}	—
D2_MDQ24	Data	F4	I/O	GV_{DD}	—
D2_MDQ25	Data	F5	I/O	GV_{DD}	—
D2_MDQ26	Data	H4	I/O	GV_{DD}	—
D2_MDQ27	Data	H6	I/O	GV_{DD}	—
D2_MDQ28	Data	E4	I/O	GV_{DD}	—
D2_MDQ29	Data	E3	I/O	GV_{DD}	—
D2_MDQ30	Data	H3	I/O	GV_{DD}	—
D2_MDQ31	Data	H1	I/O	GV_{DD}	—
D2_MDQ32	Data	AG4	I/O	GV_{DD}	—
D2_MDQ33	Data	AG2	I/O	GV_{DD}	—
D2_MDQ34	Data	AJ3	I/O	GV_{DD}	—
D2_MDQ35	Data	AJ1	I/O	GV_{DD}	—
D2_MDQ36	Data	AF4	I/O	GV_{DD}	—
D2_MDQ37	Data	AF3	I/O	GV_{DD}	—
D2_MDQ38	Data	AH1	I/O	GV_{DD}	—
D2_MDQ39	Data	AJ4	I/O	GV_{DD}	—
D2_MDQ40	Data	AL6	I/O	GV_{DD}	—
D2_MDQ41	Data	AL5	I/O	GV_{DD}	—
D2_MDQ42	Data	AN4	I/O	GV_{DD}	—
D2_MDQ43	Data	AN5	I/O	GV_{DD}	—
D2_MDQ44	Data	AK5	I/O	GV_{DD}	—
D2_MDQ45	Data	AK4	I/O	GV_{DD}	—
D2_MDQ46	Data	AM6	I/O	GV_{DD}	—
D2_MDQ47	Data	AM7	I/O	GV_{DD}	—
D2_MDQ48	Data	AN1	I/O	GV_{DD}	—
D2_MDQ49	Data	AP3	I/O	GV_{DD}	—
D2_MDQ50	Data	AT1	I/O	GV_{DD}	—
D2_MDQ51	Data	AT2	I/O	GV_{DD}	—
D2_MDQ52	Data	AM1	I/O	GV_{DD}	—
D2_MDQ53	Data	AN2	I/O	GV_{DD}	—
D2_MDQ54	Data	AR3	I/O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MDQ55	Data	AT3	I/O	GV_{DD}	—
D2_MDQ56	Data	AP5	I/O	GV_{DD}	—
D2_MDQ57	Data	AT5	I/O	GV_{DD}	—
D2_MDQ58	Data	AP8	I/O	GV_{DD}	—
D2_MDQ59	Data	AT8	I/O	GV_{DD}	—
D2_MDQ60	Data	AR4	I/O	GV_{DD}	—
D2_MDQ61	Data	AT4	I/O	GV_{DD}	—
D2_MDQ62	Data	AR7	I/O	GV_{DD}	—
D2_MDQ63	Data	AT7	I/O	GV_{DD}	—
D2_MECC0	Error Correcting Code	J1	I/O	GV_{DD}	—
D2_MECC1	Error Correcting Code	K3	I/O	GV_{DD}	—
D2_MECC2	Error Correcting Code	M5	I/O	GV_{DD}	—
D2_MECC3	Error Correcting Code	N5	I/O	GV_{DD}	—
D2_MECC4	Error Correcting Code	J4	I/O	GV_{DD}	—
D2_MECC5	Error Correcting Code	J2	I/O	GV_{DD}	—
D2_MECC6	Error Correcting Code	L3	I/O	GV_{DD}	—
D2_MECC7	Error Correcting Code	L4	I/O	GV_{DD}	—
$\overline{\text{D2\_MAPAR\_ERR}}$	Address Parity Error	N2	I	GV_{DD}	—
D2_MAPAR_OUT	Address Parity Out	Y1	O	GV_{DD}	—
D2_MDM0	Data Mask	B12	O	GV_{DD}	—
D2_MDM1	Data Mask	B6	O	GV_{DD}	—
D2_MDM2	Data Mask	C4	O	GV_{DD}	—
D2_MDM3	Data Mask	G3	O	GV_{DD}	—
D2_MDM4	Data Mask	AG1	O	GV_{DD}	—
D2_MDM5	Data Mask	AL3	O	GV_{DD}	—
D2_MDM6	Data Mask	AP2	O	GV_{DD}	—
D2_MDM7	Data Mask	AP6	O	GV_{DD}	—
D2_MDM8	Data Mask	K2	O	GV_{DD}	—
D2_MDQS0	Data Strobe	A10	I/O	GV_{DD}	—
D2_MDQS1	Data Strobe	A5	I/O	GV_{DD}	—
D2_MDQS2	Data Strobe	C2	I/O	GV_{DD}	—
D2_MDQS3	Data Strobe	G6	I/O	GV_{DD}	—
D2_MDQS4	Data Strobe	AH2	I/O	GV_{DD}	—
D2_MDQS5	Data Strobe	AM4	I/O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MDQS6	Data Strobe	AR1	I/O	GV_{DD}	—
D2_MDQS7	Data Strobe	AR6	I/O	GV_{DD}	—
D2_MDQS8	Data Strobe	L1	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS0}}$	Data Strobe	A11	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS1}}$	Data Strobe	A6	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS2}}$	Data Strobe	C1	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS3}}$	Data Strobe	G5	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS4}}$	Data Strobe	AH3	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS5}}$	Data Strobe	AM3	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS6}}$	Data Strobe	AP1	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS7}}$	Data Strobe	AT6	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS8}}$	Data Strobe	K1	I/O	GV_{DD}	—
D2_MBA0	Bank Select	AA3	O	GV_{DD}	—
D2_MBA1	Bank Select	AA1	O	GV_{DD}	—
D2_MBA2	Bank Select	M1	O	GV_{DD}	—
D2_MA00	Address	Y4	O	GV_{DD}	—
D2_MA01	Address	U1	O	GV_{DD}	—
D2_MA02	Address	U4	O	GV_{DD}	—
D2_MA03	Address	T1	O	GV_{DD}	—
D2_MA04	Address	T2	O	GV_{DD}	—
D2_MA05	Address	T3	O	GV_{DD}	—
D2_MA06	Address	R1	O	GV_{DD}	—
D2_MA07	Address	R4	O	GV_{DD}	—
D2_MA08	Address	R2	O	GV_{DD}	—
D2_MA09	Address	P1	O	GV_{DD}	—
D2_MA10	Address	AA2	O	GV_{DD}	—
D2_MA11	Address	P3	O	GV_{DD}	—
D2_MA12	Address	N1	O	GV_{DD}	—
D2_MA13	Address	AC4	O	GV_{DD}	—
D2_MA14	Address	N3	O	GV_{DD}	—
D2_MA15	Address	M2	O	GV_{DD}	—
$\overline{\text{D2\_MWE}}$	Write Enable	AB2	O	GV_{DD}	—
$\overline{\text{D2\_MRAS}}$	Row Address Strobe	AB1	O	GV_{DD}	—
$\overline{\text{D2\_MCAS}}$	Column Address Strobe	AC3	O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
$\overline{\text{D2\_MCS0}}$	Chip Select	AC1	O	GV_{DD}	—
$\overline{\text{D2\_MCS1}}$	Chip Select	AE1	O	GV_{DD}	—
$\overline{\text{D2\_MCS2}}$	Chip Select	AB3	O	GV_{DD}	—
$\overline{\text{D2\_MCS3}}$	Chip Select	AE2	O	GV_{DD}	—
D2_MCKE0	Clock Enable	R5	O	GV_{DD}	—
D2_MCKE1	Clock Enable	T5	O	GV_{DD}	—
D2_MCKE2	Clock Enable	P4	O	GV_{DD}	—
D2_MCKE3	Clock Enable	M4	O	GV_{DD}	—
D2_MCK0	Clock	W3	O	GV_{DD}	—
D2_MCK1	Clock	V3	O	GV_{DD}	—
D2_MCK2	Clock	V1	O	GV_{DD}	—
D2_MCK3	Clock	W2	O	GV_{DD}	—
$\overline{\text{D2\_MCK0}}$	Clock Complements	W4	O	GV_{DD}	—
$\overline{\text{D2\_MCK1}}$	Clock Complements	V4	O	GV_{DD}	—
$\overline{\text{D2\_MCK2}}$	Clock Complements	V2	O	GV_{DD}	—
$\overline{\text{D2\_MCK3}}$	Clock Complements	W1	O	GV_{DD}	—
D2_MODT0	On Die Termination	AD2	O	GV_{DD}	—
D2_MODT1	On Die Termination	AF1	O	GV_{DD}	—
D2_MODT2	On Die Termination	AD1	O	GV_{DD}	—
D2_MODT3	On Die Termination	AE3	O	GV_{DD}	—
D2_MDIC0	Driver Impedance Calibration	AA4	I/O	GV_{DD}	16
D2_MDIC1	Driver Impedance Calibration	Y6	I/O	GV_{DD}	16
Local bus controller interface					
LAD00	Muxed Data/Address	K26	I/O	BV_{DD}	3
LAD01	Muxed Data/Address	L26	I/O	BV_{DD}	3
LAD02	Muxed Data/Address	J26	I/O	BV_{DD}	3
LAD03	Muxed Data/Address	H25	I/O	BV_{DD}	3
LAD04	Muxed Data/Address	F25	I/O	BV_{DD}	3
LAD05	Muxed Data/Address	H24	I/O	BV_{DD}	3
LAD06	Muxed Data/Address	G24	I/O	BV_{DD}	3
LAD07	Muxed Data/Address	G23	I/O	BV_{DD}	3
LAD08	Muxed Data/Address	E23	I/O	BV_{DD}	3
LAD09	Muxed Data/Address	D23	I/O	BV_{DD}	3
LAD10	Muxed Data/Address	J22	I/O	BV_{DD}	3

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
LAD11	Muxed Data/Address	G22	I/O	BV_{DD}	3
LAD12	Muxed Data/Address	F19	I/O	BV_{DD}	3
LAD13	Muxed Data/Address	J18	I/O	BV_{DD}	3
LAD14	Muxed Data/Address	K18	I/O	BV_{DD}	3
LAD15	Muxed Data/Address	J17	I/O	BV_{DD}	3
LAD16	Muxed Data/Address	J25	I/O	BV_{DD}	3
LAD17	Muxed Data/Address	G25	I/O	BV_{DD}	3
LAD18	Muxed Data/Address	H23	I/O	BV_{DD}	3,35
LAD19	Muxed Data/Address	F22	I/O	BV_{DD}	3,35
LAD20	Muxed Data/Address	H22	I/O	BV_{DD}	3,35
LAD21	Muxed Data/Address	E21	I/O	BV_{DD}	3,35
LAD22	Muxed Data/Address	F21	I/O	BV_{DD}	3,35
LAD23	Muxed Data/Address	H21	I/O	BV_{DD}	3
LAD24	Muxed Data/Address	K21	I/O	BV_{DD}	3
LAD25	Muxed Data/Address	G20	I/O	BV_{DD}	3,35
LAD26	Muxed Data/Address	J20	I/O	BV_{DD}	32
LAD27	Muxed Data/Address	D26	I/O	BV_{DD}	—
LAD28	Muxed Data/Address	E18	I/O	BV_{DD}	—
LAD29	Muxed Data/Address	F18	I/O	BV_{DD}	—
LAD30	Muxed Data/Address	J15	I/O	BV_{DD}	—
LAD31	Muxed Data/Address	F17	I/O	BV_{DD}	—
LDP0	Data Parity	J24	I/O	BV_{DD}	—
LDP1	Data Parity	K23	I/O	BV_{DD}	—
LDP2	Data Parity	H17	I/O	BV_{DD}	—
LDP3	Data Parity	H16	I/O	BV_{DD}	—
LA27	Address	K20	O	BV_{DD}	—
LA28	Address	G19	O	BV_{DD}	35
LA29	Address	H19	O	BV_{DD}	35
LA30	Address	J19	O	BV_{DD}	35
LA31	Address	G18	O	BV_{DD}	35
$\overline{\text{LCS0}}$	Chip Selects	D19	O	BV_{DD}	5
$\overline{\text{LCS1}}$	Chip Selects	D20	O	BV_{DD}	5
$\overline{\text{LCS2}}$	Chip Selects	E20	O	BV_{DD}	5
$\overline{\text{LCS3}}$	Chip Selects	D21	O	BV_{DD}	5

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
$\overline{\text{LCS4}}$	Chip Selects	D22	O	BV_{DD}	5
$\overline{\text{LCS5}}$	Chip Selects	B23	O	BV_{DD}	5
$\overline{\text{LCS6}}$	Chip Selects	F24	O	BV_{DD}	5
$\overline{\text{LCS7}}$	Chip Selects	G26	O	BV_{DD}	5
$\overline{\text{LWE0}}$	Write Enable	D24	O	BV_{DD}	—
$\overline{\text{LWE1}}$	Write Enable	A24	O	BV_{DD}	—
$\overline{\text{LWE2}}$	Write Enable	J16	O	BV_{DD}	—
$\overline{\text{LWE3}}$	Write Enable	K15	O	BV_{DD}	—
LBCTL	Buffer Control	C22	O	BV_{DD}	—
LALE	Address Latch Enable	A23	I/O	BV_{DD}	—
LGPL0/LFCLE	UPM General Purpose Line 0/ LFCLE—FCM	B25	O	BV_{DD}	3, 4
LGPL1/LFALE	UPM General Purpose Line 1/ LFALE—FCM	E25	O	BV_{DD}	3, 4
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM General Purpose Line 2/ LOE_B—Output Enable	D25	O	BV_{DD}	3, 4
LGPL3/$\overline{\text{LFWP}}$	UPM General Purpose LIne 3/ LFWP_B—FCM	H26	O	BV_{DD}	3, 4
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	UPM General Purpose Line 4/ LGTA_B—FCM	C25	I/O	BV_{DD}	39
LGPL5	UPM General Purpose Line 5 / Amux	E26	O	BV_{DD}	3, 4
LCLK0	Local Bus Clock	C24	O	BV_{DD}	—
LCLK1	Local Bus Clock	C23	O	BV_{DD}	—
DMA					
$\overline{\text{DMA1\_DREQ0}}$/GPIO18	DMA1 Channel 0 Request	AP21	I	OV_{DD}	26
$\overline{\text{DMA1\_DACK0}}$/GPIO19	DMA1 Channel 0 Acknowledge	AL19	O	OV_{DD}	26
$\overline{\text{DMA1\_DDONE0}}$	DMA1 Channel 0 Done	AN21	O	OV_{DD}	27
$\overline{\text{DMA2\_DREQ0}}$/GPIO20/ALT_MDVAL	DMA2 Channel 0 Request	AJ20	I	OV_{DD}	26
$\overline{\text{DMA2\_DACK0}}$/$\overline{\text{EVT7}}$/ALT_MDSRCID0	DMA2 Channel 0 Acknowledge	AG19	O	OV_{DD}	26
$\overline{\text{DMA2\_DDONE0}}$/$\overline{\text{EVT8}}$/ALT_MDSRCID1	DMA2 Channel 0 Done	AP20	O	OV_{DD}	26
USB Port 1					
USB1_UDP	USB1 PHY Data Plus	AT27	I/O	USB_V_{DD}_3P3	—
USB1_UDM	USB1 PHY Data Minus	AT26	I/O	USB_V_{DD}_3P3	—
USB1_VBUS_CLMP	USB1 PHY VBUS Divided Signal	AK25	I	USB_V_{DD}_3P3	38

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB1_UID	USB1 PHY ID Detect	AK24	I	USB1_V_{DD}_1P8_DECAP	—
USB1_DRVVBUS/GPIO04	USB1 5V Supply Enable	AH21	O	OV_{DD}	26,38
USB1_PWRFAULT/GPIO05	USB1 Power Fault	AJ21	I	OV_{DD}	26,38
USB_CLKIN	USB PHY Clock Input	AM24	I	OV_{DD}	—
USB Port 2					
USB2_UDP	USB2 PHY Data Plus	AP27	I/O	USB_V_{DD}_3P3	—
USB2_UDM	USB2 PHY Data Minus	AP26	I/O	USB_V_{DD}_3P3	—
USB2_VBUS_CLMP	USB2 PHY VBUS Divided Signal	AK26	I	USB_V_{DD}_3P3	38
USB2_UID	USB2 PHY ID Detect	AK27	I	USB2_V_{DD}_1P8_DECAP	—
USB2_DRVVBUS/GPIO06	USB2 5V Supply Enable	AK21	O	OV_{DD}	26,38
USB2_PWRFAULT/GPIO07	USB2 Power Fault	AG20	O	OV_{DD}	26,38
Programmable Interrupt controller					
IRQ00	External Interrupts	AJ16	I	OV_{DD}	—
IRQ01	External Interrupts	AH16	I	OV_{DD}	—
IRQ02	External Interrupts	AK12	I	OV_{DD}	—
IRQ03/GPIO21	External Interrupts	AJ15	I	OV_{DD}	26
IRQ04/GPIO22	External Interrupts	AH17	I	OV_{DD}	26
IRQ05/GPIO23	External Interrupts	AJ13	I	OV_{DD}	26
IRQ06/GPIO24	External Interrupts	AG17	I	OV_{DD}	26
IRQ07/GPIO25	External Interrupts	AM13	I	OV_{DD}	26
IRQ08/GPIO26	External Interrupts	AG13	I	OV_{DD}	26
IRQ09/GPIO27	External Interrupts	AK11	I	OV_{DD}	26
IRQ10/GPIO28	External Interrupts	AH14	I	OV_{DD}	26
IRQ11/GPIO29	External Interrupts	AL12	I	OV_{DD}	26
$\overline{\text{IRQ\_OUT}}$/EVT9	Interrupt Output	AK14	O	OV_{DD}	1, 2, 26
Trust					
$\overline{\text{TMP\_DETECT}}$	Tamper Detect	AN19	I	OV_{DD}	27
$\overline{\text{LP\_TMP\_DETECT}}$	Low Power Tamper Detect	AE28	I	V_{DD_LP}	—
eSDHC					
SDHC_CMD	Command/Response	AG23	I/O	CV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SDHC_DAT0	Data	AP24	I/O	CV_{DD}	—
SDHC_DAT1	Data	AT24	I/O	CV_{DD}	—
SDHC_DAT2	Data	AM23	I/O	CV_{DD}	—
SDHC_DAT3	Data	AG22	I/O	CV_{DD}	—
SDHC_DAT4/$\overline{\text{SPI\_CS0}}$	Data	AN29	I/O	CV_{DD}	26, 31
SDHC_DAT5/$\overline{\text{SPI\_CS1}}$	Data	AJ28	I/O	CV_{DD}	26, 31
SDHC_DAT6/$\overline{\text{SPI\_CS2}}$	Data	AR29	I/O	CV_{DD}	26, 31
SDHC_DAT7/$\overline{\text{SPI\_CS3}}$	Data	AM29	I/O	CV_{DD}	26, 31
SDHC_CLK	Host to Card Clock	AL23	O	CV_{DD}	—
$\overline{\text{SDHC\_CD}}$/IIC3_SCL/GPIO16	Card Detection	AK13	I	OV_{DD}	26,27,31
SDHC_WP/IIC3_SDA/GPIO17	Card Write Protection	AM14	I	OV_{DD}	26,27,31
eSPI					
SPI_MOSI	Master Out Slave In	AT29	I/O	CV_{DD}	—
SPI_MISO	Master In Slave Out	AH28	I	CV_{DD}	—
SPI_CLK	eSPI clock	AK29	O	CV_{DD}	—
$\overline{\text{SPI\_CS0}}$/SDHC_DAT4	eSPI chip select	AN29	O	CV_{DD}	26
$\overline{\text{SPI\_CS1}}$/SDHC_DAT5	eSPI chip select	AJ28	O	CV_{DD}	26
$\overline{\text{SPI\_CS2}}$/SDHC_DAT6	eSPI chip select	AR29	O	CV_{DD}	26
$\overline{\text{SPI\_CS3}}$/SDHC_DAT7	eSPI chip select	AM29	O	CV_{DD}	26
IEEE 1588					
TSEC_1588_CLK_IN	Clock In	AL35	I	LV_{DD}	—
TSEC_1588_TRIG_IN1	Trigger In 1	AL36	I	LV_{DD}	—
TSEC_1588_TRIG_IN2/EC1_RX_ER	Trigger In 2	AK36	I	LV_{DD}	—
TSEC_1588_ALARM_OUT1	Alarm Out 1	AJ36	O	LV_{DD}	—
TSEC_1588_ALARM_OUT2/EC1_COL/GPIO30	Alarm Out 2	AK35	O	LV_{DD}	26
TSEC_1588_CLK_OUT	Clock Out	AM30	O	LV_{DD}	—
TSEC_1588_PULSE_OUT1	Pulse Out1	AL30	O	LV_{DD}	—
TSEC_1588_PULSE_OUT2/EC1_CRS/GPIO31	Pulse Out2	AJ34	O	LV_{DD}	26
Ethernet Management interface 1					
EMI1_MDC	Management Data Clock	AJ33	O	LV_{DD}	—
EMI1_MDIO	Management Data In/Out	AL32	I/O	LV_{DD}	—
Ethernet Management interface 2					
EMI2_MDC	Management Data Clock	AK30	O	1.2 V	2, 18, 22

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EMI2_MDIO	Management Data In/Out	AJ30	I/O	1.2 V	2, 18, 22
Ethernet Reference Clock					
EC1_GTX_CLK125/ EC1_TX_CLK	Reference Clock (RGMII) Transmit Clock (MII)	AK34	I	LV_{DD}	27
EC2_GTX_CLK125/ EC2_TX_CLK	Reference Clock (RGMII) Transmit Clock (MII)	AL33	I	LV_{DD}	27
Ethernet External Timestamping					
EC_XTRNL_TX_STMP1	External Timestamp Transmit 1	AM31	I	LV_{DD}	—
EC_XTRNL_RX_STMP1	External Timestamp Receive 1	AK32	I	LV_{DD}	—
EC_XTRNL_TX_STMP2/EC2_COL	External Timestamp Transmit 2	AJ31	I	LV_{DD}	—
EC_XTRNL_RX_STMP2/EC2_CRS	External Timestamp Receive 2	AK31	I	LV_{DD}	—
Three-Speed Ethernet controller 1					
EC1_TXD3	Transmit Data	AP36	O	LV_{DD}	35
EC1_TXD2	Transmit Data	AT34	O	LV_{DD}	35
EC1_TXD1	Transmit Data	AR34	O	LV_{DD}	35
EC1_TXD0	Transmit Data	AT35	O	LV_{DD}	35
EC1_TX_EN	Transmit Enable	AR36	O	LV_{DD}	15
EC1_GTX_CLK/ EC1_TX_ER	Transmit Clock Out (RGMII) Transmit Error (MII)	AP35	O	LV_{DD}	26
EC1_RXD3	Receive Data	AM33	I	LV_{DD}	27
EC1_RXD2	Receive Data	AN34	I	LV_{DD}	27
EC1_RXD1	Receive Data	AN35	I	LV_{DD}	27
EC1_RXD0	Receive Data	AN36	I	LV_{DD}	27
EC1_RX_DV	Receive Data Valid	AM34	I	LV_{DD}	27
EC1_RX_CLK	Receive Clock	AM36	I	LV_{DD}	27
EC1_RX_ER/TSEC_1588_TRIG_IN2	Receive Error (MII)	AK36	I	LV_{DD}	—
EC1_COL/GPIO30/TSEC_1588_ALARM_OUT2	Collision Detect (MII)	AK35	O	LV_{DD}	26
EC1_CRS/GPIO31/TSEC_1588_PULSE_OUT2	Carrier Sense (MII)	AJ34	O	LV_{DD}	26
Three-Speed Ethernet controller 2					
EC2_TXD3	Transmit Data	AT31	O	LV_{DD}	35
EC2_TXD2	Transmit Data	AP30	O	LV_{DD}	35
EC2_TXD1	Transmit Data	AR30	O	LV_{DD}	35
EC2_TXD0	Transmit Data	AT30	O	LV_{DD}	35
EC2_TX_EN	Transmit Enable	AR31	O	LV_{DD}	15

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EC2_GTX_CLK/ EC2_TX_ER	Transmit Clock Out (RGMII) Transmit Error (MII)	AN31	O	LV_{DD}	26
EC2_RXD3	Receive Data	AP33	I	LV_{DD}	27
EC2_RXD2	Receive Data	AN32	I	LV_{DD}	27
EC2_RXD1	Receive Data	AP32	I	LV_{DD}	26, 27
EC2_RXD0	Receive Data	AT32	I	LV_{DD}	26, 27
EC2_RX_DV	Receive Data Valid	AR33	I	LV_{DD}	27
EC2_RX_CLK	Receive Clock	AT33	I	LV_{DD}	27
EC2_RX_ER	Receive Error (MII)	AH29	I	LV_{DD}	—
EC2_COL/EC_XTRNL_TX_STMP2	Collision Detect (MII)	AJ31	O	LV_{DD}	26
EC2_CRS/EC_XTRNL_RX_STMP2	Carrier Sense (MII)	AK31	O	LV_{DD}	26
UART					
UART1_SOUT/GPIO8	Transmit Data	AL22	O	OV_{DD}	26
UART2_SOUT/GPIO9	Transmit Data	AJ22	O	OV_{DD}	26
UART1_SIN/GPIO10	Receive Data	AR23	I	OV_{DD}	26
UART2_SIN/GPIO11	Receive Data	AN23	I	OV_{DD}	26
$\overline{\text{UART1\_RTS}}$/UART3_SOUT/GPIO12	Ready to Send	AM22	O	OV_{DD}	26
$\overline{\text{UART2\_RTS}}$/UART4_SOUT/GPIO13	Ready to Send	AK23	O	OV_{DD}	26
$\overline{\text{UART1\_CTS}}$/UART3_SIN/GPIO14	Clear to Send	AP22	I	OV_{DD}	26
$\overline{\text{UART2\_CTS}}$/UART4_SIN/GPIO15	Clear to Send	AH23	I	OV_{DD}	26
I^2C interface					
IIC1_SCL	Serial Clock	AH15	I/O	OV_{DD}	2, 14
IIC1_SDA	Serial Data	AN14	I/O	OV_{DD}	2, 14
IIC2_SCL	Serial Clock	AM15	I/O	OV_{DD}	2, 14
IIC2_SDA	Serial Data	AL14	I/O	OV_{DD}	2, 14
IIC3_SCL/$\overline{\text{SDHC\_CD}}$/GPIO16	Serial Clock	AK13	I/O	OV_{DD}	2, 14, 27
IIC3_SDA/SDHC_WP/GPIO17	Serial Data	AM14	I/O	OV_{DD}	2, 14, 27
IIC4_SCL/$\overline{\text{EVT5}}$	Serial Clock	AG14	I/O	OV_{DD}	2, 14
IIC4_SDA/$\overline{\text{EVT6}}$	Serial Data	AL15	I/O	OV_{DD}	2, 14
SerDes (x20) PCIe, Aurora, 10GE, 1GE, SATA					
SD_TX19	Transmit Data (positive)	AG25	O	XV_{DD}	—
SD_TX18	Transmit Data (positive)	AB28	O	XV_{DD}	—
SD_TX17	Transmit Data (positive)	AG31	O	XV_{DD}	—
SD_TX16	Transmit Data (positive)	AE31	O	XV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_TX15	Transmit Data (positive)	AB33	O	XV_{DD}	—
SD_TX14	Transmit Data (positive)	AA31	O	XV_{DD}	—
SD_TX13	Transmit Data (positive)	Y29	O	XV_{DD}	—
SD_TX12	Transmit Data (positive)	W31	O	XV_{DD}	—
SD_TX11	Transmit Data (positive)	T30	O	XV_{DD}	—
SD_TX10	Transmit Data (positive)	P31	O	XV_{DD}	—
SD_TX09	Transmit Data (positive)	N33	O	XV_{DD}	—
SD_TX08	Transmit Data (positive)	M31	O	XV_{DD}	—
SD_TX07	Transmit Data (positive)	K31	O	XV_{DD}	—
SD_TX06	Transmit Data (positive)	J33	O	XV_{DD}	—
SD_TX05	Transmit Data (positive)	G33	O	XV_{DD}	—
SD_TX04	Transmit Data (positive)	D34	O	XV_{DD}	—
SD_TX03	Transmit Data (positive)	F31	O	XV_{DD}	—
SD_TX02	Transmit Data (positive)	H30	O	XV_{DD}	—
SD_TX01	Transmit Data (positive)	F29	O	XV_{DD}	—
SD_TX00	Transmit Data (positive)	H28	O	XV_{DD}	—
$\overline{\text{SD\_TX19}}$	Transmit Data (negative)	AG26	O	XV_{DD}	—
$\overline{\text{SD\_TX18}}$	Transmit Data (negative)	AB29	O	XV_{DD}	—
$\overline{\text{SD\_TX17}}$	Transmit Data (negative)	AG32	O	XV_{DD}	—
$\overline{\text{SD\_TX16}}$	Transmit Data (negative)	AE32	O	XV_{DD}	—
$\overline{\text{SD\_TX15}}$	Transmit Data (negative)	AB34	O	XV_{DD}	—
$\overline{\text{SD\_TX14}}$	Transmit Data (negative)	AA32	O	XV_{DD}	—
$\overline{\text{SD\_TX13}}$	Transmit Data (negative)	Y30	O	XV_{DD}	—
$\overline{\text{SD\_TX12}}$	Transmit Data (negative)	W32	O	XV_{DD}	—
$\overline{\text{SD\_TX11}}$	Transmit Data (negative)	T31	O	XV_{DD}	—
$\overline{\text{SD\_TX10}}$	Transmit Data (negative)	P32	O	XV_{DD}	—
$\overline{\text{SD\_TX09}}$	Transmit Data (negative)	N34	O	XV_{DD}	—
$\overline{\text{SD\_TX08}}$	Transmit Data (negative)	M32	O	XV_{DD}	—
$\overline{\text{SD\_TX07}}$	Transmit Data (negative)	K32	O	XV_{DD}	—
$\overline{\text{SD\_TX06}}$	Transmit Data (negative)	J34	O	XV_{DD}	—
$\overline{\text{SD\_TX05}}$	Transmit Data (negative)	F33	O	XV_{DD}	—
$\overline{\text{SD\_TX04}}$	Transmit Data (negative)	E34	O	XV_{DD}	—
$\overline{\text{SD\_TX03}}$	Transmit Data (negative)	E31	O	XV_{DD}	—
$\overline{\text{SD\_TX02}}$	Transmit Data (negative)	G30	O	XV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
$\overline{\text{SD\_TX01}}$	Transmit Data (negative)	E29	O	XV_{DD}	—
$\overline{\text{SD\_TX00}}$	Transmit Data (negative)	G28	O	XV_{DD}	—
SD_RX19	Receive Data (positive)	AF27	I	XV_{DD}	—
SD_RX18	Receive Data (positive)	AD29	I	XV_{DD}	—
SD_RX17	Receive Data (positive)	AG36	I	XV_{DD}	—
SD_RX16	Receive Data (positive)	AF34	I	XV_{DD}	—
SD_RX15	Receive Data (positive)	AC36	I	XV_{DD}	—
SD_RX14	Receive Data (positive)	AA36	I	XV_{DD}	—
SD_RX13	Receive Data (positive)	Y34	I	XV_{DD}	—
SD_RX12	Receive Data (positive)	W36	I	XV_{DD}	—
SD_RX11	Receive Data (positive)	T34	I	XV_{DD}	—
SD_RX10	Receive Data (positive)	P36	I	XV_{DD}	—
SD_RX09	Receive Data (positive)	M36	I	XV_{DD}	—
SD_RX08	Receive Data (positive)	L34	I	XV_{DD}	—
SD_RX07	Receive Data (positive)	K36	I	XV_{DD}	—
SD_RX06	Receive Data (positive)	H36	I	XV_{DD}	—
SD_RX05	Receive Data (positive)	F36	I	XV_{DD}	—
SD_RX04	Receive Data (positive)	D36	I	XV_{DD}	—
SD_RX03	Receive Data (positive)	A31	I	XV_{DD}	—
SD_RX02	Receive Data (positive)	C30	I	XV_{DD}	—
SD_RX01	Receive Data (positive)	A29	I	XV_{DD}	—
SD_RX00	Receive Data (positive)	C28	I	XV_{DD}	—
$\overline{\text{SD\_RX19}}$	Receive Data (negative)	AF28	I	XV_{DD}	—
$\overline{\text{SD\_RX18}}$	Receive Data (negative)	AE29	I	XV_{DD}	—
$\overline{\text{SD\_RX17}}$	Receive Data (negative)	AG35	I	XV_{DD}	—
$\overline{\text{SD\_RX16}}$	Receive Data (negative)	AF33	I	XV_{DD}	—
$\overline{\text{SD\_RX15}}$	Receive Data (negative)	AC35	I	XV_{DD}	—
$\overline{\text{SD\_RX14}}$	Receive Data (negative)	AA35	I	XV_{DD}	—
$\overline{\text{SD\_RX13}}$	Receive Data (negative)	Y33	I	XV_{DD}	—
$\overline{\text{SD\_RX12}}$	Receive Data (negative)	W35	I	XV_{DD}	—
$\overline{\text{SD\_RX11}}$	Receive Data (negative)	T33	I	XV_{DD}	—
$\overline{\text{SD\_RX10}}$	Receive Data (negative)	P35	I	XV_{DD}	—
$\overline{\text{SD\_RX09}}$	Receive Data (negative)	M35	I	XV_{DD}	—
$\overline{\text{SD\_RX08}}$	Receive Data (negative)	L33	I	XV_{DD}	—