Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

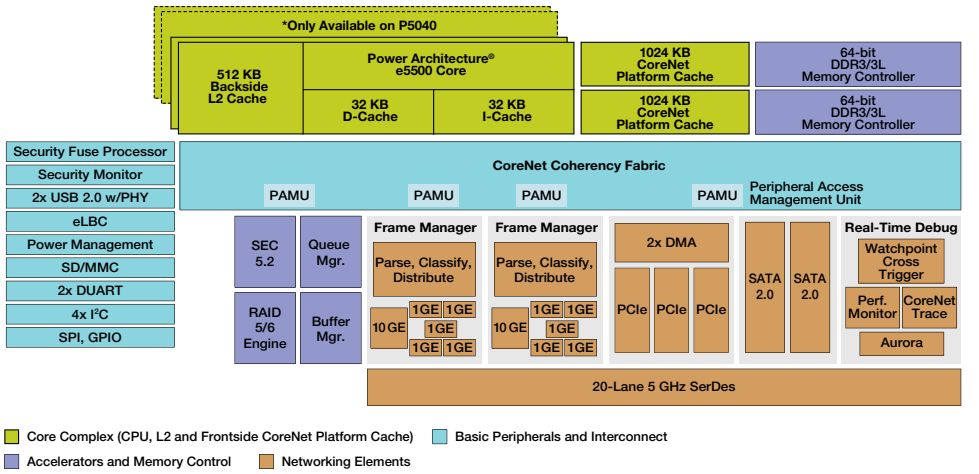
QorIQ Communications Platforms

QorIQ P5040/P5021 Processors

Overview

The QorIQ P5 family delivers scalable 64-bit processing with single-, dual- and quad-core devices. With frequencies scaling up to 2.4 GHz, a tightly coupled cache hierarchy for low latency, and integrated hardware acceleration, the P5040 (quad-core) and P5021 (dual-core) devices are ideally suited for compute intensive, power-conscious control plane applications.

QorIQ P5040/P5021 Processors



P5 Family Comparison Chart

	P5020/P5010	P5040/P5021
CPU cores	2x 64-bit e5500, 1x (P5010)	4x 64-bit e5500, 2x (P5021)
Threads	2/1 (single thread per core)	4/2 (single thread per core)
Max. core frequency	1.6 to 2.0 GHz	1.8 to 2.4 GHz
L2	512 KB per core	512 KB per core
L3/Platform	2 MB (P5020)/1 MB (P5010)	2 MB (both P5040 and P5021)
DDR I/F	2x 64-bit DDR3 (up to 1333 MT/s) 1x 64-bit DDR3 (P5010)	2x 64-bit DDR3 (up to 1600 MT/s)
PCI Express®	4x PCIe v2.0	3x PCIe v2.0 (incl. 1x 8)
GbE, 10 GbE	5x 1 GbE, 1x 10 GbE	10x 1 GbE, 2x 10 GbE
SRIO	2x SRIO v2.1 (supports type 9 and type 11 messaging)	N/A
SerDes lanes	18 lanes	20 lanes
Package	1295-pin 37.5 x 37.5 mm FC-PBGA	1295-pin 37.5 x 37.5 mm FC-PBGA

Target Markets and Applications

The P5040 is designed for high-performance, power-constrained control plane applications. The P5040 provides an ideal combination of core performance, integrated accelerators and advanced I/O required for the following compute-intensive applications:

- Enterprise equipment: Router, switch, services
- Data center: Server appliance, SAN storage controller, iSCSI controller, FCoE bridging
- Aerospace and defense
- Industrial computing: Single-board computers, test/measurement, robotics

e5500 Core

The P5040 is based on the 64-bit e5500 Power Architecture® core. The e5500 core uses a seven-stage pipeline for low latency response to unpredictable code execution paths, boosting its single-threaded performance. Key features:

- Supports up to 2.4 GHz core frequencies
- Tightly-coupled low latency cache hierarchy: 32 KB I/D (L1), 512 KB L2 per core
- Up to 2 MB of shared platform cache (L3)
- 3.0 DMIPS/MHz per core
- Up to 64 GB of addressable memory space
- Hybrid 32-bit mode to support legacy software and seamless transition to 64-bit architecture

Virtualization

The P5040 includes support for hardware-assisted virtualization. The e5500 core offers an extra core privilege level (hypervisor). Virtualization software for the P5 family includes kernel-based virtual machine, Linux® containers, Freescale hypervisor and commercial virtualization software from Green Hills® Software and Enea®.

DPAA Hardware Accelerators

Frame manager (FMAN)	24 Gbps classify, parse and distribute
Buffer manager (BMAN)	64 buffer pools
Queue manager (QMAN)	Up to 2^{24} queues
Security (SEC)	17 Gbps: 3 DES, AES
RAID5/6 Engine	Calculates parity for network attached storage and direct attached storage applications

Data Path Acceleration Architecture (DPAA)

The P5040 integrates QorIQ DPAA, an innovative multicore infrastructure for scheduling work to cores (physical and virtual), hardware accelerators and network interfaces. The FMAN, a primary element of the DPAA, parses headers from incoming packets and classifies and selects data buffers with optional policing and congestion management. The FMAN passes its work to the QMAN, which assigns it to cores or accelerators with a multi-level scheduling hierarchy. The P5040 also offers accelerators for cryptography and RAID5/6 offload.

System Peripherals and Networking

For networking, there are dual FMANs with dual 10 Gb/s and 10x 1 Gb/s MAC controllers that connect to PHYs, switches and backplanes over RGMII, SGMII and XAUI. High-speed system expansion is supported through three PCI Express® v2.0 controllers that support a variety of lane widths. Other peripherals include SATA, SD/MMC, I²C, UART, SPI, NOR/NAND controller, GPIO and dual 1600 MT/s DDR3/3L controllers.

P5040/P5021 Features List

Four (P5040) or two (P5021) single threaded e5500 cores built on Power Architecture® technology	• Up to 2.4 GHz with 64-bit ISA support (Power Architecture V2.06 compliant) • Three levels of instruction: User, supervisor, hypervisor • Hybrid 32-bit mode to support legacy software and transition to 64-bit architecture
CoreNet platform cache (CPC)	• 2.0 MB configured as dual 1 MB blocks
Hierarchical interconnect fabric	• CoreNet fabric supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet endpoints • QMAN fabric supporting packet-level queue management and quality of service scheduling
Two 64-bit DDR3/3L SDRAM memory controllers with ECC and interleaving support	• Up to 1600 MT/s • Memory pre-fetch engine
DPAA incorporating acceleration for the following functions	• Packet parsing, classification and distribution (FMAN) • QMAN for scheduling, packet sequencing and congestion management • Hardware BMAN for buffer allocation and de-allocation • Cryptography acceleration (SEC 5.0) at up to 40 Gb/s
SerDes	• 20 lanes at up to 5 Gb/s • Supports SGMII, XAUI, PCIe rev1.1/2.0, SATA
Ethernet interfaces	• Two 10 Gb/s Ethernet MACs • 10x 1 Gb/s Ethernet MACs
High-speed peripheral interfaces	• Three PCI Express 2.0 controllers • Two serial ATA (SATA 2.0) controllers
Additional peripheral interfaces	• Two High-Speed USB 2.0 controllers with integrated PHY • Enhanced secure digital host controller (SD/MMC/eMMC) • Enhanced serial peripheral interface • Four I²C controllers • Four UARTs • Integrated flash controller supporting NAND and NOR flash
DMA	• Dual four channel
Support for hardware virtualization and partitioning enforcement	• Extra privileged level for hypervisor support
QorIQ trust architecture 1.1	• Secure boot, secure debug, tamper detection, volatile key storage

Software and Tool Support

- Enea: Real-time operating system support and virtualization software
- Green Hills: Comprehensive portfolio of software and hardware development tools, trace tools, real-time operating systems and virtualization software
- Mentor Graphics®: Commercial-grade Linux solution
- QNX®: Real-time OS and development tool support
- QorIQ P5040 development system (P5040QDS-PA) available June 2012

For more information, please visit freescale.com/QorIQ

freescale™

Document Number: P50405021FS REV 1