Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

2/3/4-PHASE PWM CONTROLLER WITH DYNAMIC VOLTAGE & FREQUENCY SCALING

IDTP62000

Description

The IDTP62000 is a multiphase interleaved synchronous buck controller ideal for personal computer applications where high efficiency and high power density are required. It contains three integrated MOSFET driver pairs to enable a 3-phase regulator solution that allows load currents up to 150A for low voltage microprocessor power requirements. It also provides a 4th PWM output phase to drive a low cost IDTP67111 single phase driver to become a full 4 phase solution.

The VID logic can be configured for applications compliant to the Intel VR11.1, Intel VR10 or AMD PVI/SVI specifications.

The maximum number of operating phases (2/3/4) is pin programmable, and depending on output loading conditions, the active number of phases can be dynamically reduced. The Dynamic Efficiency Control (DEC) feature enables all configured phases when full current output is required, and dynamically reduces the number of active phases at reduced current levels. Combined with Dynamic Voltage Change (DVC) and Dynamic Frequency Change (DFC) this allows full output current while also providing for more efficient operation at lower power output.

The design allows a positive or negative offset to the VID voltage being used for regulation and supports both external, resistor based, and internal, register based, programming of this offset voltage.

An internal soft start (SS) is included in the design to prevent large inrush currents at power on. The ramp rate of the soft start can be adjusted with an external resistor.

A DCR current sensing method combined with rapid transient response architecture enables superior phase current matching, accurate current limit and precise load-line control. Furthermore, this device incorporates a proprietary scheme for fast and accurate transient-response performance, as well as precise load sharing.

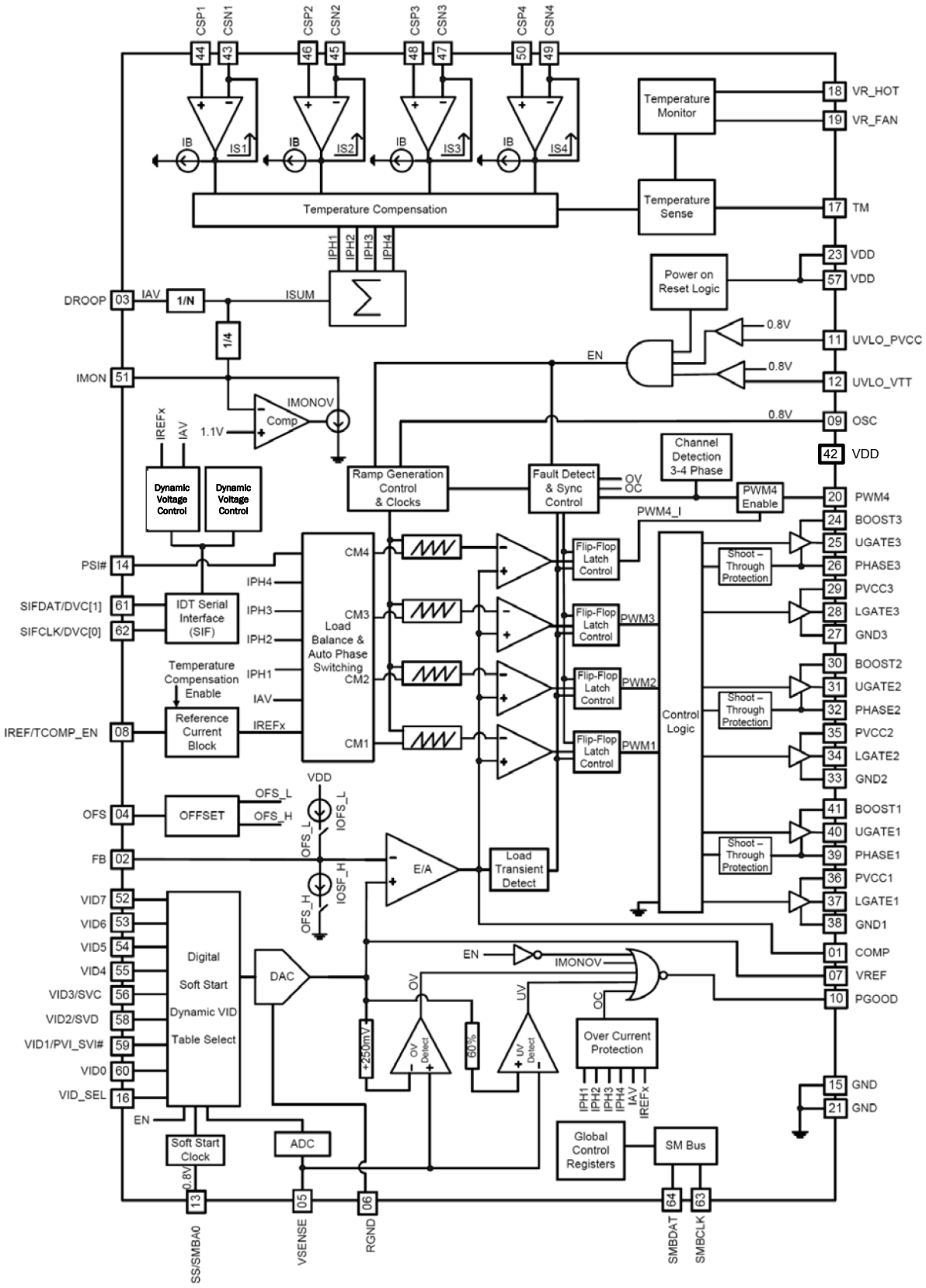
Features

- **Proprietary Dynamic Voltage & Frequency Scaling providing efficiency and performance optimization**
  - **– Dynamic Voltage Change (DVC) as a standalone capability**
  - **– Dynamic Frequency Change (DFC) when combined with 9CPS4592 clock generator**
  - **– SIF interface to communicate with clock sub-system**
- **Dynamic Efficiency Control (DEC) for improved efficiency at light loads**
- Intel VR11.1, Intel VR10 or AMD PVI/SVI operating modes
- Three integrated drivers with additional fourth phase PWM output
- 2, 3 or 4-phase operation with automatic selection at power-on
- Ability to communicate with the clock subsystem using a Serial Interface (SIF)
- User configurability through SMBus
- Overshoot and Undershoot transient suppression
- Adjustable operating frequency (up to 1 MHz per phase)
- Pb Free, RoHS compliant 64-pin QFN-64 package

Applications

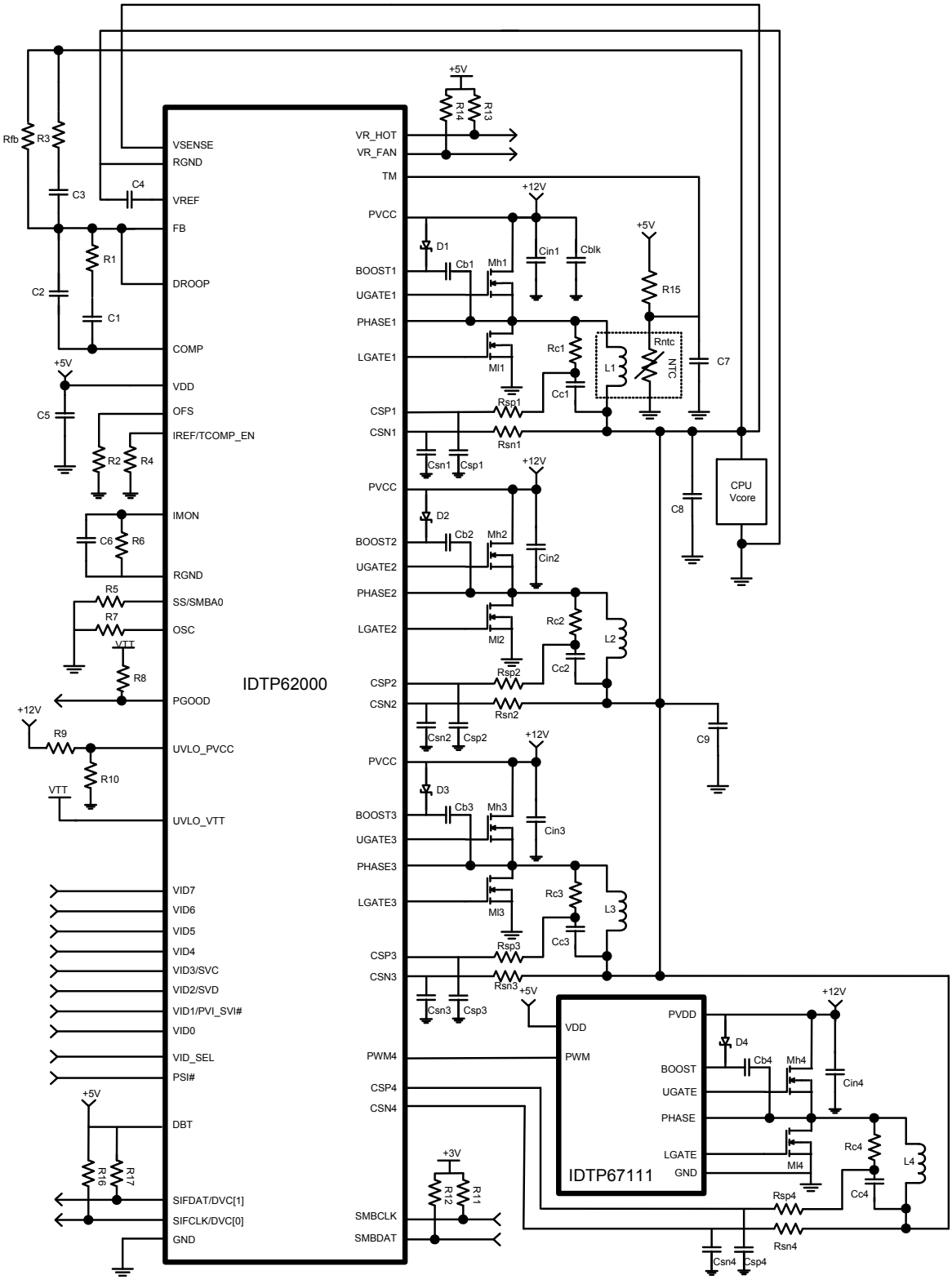
- Gaming Machine
- Server, Workstations
- All-in-one LCD PCs
- Voltage Regulator Modules

Block Diagram



Applications Information

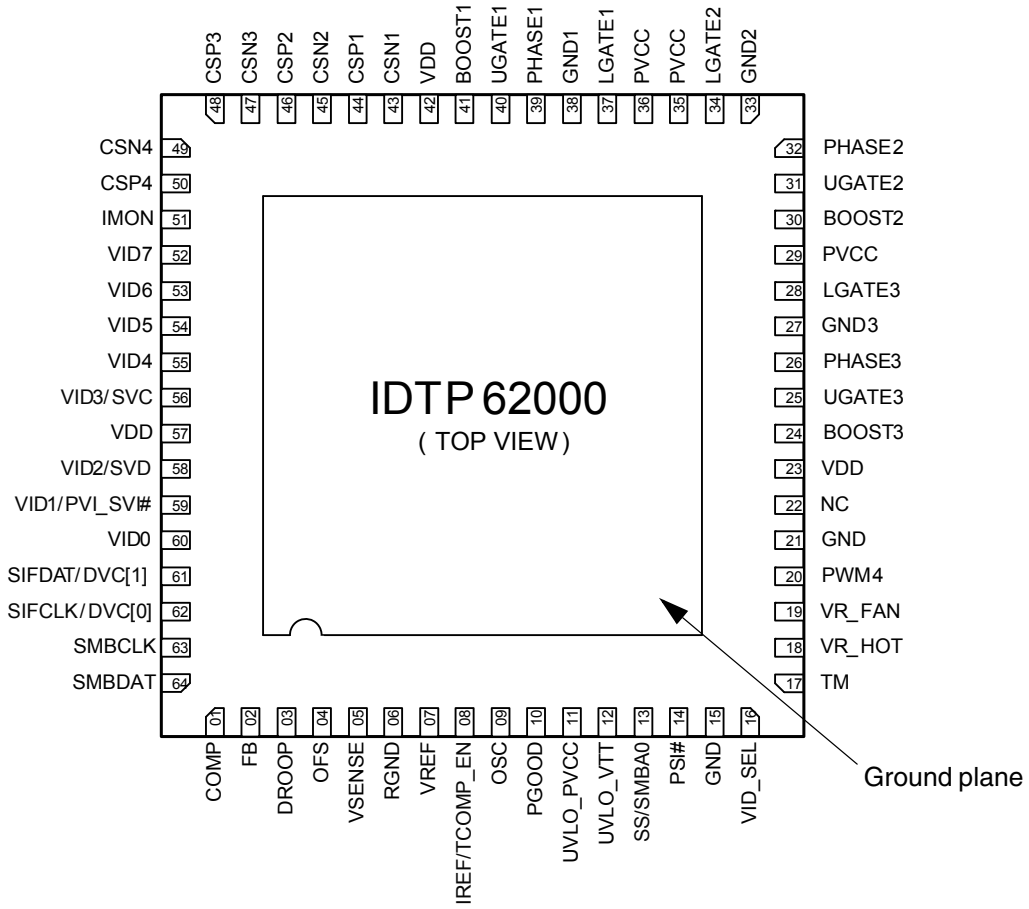
Figure: 4-Phase Applications Reference Circuit



4-Phase Component Values

Component	Pin	Value	Package	Description
R1	FB, COMP	10k	0603	10kΩ 1% Resistor
R2	OFS	52k	0603	52kΩ 1% Resistor
R3	FB	500	0603	500Ω 1% Resistor
Rfb	FB	2.5k	0603	2.5kΩ 1% Resistor
R4	IREF/TCOMP_EN	40.2k	0603	40.2kΩ 1% Resistor
R5	SS/SMBA0	100k	0603	100kΩ 1% Resistor
R6	IMON	22.6k	0603	22.6kΩ 1% Resistor
R7	OSC	82k	0603	82kΩ 1% Resistor
R8	PGOOD	1k	0603	5kΩ 5% Resistor
R9	UVLO_PVCC	27k	0603	27kΩ 1% Resistor
R10	UVLO_PVCC	3.01k	0603	3.01kΩ 1% Resistor
R11	SMCLK	4.7k	0603	4.7kΩ 5% Resistor
R12	SMBDAT	4.7k	0603	4.7kΩ 5% Resistor
R13	VR_HOT	1k	0603	1kΩ 5% Resistor
R14	VR_FAN	1k	0603	1kΩ 5% Resistor
R15	TM	1k	0603	1kΩ 1% Resistor
R16	SIFCLK	Do not populate	0603	
R17	SIFDAT	Do not populate	0603	
Rntc	TM	R_{25C} = 6.8kΩ	0805	Vishay 6.8kΩ 3% NTC Thermistor, Beta = 3477
Rc1, Rc2, Rc3, Rc4	PHASEx, CSPx	6k	0603	6kΩ 1% Resistor
Rsp1. Rsp2, Rsp3, Rsp4	PHASEx, CSPx	625	0603	625Ω 1% Resistor
Rsn1. Rsn2. Rsn3. Rsn4	CSNx	625	0603	625Ω 1% Resistor
C1	FB, COMP	2n	0603	2nF 10V X7R Ceramic capacitor
C2	FB, COMP	36p	0603	36pF 10V NPO Ceramic capacitor
C3	FB	0.5n	0603	0.5nF 10V NPO Ceramic capacitor
C4	VREF	1n	0603	1nF 10V X7R Ceramic capacitor
C5	VDD	1µ (x2)	0603	1µF 10V X5R Ceramic capacitor
C6	IMON	20n	0603	20nF 10V X7R Ceramic capacitor
C7	TM	Do not populate	0603	
C8	vcore	820µF (x12) = 9,840µF	Radial Capacitor	
C9	vcore	22µF (x18) = 396µF	0805	X5R 25V Ceramic capacitor
Cb1, Cb2, Cb3, Cb4	BOOSTn	1µ	0603	1µF X5R 25V Ceramic capacitor
Cc1, Cc2, Cc3, Cc4	CSPn	0.1µ	0603	0.1µF 10V X7R Ceramic capacitor
Csn1, Csn2, Csn3, Csn4	CSNn	36p	0603	X7R 10V Ceramic capacitor
Csp1, Csp2, Csp3, Csp4	CSPn	36p	0603	X7R 10V Ceramic capacitor
Cin1, Cin2, Cin3, Cin4	PVDD	4.7µ (x2 per Mh1-Mh4 mosfet = 8 total)	0805	4.7µF X5R 25V Ceramic capacitor
cblk		470µ (x2) = 940 µF	Radial Capacitor	470µF 16V
L1, L2, L3, L4	PHASEn	0.6µ	Through hole	0.60µH 35A 1.0mΩ DCR Inductor
Mh1, Mh2, Mh3, Mh4	PHASEn	P0903BDG	TO-252	Upper Drive Mosfet
MI1, MI2, MI3, MI4	PHASEn	P75N02LDG	TO-252	Lower Drive Mosfet
D1 - D4		BAT54A	SOT-23	Schottky Bootstrap Diode

Pin Assignment



64 Pin VFQFP-64 (9x9 mm)

Pin Types

I/O Type	Description
A-I, A-O & A-IO	Analog Levels: Input, Output & Input/Output
D-I, D-O	Digital Levels: Input, Output. Voltage levels are all digital levels
GND	Ground: Any connection to Ground
GP-IN, GP-OUT, GPIO	General Purpose: Input, Output, Input/Output. Inputs are 3.3 V (5 V tolerant) Outputs are open-drain capable
I2C-I, I2C-O & I2CIO	I²C: Input, Output & Input/Output Inputs are CMOS Outputs are open-drain capable.
P-I, P-O	Power Supply: Input, Output

Pin Descriptions

Pin #	Pin Name	Pin Type	Pin Description
1	COMP	A-I/O	Connected to the internal error amplifier. It is used with the FB pin to compensate the error amplifier. It is the output of the error amplifier.
2	FB	A-I/O	Negative input terminal to the internal differential error amplifier. It is used with the COMP pin to compensate the error amplifier.
3	DROOP	A-I/O	A current proportional to the total output current is sourced from this pin. Connecting this pin to FB allows the controller to compensate output voltage droop in the output.
4	OFS	A-I/O	The OFS pin provides a means to program a DC current for generating an offset voltage across the resistor between FB and VSENSE. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VDD. For no offset, the OFS pin should be left unconnected.
5	VSENSE	A-I	Connect directly to VCORE. It used only by the OVP and UVP blocks.
6	RGND	GND	Reference ground for the load, which is used for remote sensing to offset the internal DAC voltage.
7	VREF	A-O	Analog output of the DAC after the DAC voltage has been referenced to RGND.
8	IREF/TCOMP_EN	A-I/O	Dual purpose pin that is used to provide: 1.Internal accurate current reference (IREF) 2.Enable for sensed load current temperature compensation (TCOMP_EN) The reference current is provided by placing a resistor from the IREF pin to GND or VDD with an internally generated bandgap reference voltage of 0.8 V applied across it. Temperature compensation is enabled if the IREF resistor is tied to GND and it is disabled if the IREF resistor is tied to VDD.
9	OSC	A-I/O	A resistor from this pin to ground selects the nominal switching frequency of the regulator. Using 100 kΩ will result in a switching frequency of 250 kHz.
10	PGOOD	D-O	The PGOOD signal is an active high signal that indicates whether or not the controller is regulating the output voltage within the proper levels, and whether any fault conditions exist. During shutdown and soft-start the PGOOD signal is pulled low and will go high after the soft-start sequence completes and the output voltage is between the over-voltage and under-voltage limits. (approximately 1 ms after the end of soft-start). During an under-voltage, over-voltage, over-current condition or when the controller output enable UVLO_PVCC is pulled low, PGOOD will go low. Moreover, PGOOD will also be pulled low when a no-CPU VID (or OFF) code is selected or during any reset event.
11	UVLO_PVCC	A-I	Pin should be externally connected to a resistor divider between PVCC and GND. It is used to detect that the PVCC level has come up. When the voltage at the pin rises above its threshold (0.8V) then the internal power on reset is released provided that the internal VDD based POR level has been also reached. It is recommended that the user bias this pin with a resistor divider that generates the POR threshold voltage when PVCC is at 2/3 of its maximum value.
12	UVLO_VTT	A-I	Another threshold-sensitive enable input for the controller. It's typically connected to the VTT output of the VTT voltage regulator in the computer mother board.
13	SS/SMBA0	A-I/O	Multiple purpose pin. One of its functions is to set the soft start ramp slope for the Intel DAC modes of operation by a resistor connected to ground. The pin also determines the value of the SMBus address A0 bit. The A0 logic level is determined by the level on this pin at power up. If the resistor is connected to VDD, the A0 bit is set to high. If the resistor is connected GND, the A0 bit is set to low.
14	PSI#	A-I	The power state indicator mode pin (PSI#) is a logical input to initiate a phase dropping scheme for higher efficiency at light load. The input conforms to the 1.2 V CMOS levels defined in the VRD11.1 specification (nominally 1.2v high, 0v low).

Pin #	Pin Name	Pin Type	Pin Description
15	GND	GND	System Ground. IC reference and bias ground.
16	VID_SEL	D-I	Select pin for the different VID modes. For VR10, this signal needs to be grounded. For VR11.1, the signal needs to be floating (>0.8 V and <1.8 V). For AMD PVI/SVI compliance the pin needs to be tied high (>1.8 V).
17	TM	A-I	Thermal monitor input pin. Its input is connected to a negative thermal coefficient (NTC) thermistor network to set the temperature thresholds for VR_HOT and VR_FAN. The TM pin is also for internal temperature compensation.
18	VR_HOT	D-O	Over-temperature alarm signal logical output. Signal is active high when the TM pin (thermal monitor) passes a set threshold. This pin is open-drain.
19	VR_FAN	D-O	Over-temperature warning signal logical output. Signal is active high when the TM pin (thermal monitor) passes a set threshold. This pin is open-drain.
20	PWM4	A-I/O	Dual function pin. In normal operation, it will act as the pulse width modulated 3-stateable output signal for an external fourth channel driver. On power-up, this pin will also act as a 3-state input pin to select the number of required phases.
21	GND	GND	System Ground. IC reference and bias ground.
22	NC	NC	No Connect
23	VDD	P-I	+5V (nominal) supply pin for “lower” voltage circuits.
24	BOOST3	P-I	Voltage supply for the upper power MOSFET gate drive. An external bootstrap capacitor is also required. An internal diode is connected to this pin for the bootstrap charge.
25	UGATE3	A-I/O	Connect this pin to the gate of upper power MOSFET 3
26	PHASE3	A-I/O	Return path for the corresponding upper power MOSFET gate driver for phase 3.
27	GND3	GND	Gate Driver 3 Ground.
28	LGATE3	A-I/O	Connect to the gates of lower power MOSFET 3.
29	PVCC	P-I	One of three supply input pins for the corresponding channel MOSFET drive. Connect to +12V supply.
30	BOOST2	P-I	Voltage supply for the upper power MOSFET gate drive. An external bootstrap capacitor is also required. An internal diode is connected to this pin for the bootstrap charge.
31	UGATE2	A-I/O	Connect this pin to the gate of upper power MOSFET 2.
32	PHASE2	A-I/O	Return path for the corresponding upper power MOSFET gate driver for phase 2.
33	GND2	GND	Gate Driver 2 Ground.
34	LGATE2	A-I/O	Connected this pin to the gates of lower power MOSFET 2.
35	PVCC	P-I	One of three supply input pins for the corresponding channel MOSFET drive. Connect to +12V supply.
36	PVCC	P-I	One of three supply input pins for the corresponding channel MOSFET drive. Connect to +12V supply.
37	LGATE1	A-I/O	Connected to the gates of lower power MOSFET 1.
38	GND1	GND	Gate Driver 1 Ground.
39	PHASE1	A-I/O	Return path for the corresponding upper power MOSFET gate driver for phase 1.
40	UGATE1	A-I/O	Connect this pin to the gate of upper power MOSFET 1.
41	BOOST1	P-I	Voltage supply for the upper power MOSFET gate drive. An external bootstrap capacitor is also required. An internal diode is connected to this pin for the bootstrap charge.
42	VDD	P-I	+5V (nominal) supply pin for “lower” voltage circuits.
43	CSN1	A-I	Phase 1 current sense - negative input.
44	CSP1	A-I	Phase 1 current sense - positive input.

Pin #	Pin Name	Pin Type	Pin Description
45	CSN2	A-I	Phase 2 current sense - negative input.
46	CSP2	A-I	Phase 2 current sense - positive input.
47	CSN3	A-I	Phase 3 current sense - negative input.
48	CSP3	A-I	Phase 3 current sense - positive input.
49	CSN4	A-I	Phase 4 current sense - negative input.
50	CSP4	A-I	Phase 4 current sense - positive input.
51	IMON	A-O	Total load current monitoring output pin. It is used with the PSI# to properly handle the dynamic phase switching for higher efficiency. IMON is limited to a max voltage of 1.1 V so as not to damage the CPU input.
52	VID7	D-I/O	The voltage identification pin VID7, connects to CPU. (See Note 1)
53	VID6	D-I/O	The voltage identification pin VID6, connects to CPU. (See Note 1)
54	VID5	D-I/O	The voltage identification pin VID5, connects to CPU. (See Note 1)
55	VID4	D-I/O	The voltage identification pin VID4, connects to CPU. (See Note 1)
56	VID3/SVC	D-I/O	The voltage identification pin VID3, connects to CPU. (See Note 1)
57	VDD	P-I	+5V (nominal) supply pin for “lower” voltage circuits.
58	VID2/SVD	D-I/O	The voltage identification pin VID2, connects to CPU. (See Note 1)
59	VID1/PVI_SVI#	D-I/O	The voltage identification pin VID1, connects to CPU. (See Note 1)
60	VID0	D-I/O	The voltage identification pin VID0, connects to CPU. (See Note 1)
61	SIFDAT/DVC[1]	I2C-O GP-OUT	Serial data output pin for the SIF bus. When in GPO mode, this pin serves as the DVC[1] logical output and requires a 4 kΩ pull-down resistor.
62	SIFCLK/DVC[0]	I2C-O GP-OUT	Serial clock output pin for the SIF bus. When in GPO mode, this pin serves as the DVC[0] logical output and requires a 4 kΩ pull-down resistor.
63	SMBCLK	A-I/O	Clock input pin for the system management bus and is compliant with the SMBus specification.
64	SMBDAT	A-I/O	Data input pin for the system management bus and is compliant with the SMBus specification.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDTP62000. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Rating	Units
Supply Voltage, VDD [Note 2]	-0.3 to 6	V
All Inputs and Outputs	GND -0.3 to VDD +0.3	V
Boost To Phase	15	V
Boost To Ground	30	V
ESD (HBM)	2000	V
Junction Temperature	0 to +150	°C
Storage Temperature	-65 to +150	°C
Soldering Temperature	260	°C

Note 2: If used in conjunction with a IDTP67111 single phase driver for the fourth phase, it must be powered with the same supply as the IDTP62000.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
VDD Power Supply Voltage (measured with respect to GND)	4.75	5	5.25	V
PVCC Power Supply Voltage (measured with respect to GND)	10.8	12	13.2	V
Power Supply Ramp-Up Time			4	ms
Ambient Operating Temperature	0		+70	°C
Junction Temperature	0		+100	°C

General I²C Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address $78_{(H)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledged**
- Controller (host) starts sending Byte **N through Byte N+X-1(note 2)**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address 78 (H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address $78_{(H)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledged**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address $79_{(H)}$
- IDT clock will **acknowledged**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address 78 (H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address 79 (H)			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not		
P	stoP bit		

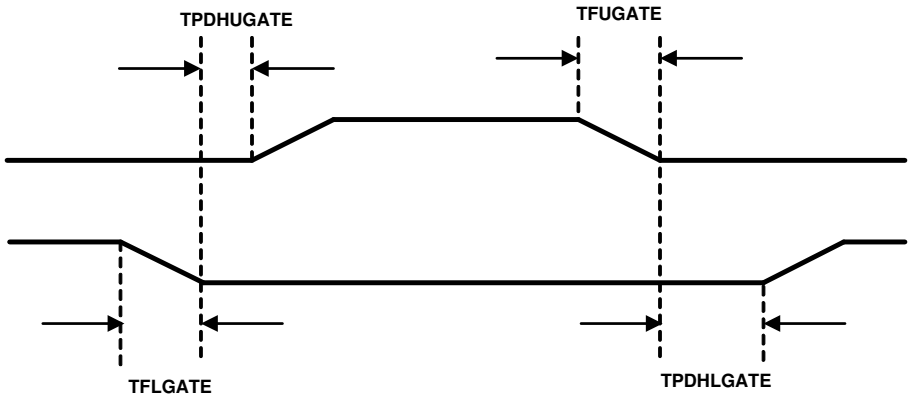
Power MOSFET Driver Electrical Characteristics

Table 1: MOSFET Driver Characteristics

Unless stated otherwise, VDD = 5.0 V ± 5 %, Junction Temperature = 0 to +100 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Current						
PVCC Quiescent Curr.	IPVCC	Switching frequency = 250 kHz (12V input pins)		30		mA
Power-On Reset						
POR threshold	PVCCRTH	PVCC Rising		6.4	6.5	V
Hysteresis	PVCCHYS			80	200	mV
Gate Output						
Output Resistance		UGATE Source 15 mA	1.25	2.0	3.0	Ω
		UGATE Sink 15 mA	0.9	1.65	3.0	Ω
		LGATE Source 15 mA	0.85	1.25	2.2	Ω
		LGATE Sink 15 mA	0.60	0.80	1.35	Ω
Output Switching Time						
UGATE Fall Time	TFUGATE	VPVCC = 12V, 3 nF load, 10% - 90%		40		ns
LGATE Fall Time	TFLGATE	VPVCC = 12V, 3 nF load, 10% - 90%		25		ns
UGATE Turn-On Non-Overlap	TPDHUGATE	VPVCC = 12V, 3 nF load		18		ns
LGATE Turn-On Non-Overlap	TPDHLGATE	VPVCC = 12V, 3 nF load		18		ns
Bootstrap diode						
Reverse Leakage		At 12 V		0.1		µA
Forward Voltage Drop		At 10 mA		0.7		V
Over-voltage Protection						
Trip Voltage		Enter OVP (VCC=12 V)		3.6		V
		Exit OVP (PVCC=12 V)		0.75		V

Figure 1: Output Switching TImes



Controller Electrical Characteristics

Unless stated otherwise, VDD = 5.0 V ± 5 %, Junction Temperature = 0 to +100 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Current						
IDDQ	IVDD	PWM 1,2,3 open (5V input pins)		18	25	mA
Power-On Reset						
POR threshold	VDDRTH	VDD Rising	4.1	4.2	4.3	V
	VDDFTH	VDD Falling		3.8		V
Hysteresis	VDDHYS			0.5		V
UVLO_PVCC Rising Threshold			0.76	0.8	0.84	V
UVLO_PVCC Hysteresis				65		mV
UVLO_VTT Rising Threshold			0.76	0.8	0.84	V
UVLO_VTT Hysteresis				65		mV
Master Oscillator						
Frequency Accuracy	F_{SW}	Rosc = 100 kΩ ± 0.1%	225	250	275	kHz
Adjustment Range of Switching Frequency	F_{SWAR}		100		1000	kHz
OSC Voltage	V_{OSC}		0.76	0.8	0.84	V
Ramp Generator						
Ramp Amplitude	V_{RA}			2.4		V
Max PWM Duty Cycle	DC_{PWM}		90			%
Reference and DAC						
System Accuracy (1.000V - 1.600V)			-0.5		+0.5	%
System Accuracy (0.800V - 1.000V)			-1.0		+1.0	%
System Accuracy (0.5V - 0.800)			-2.0		+2.0	%
VID Input Low Voltage (VR10, VR11.1)	V_{ILVIDI}		-0.3		0.3	V
VID Input High Voltage (VR10, VR11.1)	V_{IHVIDI}		0.8		VDD + 0.3	V
OFS Source Current Accuracy (Negative Offset)	I_{OFFSET}	R_{OFS} = 10 kΩ from OFS to GND	37.0	40.0	43.0	µA
OFS Sink Current Accuracy (Positive Offset)	I_{OFFSET}	R_{OFS} = 30 kΩ from OFS to VDD	50.5	53.5	56.5	µA
OFS Range		± 10% Accuracy at limits of range	-150		150	µA
VID Input Pull-up to 1.2V (Intel)	I_{VID}	Input = 0.0V		30	50	µA
Current Reference						
IREF Current	I_{REF}	R_{IREF} = 40 kΩ ±1% from IREF to GND	19	20	21	µA
IREF Current Range	I_{REF-R}		19.0	20.0	33.6	µA
IREF Voltage	V_{IREFL}	R_{IREF} = 40 kΩ from IREF to GND	0.76	0.8	0.84	V
	V_{IREFH}	R_{IREF} = 40 kΩ from IREF to VDD	VDD -0.76	VDD -0.8	VDD -0.84	V
Soft-Start Ramp						
Soft-Start Reference Voltage, (Intel modes)	V_{SS}	Rss = 100 kΩ	0.76	0.8	0.84	V
Soft-Start Ramp Rate, (Intel modes)	SS_{INTEL}	VR10/VR11.1, Rss= 100 kΩ		1.5		mV/µs
		Adjustment Range of SS ramp rate	0.6		6.0	mV/µs
	R_{SS}	Soft Start Resistor Value	25		250	kΩ
Soft-Start Step Voltage (AMD mode)	SS_{AMD}	Rate = 6.25 mV every 3.03 µs		6.25		mV
Soft-Start Step Time (AMD mode)				3.03		µs
PWM Output						
PWM Output Voltage Low Threshold		Load = ± 1 mA			0.4	V
PWM Output Voltage High Threshold		Load = ± 1 mA	4.0			V

Controller Electrical Characteristics (cont.)

Unless stated otherwise, VDD = 5.0 V ± 5 %, Junction Temperature = 0 to +100 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
OV and UV Protection						
UV Threshold Rise	V_{UVR}	FB rising	66	70	74	%VID
UV Threshold Fall	V_{UVF}	FB falling	57	60	63	%VID
OV Threshold		Intel mode (SS Prior to Vboot period end)	1.30	1.35	1.40	V
		Intel mode (SS after Vboot period end)	1.30	1.35	1.40	V
		Greater of:	-5%	V_{DAC} + 250 mV	+5%	V
		Intel mode (After SS complete)	-5%	V_{DAC} + 250 mV	+5%	V
		AMD mode	1.75	1.8	1.85	V
Thermal Monitor						
VR_FAN Fall Threshold	V_{FANF}	VTM falling (assert)		0.394 x VDD		V
VR_FAN Rise Threshold	V_{FANR}	VTM rising (de-assert)		0.445 x VDD		V
VR_HOT Fall Threshold	V_{HOTF}	VTM falling (assert)		0.333 x VDD		V
VR_HOT Rise Threshold	V_{HOTR}	VTM rising (de-assert)		0.394 x VDD		V
Over-Current Protection						
Dead-Zone Bias Current	I_{OCDZ}	Normal operation = 0.6 * (I_{REF} @ 20µA)	11.3	12.0	12.7	µA
Average Over-Current Threshold Level	I_{OCAVG}	Normal operation = 2.5 * (I_{REF} @ 20 µA)	44	50	56	µA
Individual Phase Over-Current Threshold Level	I_{OCPH}	Normal operation = 3.0 * (I_{REF} @ 20 µA)	52	60	67	µA
PSI Input						
Input High	V_{IHPSI}		0.8			V
Input Low	V_{ILPSI}				0.3	V
VID_SEL Input						
VID_SEL V_{IH}	$V_{IHVIDSEL}$		2			V
VID_SEL V_{IL}	$V_{ILVIDSEL}$				0.8	V
VID_SEL Leakage	$V_{IOVIDSEL}$			100		µA
PWM4 Input						
Input High	V_{IHPWM}		0.8 x VDD			V
Input Low	V_{ILPWM}				0.2 x VDD	V
Error Amplifier						
DC Gain		R_L = 10 kΩ to ground		70		dB
Gain-Bandwidth Product		C_L = 100 pF, R_L = 10k to ground		12		MHz
Slew Rate		C_L = 100 pF, Load = ± 400 µA		8		V/µs
Maximum Output Voltage			3.9	4.2		V
Minimum Output Voltage				1.30	1.5	V

SIFDAT and SIFCLK Line Characteristics

Unless stated otherwise, VDD = 5.0 V ± 5 %, Junction Temperature = 0 to +100 °C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Timing					
SIFCLK clock frequency	F_{SIFCLK}	500	667	833	kHz
LOW period of the SIFCLK clock	t_{LOW}	700	875		ns
HIGH period of the SIFCLK clock	t_{HIGH}	500	625		ns
Set-up time for a repeated START condition	$t_{SU;STA}$	200			ns
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	200			ns
Data hold time (provided when SIFDAT is output)	$t_{HD;DAT}$	200	250	450	ns
Data set-up time (provided when SIFDAT is output)	$t_{SU;DAT}$	200	250		ns
Rise time of both SIFDAT and SIFCLK signals	t_r	5		50	ns
Fall time of both SIFDAT and SIFCLK signals	t_f	5		50	ns
Set-up time for a STOP condition	$t_{SU;STO}$	200			ns
Bus free time between a STOP and START condition	t_{BUF}	500			ns
Capacitive load for each bus line	C_b			30	pF
Input parameters					
Noise margin at the LOW level for each connected device	V_{nL}	0.1 x VDD			V
Noise margin at the HIGH level for each connected device	V_{nH}	0.2 x VDD			V
LOW level input voltage	V_{IL}	0		0.3 x VDD	V
HIGH level input voltage	V_{IH}	0.7 x VDD		VDD + 0.5	V
Capacitance for each I/O pin	C_i			10	pF
Output parameters					
LOW level output voltage @ ± 1 mA load	V_{OLSIF}			0.15 x VDD	V
HIGH level output voltage @ ± 1 mA load	V_{OHSIF}	0.85 x VDD			V

Typical Operating Characteristics

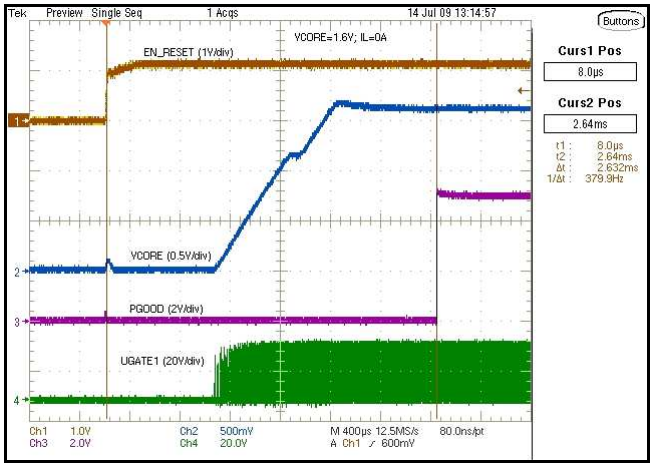


Figure 3: Startup vs. Time (Load = 0 A)

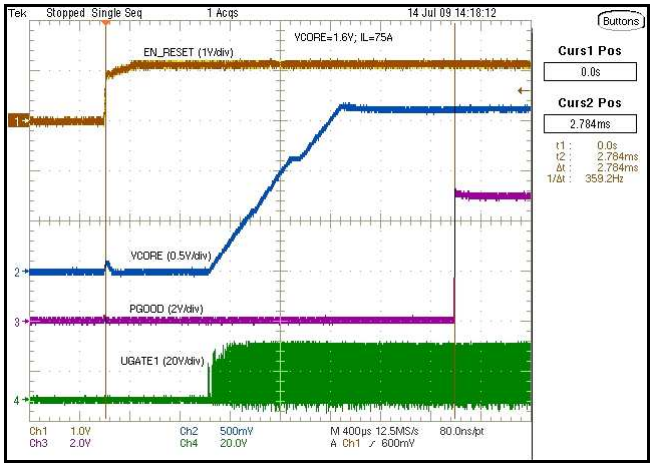


Figure 4: Startup vs. Time (Load = 75 A)

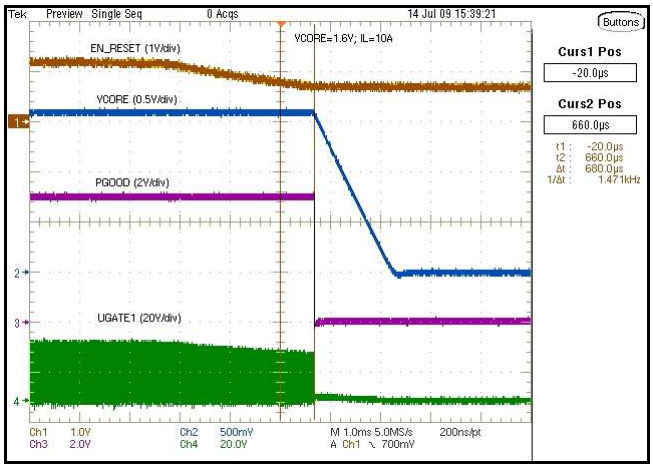


Figure 5: Shutdown vs. Time (10 A)

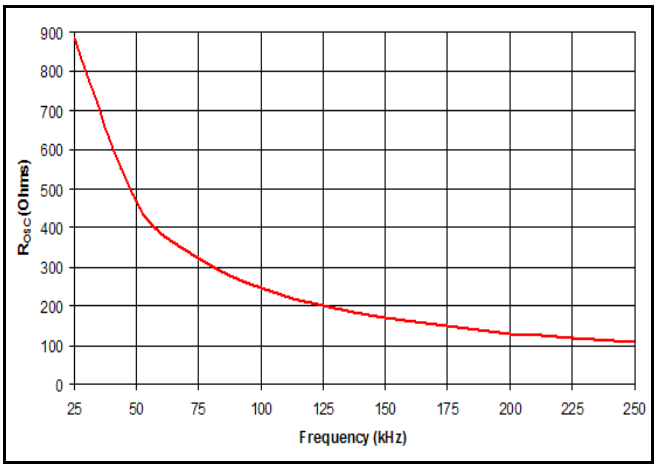


Figure 6: Oscillator Frequency vs. R_{OSC} Resistance

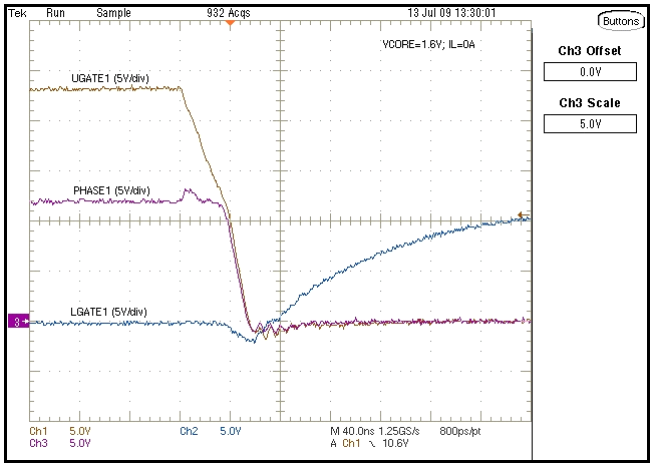


Figure 7: Gate Drive vs. Time (Load = 0 A, Falling Edge)

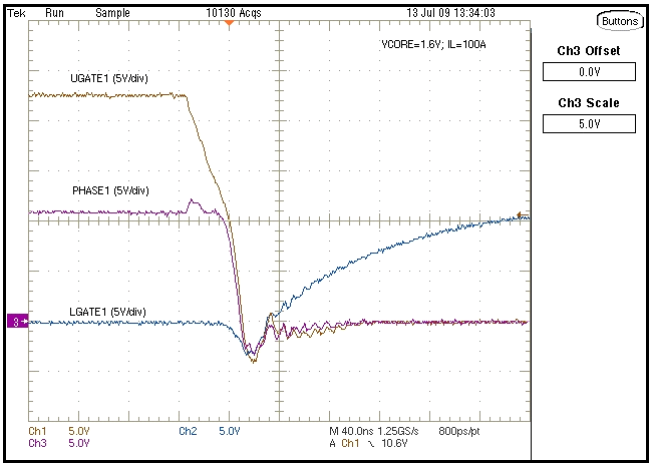


Figure 8: Gate Drive vs. Time (Load=100 A, Falling Edge)

Typical Operating Characteristics (cont.)

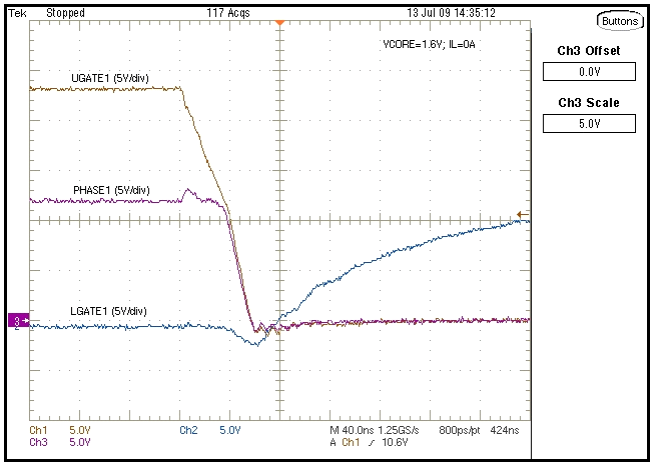


Figure 9: Gate Drive vs. Time (Load = 0 A, Rising Edge)

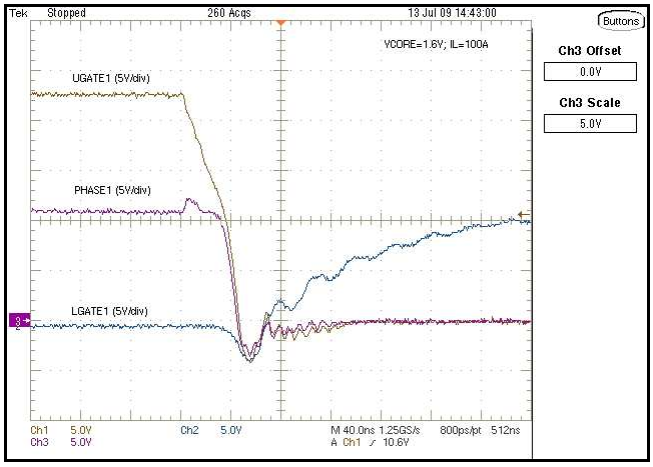


Figure 10: Gate Drive vs. Time (Load =100 A, Rising Edge)

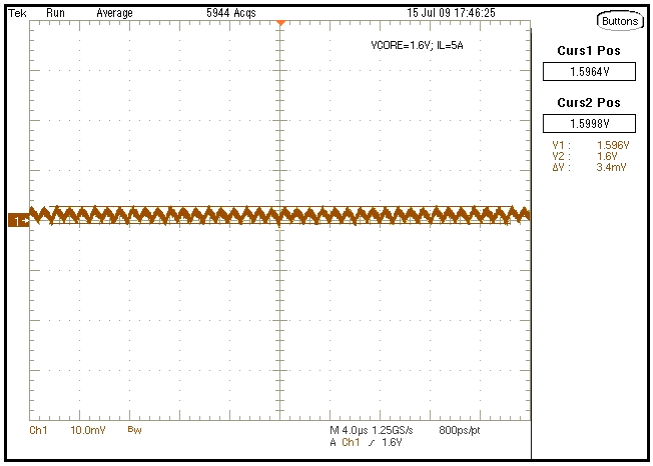


Figure 11: Steady State Output Ripple vs. Time (Load = 5 A)

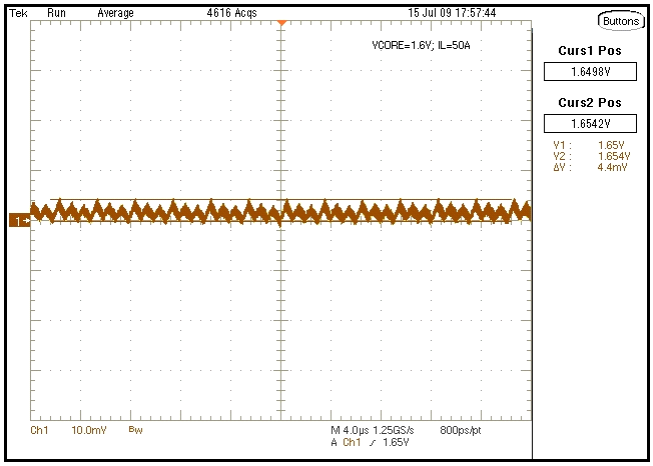


Figure 12: Steady State Output Ripple vs. Time (Load = 50 A)

Introduction

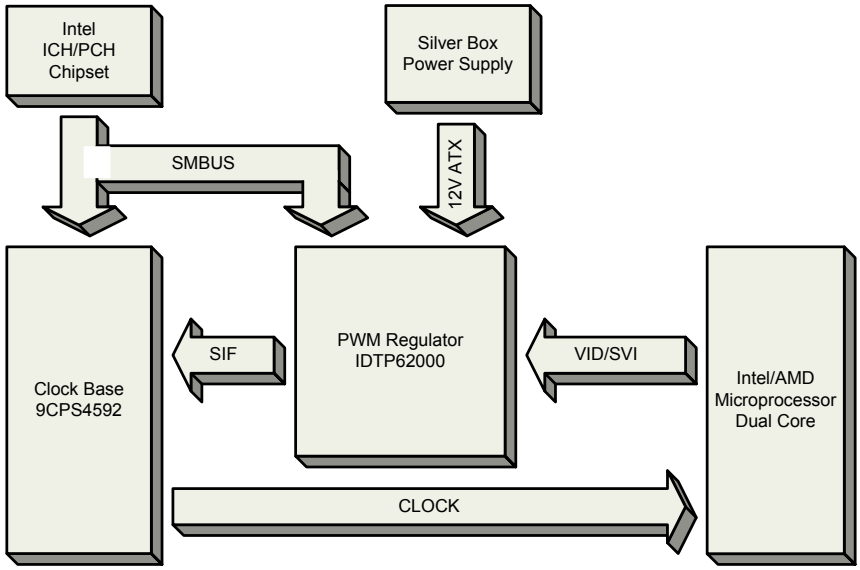
The IDTP62000 is a 2/3/4 phase PWM control IC that is compliant with Intel VR10.x, VR11.x, and AMD PVI/SVI CPU power specifications. The IDTP62000 integrates three MOSFET gate drivers to minimize total solution size, parts count, and cost. Four phase operation is supported with the addition of an IDTP67111 single phase driver IC.

The IDTP62000 includes many features and capabilities in addition those required by Intel and AMD CPUs. Proprietary Hypergear™ dynamic control provides programmable scaling of CPU voltage and clock frequency to enable system level performance and efficiency improvements. Complete Hypergear™ implementation includes an IDT SCPC (system clock power console) IC and related software. Programmable Dynamic Voltage Control (DVC) and Dynamic Frequency Control (DFC) allow performance and power consumption to be optimized as a function of load CPU current. Dynamic Efficiency Control (DEC) enables all configured phases to operate when full current output is required and dynamically reduces the number of active phases at reduced current levels.

An SMBus interface allows programming of IC configuration parameters and provides diagnostic and operational telemetry data to the host system. The output voltage can be offset either in a positive or negative manner using a single external resistor or by programming through the SMBUS interface. The IDTP62000 device contains an advanced control loop algorithm that allows all phases to respond to load steps to minimize output capacitacnce.

The IDTP62000 can operate in stand-alone mode or it can be one part of a two chipset solution for implementing a high performance, energy saving, computing system. The IDTP62000 PWM controller and 9CPS4592 clock generator coordinate adjustments to the output voltage with changes in the clock frequency to optimize system performance. Figure 13 provdes a simplified view of this system.

Figure 13: Two Part System using the IDTP62000 and the 9CPS4592



Operation

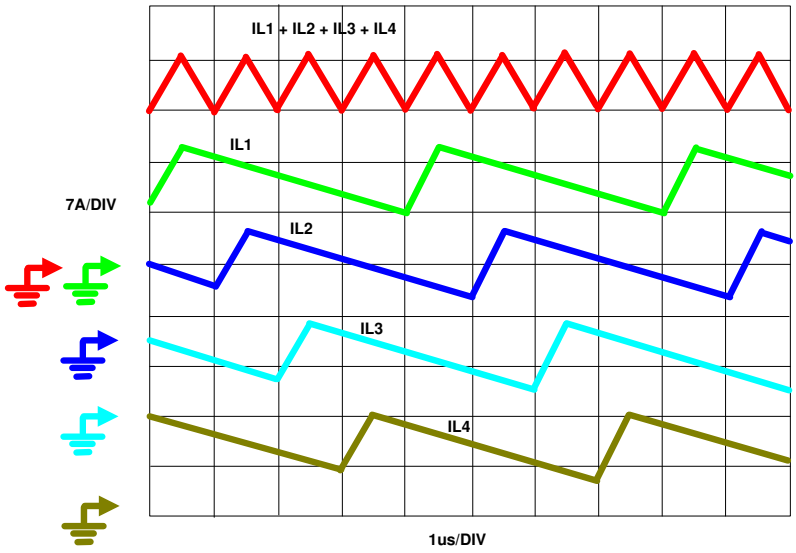
Multi-phase Power Conversion

As microprocessors have evolved in computing power so have PWM V_{CORE} regulators. Single phase operation regulators are no longer feasible for desktop power supplies. Although multi-phase power management regulators has been in existence for decades, recent strides in computing power have mandated that it be applied to microprocessors. These processors are no longer powered by low supply currents but can easily crest to 150A or more during heavy loading transients. The only way to satisfy such heavy demands is to implement a multi-phase power supply. With very little design effort the high current required can be obtained by breaking up the supply into smaller segments, thus realizing an improved component count and minimizing heat dissipation.

Interleaving

In multi-phase PWM regulators the individual channels switching periods are evenly distributed over the PWM clock period. In a four phase PWM regulator, for example, each channel will have time slots equally spaced exactly $T_{Period}/4$ from each other. Additionally, the combined ripple frequency will be 4x higher than for a single channel. The total ripple frequency will have a peak-to-peak amplitude less than 1/4 that of a single phase. The translated benefit is that much smaller inductors are required and the output capacitors can be of a much smaller size (as compared to a single channel PWM regulator.) Figure 14 depicts this combined multi-phase behavior where the total output ripple current is much smaller and thus much smaller input and output capacitors are required. Although passive components have natural variation from one phase to another, the IDTP62000 is able to balance the load even if the inductor DCRs are mismatched by up to 40%.

Figure 14: Inductor–Current Waveforms for a 4-Phase Converter



Voltage Regulation

Load Line (DROOP) Regulation (Adaptive Voltage Positioning)

During power supply operation, the load current of the microprocessor changes often. Due to the equivalent series resistance of the output capacitor, an output voltage spike may occur in the load transient. To optimize the system's reliability, performance and cost trade-offs, it is necessary that the voltage regulator adjust the output voltage proportional to changes in the load current. This feature is called adaptive voltage positioning or droop.

By connecting the DROOP and FB pins together, a current IDROOP which is proportional to the average load current flows from FB through the feedback resistor RFB to generate the droop voltage. The output voltage is then adjusted by the droop voltage which is proportional to the load current. The output voltage can be effectively adjusted in the direction to eliminate spikes or drops or to implement load regulation dependency.

In order to avoid abrupt changes in IDROOP in DEC mode when the number of active phases changes, the I_{DROOP} is defined as the total current divided by the number of configured phases rather than active phases. This ensures that the load line will not change when phases are shed.

At light load conditions, a negative inductor current may occur which can cause the current in the current sense amplifier negative input to fall to zero. This is called the “dead zone” of the load line regulation. The IDTP62000 implements an internal bias current on each phase I_{OCDZ} that is a scaled-down version of IREF. This bias current is used to shift the current level up to compensate for negative current during light load operation, which effectively eliminates the dead zone. As shown in Figure 15, there is no dead zone and the load line resistance RLL is 1 mΩ

(Eq.)
Vdroop = Rfb x (DCR / Rsn) x (Iload /n)
where n = # of configured phases

Figure 15: Load Line showing no “Dead Zone”

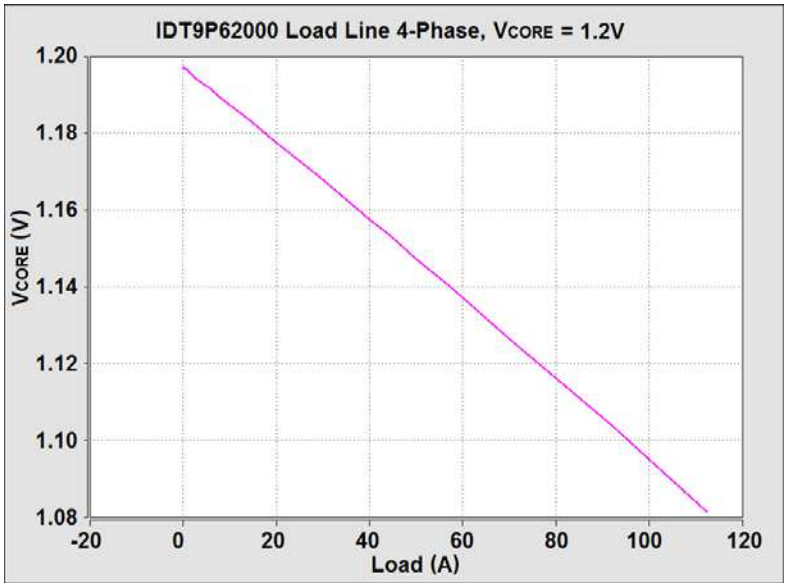
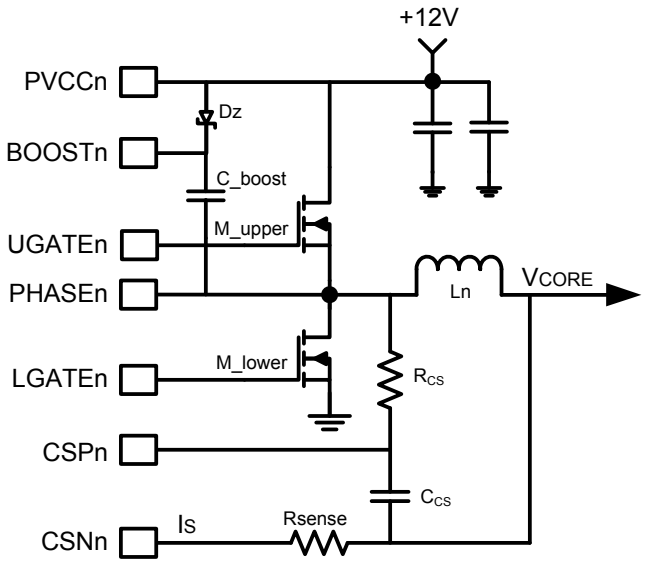


Figure 16: Inductor DCR Current Sensing Configuration



Continuous Current Sensing

The IDTP62000 uses a DCR-based load current sensing for each phase. This sensing scheme uses a pole-zero cancellation technique to allow sensing across the inductor DCR. By doing this, efficiency loss due to an additional sense resistor in the high current path is avoided. The DCR scheme requires a low pass filter consisting of an external resistor and capacitor to be placed across the inductor. See Figure 16. The relationship between the sensed current IS and the inductor current IL is as follows:

(Eq. 1)

$$I_S = \frac{R_{DCR}}{R_{ISENS}} \times \left[\frac{1 + sL/R_{DCR}}{1 + sC_{CS}R_{CS}} \right] \times I_L$$

When the inductor's L/RDCR time constant is set equal to the $C_{CS}R_{CS}$ time constant the term in the square brackets becomes a “1” and effectively disappears from the equation.

The internal sense currents for each phase are used for calculating the droop current, the IMON current, the over-current trip points (average and per phase) and to correct load imbalance among the phases. Furthermore, the average of the sensed currents is used to determine the threshold for transitioning between DVC offsets or DEC modes.

PWM Function and Current Balance Adjustment

The load balance among different phases in IDTP62000 is achieved by modulating the duty cycle of the PWM pulses of the corresponding phase. The IDTP62000 uses trailing edge modulation of the internal triangular waveform by the error amplifier output. The duty cycle of the PWM pulse for a phase is determined by the difference between error signal with the common mode of that phase's triangular waveform.

Load balancing among the active phases is achieved by controlling the duty cycle of each phase through current mode feedback loop derived from the sensed current.

IMON Resistor Calculation (R6 in “4-Phase Applications Reference Circuit” diagram)

R6 = 0.9 x (Sum of sensed currents of all configured phases) / 4

Dynamic Efficiency Control (DEC) Mode of Operation

For efficiency optimization, the IDTP62000 contains a unique and proprietary technique to monitor and adjust the number of active phases based on the sensed load current. An internal determination is used to judge when phases should be turned on and off. Traditional PWM regulators are typically programmed to satisfy the highest load demand. Lighter loads suffer the most inefficiency due to the fixed nature of classic PWM architectures.

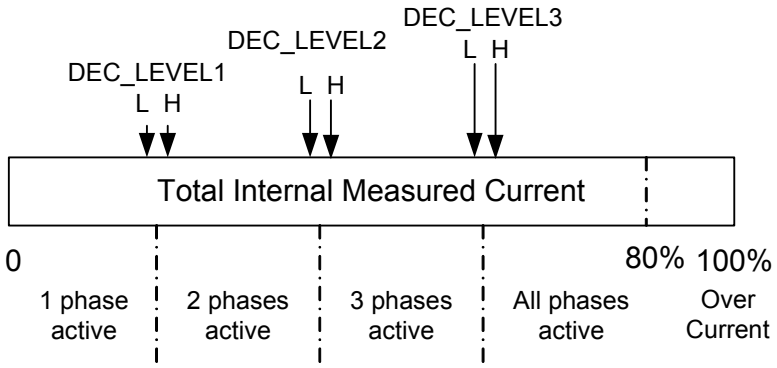
DEC is implemented to improve switching efficiency during light processor loads. In DEC mode, the controller continuously monitors the current load and turns on/off one or more phases according to the load current requirements. The minimum number of phases in DEC mode is configurable and the controller has 3 DEC threshold levels which can each be configured independently.

All DEC levels are defined as a percentage of the scaled average phase current level that triggers an over current protection condition.

The equation for each DEC trip point is given by:
(Eq. 2)

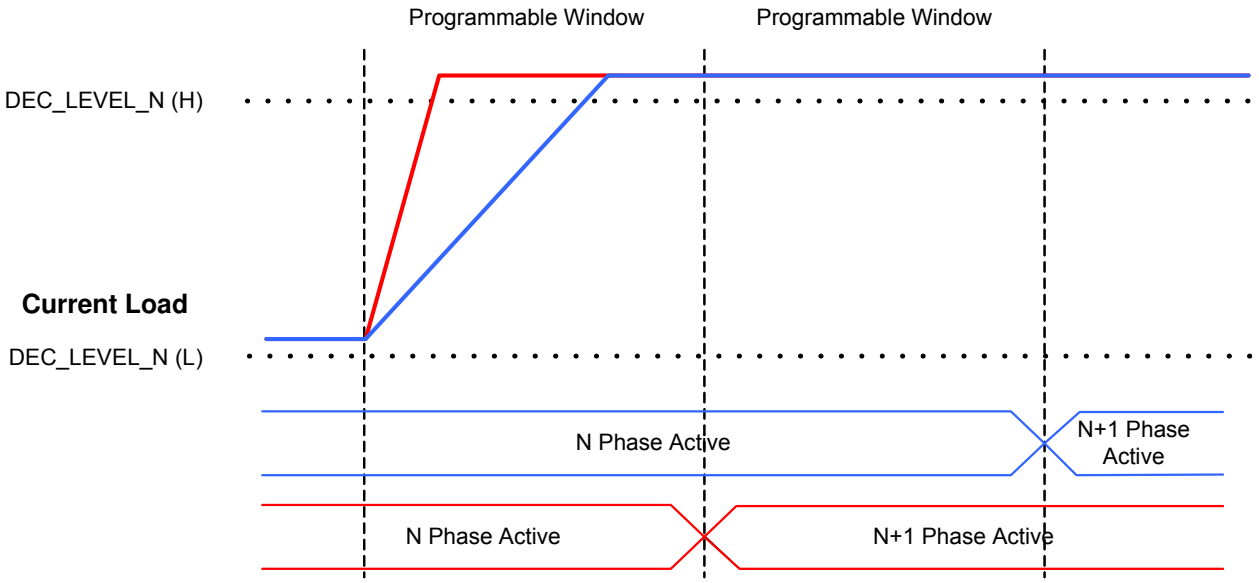
$$\frac{I_{OCAVG} \times (LEVEL[4:0]+1)}{64}$$

Figure 17: DEC Levels showing Hysteresis



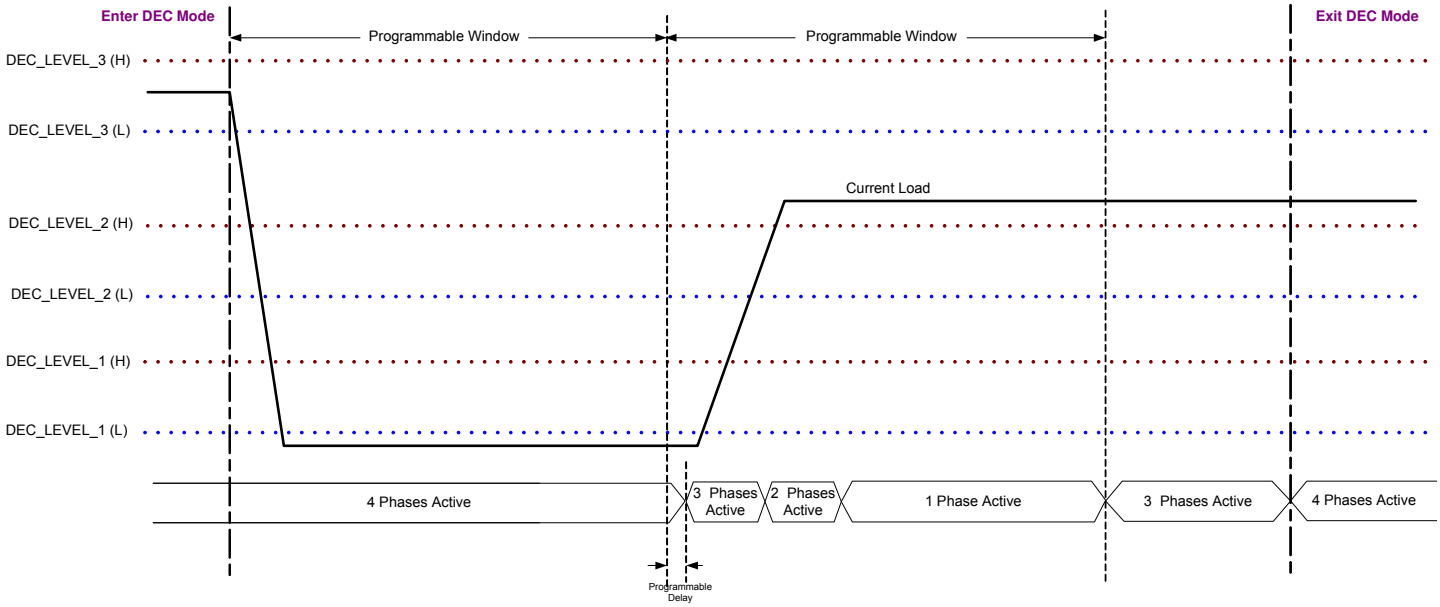
DEC mode is not enabled by default. DEC mode is enabled when the DEC_EN field of the DEC_CTRL register is set to 1b and the maximum number of available phases (based on the total number of configured phases) are turned on. Within a programmable window delay, the controller compares the current load with the three programmed DEC thresholds (all DEC H levels above the current level and all DEC L levels below the current level). No DEC L levels are checked when only 1 phase is enabled, and no DEC H levels are checked when all phases are enabled. If a DEC level transitions across a threshold and remains there for more than 50% of the programmed window period then the number of active phases will be adjusted accordingly.

Figure 18: A Change Across a DEC Threshold Level for >50% Time Duration is Necessary to Trigger Transition



If the load demand increases, all the necessary phases are turned on at the same time. However as the processor load decreases, DEC disables one phase at a time (after a programmable delay) as each DEC level is crossed. The delay comparison period is separately programmable to ensure that the load current remains at the new level long enough to justify a change in the active number of phases.

Figure 19: Normal Operation in DEC Mode

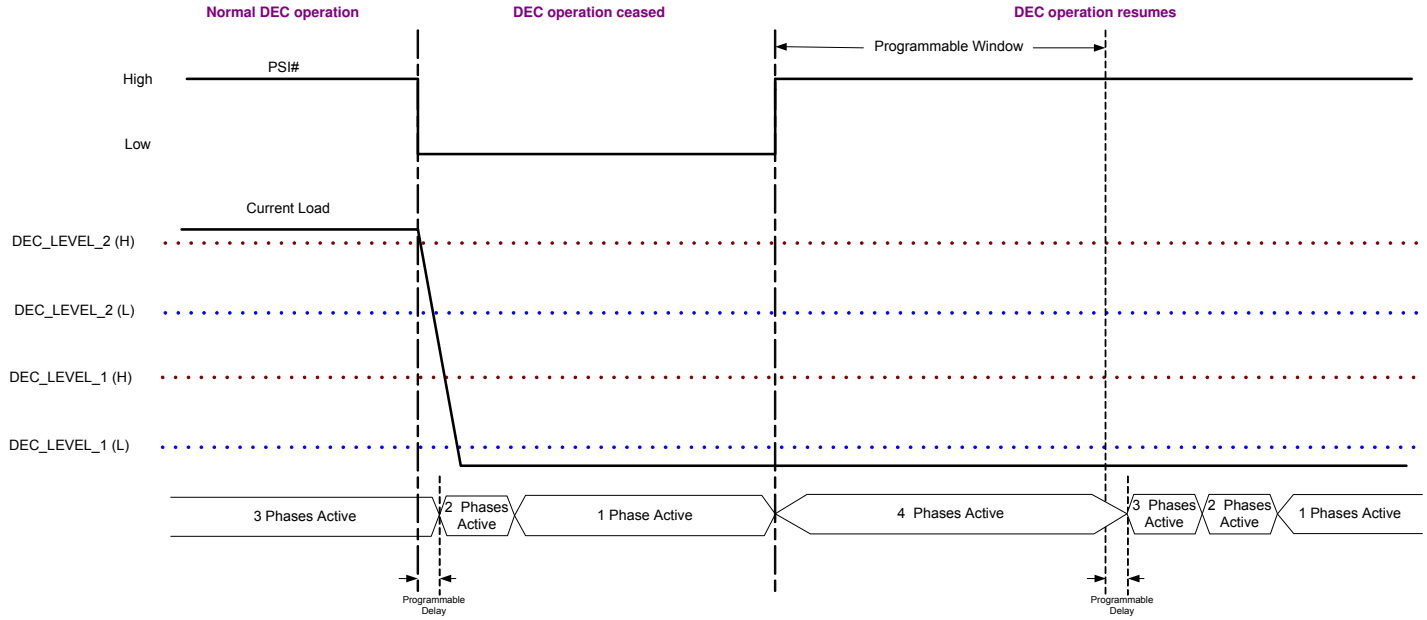


If either an undershoot in VCORE or 50% of the OCP average is detected, DEC mode is exited and the maximum number of phases is immediately reactivated. Once both of these conditions no longer exist, normal DEC operation automatically

resumes.

If PSI and DEC are both enabled, PSI# low indicates that the minimum number of DEC phases is used regardless of the current load. When PSI# is raised from low to high, all phases are used and then normal DEC operation resumes.

Figure 20: DEC Level with PSI Assertion/De-assertion



Oscillator Frequency Selection

The IDTP62000 oscillator can be programmed by an external Rosc resistor. The resistor can be calculated from the following equation:
(Eq. 3)

$$R_{OSC} = 43839 \times f_{SW}^{-1.0971}$$

where f_{sw} is the switching frequency of the PWM regulator in kHz, and R_{osc} is in kΩ

Conversely a given R_{osc} will yield a specific frequency:
(Eq. 4)

$$f_{SW} = 17015 \times R_{OSC}^{-0.9114}$$

Example 1: Given a required switching frequency of 250 kHz and using Equation 3 the resulting R_{osc} value is 102.6 kΩ Using Equation 4 and selecting the closest standard 1% value of 102 kΩ results in a switching frequency of 251.3 kHz.

Example 2: Given a required switching frequency of 500 kHz and using Equation 3 the resulting R_{osc} value is 47.95 kΩ Using Equation 4 and selecting the closest standard 1% value of 47.5 kΩ results in a switching frequency of 504.3 kHz.

Dynamic Voltage Change

The IDTP62000 incorporates a feature whereby the V_{CORE} voltage can be dynamically changed based on the sensed load current. It also supports the existing DFC capability of the clock generator design.

There are four DFC states available in the 9CPS4592 clock generator design. IDTP62000 has four DVC states to match the 9CPS4592. The controller compares the sensed dynamic load current of the processor and compares this sensed level with three load thresholds (DVC_LEVEL) that are register programmed through the SMBUS. As shown in Figure 17, each threshold has one value for rising currents (called “H” for high) and another for falling currents (called “L” for low), so that hysteresis can be implemented in DVC level changes. In addition, each DVC level has an associated register programmed VID code offset value.

The DVC function of IDTP62000 combined with the 9CPS4592 DFC function in a system provides a solution for system design to have optimal performance enhancement and power saving features.

Output-Voltage Offset Programming

Converter output voltage can be offset either higher or lower than the VID voltage. If a resistor is connected between the OFS pin and Vdd the IDTP62000 regulates the voltage across the resistor to 1.6 V. The resulting current is mirrored and will flow from FB pin to ground creating a positive off set in converter output voltage. If a resistor is connected between the OFS pin and ground the voltage across the resistor is regulated to 0.4V and the resulting current is mirrored into the FB pin creating a negative offset voltage. The max offset voltage in either direction is 150µA multiplied by the resistance of RFB. If the OFS pin is left floating then no offset is applied. Equations 7 and 8 describe pin programming of offset voltage. Offset voltage can also be programmed using the SMBus. This works by modifying the VID code and adjusting the under voltage and over voltage thresholds accordingly

Voffset (+) = RFB x (VDD - 1.6) / ROFS (equation 7)
Voffset (-) = RFB x 0.4 / ROFS (equation 8)

DVC Programming

The DVC registers should only be programmed when the DVC mode is disabled i.e. when the DVC_EN bit of the DVC_CTRL register is low. By default, the DVC feature is disabled. It can be enabled by setting the DVC_EN bit to high in the DVC_CTRL register.

Sensed Load Current Thresholds and Filters

IDTP62000 has four output voltage offset values which are delineated by three pairs of sensed load current levels. Each level has user programmable upper and lower threshold level that facilitates the addition of hysteresis. The threshold levels and offsets are illustrated below. When a threshold crossing has been detected, the filter timer DVC_WIN is initiated. The current level has to stay above (or below) the threshold for at least 50% of the timer duration in order for it to be recognized as a DVC trigger event. All DVC levels are defined as a percentage of the average phase current level that triggers an over-current condition (IOCAVG), and are given by IOCAVG*(LEVEL[4:0] + 1)/32.

AMD PVI/SVI Dynamic VID Transitions

In AMD mode, D-VID can “jump” or change by more than one bit step at a time. If the new VID code is stable for 200 ns, the controller will recognize the change and begin to adjust the DAC at a rate of 3.125 mV per 1 µs until the VID and DAC are equal. This means that the total time for a change is dependant on the size of the D-VID change.

Chip Enable and Disable

Proper function of both the controller and the driver requires that the bias voltage applied at VDD, UVLO_PVCC and UVLO_VTT must reach the appropriate threshold voltages as defined in Table 1 and Table 2. The hysteresis between the rising and falling thresholds assures that once enabled, the product will not turn off unless there is a substantial drop in supply voltage bias. A recommended connection for the UVLO_PVCC pin is a voltage divider on the 12 volt supply such that when UVLO_PVCC goes above 0.8 V, the driver will already have been powered up. A fixed hysteresis of 65 mV is internally added such that UVLO_PVCC will not be deactivated until the level drops to 0.735 V.

Similarly, UVLO_VTT uses a voltage divider on the motherboard's VTT supply such that when UVLO_VTT goes above 0.8 V, the driver will already have been powered up. Hysteresis of 65 mV (typical) is again added such that UVLO_VTT will not be deactivated until the level drops to 0.735 V.

There are two means by which the controller can be reset: the internal power-on (POR) reset and the external reset pins, UVLO_PVCC and UVLO_VTT. The internal power-on reset is asserted when the device determines that VDD has reached the voltage defined in Table 2. The external UVLO_PVCC and UVLO_VTT are asserted when each pin has reached the voltage defined in Table 2. POR and both reset pins must be asserted to allow normal operation. Deasserting and then reasserting either one will cause the IDTP62000 to immediately reset and perform a soft start. For a POR reset, all CSR registers are returned to their initial, power-on condition (including fuse and OTP values). For a reset cycle caused by either UVLO_PVCC or UVLO_VTT (called a soft reset) the only registers that will be reset are the status registers in DEV_STAT1 and DEV_STAT2. A soft reset can also be induced by writing a 1 to the SOFT_RESET CSR bit.

Initialization

During power up, the device is tolerant of any permutation of power ramping of the 5 V and 12 V supplies.

It is important to properly determine the number of phases and the appropriate VID table selection before the system starts up. This is done by appropriately connecting VID_SEL and PWM4 pins.

During internal power-on reset, the VID_SEL pin state shall determine which VID table is used. Its value is set by an external pull-up or pull-down resistor where pull-up selects the VRD11 8-bit VID table; pull-down selects the VRD10 6-bit VID table; and floating selects AMD PVI or SVI VID table.

Selection of Phase Number

The IDTP62000 determines the number of phases to be enabled by evaluating the state of the PWM4 pin at power-up. If PWM4 is pulled high, 3 phase mode is selected. If PWM4 is pulled low, 2-phase mode is selected. When used in a 4 phase configuration, an external single phase driver must be used and connected to PWM4. Leakage resistors on this driver's input must cause the PWM4 signal to float to midrail during power up. When this midrail condition is detected, 4 phase mode is selected. The external single phase driver must be powered with the same VDD that is used to power the IDTP62000. The number of phases can be changed using the PhaseN fields in DEV_CTRL1[3:0] register.

The selection table is shown below:

Table 4: PWM4 Level vs. Number of Phases

PWM4 Level	High	MID Voltage	Low
Number of Phases	3-phase	4-phase	2-phase