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DATA SHEET

P80C31X2/32X2

P80C51X2/52X2/54X2/58X2

P87C51X2/52X2/54X2/58X2

80C51 8-bit microcontroller family

4K/8K/16K/32K ROM/OTP

128B/256B RAM

low voltage (2.7 to 5.5 V), low power, high speed (30/33 MHz)

Product data
Supersedes data of 2002 Sep 12

2003 Jan 24

80C51 8-bit microcontroller family
4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
P87C5xX2

DESCRIPTION

The Philips microcontrollers described in this data sheet are high-performance static 80C51 designs incorporating Philips' high-density CMOS technology with operation from 2.7 V to 5.5 V. They support both 6-clock and 12-clock operation.

The P8xC31X2/51X2 and P8xC32X2/52X2/54X2/58X2 contain 128 byte RAM and 256 byte RAM respectively, 32 I/O lines, three 16-bit counter/timers, a six-source, four-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the devices are low power static designs which offer a wide range of operating frequencies down to zero. Two software

selectable modes of power reduction — idle mode and power-down mode — are available. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative. Since the design is static, the clock can be stopped without loss of user data. Then the execution can be resumed from the point the clock was stopped.

SELECTION TABLE

For applications requiring more ROM and RAM, as well as more on-chip peripherals, see the P89C66x and P89C51Rx2 data sheets.

Type	Memory				Timers				Serial Interfaces				ADC bits/ch.	I/O Pins	Interrupts (External)	Program Security	Default Clock Rate	Optional Clock Rate	Max. Freq. at 6-clk / 12-clk (MHz)	Freq. Range at 3V (MHz)	Freq. Range at 5V (MHz)
	RAM	ROM	OTP	Flash	# of Timers	PWM	PCA	WD	UART	I ² C	CAN	SPI									
P87C58X2	256B	—	32K	—	3	—	—	—	✓	—	—	—	—	32	6 (2)	✓	12-clk	6-clk	30/33	0–16	0–30/33
P80C58X2	256B	32K	—	—	3	—	—	—	✓	—	—	—	—	32	6 (2)	✓	12-clk	6-clk	30/33	0–16	0–30/33
P87C54X2	256B	—	16K	—	3	—	—	—	✓	—	—	—	—	32	6 (2)	✓	12-clk	6-clk	30/33	0–16	0–30/33
P80C54X2	256B	16K	—	—	3	—	—	—	✓	—	—	—	—	32	6 (2)	✓	12-clk	6-clk	30/33	0–16	0–30/33
P87C52X2	256B	—	8K	—	3	—	—	—	✓	—	—	—	—	32	6 (2)	✓	12-clk	6-clk	30/33	0–16	0–30/33
P80C52X2	256B	8K	—	—	3	—	—	—	✓	—	—	—	—	32	6 (2)	✓	12-clk	6-clk	30/33	0–16	0–30/33
P87C51X2	128B	—	4K	—	3	—	—	—	✓	—	—	—	—	32	6 (2)	✓	12-clk	6-clk	30/33	0–16	0–30/33
P80C51X2	128B	4K	—	—	3	—	—	—	✓	—	—	—	—	32	6 (2)	✓	12-clk	6-clk	30/33	0–16	0–30/33
P80C32X2	256B	—	—	—	3	—	—	—	✓	—	—	—	—	32	6 (2)	—	12-clk	6-clk	30/33	0–16	0–30/33
P80C31X2	128B	—	—	—	3	—	—	—	✓	—	—	—	—	32	6 (2)	—	12-clk	6-clk	30/33	0–16	0–30/33

NOTE:

- I²C = Inter-Integrated Circuit Bus; CAN = Controller Area Network; SPI = Serial Peripheral Interface; PCA = Programmable Counter Array; ADC = Analog-to-Digital Converter; PWM = Pulse Width Modulation

80C51 8-bit microcontroller family
 4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
 low power, high speed (30/33 MHz)

**P80C3xX2; P80C5xX2;
 P87C5xX2**

FEATURES

- 80C51 Central Processing Unit
 - 4 kbytes ROM/EPROM (P80/P87C51X2)
 - 8 kbytes ROM/EPROM (P80/P87C52X2)
 - 16 kbytes ROM/EPROM (P80/P87C54X2)
 - 32 kbytes ROM/EPROM (P80/P87C58X2)
 - 128 byte RAM (P80/P87C51X2 and P80C31X2)
 - 256 byte RAM (P80/P87C52/54X2/58X2 and P80C32X2)
 - Boolean processor
 - Fully static operation
 - Low voltage (2.7 V to 5.5 V at 16 MHz) operation
- 12-clock operation with selectable 6-clock operation (via software or via parallel programmer)
- Memory addressing capability
 - Up to 64 kbytes ROM and 64 kbytes RAM
- Power control modes:
 - Clock can be stopped and resumed
 - Idle mode
 - Power-down mode
- CMOS and TTL compatible
- Two speed ranges at $V_{CC} = 5\text{ V}$
 - 0 to 30 MHz with 6-clock operation
 - 0 to 33 MHz with 12-clock operation
- PLCC, DIP, TSSOP or LQFP packages
- Extended temperature ranges
- Dual Data Pointers
- Security bits:
 - ROM (2 bits)
 - OTP (3 bits)
- Encryption array - 64 bytes
- Four interrupt priority levels
- Six interrupt sources
- Four 8-bit I/O ports
- Full-duplex enhanced UART
 - Framing error detection
 - Automatic address recognition
- Three 16-bit timers/counters T0, T1 (standard 80C51) and additional T2 (capture and compare)
- Programmable clock-out pin
- Asynchronous port reset
- Low EMI (inhibit ALE, slew rate controlled outputs, and 6-clock mode)
- Wake-up from Power Down by an external interrupt.

80C51 8-bit microcontroller family
4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
P87C5xX2

P80C31/32X2 ORDERING INFORMATION (ROMLESS)

Type number	Package			Temperature Range (°C)
	Name	Description	Version	
P80C31X2BA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2	0 to +70
P80C31X2BN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	0 to +70
P80C32X2BA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2	0 to +70
P80C32X2BN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	0 to +70
P80C32X2BBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	0 to +70
P80C32X2FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2	-40 to +85
P80C32X2FN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	-40 to +85

P87C51X2 ORDERING INFORMATION (4 KBYTE OTP)

Type number	Package			Temperature Range (°C)
	Name	Description	Version	
P87C51X2BA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2	0 to +70
P87C51X2BN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	0 to +70
P87C51X2BBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	0 to +70
P87C51X2FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2	-40 to +85
P87C51X2FBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	-40 to +85

P87C52X2 ORDERING INFORMATION (8 KBYTE OTP)

Type number	Package			Temperature Range (°C)
	Name	Description	Version	
P87C52X2BA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2	0 to +70
P87C52X2BN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	0 to +70
P87C52X2BBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	0 to +70
P87C52X2FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2	-40 to +85
P87C52X2FN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	-40 to +85
P87C52X2FBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	-40 to +85

P87C54X2 ORDERING INFORMATION (16 KBYTE OTP)

Type number	Package			Temperature Range (°C)
	Name	Description	Version	
P87C54X2BA	PLCC44	plastic lead chip carrier; 44 leads	SOT187-2	0 to +70
P87C54X2BN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	0 to +70
P87C54X2BBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	0 to +70
P87C54X2BDH	TSSOP38	plastic thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm	SOT510-1	0 to +70
P87C54X2FA	PLCC44	plastic lead chip carrier; 44 leads	SOT187-2	-40 to +85
P87C54X2FBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	-40 to +85

P87C58X2 ORDERING INFORMATION (32 KBYTE OTP)

Type number	Package			Temperature Range (°C)
	Name	Description	Version	
P87C58X2BA	PLCC44	plastic lead chip carrier; 44 leads	SOT187-2	0 to +70
P87C58X2BN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	0 to +70
P87C58X2BBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	0 to +70
P87C58X2FA	PLCC44	plastic lead chip carrier; 44 leads	SOT187-2	-40 to +85
P87C58X2FBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm	SOT389-1	-40 to +85
P87C58X2FN	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1	-40 to +85

All OTP parts listed here are also available as ROM parts (80C5xX2). Please contact your Philips representative if you would like to order a ROM part.

80C51 8-bit microcontroller family
 4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
 low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
 P87C5xX2

PART NUMBER DERIVATION

Memory	Temperature Range	Package
<p>P87C51X2</p> <p>7 = OTP 0 = ROM or ROMless</p> <p>5 = ROM/OTP 3 = ROMless</p> <p>1 = 128 BYTES RAM 4 KBYTES ROM/OTP 2 = 256 BYTES RAM 8 KBYTES ROM/OTP 4 = 256 BYTES RAM 16 KBYTES ROM/OTP 8 = 256 BYTES RAM 32 KBYTES ROM/OTP</p> <p>X2 = 6-clock mode available</p>	<p>B = 0 °C TO +70 °C F = -40 °C TO +85 °C</p>	<p>A = PLCC N = DIP BD = LQFP DH = TSSOP</p>

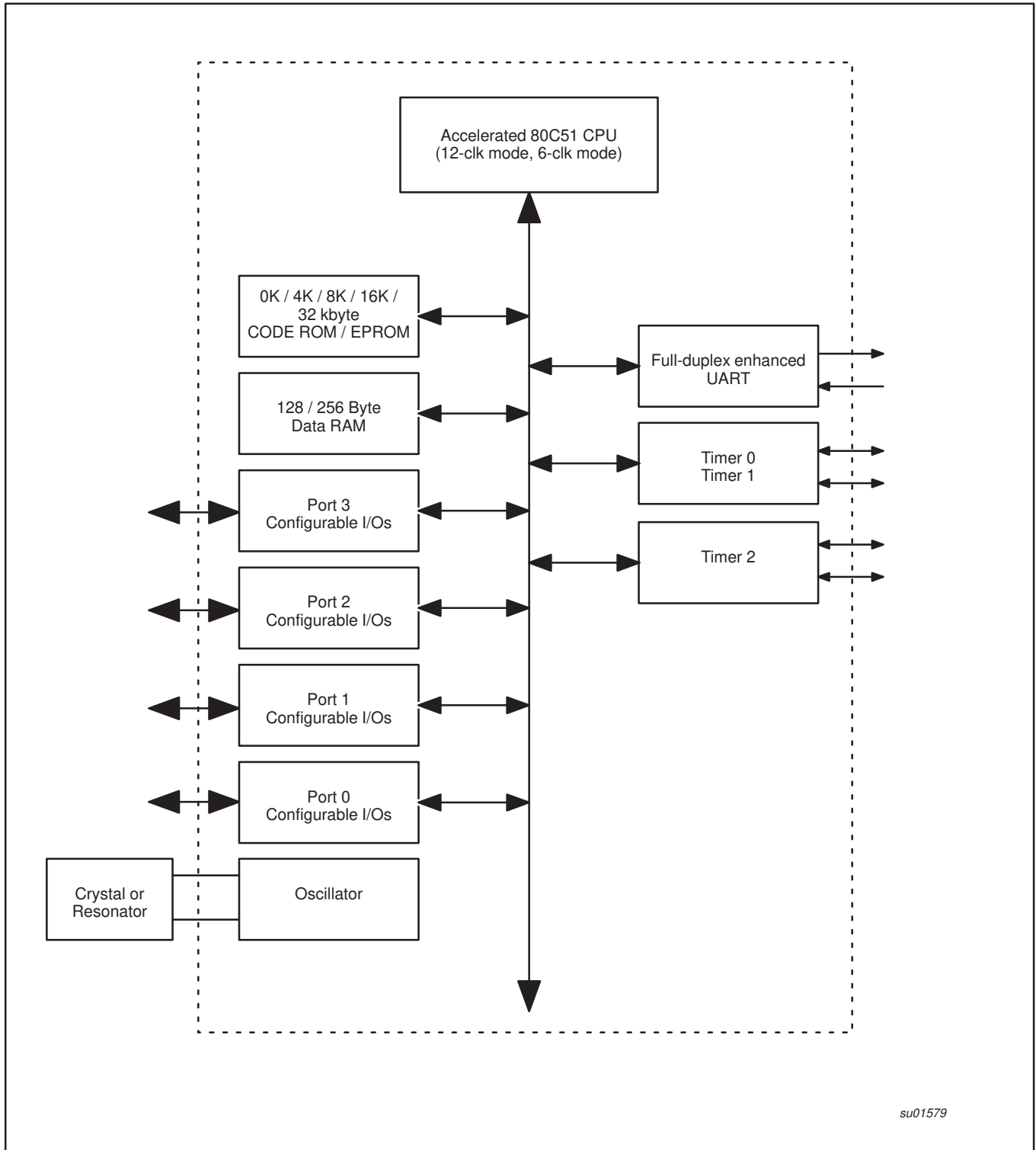
The following table illustrates the correlation between operating mode, power supply and maximum external clock frequency:

Operating Mode	Power Supply	Maximum Clock Frequency
6-clock	5 V ± 10%	30 MHz
6-clock	2.7 V to 5.5 V	16 MHz
12-clock	5 V ± 10%	33 MHz
12-clock	2.7 V to 5.5 V	16 MHz

80C51 8-bit microcontroller family
4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
P87C5xX2

BLOCK DIAGRAM 1

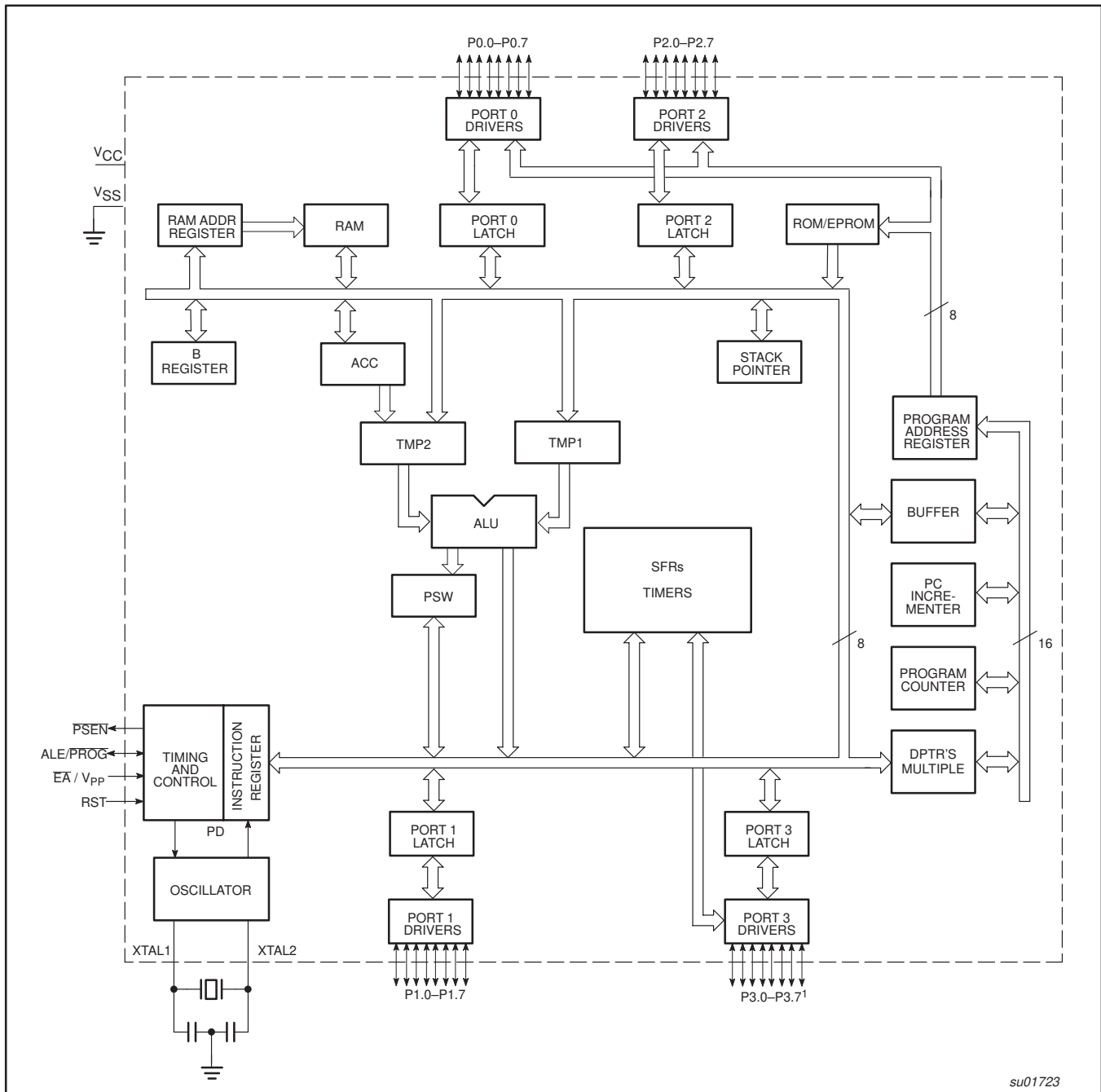


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80C51 8-bit microcontroller family
 4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
 low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
 P87C5xX2

BLOCK DIAGRAM 2 (CPU-ORIENTED)



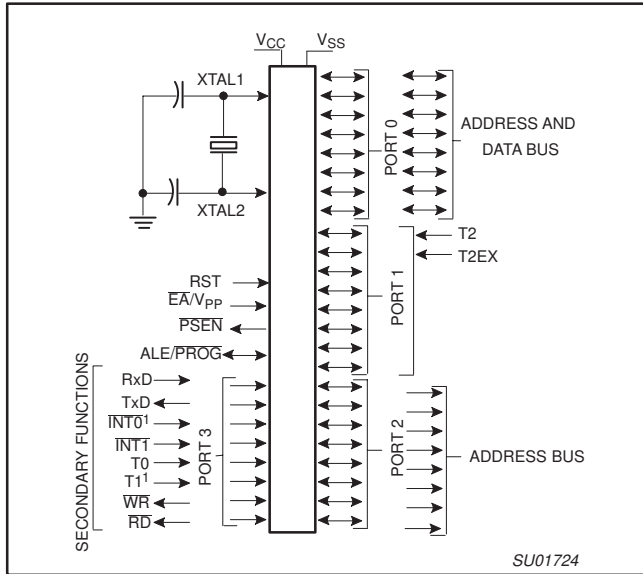
NOTE:

1. P3.2 and P3.5 absent in the TSSOP38 package.

80C51 8-bit microcontroller family
 4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
 low power, high speed (30/33 MHz)

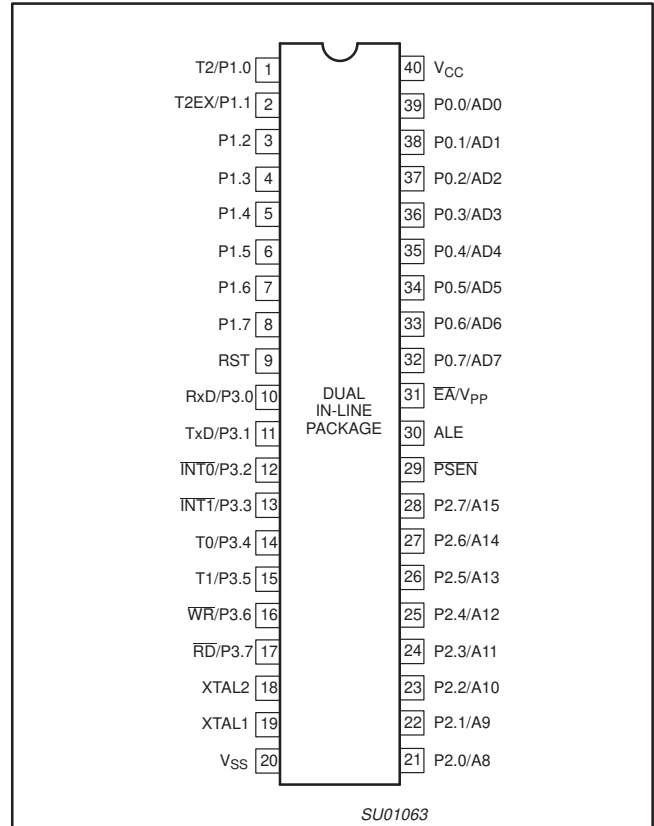
P80C3xX2; P80C5xX2;
 P87C5xX2

LOGIC SYMBOL



NOTE:
 1. INT0/P3.2 and T1/P3.5 are absent in the TSSOP38 package.

**PLASTIC DUAL IN-LINE PACKAGE
 PIN CONFIGURATIONS**



80C51 8-bit microcontroller family
 4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
 low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
 P87C5xX2

PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS

Pin	Function	Pin	Function	Pin	Function
1	NIC*	16	P3.4/T0	31	P2.7/A15
2	P1.0/T2	17	P3.5/T1	32	PSEN
3	P1.1/T2EX	18	P3.6/WR	33	ALE
4	P1.2	19	P3.7/RD	34	NIC*
5	P1.3	20	XTAL2	35	EA/V _{PP}
6	P1.4	21	XTAL1	36	P0.7/AD7
7	P1.5	22	V _{SS}	37	P0.6/AD6
8	P1.6	23	NIC*	38	P0.5/AD5
9	P1.7	24	P2.0/A8	39	P0.4/AD4
10	RST	25	P2.1/A9	40	P0.3/AD3
11	P3.0/RxD	26	P2.2/A10	41	P0.2/AD2
12	NIC*	27	P2.3/A11	42	P0.1/AD1
13	P3.1/TxD	28	P2.4/A12	43	P0.0/AD0
14	P3.2/INT0	29	P2.5/A13	44	V _{CC}
15	P3.3/INTT	30	P2.6/A14		

* NO INTERNAL CONNECTION

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PLASTIC THIN SHRINK SMALL OUTLINE PACK PIN FUNCTIONS

Pin	Function	Pin	Function	Pin	Function
1	P3.0/RxD	14	P2.4/A12	27	P0.1/AD1
2	P3.1/TxD	15	P2.5/A13	28	P0.0/AD0
3	P3.3/INTT	16	P2.6/A14	29	V _{DD}
4	P3.4/T0	17	P2.7/A15	30	P1.0/T2
5	P3.6/WR	18	PSEN	31	P1.1/T2EX
6	P3.7/RD	19	ALE/PROG	32	P1.2
7	XTAL2	20	EA/V _{PP}	33	P1.3
8	XTAL1	21	P0.7/AD7	34	P1.4
9	V _{SS}	22	P0.6/AD6	35	P1.5
10	P2.0/A8	23	P0.5/AD5	36	P1.6
11	P2.1/A9	24	P0.4/AD4	37	P1.7
12	P2.2/A10	25	P0.3/AD3	38	RST
13	P2.3/A11	26	P0.2/AD2		

su01725

LOW PROFILE QUAD FLAT PACK PIN FUNCTIONS

Pin	Function	Pin	Function	Pin	Function
1	P1.5	16	V _{SS}	31	P0.6/AD6
2	P1.6	17	NIC*	32	P0.5/AD5
3	P1.7	18	P2.0/A8	33	P0.4/AD4
4	RST	19	P2.1/A9	34	P0.3/AD3
5	P3.0/RxD	20	P2.2/A10	35	P0.2/AD2
6	NIC*	21	P2.3/A11	36	P0.1/AD1
7	P3.1/TxD	22	P2.4/A12	37	P0.0/AD0
8	P3.2/INT0	23	P2.5/A13	38	V _{CC}
9	P3.3/INTT	24	P2.6/A14	39	NIC*
10	P3.4/T0	25	P2.7/A15	40	P1.0/T2
11	P3.5/T1	26	PSEN	41	P1.1/T2EX
12	P3.6/WR	27	ALE	42	P1.2
13	P3.7/RD	28	NIC*	43	P1.3
14	XTAL2	29	EA/V _{PP}	44	P1.4
15	XTAL1	30	P0.7/AD7		

* NO INTERNAL CONNECTION

SU01487

80C51 8-bit microcontroller family
4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
P87C5xX2

PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER				TYPE	NAME AND FUNCTION
	DIP	PLCC	LQFP	TSSOP		
V _{SS}	20	22	16	9	I	Ground: 0 V reference.
V _{CC}	40	44	38	29	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.
P0.0-0.7	39-32	43-36	37-30	28-21	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification and received code bytes during EPROM programming. External pull-ups are required during program verification.
P1.0-P1.7	1-8	2-9	40-44, 1-3	30-37	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions for Port 1 include:
	1	2	40	30	I/O	T2 (P1.0): Timer/Counter 2 external count input/clockout (see Programmable Clock-Out)
P2.0-P2.7	2	3	41	31	I	T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction control
	21-28	24-31	18-25	10-17	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. Some Port 2 pins receive the high order address bits during EPROM programming and verification.
P3.0-P3.7	10-17	11, 13-19	5, 7-13	1-6	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	5	1	I	RxD (P3.0): Serial input port
	11	13	7	2	O	TxD (P3.1): Serial output port
	12	14	8		I	INT0 (P3.2): External interrupt ¹
	13	15	9	3	I	INT1 (P3.3): External interrupt
	14	16	10	4	I	T0 (P3.4): Timer 0 external input
	15	17	11		I	T1 (P3.5): Timer 1 external input ¹
	16	18	12	5	O	WR (P3.6): External data memory write strobe
	17	19	13	6	O	RD (P3.7): External data memory read strobe
	RST	9	10	4	38	I
ALE/PROG	30	33	27	19	O	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (12-clock Mode) or 1/3 (6-clock Mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming. ALE can be disabled by setting SFR auxiliary.0. With this bit set, ALE will be active only during a MOVX instruction.

80C51 8-bit microcontroller family
 4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
 low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
 P87C5xX2

MNEMONIC	PIN NUMBER				TYPE	NAME AND FUNCTION
	DIP	PLCC	LQFP	TSSOP		
$\overline{\text{PSEN}}$	29	32	26	18	O	Program Store Enable: The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}/V_{\text{PP}}$	31	35	29	20	I	External Access Enable/Programming Supply Voltage: $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to 0FFFH/1FFFH/3FFFH/7FFFH. If $\overline{\text{EA}}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than the on-chip ROM/OTP. This pin also receives the 12.75 V programming supply voltage (V_{PP}) during EPROM programming. If security bit 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	8	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	7	O	Crystal 2: Output from the inverting oscillator amplifier.

NOTES:

To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than $V_{\text{CC}} + 0.5 \text{ V}$ or $V_{\text{SS}} - 0.5 \text{ V}$, respectively.

1. Absent in the TSSOP38 package.

80C51 8-bit microcontroller family
 4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
 low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
 P87C5xX2

Table 1. Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE
			MSB				LSB				
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	–	–	–	–	–	–	–	AO	xxxxxxx0B
AUXR1#	Auxiliary 1	A2H	–	–	–	LPEP ²	WUPD	0	–	DPS	xxx000x0B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
CKCON	Clock Control Register	8FH	–	–	–	–	–	–	–	X2	xxx00000B
DPTR:	Data Pointer (2 bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*	Interrupt Enable	A8H	EA	–	ET2	ES	ET1	EX1	ET0	EX0	0x000000B
			BF	BE	BD	BC	BB	BA	B9	B8	
IP*	Interrupt Priority	B8H	–	–	PT2	PS	PT1	PX1	PT0	PX0	xx000000B
IPH#	Interrupt Priority High	B7H	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	xx000000B
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	–	–	–	–	–	–	T2EX	T2	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	RD	WR	T1	T0	INT1	INT0	TxD	RxD	FFH
PCON# ¹	Power Control	87H	SMOD1	SMOD0	–	POF	GF1	GF0	PD	IDL	00xx0000B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	000000x0B
RACAP2H#	Timer 2 Capture High	CBH									00H
RACAP2L#	Timer 2 Capture Low	CAH									00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	T1	RI	00H
SP	Stack Pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00H
T2MOD#	Timer 2 Mode Control	C9H	–	–	–	–	–	–	T2OE	DCEN	xxxxxx00B
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH									00H
TMOD	Timer Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H

NOTE:

Unused register bits that are not defined should not be set by the user's program. If violated, the device could function incorrectly.

* SFRs are bit addressable.

SFRs are modified from or added to the 80C51 SFRs.

– Reserved bits.

1. Reset value depends on reset source.

2. LPEP – Low Power EPROM operation (OTP only)

80C51 8-bit microcontroller family
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P80C3xX2; P80C5xX2;
 P87C5xX2

OSCILLATOR CHARACTERISTICS

Using the oscillator

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. However, minimum and maximum high and low times specified in the data sheet must be observed.

Clock Control Register (CKCON)

This device provides control of the 6-clock/12-clock mode by both an SFR bit (bit X2 in register CKCON and an OTP bit (bit OX2). When X2 is 0, 12-clock mode is activated. By setting this bit to 1, the system is switching to 6-clock mode. Having this option implemented as SFR bit, it can be accessed anytime and changed to either value. Changing X2 from 0 to 1 will result in executing user code at twice the speed, since all system time intervals will be divided by 2. Changing back from 6-clock to 12-clock mode will slow down running code by a factor of 2.

The OTP clock control bit (OX2) activates the 6-clock mode when programmed using a parallel programmer, superceding the X2 bit (CKCON.0). Please also see Table 2 below.

Table 2.

OX2 clock mode bit (can only be set by parallel programmer)	X2 bit (CKCON.0)	CPU clock mode
erased	0	12-clock mode (default)
erased	1	6-clock mode
programmed	X	6-clock mode

Programmable Clock-Out

A 50% duty cycle clock can be programmed to be output on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

- to input the external clock for Timer/Counter 2, or
- to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency in 12-clock mode (122 Hz to 8 MHz in 6-clock mode).

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{Oscillator Frequency}}{n \times (65536 - \text{RCAP2H}, \text{RCAP2L})}$$

Where:

n = 2 in 6-clock mode, 4 in 12-clock mode.

(RCAP2H, RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock

generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

RESET

A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods in 12-clock and 12 oscillator periods in 6-clock mode), while the oscillator is running. To insure a reliable power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. After the reset, the part runs in 12-clock mode, unless it has been set to 6-clock operation using a parallel programmer.

LOW POWER MODES

Stop Clock Mode

The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and Special Function Registers retain their values. This mode allows step-by-step utilization and permits reduced system power consumption by lowering the clock frequency down to any value. For lowest power consumption the Power Down mode is suggested.

Idle Mode

In idle mode (see Table 3), the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power Down mode (see Table 3) can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values down to 2.0 V and care must be taken to return V_{CC} to the minimum specified operating voltages before the Power Down Mode is terminated.

Either a hardware reset or external interrupt can be used to exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values. WUPD (AUXR1.3—Wakeup from Power Down) enables or disables the wakeup from power down with external interrupt. Where:

WUPD = 0: Disable
 WUPD = 1: Enable

To properly terminate Power Down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

To terminate Power Down with an external interrupt, INT0 or INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

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P87C5xX2

Low-Power EPROM operation (LPEP)

The EPROM array contains some analog circuits that are not required when V_{CC} is less than 4 V, but are required for a V_{CC} greater than 4 V. The LPEP bit (AUXR.4), when set, will powerdown these analog circuits resulting in a reduced supply current. This bit should be set ONLY for applications that operate at a V_{CC} less than 4 V.

Design Consideration

When the idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction

following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE™ Mode

The ONCE (“On-Circuit Emulation”) Mode facilitates testing and debugging of systems without the device having to be removed from the circuit. The ONCE Mode is invoked in the following way:

1. Pull ALE low while the device is in reset and \overline{PSEN} is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and \overline{PSEN} are weakly pulled high. The oscillator circuit remains active. While the device is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 3. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

TIMER 0 AND TIMER 1 OPERATION

Timer 0 and Timer 1

The “Timer” or “Counter” function is selected by control bits C/T in the Special Function Register TMOD. These two Timer/Counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different. The four operating modes are described in the following text.

Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. Figure 2 shows the Mode 0 operation.

In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TF_n. The counted input is enabled to the Timer when TR_n = 1 and either GATE = 0 or \overline{INTn} = 1. (Setting GATE = 1 allows the Timer to be controlled by external input \overline{INTn} , to facilitate pulse width measurements). TR_n is a control bit in the Special Function Register TCON (Figure 3).

The 13-bit register consists of all 8 bits of TH_n and the lower 5 bits of TL_n. The upper 3 bits of TL_n are indeterminate and should be ignored. Setting the run flag (TR_n) does not clear the registers.

Mode 0 operation is the same for Timer 0 as for Timer 1. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

Mode 1

Mode 1 is the same as Mode 0, except that the Timer register is being run with all 16 bits.

Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TL_n) with automatic reload, as shown in Figure 4. Overflow from TL_n not only sets TF_n, but also reloads TL_n with the contents of TH_n, which is preset by software. The reload leaves TH_n unchanged.

Mode 2 operation is the same for Timer 0 as for Timer 1.

Mode 3

Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in Figure 5. TL0 uses the Timer 0 control bits: C/T, GATE, TR0, and TF0 as well as pin $\overline{INT0}$. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the “Timer 1” interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer on the counter. With Timer 0 in Mode 3, an 80C51 can look like it has three Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or can still be used by the serial port as a baud rate generator, or in fact, in any application not requiring an interrupt.

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P80C3xX2; P80C5xX2;
 P87C5xX2

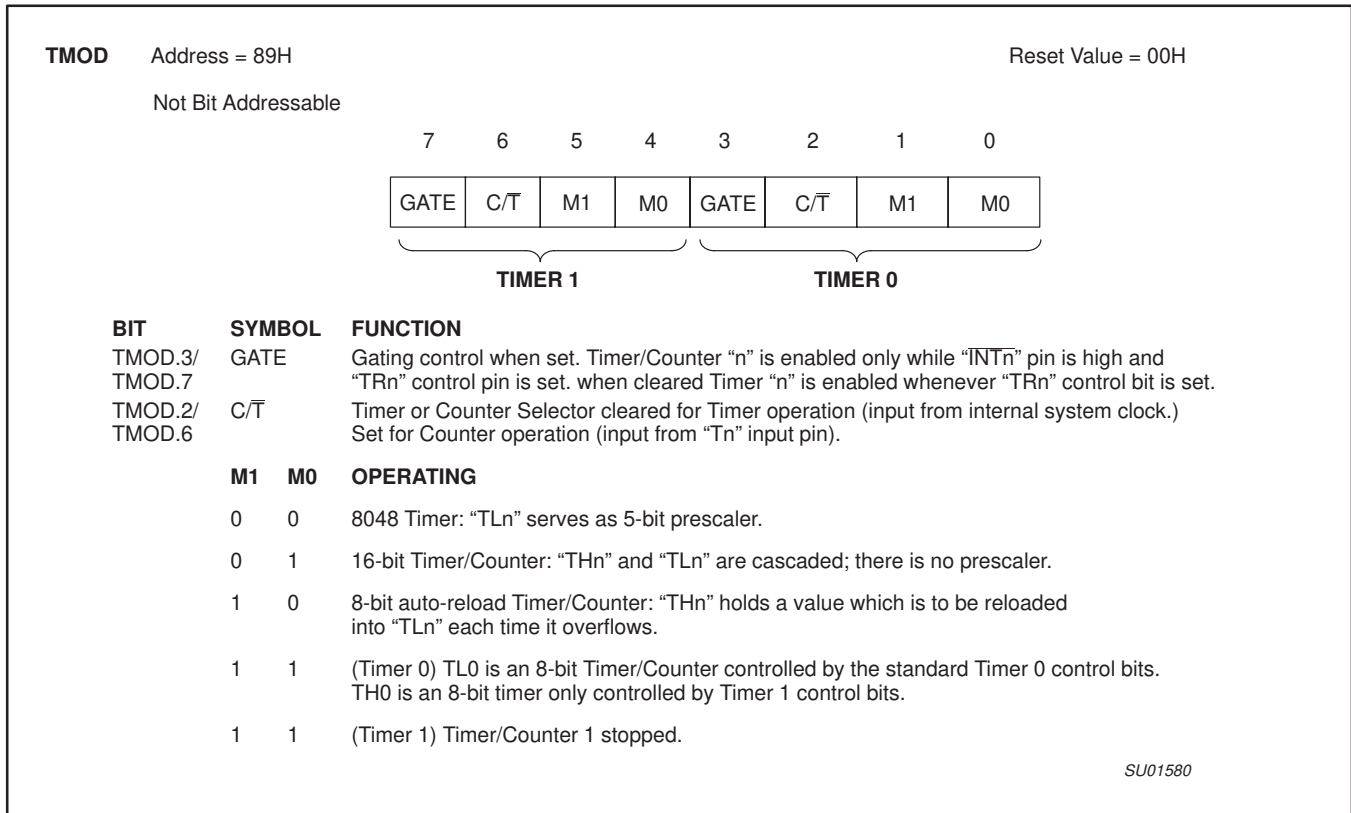


Figure 1. Timer/Counter 0/1 Mode Control (TMOD) Register

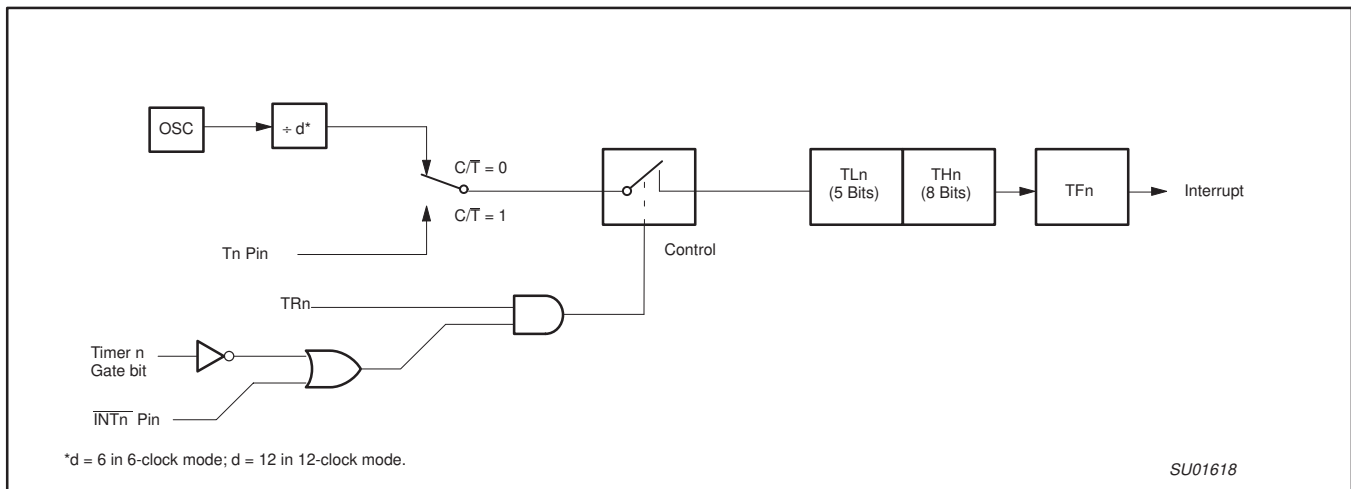


Figure 2. Timer/Counter 0/1 Mode 0: 13-Bit Timer/Counter

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P80C3xX2; P80C5xX2;
 P87C5xX2

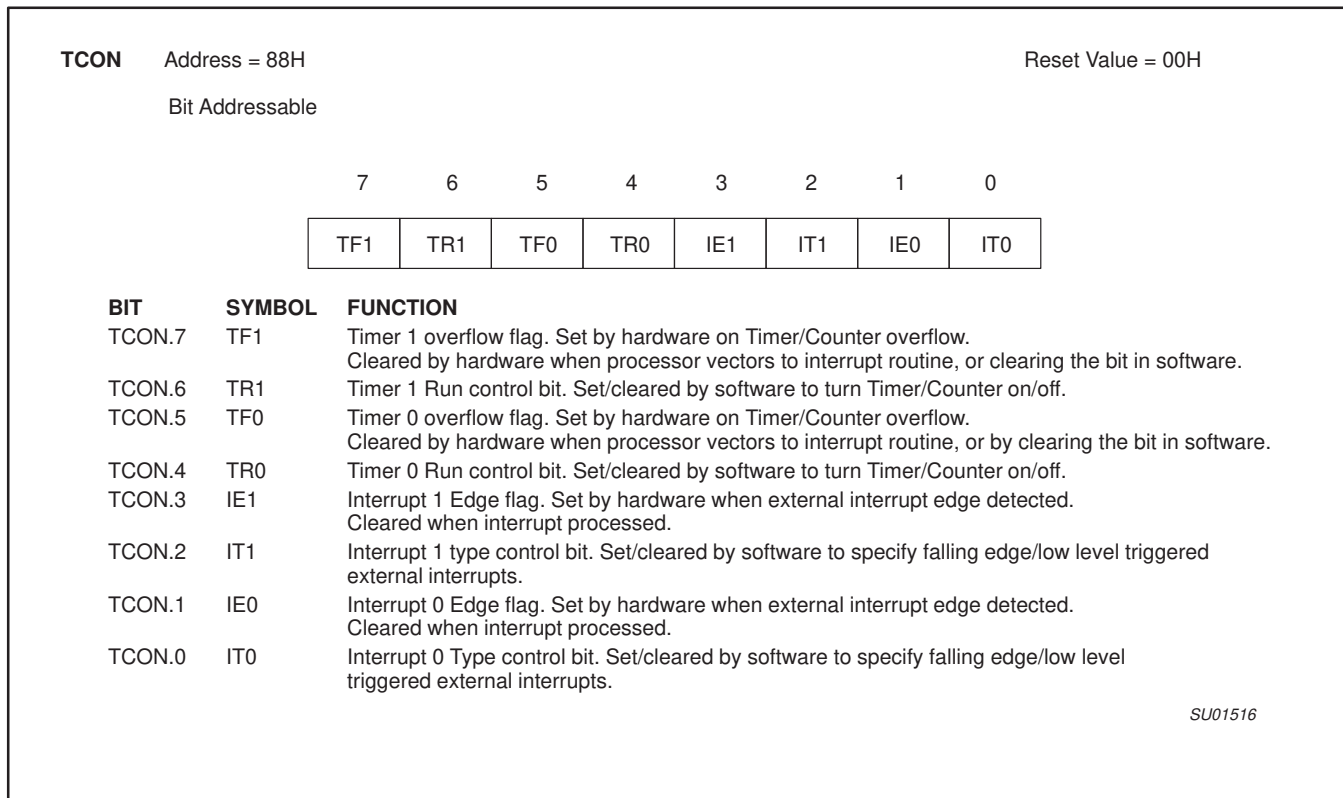


Figure 3. Timer/Counter 0/1 Control (TCON) Register

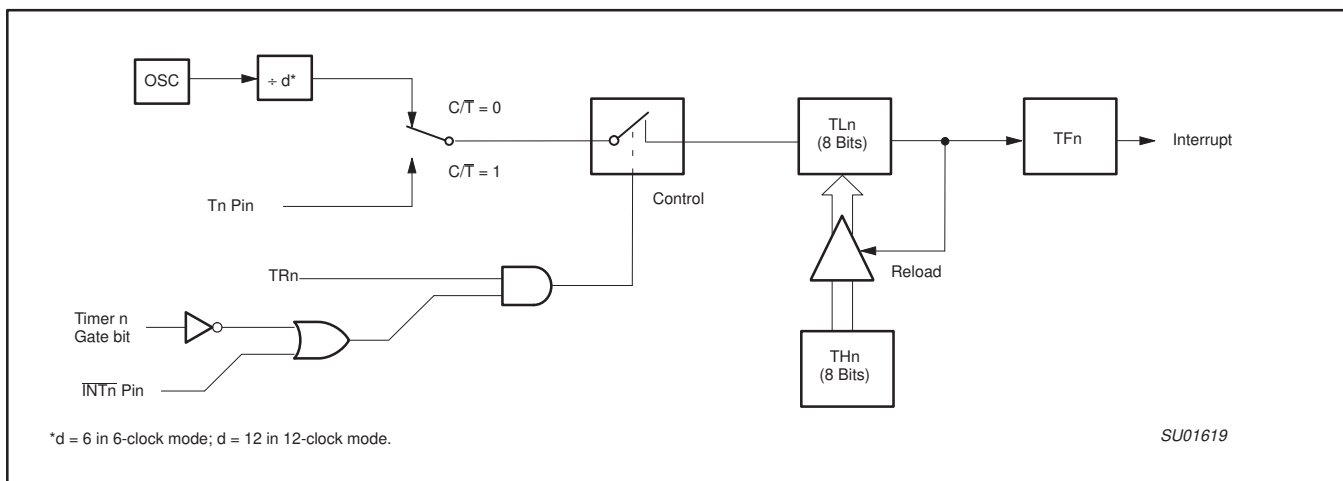


Figure 4. Timer/Counter 0/1 Mode 2: 8-Bit Auto-Reload

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4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
P87C5xX2

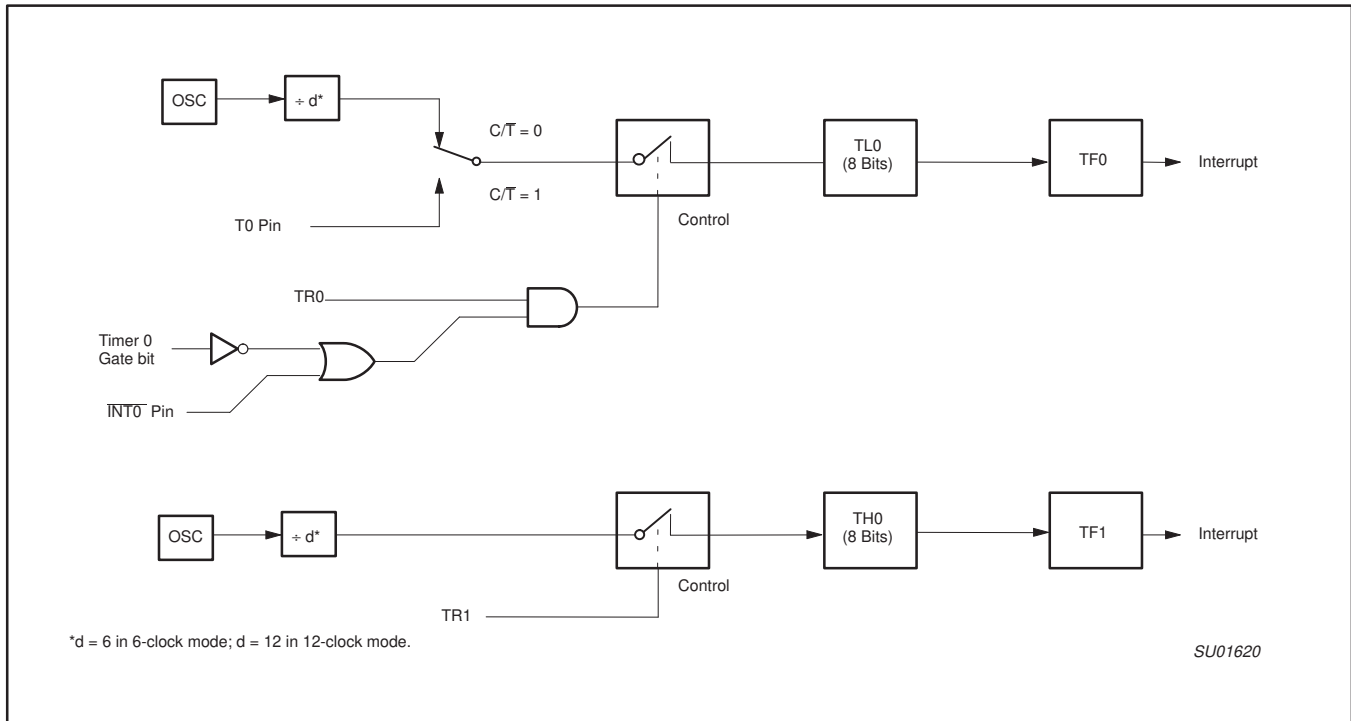


Figure 5. Timer/Counter 0 Mode 3: Two 8-Bit Counters

TIMER 2 OPERATION

Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by $C/T2$ in the special function register T2CON (see Figure 6). Timer 2 has three operating modes: Capture, Auto-reload (up or down counting), and Baud Rate Generator, which are selected by bits in the T2CON as shown in Table 4.

Capture Mode

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2=0, then timer 2 is a 16-bit timer or counter (as selected by $C/T2$ in T2CON) which, upon overflowing, sets bit TF2, the timer 2 overflow bit. This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IE register). If EXEN2=1, Timer 2 operates as described above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 (like TF2) can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt). The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt). The capture mode is illustrated in Figure 7 (There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2EX pin transitions or $osc/12$ (12-clock Mode) or $osc/6$ (6-clock Mode) pulses).

Auto-Reload Mode (Up or Down Counter)

In the 16-bit auto-reload mode, Timer 2 can be configured as either a timer or counter ($C/T2$ in T2CON), then programmed to count up or down. The counting direction is determined by bit DCEN (Down

Counter Enable) which is located in the T2MOD register (see Figure 8). After reset, DCEN=0 which means Timer 2 will default to counting up. If DCEN is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Figure 9 shows Timer 2 which will count up automatically since DCEN=0. In this mode there are two options selected by bit EXEN2 in T2CON register. If EXEN2=0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software.

If EXEN2=1, then a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are 1.

In Figure 10 DCEN=1 which enables Timer 2 to count up or down. This mode allows pin T2EX to control the direction of count. When a logic 1 is applied at pin T2EX, Timer 2 will count up. Timer 2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

A logic 0 applied to pin T2EX causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. A Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2.

The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

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P80C3xX2; P80C5xX2;
 P87C5xX2

Table 4. Timer 2 Operating Modes

RCLK + TCLK	CP/RL2	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud rate generator
X	X	0	(off)

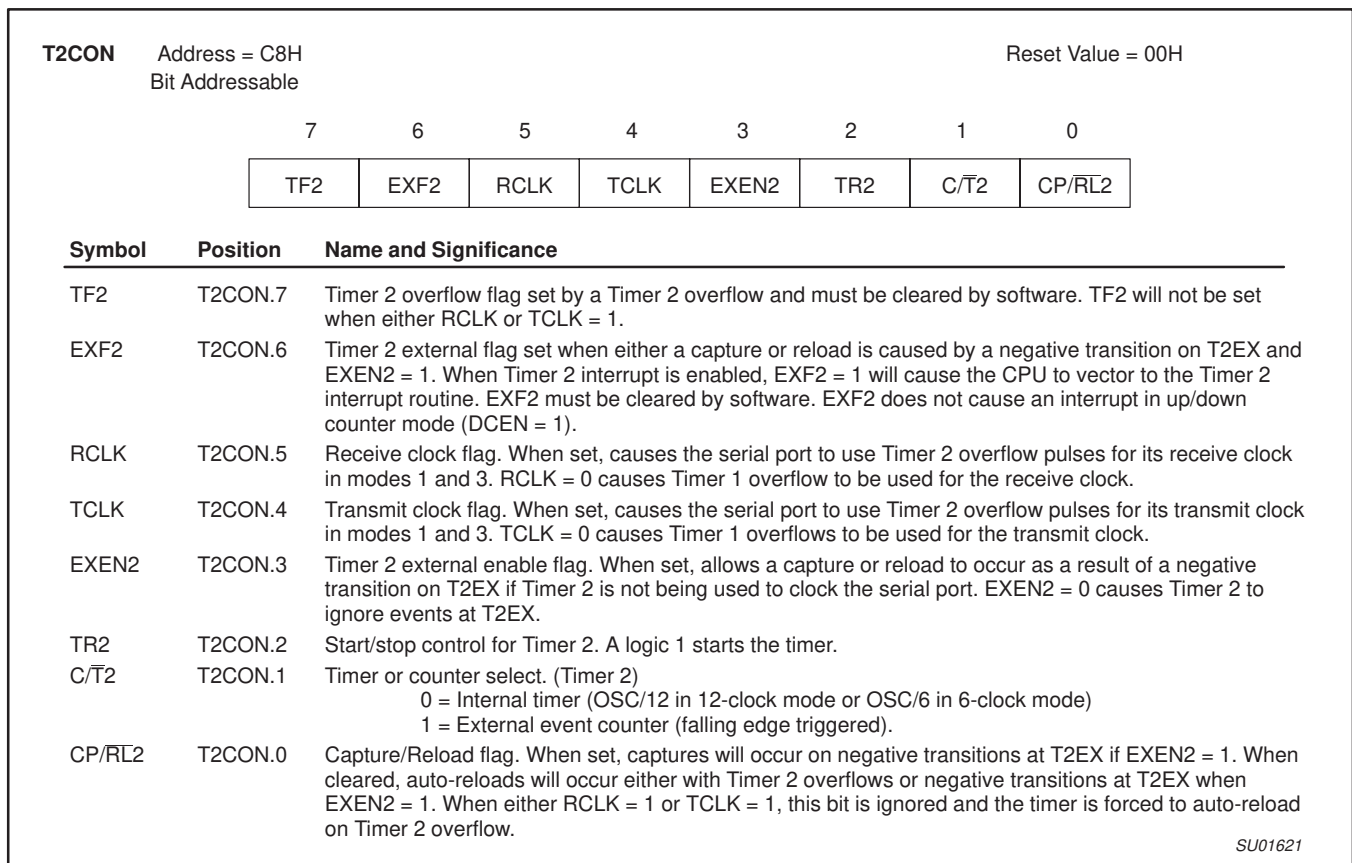


Figure 6. Timer/Counter 2 (T2CON) Control Register

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P80C3xX2; P80C5xX2;
 P87C5xX2

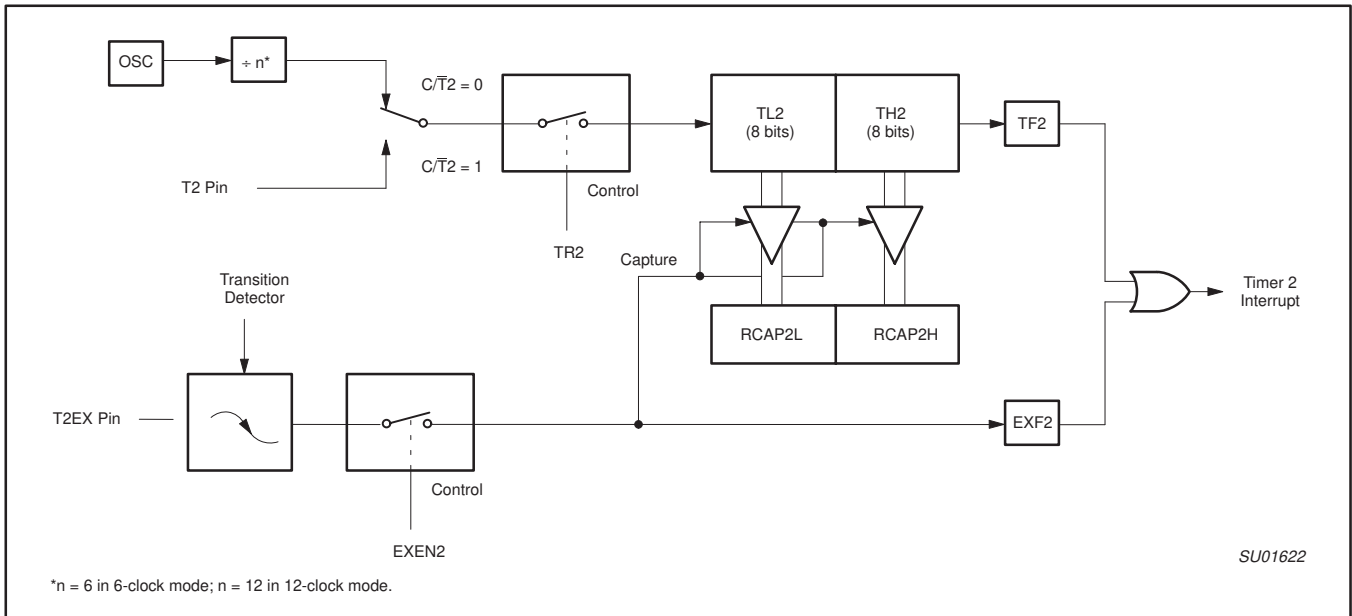


Figure 7. Timer 2 in Capture Mode

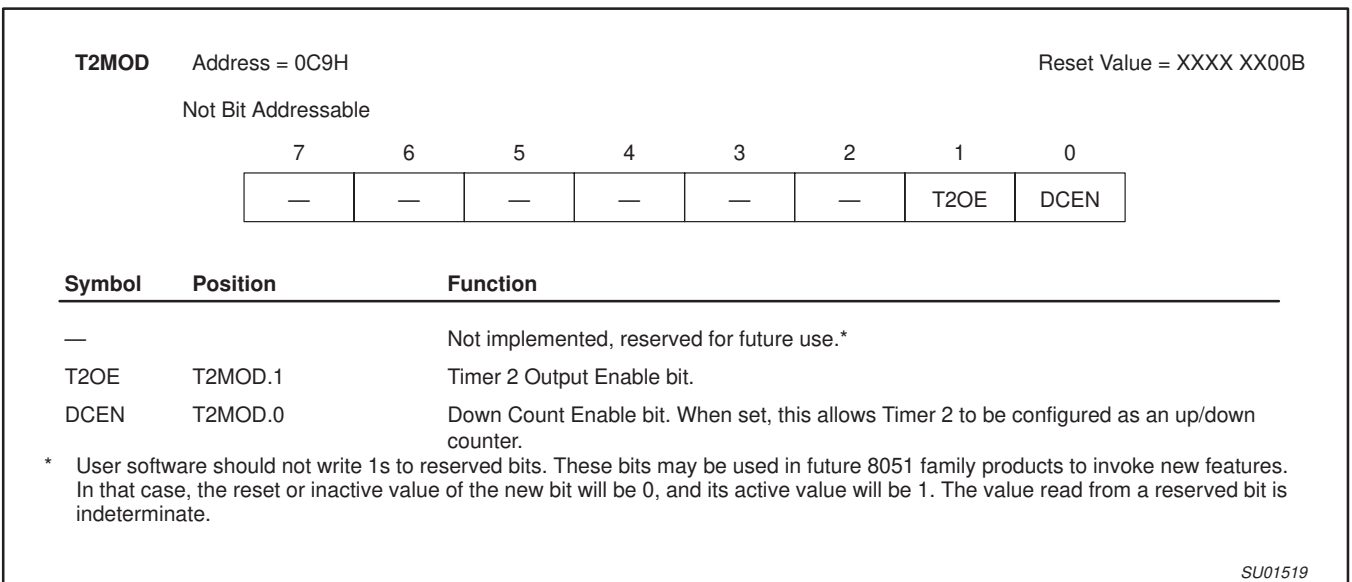


Figure 8. Timer 2 Mode (T2MOD) Control Register

80C51 8-bit microcontroller family
 4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
 low power, high speed (30/33 MHz)

P80C3xX2; P80C5xX2;
 P87C5xX2

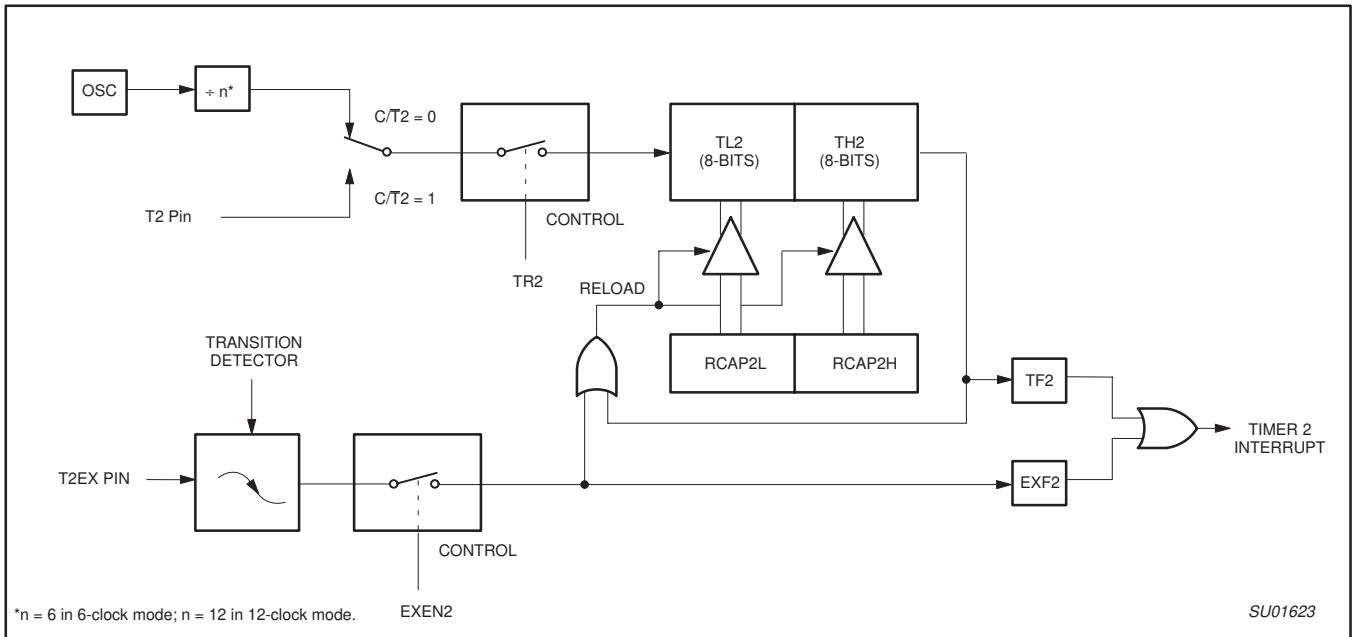


Figure 9. Timer 2 in Auto-Reload Mode (DCEN = 0)

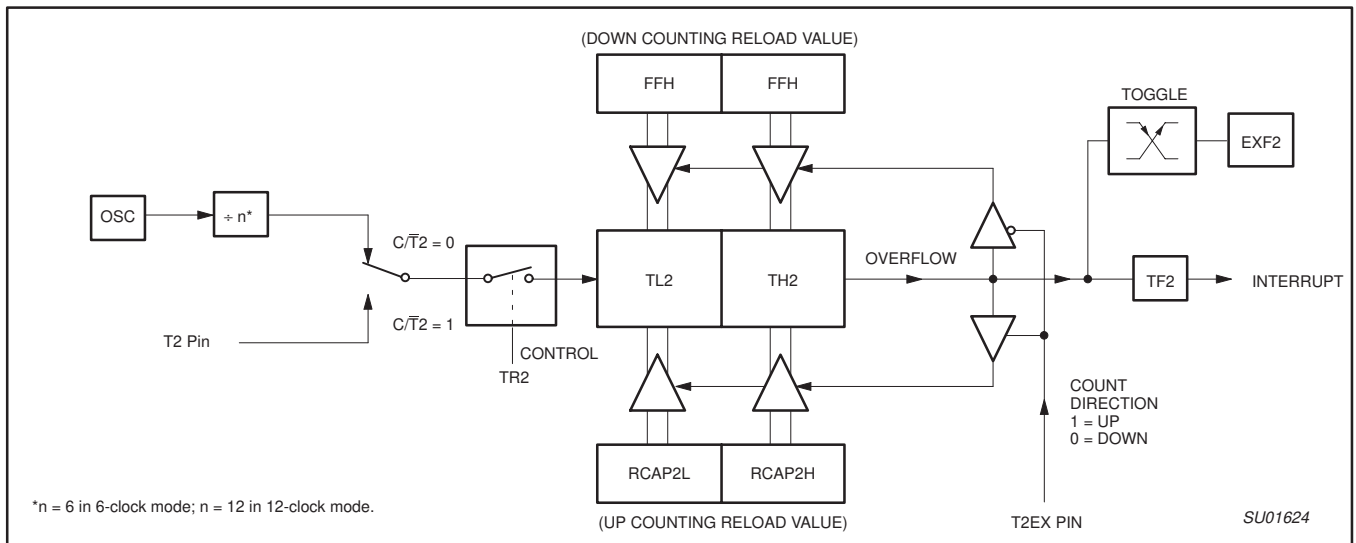


Figure 10. Timer 2 Auto Reload Mode (DCEN = 1)

80C51 8-bit microcontroller family
 4K/8K/16K/32K ROM/OTP, low voltage (2.7 to 5.5 V),
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P80C3xX2; P80C5xX2;
 P87C5xX2

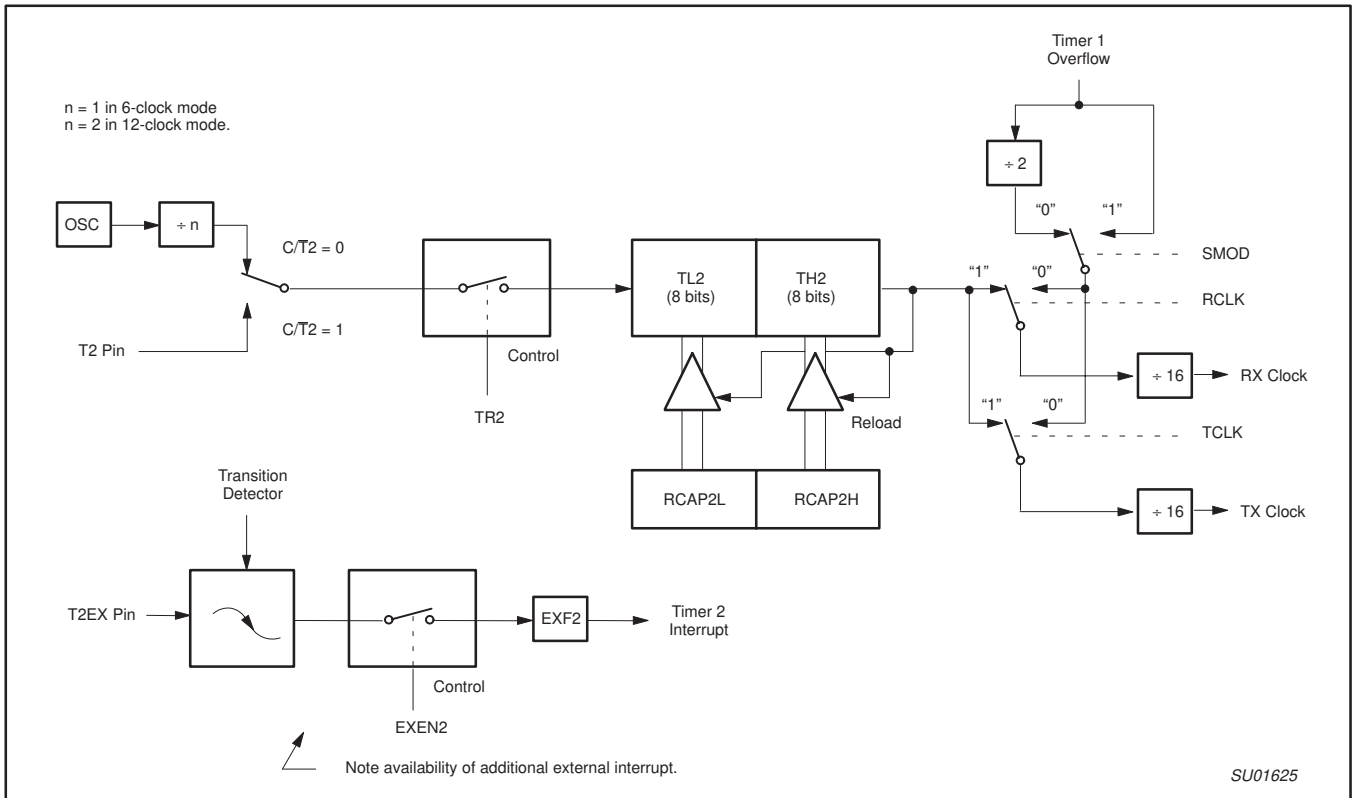


Figure 11. Timer 2 in Baud Rate Generator Mode

Baud Rate Generator Mode

Bits TCLK and/or RCLK in T2CON (Table 4) allow the serial port transmit and receive baud rates to be derived from either Timer 1 or Timer 2. When TCLK= 0, Timer 1 is used as the serial port transmit baud rate generator. When TCLK= 1, Timer 2 is used as the serial port transmit baud rate generator. RCLK has the same effect for the serial port receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates – one generated by Timer 1, the other by Timer 2.

Figure 11 shows the Timer 2 in baud rate generation mode. The baud rate generation mode is like the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The timer can be configured for either "timer" or "counter" operation. In many applications, it is configured for "timer" operation (C/T2=0). Timer operation is different for Timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e., 1/6 the oscillator frequency in 6-clock mode or 1/12 the oscillator frequency in 12-clock mode). As a baud rate generator, it increments at the oscillator frequency in 6-clock mode or at 1/2 the oscillator frequency in 12-clock mode. Thus the baud rate formula is as follows:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Oscillator Frequency}}{[n \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]]}$$

Where:

n = 16 in 6-clock mode, 32 in 12-clock mode.

(RCAP2H, RCAP2L)= The content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 as a baud rate generator mode shown in Figure 11 is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/counter 2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Therefore when Timer 2 is in use as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

When Timer 2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. As a baud rate generator, Timer 2 is incremented every state time (osc/2) or asynchronously from pin T2; under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 5 shows commonly used baud rates and how they can be obtained from Timer 2.

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P80C3xX2; P80C5xX2;
 P87C5xX2

Table 5. Timer 2 Generated Commonly Used Baud Rates

Baud Rate		Osc Freq	Timer 2	
12-clk mode	6-clk mode		RCAP2H	RCAP2L
375 K	750 K	12 MHz	FF	FF
9.6 K	19.2 K	12 MHz	FF	D9
4.8 K	9.6 K	12 MHz	FF	B2
2.4 K	4.8 K	12 MHz	FF	64
1.2 K	2.4 K	12 MHz	FE	C8
300	600	12 MHz	FB	1E
110	220	12 MHz	F2	AF
300	600	6 MHz	FD	8F
110	220	6 MHz	F9	57

Summary Of Baud Rate Equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2(P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

If Timer 2 is being clocked internally, the baud rate is:

$$\text{Baud Rate} = \frac{f_{\text{osc}}}{[n \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]]}$$

Where:

n = 16 in 6-clock mode, 32 in 12-clock mode.

f_{osc} = Oscillator Frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$\text{RCAP2H}, \text{RCAP2L} = 65536 - \left(\frac{f_{\text{osc}}}{n \times \text{Baud Rate}} \right)$$

Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. See Table 6 for set-up of Timer 2 as a timer. Also see Table 7 for set-up of Timer 2 as a counter.

Table 6. Timer 2 as a Timer

MODE	T2CON	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

Table 7. Timer 2 as a Counter

MODE	TMOD	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit	02H	0AH
Auto-Reload	03H	0BH

NOTES:

1. Capture/reload occurs only on timer/counter overflow.
2. Capture/reload occurs on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generator mode.

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FULL-DUPLEX ENHANCED UART

Standard UART operation

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost.) The serial port receive and transmit registers are both accessed at Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

- Mode 0:** Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 the oscillator frequency in 12-clock mode or 1/6 the oscillator frequency in 6-clock mode.
- Mode 1:** 10 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.
- Mode 2:** 11 bits are transmitted (through TxD) or received (through RxD): start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On Transmit, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency in 12-clock mode or 1/16 or 1/32 the oscillator frequency in 6-clock mode.
- Mode 3:** 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

Multiprocessor Communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming.

The slaves that weren't being addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

Serial Port Control Register

The serial port control and status register is the Special Function Register SCON, shown in Figure 12. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Baud Rates

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = Oscillator Frequency / 12 (12-clock mode) or / 6 (6-clock mode). The baud rate in Mode 2 depends on the value of bit SMOD in Special Function Register PCON. If SMOD = 0 (which is the value on reset), and the port pins in 12-clock mode, the baud rate is 1/64 the oscillator frequency. If SMOD = 1, the baud rate is 1/32 the oscillator frequency. In 6-clock mode, the baud rate is 1/32 or 1/16 the oscillator frequency, respectively.

Mode 2 Baud Rate =

$$\frac{2^{\text{SMOD}}}{n} \times (\text{Oscillator Frequency})$$

Where:

$$n = 64 \text{ in 12-clock mode, } 32 \text{ in 6-clock mode}$$

The baud rates in Modes 1 and 3 are determined by the Timer 1 or Timer 2 overflow rate.

Using Timer 1 to Generate Baud Rates

When Timer 1 is used as the baud rate generator (T2CON.RCLK = 0, T2CON.TCLK = 0), the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

Mode 1, 3 Baud Rate =

$$\frac{2^{\text{SMOD}}}{n} \times (\text{Timer 1 Overflow Rate})$$

Where:

$$n = 32 \text{ in 12-clock mode, } 16 \text{ in 6-clock mode}$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In the most typical applications, it is configured for "timer" operation, in the auto-reload mode (high nibble of TMOD = 0010B). In that case the baud rate is given by the formula:

Mode 1, 3 Baud Rate =

$$\frac{2^{\text{SMOD}}}{n} \times \frac{\text{Oscillator Frequency}}{12 \times [256 - (\text{TH1})]}$$

Where:

$$n = 32 \text{ in 12-clock mode, } 16 \text{ in 6-clock mode}$$

One can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload. Figure 13 lists various commonly used baud rates and how they can be obtained from Timer 1.

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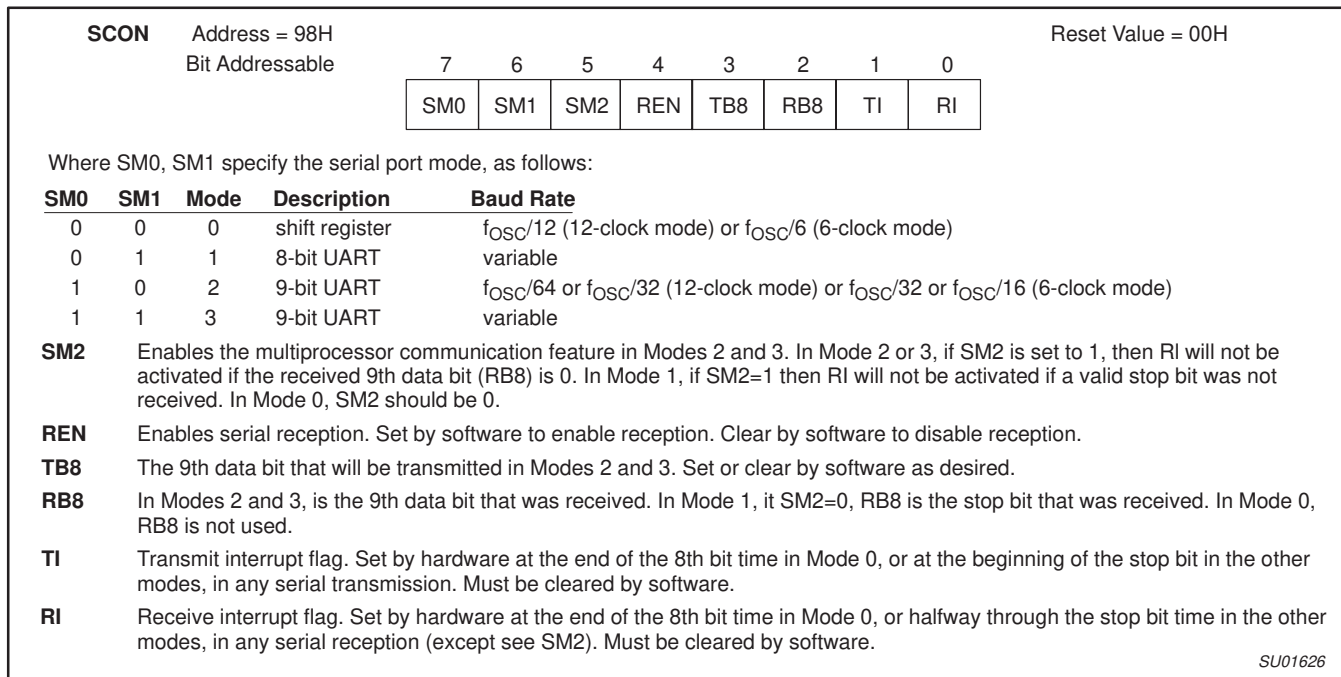


Figure 12. Serial Port Control (SCON) Register

Baud Rate			f _{osc}	SMOD	Timer 1		
Mode	12-clock mode	6-clock mode			C/T	Mode	Reload Value
Mode 0 Max	1.67 MHz	3.34 MHz	20 MHz	X	X	X	X
Mode 2 Max	625 k	1250 k	20 MHz	1	X	X	X
Mode 1, 3 Max	104.2 k	208.4 k	20 MHz	1	0	2	FFH
Mode 1, 3	19.2 k	38.4 k	11.059 MHz	1	0	2	FDH
	9.6 k	19.2 k	11.059 MHz	0	0	2	FDH
	4.8 k	9.6 k	11.059 MHz	0	0	2	FAH
	2.4 k	4.8 k	11.059 MHz	0	0	2	F4H
	1.2 k	2.4 k	11.059 MHz	0	0	2	E8H
	137.5	275	11.986 MHz	0	0	2	1DH
	110	220	6 MHz	0	0	2	72H
	110	220	12 MHz	0	0	1	FEEBH

Figure 13. Timer 1 Generated Commonly Used Baud Rates

More About Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed a 1/12 the oscillator frequency (12-clock mode) or 1/6 the oscillator frequency (6-clock mode).

Figure 14 shows a simplified functional diagram of the serial port in Mode 0, and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal at S6P2 also loads a 1 into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full machine cycle will elapse between "write to SBUF" and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P3.0 and also enable SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1, and S2. At

S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift are shifted to the right one position.

As data bits shift out to the right, zeros come in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control block to do one last shift and then deactivate SEND and set T1. Both of these actions occur at S1P1 of the 10th machine cycle after "write to SBUF."

Reception is initiated by the condition REN = 1 and R1 = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 11111110 to the receive shift register, and in the next clock phase activates RECEIVE.

RECEIVE enable SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are

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shifted to the left one position. The value that comes in from the right is the value that was sampled at the P3.0 pin at S5P2 of the same machine cycle.

As data bits come in from the right, 1s shift out to the left. When the 0 that was initially loaded into the rightmost position arrives at the leftmost position in the shift register, it flags the RX Control block to do one last shift and load SBUF. At S1P1 of the 10th machine cycle after the write to SCON that cleared RI, RECEIVE is cleared as RI is set.

More About Mode 1

Ten bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the 80C51 the baud rate is determined by the Timer 1 or Timer 2 overflow rate.

Figure 15 shows a simplified functional diagram of the serial port in Mode 1, and associated timings for transmit receive.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads a 1 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal.)

The transmission begins with activation of SEND which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeros are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 10th divide-by-16 rollover after "write to SBUF."

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RxD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in mode 1 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.:

1. RI = 0, and
2. Either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time,

whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RxD.

More About Modes 2 and 3

Eleven bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of 0 or 1. On receive, the 9th data bit goes into RB8 in SCON. The baud rate is programmable to either 1/32 or 1/64 (12-clock mode) or 1/16 or 1/32 the oscillator frequency (6-clock mode) the oscillator frequency in Mode 2. Mode 3 may have a variable baud rate generated from Timer 1 or Timer 2.

Figures 16 and 17 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal.)

The transmission begins with activation of SEND, which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeros are clocked in. Thus, as data bits shift out to the right, zeros are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after "write to SBUF."

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of R-D. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.

1. RI = 0, and
2. Either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a 1-to-0 transition at the RxD input.