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P89LPC912/913/914

8-bit microcontrollers with two-clock 80C51 core, 1 kB 3 V flash with 128-byte RAM

Rev. 05 — 28 September 2007 Product data sheet

1. General description

The P89LPC912/913/914 are single-chip microcontrollers in low-cost 14-pin packages, based on a high performance processor architecture that executes instructions in two to four clocks, six times the rate of standard 80C51 devices. Many system-level functions have been incorporated into the P89LPC912/913/914 in order to reduce component count, board space, and system cost.

2. Features

2.1 Principal features

- 1 kB byte-erasable flash code memory organized into 256 B sectors and 16 B pages. Single-byte erasing allows any byte(s) to be used as non-volatile data storage.
- 128 B RAM data memory.
- Two 16-bit counter/timers. Each timer may be configured to toggle a port output upon timer overflow or to become a PWM output.
- 23-bit system timer that can also be used as a RTC.
- Two analog comparators with selectable inputs and reference source.
- Enhanced UART with fractional baud rate generator, break detect, framing error detection, automatic address detection and versatile interrupt capabilities (P89LPC913, P89LPC914).
- SPI communication port.
- Internal RC oscillator (factory calibrated to ±1 %) option allows operation without external oscillator components. The RC oscillator option is selectable and fine tunable.
- 2.4 V to 3.6 V V_{DD} operating range. I/O pins are 5 V tolerant (may be pulled up or driven to 5.5 V).
- Up to 12 I/O pins when using internal oscillator and reset options.

2.2 Additional features

- 14-pin TSSOP packages.
- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz (167 ns to 333 ns at 12 MHz). This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- In-Application Programming (IAP-Lite) and byte erase allows code memory to be used for non-volatile data storage.

- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from eight values.
- Low voltage reset (brownout detect) allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz (P89LPC912, P89LPC913).
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open-drain, push-pull, input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC912/913/914 when internal reset option is selected.
- Four interrupt priority levels.
- Four keypad interrupt inputs.
- Second data pointer.
- Schmitt trigger port inputs.
- Emulation support.

3. Product comparison

Table 1 highlights the differences between these three devices. For a complete list of device features, please see Section 2 “Features” on page 1.

Table 1. Product comparison

Type number	External crystal pins	X2 CLKOUT	T0 PWM output	SPI with $\overline{SS}$ pin	SPI without $\overline{SS}$ pin	UART		Max f_{osc} (MHz)
						TXD	RXD	
P89LPC912	X	X	X	X	-	-	-	18
P89LPC913	X	X	-	-	X	X	X	18
P89LPC914	-	-	X	X	-	X	X	12

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
P89LPC912FDH	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
P89LPC912HDH			
P89LPC913FDH			
P89LPC914FDH			

4.1 Ordering options

Table 3. Ordering options

Type number	Temperature range	Frequency
P89LPC912FDH	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC912HDH	–40 °C to +125 °C	0 MHz to 18 MHz
P89LPC913FDH	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC914FDH	–40 °C to +85 °C	0 MHz to 12 MHz

5. Block diagram

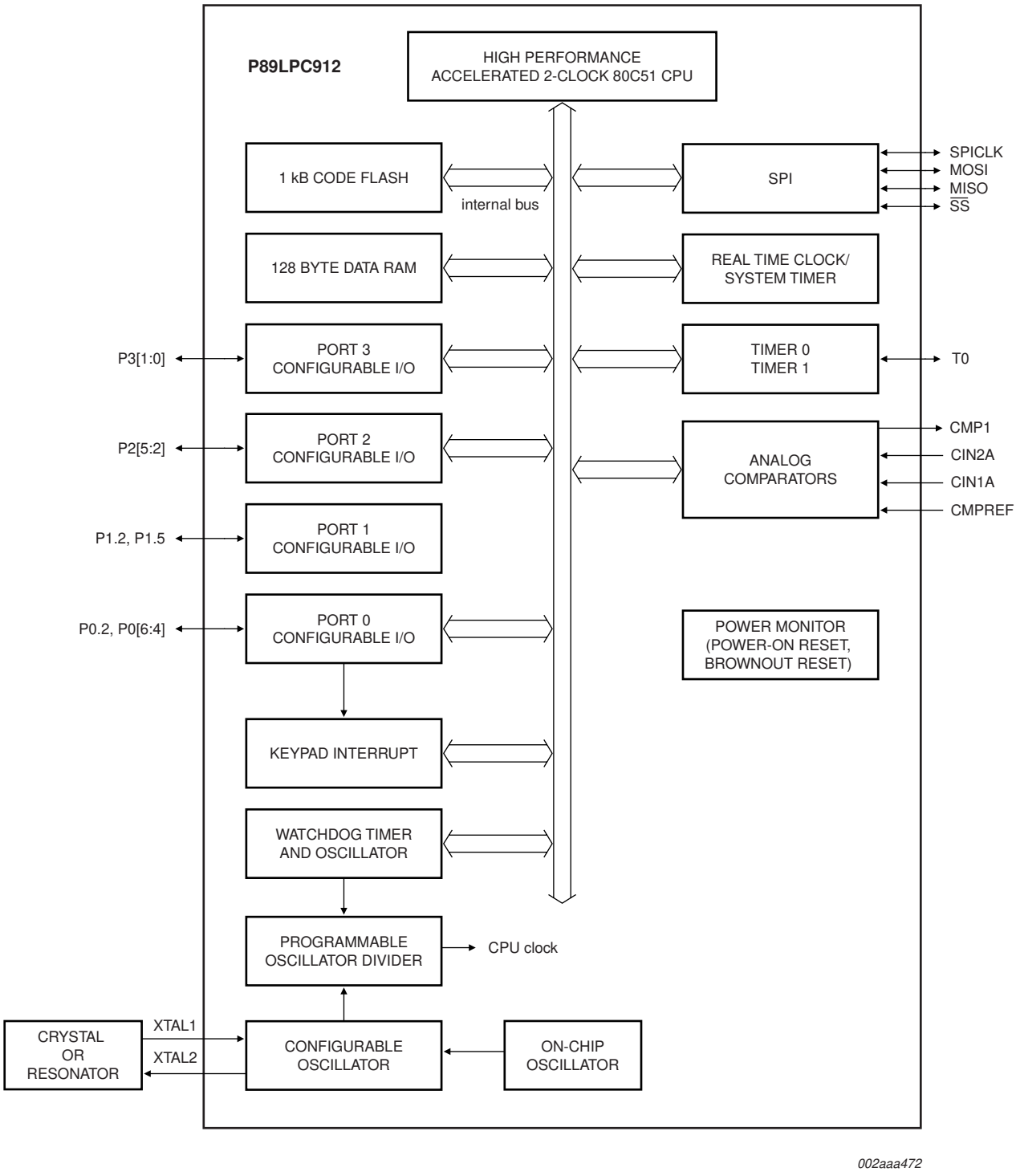

Fig 1. P89LPC912 block diagram

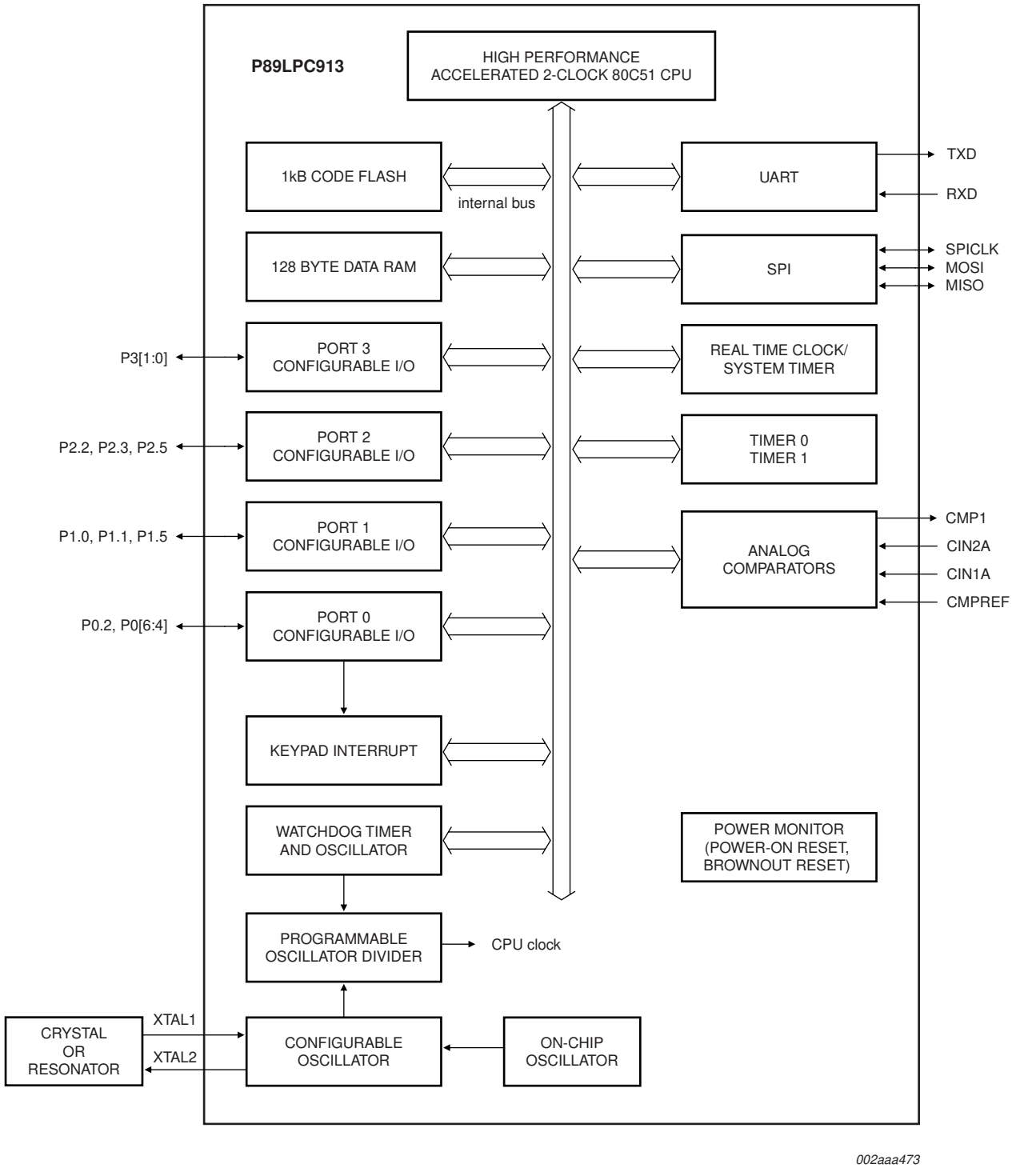

Fig 2. P89LPC913 block diagram

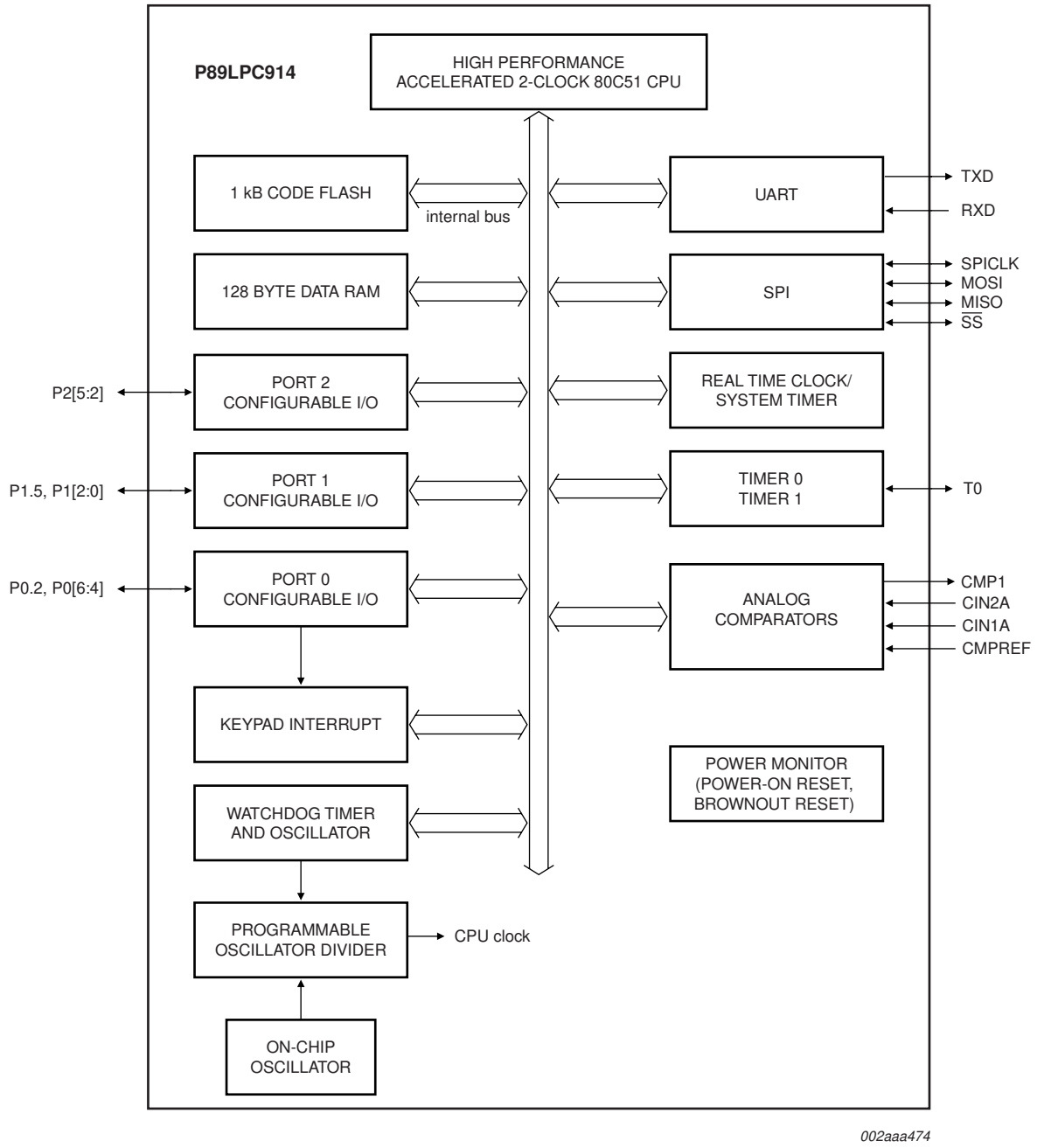

Fig 3. P89LPC914 block diagram

6. Functional diagram

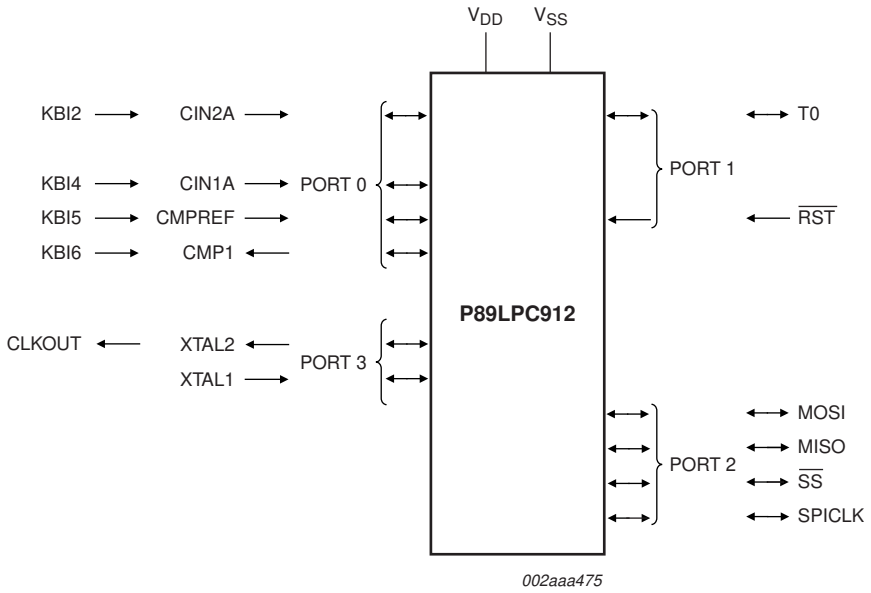

Fig 4. P89LPC912 functional diagram

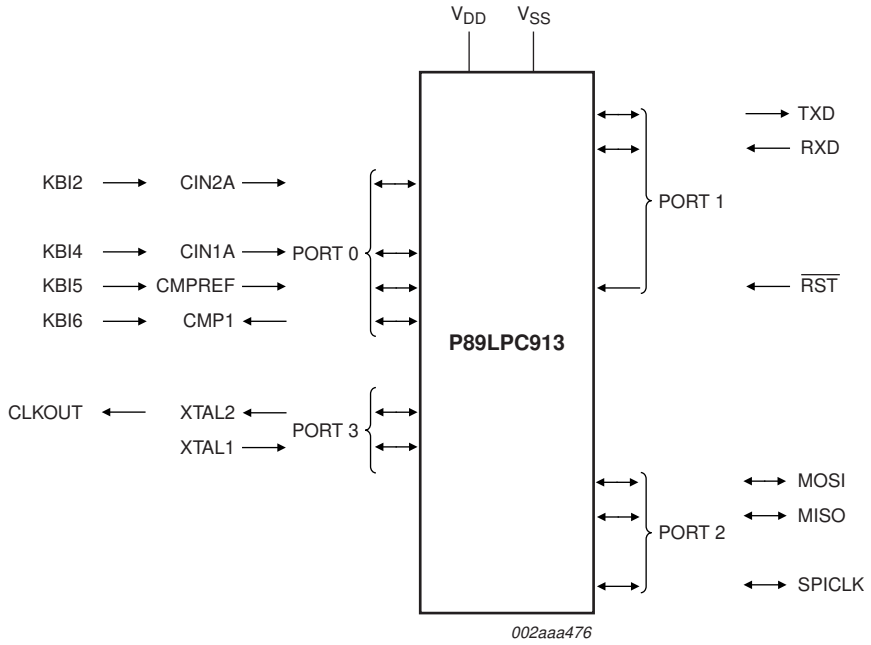

Fig 5. P89LPC913 functional diagram

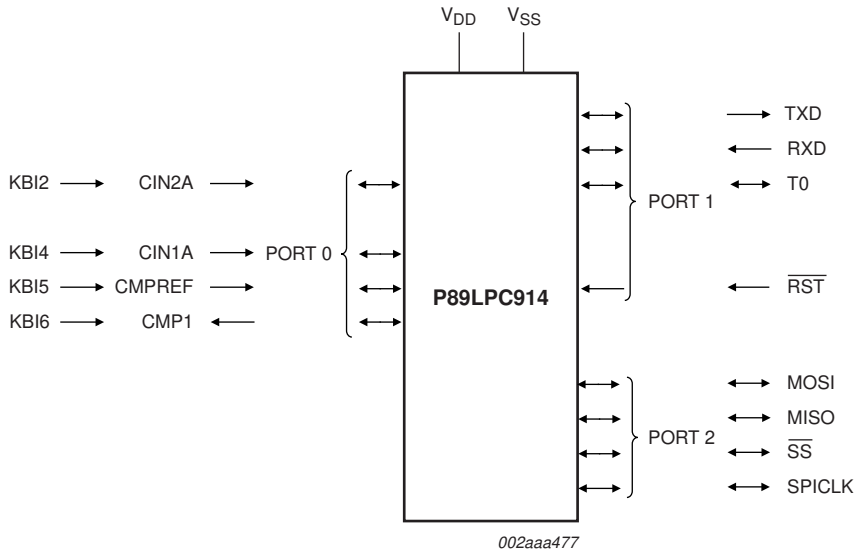

Fig 6. P89LPC914 functional diagram

7. Pinning information

7.1 Pinning

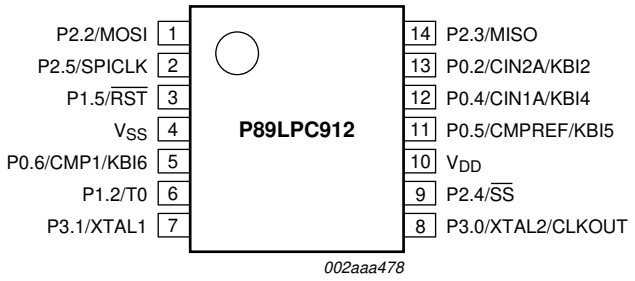

Fig 7. P89LPC912 TSSOP14 pin configuration

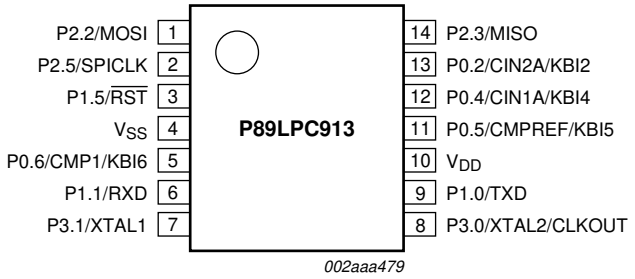

Fig 8. P89LPC913 TSSOP14 pin configuration

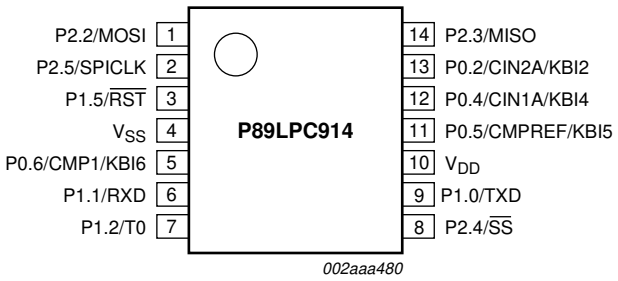

Fig 9. P89LPC914 TSSOP14 pin configuration

7.2 Pin description

Table 4. P89LPC912 pin description

Symbol	Pin	Type	Description
P0.2, P0.4 to P0.6		I/O	**Port 0:** Port 0 is a 4-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 “Port configurations” and Table 13 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.2/CIN2A/ KBI2	13	I/O	**P0.2** — Port 0 bit 2.
		I	**CIN2A** — Comparator 2 positive input A.
		I	**KBI2** — Keyboard input 2.
P0.4/CIN1A/ KBI4	12	I/O	**P0.4** — Port 0 bit 4.
		I	**CIN1A** — Comparator 1 positive input A.
		I	**KBI4** — Keyboard input 4.
P0.5/CMPREF/ KBI5	11	I/O	**P0.5** — Port 0 bit 5.
		I	**CMPREF** — Comparator reference (negative) input.
		I	**KBI5** — Keyboard input 5.
P0.6/CMP1/ KBI6	5	I/O	**P0.6** — Port 0 bit 6.
		O	**CMP1** — Comparator 1 output.
		I	**KBI6** — Keyboard input 6.
P1.2, P1.5		I/O (P1.2); I (P1.5)	**Port 1:** Port 1 is a 2-bit I/O port with P1.2 having a user-configurable output type as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the P1.2 input and outputs depends upon the port configuration selected. Refer to Section 8.12.1 “Port configurations” and Table 13 “Static characteristics” for details. P1.2 is an open drain when used as an output. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.2/T0	6	I/O	**P1.2** — Port 1 bit 2. (Open drain when used as an output.)
		I/O	**T0** — Timer/counter 0 external count input or overflow output. (Open drain when used as outputs.).
P1.5/$\overline{\text{RST}}$	3	I	**P1.5** — Port 1 bit 5. (Input only.)
		I	**$\overline{\text{RST}}$** — External Reset input during power-on or if selected via UCFG1. When functioning as a reset input a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

Table 4. P89LPC912 pin description *...continued*

Symbol	Pin	Type	Description
P2.2 to P2.5		I/O	**Port 2:** Port 2 is a 4-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.2/MOSI	1	I/O	**P2.2 —** Port 2 bit 2.
		I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output, when configured as slave, this pin is input.
P2.3/MISO	14	I/O	**P2.3 —** Port 2 bit 3.
		I/O	**MISO —** SPI master in slave out. When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{SS}$	9	I/O	**P2.4 —** Port 2 bit 4.
		I	**$\overline{SS}$ —** SPI Slave select.
P2.5/SPICLK	2	I/O	**P2.5 —** Port 2 bit 5.
		I/O	**SPICLK —** SPI clock. When configured as master, this pin is output, when configured as slave, this pin is input.
P3.0 to P3.1		I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	8	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration).
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the Real-Time clock/system timer.
P3.1/XTAL1	7	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the Real-Time clock/system timer.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	10	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

Table 5. P89LPC913 pin description

Symbol	Pin	Type	Description
P0.2, P0.4 to P0.6		I/O	**Port 0:** Port 0 is a 4-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.2/CIN2A/ KBI2	13	I/O	**P0.2** — Port 0 bit 2.
		I	**CIN2A** — Comparator 2 positive input A.
		I	**KBI2** — Keyboard input 2.
P0.4/CIN1A/ KBI4	12	I/O	**P0.4** — Port 0 bit 4.
		I	**CIN1A** — Comparator 1 positive input A.
		I	**KBI4** — Keyboard input 4.
P0.5/CMPREF/ KBI5	11	I/O	**P0.5** — Port 0 bit 5.
		I	**CMPREF** — Comparator reference (negative) input.
		I	**KBI5** — Keyboard input 5.
P0.6/CMP1/ KBI6	5	I/O	**P0.6** — Port 0 bit 6.
		O	**CMP1** — Comparator 1 output.
		I	**KBI6** — Keyboard input 6.
P1.0, P1.1, P1.5		I/O (P1.0, P1.1); I (P1.5)	**Port 1:** Port 1 is a 3-bit I/O port with a user-configurable output type, except for P1.5 noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	9	I/O	**P1.0** — Port 1 bit 0.
		O	**TXD** — Transmitter output for the serial port.
P1.1/RXD	6	I/O	**P1.1** — Port 1 bit 1.
		I	**RXD** — Receiver input for the serial port.
P1.5/$\overline{\text{RST}}$	3	I	**P1.5** — Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$** — External Reset input during Power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

Table 5. P89LPC913 pin description *...continued*

Symbol	Pin	Type	Description
P2.2, P2.3, P2.5		I/O	**Port 2:** Port 2 is a 3-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.2/MOSI	1	I/O	**P2.2** — Port 2 bit 2.
		I/O	**MOSI** — SPI master out slave in. When configured as master, this pin is output, when configured as slave, this pin is input.
P2.3/MISO	14	I/O	**P2.3** — Port 2 bit 3.
		I/O	**MISO** — SPI master in slave out. When configured as master, this pin is input, when configured as slave, this pin is output.
P2.5/SPICLK	2	I/O	**P2.5** — Port 2 bit 5.
		I/O	**SPICLK** — SPI clock. When configured as master, this pin is output, when configured as slave, this pin is input.
P3.0 to P3.1		I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	8	I/O	**P3.0** — Port 3 bit 0.
		O	**XTAL2** — Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration).
		O	**CLKOUT** — CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the Real-Time clock/system timer.
P3.1/XTAL1	7	I/O	**P3.1** — Port 3 bit 1.
		I	**XTAL1** — Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the Real-Time clock/system timer.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	10	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

Table 6. P89LPC914 pin description

Symbol	Pin	Type	Description
P0.2, P0.4 to P0.6		I/O	**Port 0:** Port 0 is a 4-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.2/CIN2A/ KBI2	13	I/O	**P0.2** — Port 0 bit 2.
		I	**CIN2A** — Comparator 2 positive input A.
		I	**KBI2** — Keyboard input 2.
P0.4/CIN1A/ KBI4	12	I/O	**P0.4** — Port 0 bit 4.
		I	**CIN1A** — Comparator 1 positive input A.
		I	**KBI4** — Keyboard input 4.
P0.5/CMPREF / KBI5	11	I/O	**P0.5** — Port 0 bit 5.
		I	**CMPREF** — Comparator reference (negative) input.
		I	**KBI5** — Keyboard input 5.
P0.6/CMP1/ KBI6	5	I/O	**P0.6** — Port 0 bit 6.
		O	**CMP1** — Comparator 1 output.
		I	**KBI6** — Keyboard input 6.
P1.0 to P1.2, P1.5		I/O (P1.0 to P1.2); I (P1.5)	**Port 1:** Port 1 is a 4-bit I/O port with a user-configurable output type, except for three pins noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. P1.2 is an open drain when used as an output. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	9	I/O	**P1.0** — Port 1 bit 0.
		O	**TXD** — Transmitter output for the serial port.
P1.1/RXD	6	I/O	**P1.1** — Port 1 bit 1.
		I	**RXD** — Receiver input for the serial port.
P1.2/T0	7	I/O	**P1.2** — Port 1 bit 2. (Open drain when used as an output.)
		I/O	**T0** — Timer/counter 0 external count input or overflow output. (Open drain when used as outputs.)
P1.5/$\overline{\text{RST}}$	3	I	**P1.5** — Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$** — External Reset input during Power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode.

Table 6. P89LPC914 pin description *...continued*

Symbol	Pin	Type	Description
P2.2 to P2.5		I/O	**Port 2:** Port 2 is a 4-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 13 "Static characteristics" for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.2/MOSI	1	I/O	**P2.2 —** Port 2 bit 2.
		I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output, when configured as slave, this pin is input.
P2.3/MISO	14	I/O	**P2.3 —** Port 2 bit 3.
		I/O	**MISO —** SPI master in slave out. When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{SS}$	8	I/O	**P2.4 —** Port 2 bit 4.
		I	**$\overline{SS}$ —** SPI Slave select.
P2.5/SPICLK	2	I/O	**P2.5 —** Port 2 bit 5.
		I/O	**SPICLK —** SPI clock. When configured as master, this pin is output, when configured as slave, this pin is input.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	10	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

8. Functional description

Remark: Please refer to the P89LPC912/913/914 *User manual* for a more detailed functional description.

8.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

Table 7. P89LPC912 Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	0000 0000
AUXR1	Auxiliary function register	A2H	CLKLP	-	-	ENT0	SRST	0	-	DPS	00[1]	0000 00x0
	Bit address		F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	0000 0000
CMP1	Comparator 1 control register	ACH	-	-	CE1	-	CN1	OE1	CO1	CMF1	00[1]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	-	CN2	-	CO2	CMF2	00[1]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H	-	-	-	-	-	-			00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
	Bit address		AF	AE	AD	AC	AB	AA	A9	A8		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	-	ET1	-	ET0	-	00	0000 0000
	Bit address		EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	-	-	-	-	ESPI	EC	EKBI	-	00[1]	00x0 0000
	Bit address		BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	-	PT1	-	PT0	-	00[1]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	-	PT1H	-	PT0H	-	00[1]	x000 0000
	Bit address		FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	-	-	-	-	PSPI	PC	PKBI	-	00[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	-	-	-	-	PSPIH	PCH	PKBIH	-	00[1]	00x0 0000

Table 7. P89LPC912 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
	Bit address		**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0*	Port 0	80H		CMP1/ KB6	CMPREF / KB5	CIN1A/ KB4		CIN2A/ KB2			[1]	
	Bit address		**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1*	Port 1	90H			$\overline{\text{RST}}$			T0			[1]	
	Bit address		**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**		
P2*	Port 2	A0H			SPICLK	$\overline{\text{SS}}$	MISO	MOSI			[1]	
	Bit address		**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P3*	Port 3	B0H							XTAL1	XTAL2	[1]	
P0M1	Port 0 output mode 1	84H		(P0M1.6)	(P0M1.5)	(P0M1.4)		(P0M1.2)			FF	1111 1111
P0M2	Port 0 output mode 2	85H		(P0M2.6)	(P0M2.5)	(P0M2.4)		(P0M2.2)			00	0000 0000
P1M1	Port 1 output mode 1	91H						(P1M1.2)			D3[1]	11x1 xx11
P1M2	Port 1 output mode 2	92H						(P1M2.2)		-	00[1]	00x0 xx00
P2M1	Port 2 output mode 1	A4H			(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)			FF	1111 1111
P2M2	Port 2 output mode 2	A5H			(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)			00	0000 0000
P3M1	Port 3 output mode 1	B1H							(P3M1.1)	(P3M1.0)	03[1]	xxxx xx11
P3M2	Port 3 output mode 2	B2H							(P3M2.1)	(P3M2.0)	00[1]	xxxx xx00
PCON	Power control register	87H	-	-	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	-	SPPD	-	-	00[1]	0000 0000
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	-	PT0AD.2	-	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	-	R_WD	R_SF	R_EX	[2]	
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1][5]	011x xx00
RTCH	Real-time clock register high	D2H									00[5]	0000 0000

Table 7. P89LPC912 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
RTCL	Real-time clock register low	D3H									00[5]	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	-	-	-	-	T0M2	00	xxx0 xxx0
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-	-	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	-	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[4] [5]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[3] [5]	
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high impedance) state after power-up.

[2] The RSTSRC register reflects the cause of the P89LPC912 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx11 0000.

[3] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[4] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[5] The only reset source that affects these SFRs is power-on reset.

Table 8. P89LPC913 Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	0000 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	-	-	SRST	0	-	DPS	00[1]	0000 00x0
	Bit address		F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	0000 0000
BRGR0[2]	Baud rate generator rate low	BEH									00	0000 0000
BRGR1[2]	Baud rate generator rate high	BFH									00	0000 0000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[6]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	-	CN1	OE1	CO1	CMF1	00[1]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	-	CN2	-	-	CMF2	00[1]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H	-	-	-	-	-	-			00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
	Bit address		AF	AE	AD	AC	AB	AA	A9	A8		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0	-	00	0000 0000
	Bit address		EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	-	EST	-	-	ESPI	EC	EKBI	-	00[1]	00x0 0000
	Bit address		BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	-	PT0	-	00[1]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	-	PT0H	-	00[1]	x000 0000

Table 8. P89LPC913 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	-	PST	-	-	PSPI	PC	PKBI	-	00[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	-	PSPIH	PCH	PKBIH	-	00[1]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
		Bit address	87	86	85	84	83	82	81	80		
P0*	Port 0	80H		CMP1/ KB6	CMPREF / KB5	CIN1A/ KB4		CIN2A/ KB2			[1]	
		Bit address	97	96	95	94	93	92	91	90		
P1*	Port 1	90H			$\overline{\text{RST}}$				RXD	TXD	[1]	
		Bit address	A7	A6	A5	A4	A3	A2	A1	A0		
P2*	Port 2	A0H			SPICLK		MISO	MOSI			[1]	
		Bit address	B7	B6	B5	B4	B3	B2	B1	B0		
P3*	Port 3	B0H							XTAL1	XTAL2	[1]	
P0M1	Port 0 output mode 1	84H		(P0M1.6)	(P0M1.5)	(P0M1.4)		(P0M1.2)			FF	1111 1111
P0M2	Port 0 output mode 2	85H		(P0M2.6)	(P0M2.5)	(P0M2.4)		(P0M2.2)			00	0000 0000
P1M1	Port 1 output mode 1	91H							(P1M1.1)	(P1M1.0)	D3[1]	11x1 xx11
P1M2	Port 1 output mode 2	92H							(P1M2.1)	(P1M2.0)	00[1]	00x0 xx00
P2M1	Port 2 output mode 1	A4H			(P2M1.5)		(P2M1.3)	(P2M1.2)			FF	1111 1111
P2M2	Port 2 output mode 2	A5H			(P2M2.5)		(P2M2.3)	(P2M2.2)			00	0000 0000
P3M1	Port 3 output mode 1	B1H							(P3M1.1)	(P3M1.0)	03[1]	xxxx xx11
P3M2	Port 3 output mode 2	B2H							(P3M2.1)	(P3M2.0)	00[1]	xxxx xx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	-	SPPD	SPD	-	00[1]	0000 0000

Table 8. P89LPC913 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		D7	D6	D5	D4	D3	D2	D1	D0		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	-	PT0AD.2	-	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX	[3]	
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1][6]	011x xx00
RTCH	Real-time clock register high	D2H									00[6]	0000 0000
RTCL	Real-time clock register low	D3H									00[6]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial port data buffer register	99H									xx	xxxx xxxx
	Bit address		9F	9E	9D	9C	9B	9A	99	98		
SCON	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
	Bit address		8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-	-	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	-	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5] [6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4] [6]	

Table 8. P89LPC913 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any of them is written if BRGEN = 1, result is unpredictable.

[3] The RSTSRC register reflects the cause of the P89LPC912 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx11 0000.

[4] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] The only reset source that affects these SFRs is power-on reset.

Table 9. P89LPC914 Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		**E7**	**E6**	**E5**	**E4**	**E3**	**E2**	**E1**	**E0**		
ACC*	Accumulator	E0H									00	0000 0000
AUXR1	Auxiliary function register	A2H	-	EBRR	-	ENT0	SRST	0	-	DPS	00[1]	0000 00x0
	Bit address		**F7**	**F6**	**F5**	**F4**	**F3**	**F2**	**F1**	**F0**		
B*	B register	F0H									00	0000 0000
BRGR0[2]	Baud rate generator rate low	BEH									00	0000 0000
BRGR1[2]	Baud rate generator rate high	BFH									00	0000 0000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[6]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	-	CN1	OE1	CO1	CMF1	00[1]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	-	CN2	-	CO2	CMF2	00[1]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H	-	-	-	-	-	-			00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
	Bit address		**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0	-	00	0000 0000
	Bit address		**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1*	Interrupt enable 1	E8H	-	EST	-	-	ESPI	EC	EKBI	-	00[1]	00x0 0000

Table 9. P89LPC914 Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	-	PT0	-	00[1]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	-	PT0H	-	00[1]	x000 0000
		Bit address	FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	-	PST	-	-	PSPI	PC	PKBI	-	00[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	-	PSPIH	PCH	PKBIH	-	00[1]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
		Bit address	87	86	85	84	83	82	81	80		
P0*	Port 0	80H		CMP1/KB6	CMPREF/KB5	CIN1A/KB4		CIN2A/KB2			[1]	
		Bit address	97	96	95	94	93	92	91	90		
P1*	Port 1	90H			$\overline{RST}$			T0	RXD	TXD	[1]	
		Bit address	A7	A6	A5	A4	A3	A2	A1	A0		
P2*	Port 2	A0H			SPICLK	$\overline{SS}$	MISO	MOSI			[1]	
P0M1	Port 0 output mode 1	84H		(P0M1.6)	(P0M1.5)	(P0M1.4)		(P0M1.2)			FF	1111 1111
P0M2	Port 0 output mode 2	85H		(P0M2.6)	(P0M2.5)	(P0M2.4)		(P0M2.2)			00	0000 0000
P1M1	Port 1 output mode 1	91H						(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[1]	11x1 xx11
P1M2	Port 1 output mode 2	92H						(P1M2.2)	(P1M2.1)	(P1M2.0)	00[1]	00x0 xx00
P2M1	Port 2 output mode 1	A4H			(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)			FF	1111 1111
P2M2	Port 2 output mode 2	A5H			(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)			00	0000 0000
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	-	SPPD	SPD	-	00[1]	0000 0000