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P89LPC9151/9161/9171

8-bit microcontroller with accelerated two-clock 80C51 core, 2 kB 3 V byte-erasable flash with 8-bit ADC

Rev. 02 — 9 February 2010 Product data sheet

1. General description

The P89LPC9151/9161/9171 is a single-chip microcontroller, available in low cost packages, based on a high performance processor architecture that executes instructions in two to four clocks, six times the rate of standard 80C51 devices. Many system-level functions have been incorporated into the device in order to reduce component count, board space, and system cost.

2. Features

2.1 Principal features

- 2 kB byte-erasable flash code memory organized into 256-byte sectors and 16-byte pages. Single-byte erasing allows any byte(s) to be used as non-volatile data storage.
- 256-byte RAM data memory.
- 4-input multiplexed 8-bit ADC/single DAC output. Two analog comparators with selectable inputs and reference source.
- Two 16-bit counter/timers. Timer 0 (and Timer 1 - P89LPC9171) may be configured to toggle a port output upon timer overflow or to become a PWM output.
- A 23-bit system timer that can also be used as real-time clock consisting of a 7-bit prescaler and a programmable and readable 16-bit timer.
- Enhanced UART with a fractional baud rate generator, break detect, framing error detection, and automatic address detection; 400 kHz byte-wide I^2C-bus communication port.
- SPI communication port (P89LPC9161).
- 2.4 V to 3.6 V V_{DD} operating range. I/O pins are 5 V tolerant (may be pulled up or driven to 5.5 V).
- Enhanced low voltage (brownout) detect allows a graceful system shutdown when power fails.
- 16-pin TSSOP with 12 I/O pins minimum and up to 14 I/O pins while using on-chip oscillator and reset options (P89LPC9161/9171), and 14-pin TSSOP packages with 10 I/O pins minimum and up to 12 I/O pins while using on-chip oscillator and reset options (P89LPC9151).

2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- In-Application Programming (IAP-Lite) and byte erase allows code memory to be used for non-volatile data storage.
- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Watchdog timer with separate on-chip oscillator, nominal 400 kHz, calibrated to ±5 %, requiring no external components. The watchdog prescaler is selectable from eight values.
- High-accuracy internal RC oscillator option, with clock doubler option, allows operation without external oscillator components. The RC oscillator option is selectable and fine tunable.
- Clock switching on the fly among internal RC oscillator, watchdog oscillator, external clock input provides optimal support of minimal power active mode with fast switching to maximum performance.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A software reset function is also available.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- High current sourcing/sinking (20 mA) at 4 I/O pins on the P89LPC9151, 3 I/O pins on the P89LPC9161 and 5 I/O pins on the P89LPC9171. All other port pins have high sinking capability (20 mA). A maximum limit is specified for the entire chip.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC9151/9161/9171 when internal reset option is selected.
- Four interrupt priority levels.
- Five/six keypad interrupt inputs, plus two additional external interrupt inputs.
- Schmitt trigger port inputs.
- Second data pointer.
- Emulation support.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
P89LPC9151FDH	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
P89LPC9161FDH	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
P89LPC9171FDH	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	Temperature range	Frequency
P89LPC9151FDH	2 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC9161FDH	2 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC9171FDH	2 kB	−40 °C to +85 °C	0 MHz to 18 MHz

4. Block diagram

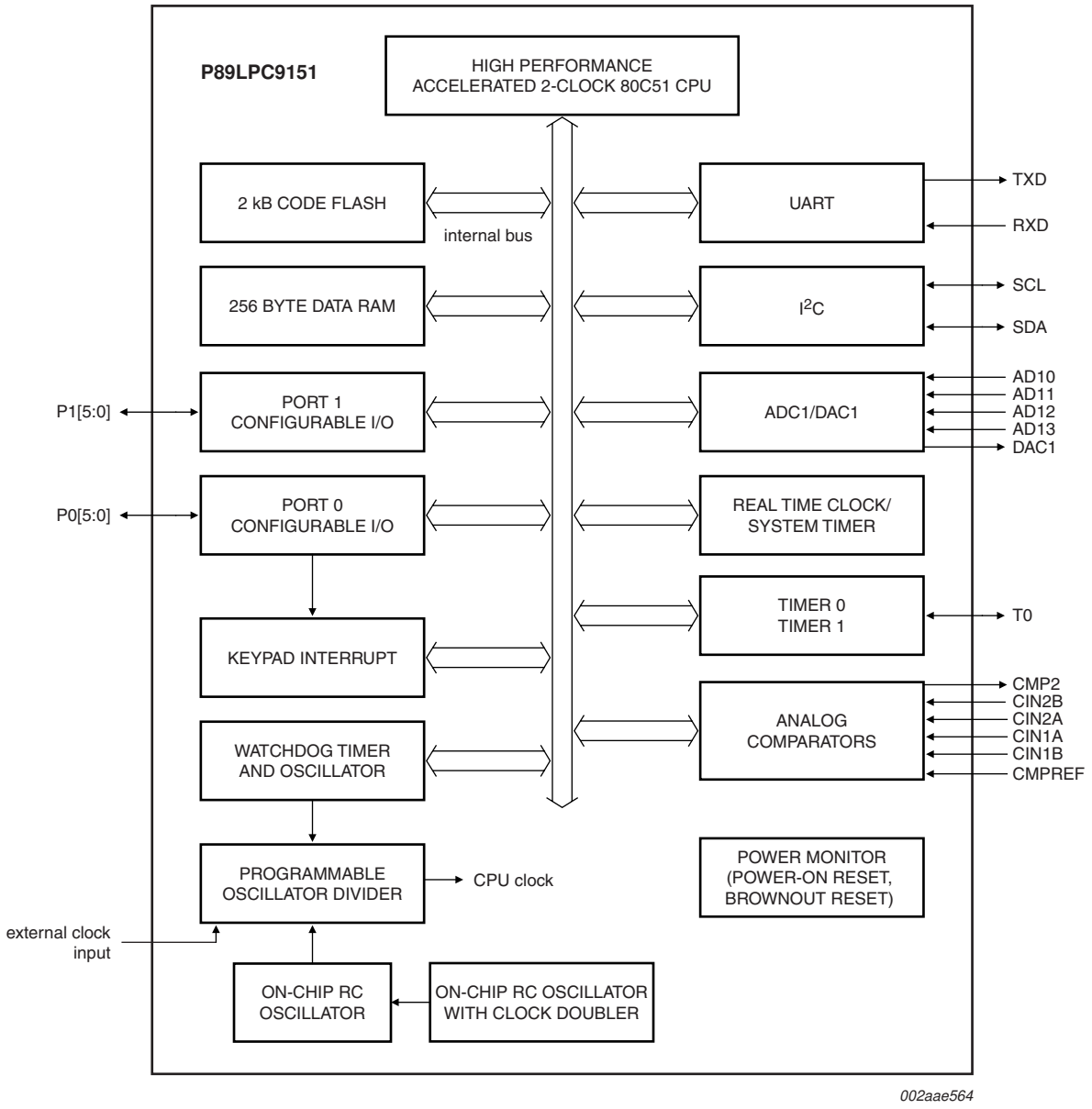

Fig 1. Block diagram (P89LPC9151)

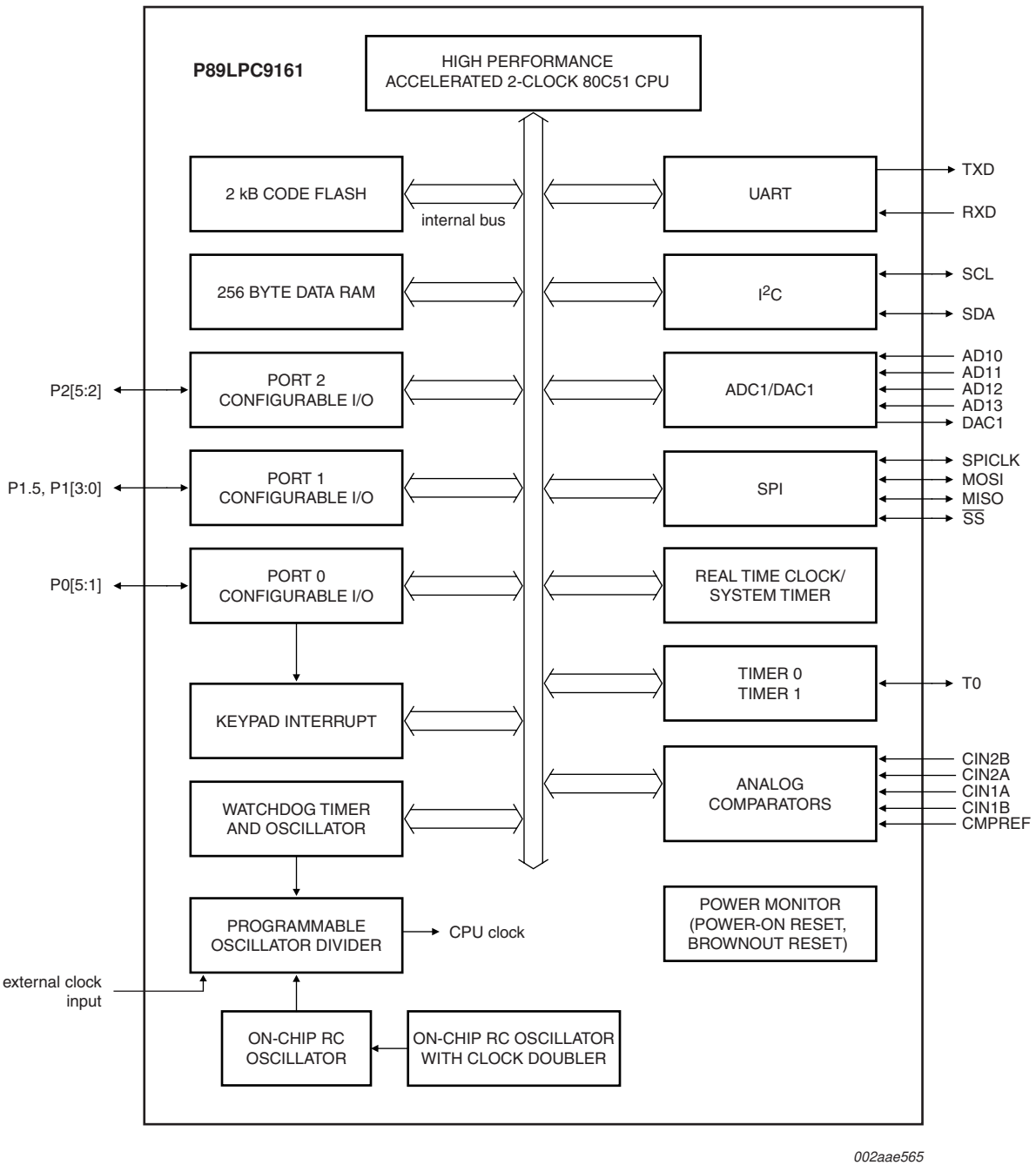

Fig 2. Block diagram (P89LPC9161)

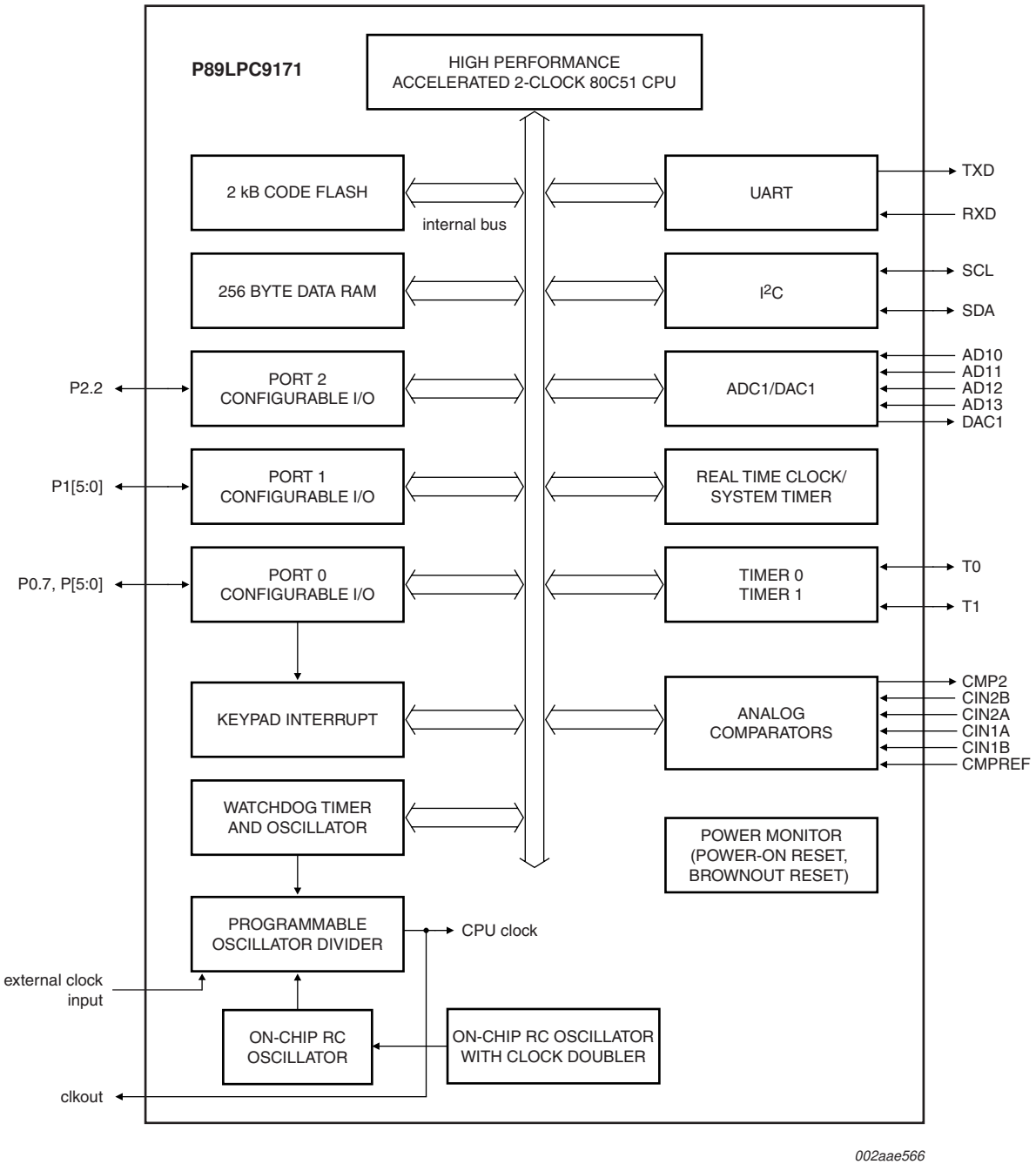

Fig 3. Block diagram (P89LPC9171)

5. Functional diagram

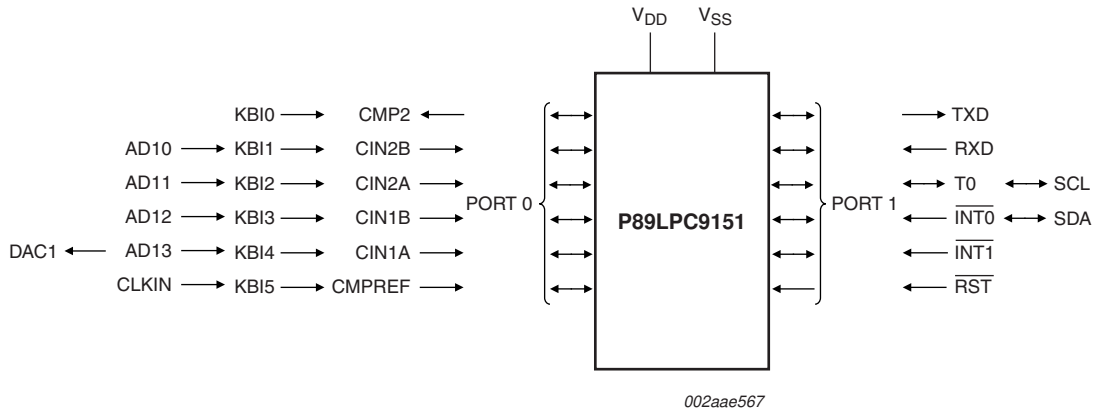

Fig 4. Functional diagram (P89LPC9151)

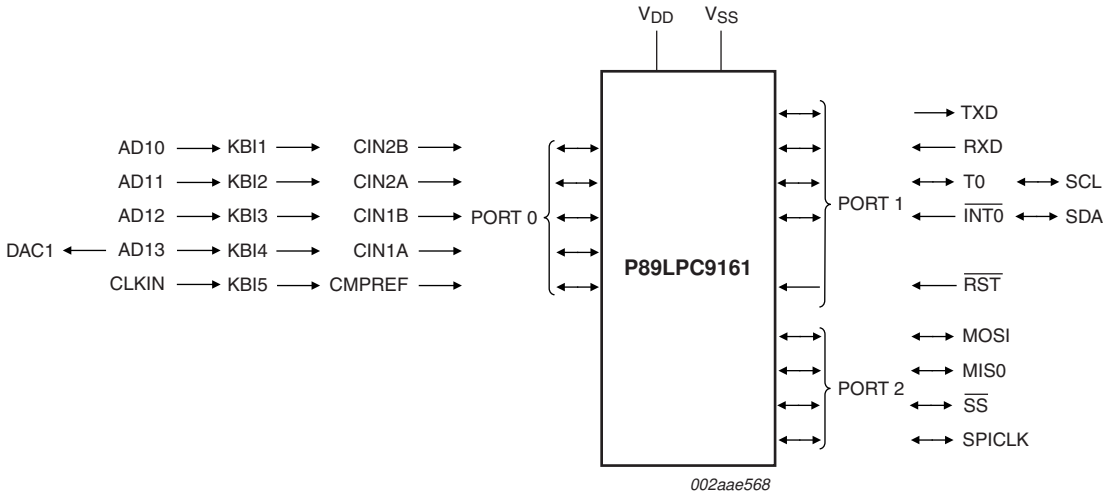

Fig 5. Functional diagram (P89LPC9161)

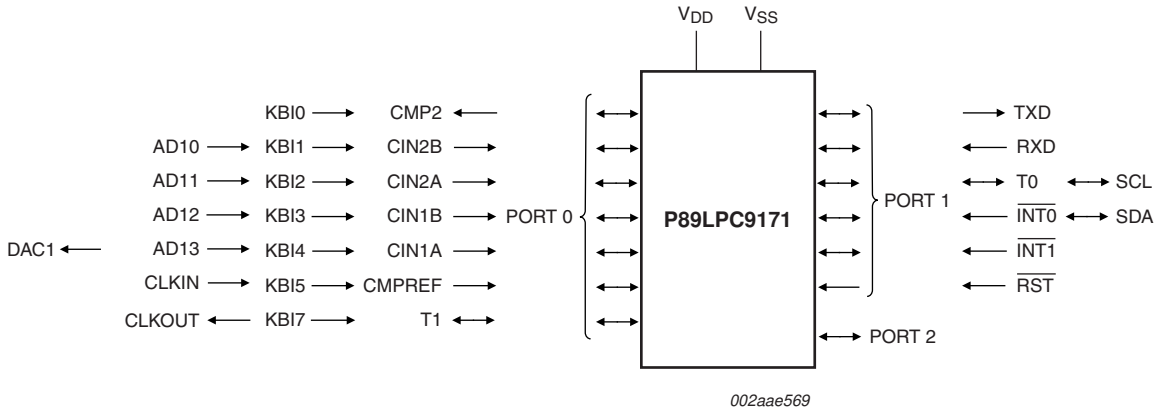

Fig 6. Functional diagram (P89LPC9171)

6. Pinning information

6.1 Pinning

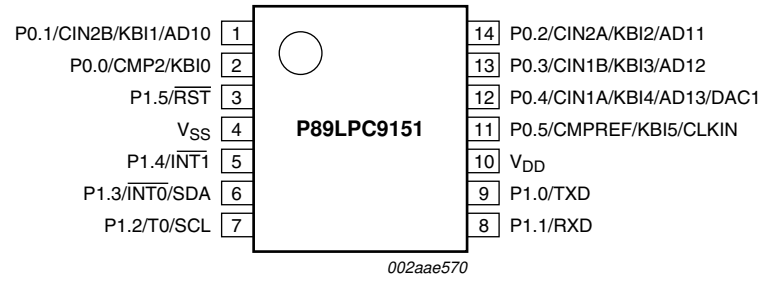

Fig 7. P89LPC9151 TSSOP14 pin configuration

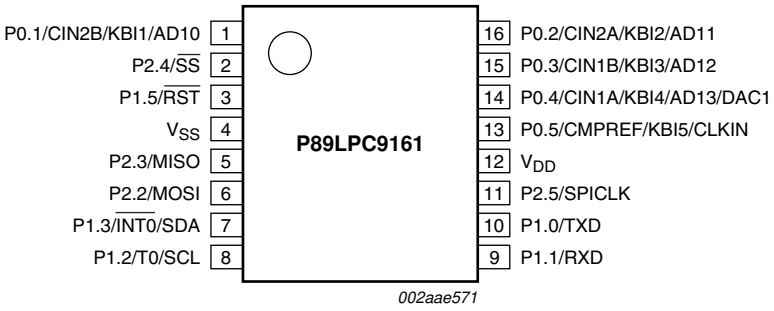

Fig 8. P89LPC9161 TSSOP16 pin configuration

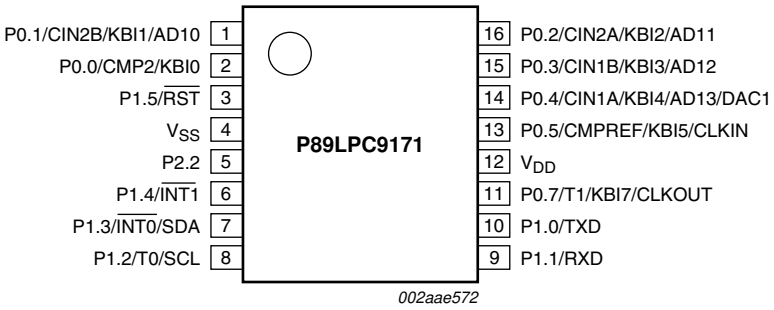

Fig 9. P89LPC9171 TSSOP16 pin configuration

6.2 Pin description

Table 3. P89LPC9151 Pin description

Symbol	Pin	Type	Description
	TSSOP14		
P0.0 to P0.5		I/O	**Port 0:** Port 0 is an 6-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.15.1 “Port configurations” and Table 16 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt trigger inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/ KBI0	2	I/O	**P0.0** — Port 0 bit 0.
		O	**CMP2** — Comparator 2 output
		I	**KBI0** — Keyboard input 0.
P0.1/CIN2B/ KBI1/AD10	1	I/O	**P0.1** — Port 0 bit 1.
		I	**CIN2B** — Comparator 2 positive input B.
		I	**KBI1** — Keyboard input 1.
		I	**AD10** — ADC1 channel 0 analog input.
P0.2/CIN2A/ KBI2/AD11	14	I/O	**P0.2** — Port 0 bit 2.
		I	**CIN2A** — Comparator 2 positive input A.
		I	**KBI2** — Keyboard input 2.
		I	**AD11** — ADC1 channel 1 analog input.
P0.3/CIN1B/ KBI3/AD12	13	I/O	**P0.3** — Port 0 bit 3. High current source.
		I	**CIN1B** — Comparator 1 positive input B.
		I	**KBI3** — Keyboard input 3.
		I	**AD12** — ADC1 channel 2 analog input.
P0.4/CIN1A/ KBI4/DAC1/AD13	12	I/O	**P0.4** — Port 0 bit 4. High current source.
		I	**CIN1A** — Comparator 1 positive input A.
		I	**KBI4** — Keyboard input 4.
		O	**DAC1** — Digital-to-analog converter output 1.
		I	**AD13** — ADC1 channel 3 analog input.
P0.5/CMPREF/ KBI5	11	I/O	**P0.5** — Port 0 bit 5. High current source.
		I	**CMPREF** — Comparator reference (negative) input.
		I	**KBI5** — Keyboard input 5.
		I	**CLKIN** — External clock input.
P1.0 to P1.5		I/O, I [1]	**Port 1:** Port 1 is an 6-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.15.1 “Port configurations” and Table 16 “Static characteristics” for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt trigger inputs. Port 1 also provides various special functions as described below:

Table 3. P89LPC9151 Pin description

Symbol	Pin	Type	Description
	TSSOP14		
P1.0/TXD	9	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Transmitter output for serial port.
P1.1/RXD	8	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Receiver input for serial port.
P1.2/T0/SCL	7	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
		I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
		I/O	**SCL —** I^2C-bus serial clock input/output.
P1.3/$\overline{INT0}$/SDA	6	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
		I	**$\overline{INT0}$ —** External interrupt 0 input.
		I/O	**SDA —** I^2C-bus serial data input/output.
P1.4/$\overline{INT1}$	5	I/O	**P1.4 —** Port 1 bit 4. High current source.
		I	**$\overline{INT1}$ —** External interrupt 1 input.
P1.5/$\overline{RST}$	3	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{RST}$ —** External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	10	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

[1] Input/output for P1.0 to P1.4. Input for P1.5.

Table 4. P89LPC9161 Pin description

Symbol	Pin	Type	Description
	TSSOP16		
P0.1 to P0.5		I/O	**Port 0:** Port 0 is an 5-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.15.1 “Port configurations” and Table 16 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt trigger inputs. Port 0 also provides various special functions as described below:
P0.1/CIN2B/ KBI1/AD10	1	I/O	**P0.1** — Port 0 bit 1.
		I	**CIN2B** — Comparator 2 positive input B.
		I	**KBI1** — Keyboard input 1.
		I	**AD10** — ADC1 channel 0 analog input.
P0.2/CIN2A/ KBI2/AD11	16	I/O	**P0.2** — Port 0 bit 2.
		I	**CIN2A** — Comparator 2 positive input A.
		I	**KBI2** — Keyboard input 2.
		I	**AD11** — ADC1 channel 1 analog input.
P0.3/CIN1B/ KBI3/AD12	15	I/O	**P0.3** — Port 0 bit 3. High current source.
		I	**CIN1B** — Comparator 1 positive input B.
		I	**KBI3** — Keyboard input 3.
		I	**AD12** — ADC1 channel 2 analog input.
P0.4/CIN1A/ KBI4/DAC1/AD13	14	I/O	**P0.4** — Port 0 bit 4. High current source.
		I	**CIN1A** — Comparator 1 positive input A.
		I	**KBI4** — Keyboard input 4.
		O	**DAC1** — Digital-to-analog converter output 1.
		I	**AD13** — ADC1 channel 3 analog input.
P0.5/CMPREF/ KBI5	13	I/O	**P0.5** — Port 0 bit 5. High current source.
		I	**CMPREF** — Comparator reference (negative) input.
		I	**KBI5** — Keyboard input 5.
		I	**CLKIN** — External clock input.
P1.0 to P1.3, P1.5		I/O, I [1]	**Port 1:** Port 1 is an 5-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.15.1 “Port configurations” and Table 16 “Static characteristics” for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt trigger inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	10	I/O	**P1.0** — Port 1 bit 0.
		O	**TXD** — Transmitter output for serial port.
P1.1/RXD	9	I/O	**P1.1** — Port 1 bit 1.
		I	**RXD** — Receiver input for serial port.

Table 4. P89LPC9161 Pin description

Symbol	Pin	Type	Description
	TSSOP16		
P1.2/T0/SCL	8	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
		I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
		I/O	**SCL —** I^2C-bus serial clock input/output.
P1.3/$\overline{INT0}$/SDA	7	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
		I	**$\overline{INT0}$ —** External interrupt 0 input.
		I/O	**SDA —** I^2C-bus serial data input/output.
P1.5/$\overline{RST}$	3	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{RST}$ —** External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode.
P2.2 to P2.5		I/O	**Port 2:** Port 2 is an 4-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.15 “I/O ports” for details. All pins have Schmitt trigger inputs. Port 2 also provides various special functions as described below:
P2.2/MOSI	6	I/O	**P2.2 —** Port 2 bit 2.
		I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.3/MISO	5	I/O	**P2.3 —** Port 2 bit 3.
		I/O	**MISO —** When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{SS}$	2	I/O	**P2.4 —** Port 2 bit 4.
		I	**$\overline{SS}$ —** SPI Slave select.
P2.5/SPICLK	11	I/O	**P2.5 —** Port 2 bit 5.
		I/O	**SPICLK —** SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	12	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

[1] Input/output for P1.0 to P1.3. Input for P1.5.

Table 5. P89LPC9171 Pin description

Symbol	Pin	Type	Description
	TSSOP16		
P0.0 to P0.5, P0.7		I/O	**Port 0:** Port 0 is an 6-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.15.1 “Port configurations” and Table 16 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt trigger inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/ KBI0	2	I/O	**P0.0** — Port 0 bit 0.
		O	**CMP2** — Comparator 2 output
		I	**KBI0** — Keyboard input 0.
P0.1/CIN2B/ KBI1/AD10	1	I/O	**P0.1** — Port 0 bit 1.
		I	**CIN2B** — Comparator 2 positive input B.
		I	**KBI1** — Keyboard input 1.
		I	**AD10** — ADC1 channel 0 analog input.
P0.2/CIN2A/ KBI2/AD11	16	I/O	**P0.2** — Port 0 bit 2.
		I	**CIN2A** — Comparator 2 positive input A.
		I	**KBI2** — Keyboard input 2.
		I	**AD11** — ADC1 channel 1 analog input.
P0.3/CIN1B/ KBI3/AD12	15	I/O	**P0.3** — Port 0 bit 3. High current source.
		I	**CIN1B** — Comparator 1 positive input B.
		I	**KBI3** — Keyboard input 3.
		I	**AD12** — ADC1 channel 2 analog input.
P0.4/CIN1A/ KBI4/DAC1/AD13	14	I/O	**P0.4** — Port 0 bit 4. High current source.
		I	**CIN1A** — Comparator 1 positive input A.
		I	**KBI4** — Keyboard input 4.
		O	**DAC1** — Digital-to-analog converter output 1.
		I	**AD13** — ADC1 channel 3 analog input.
P0.5/CMPREF/ KBI5/CLKIN	13	I/O	**P0.5** — Port 0 bit 5. High current source.
		I	**CMPREF** — Comparator reference (negative) input.
		I	**KBI5** — Keyboard input 5.
		I	**CLKIN** — External clock input.
P0.7/T1/KBI7/CLK OUT	11	I/O	**P0.7** — Port 0 bit 7. High current source.
		I/O	**T1** — Timer/counter 1 external count input or overflow output.
		I	**KBI7** — Keyboard input 7.
		O	**CLKOUT** — Clock output.

Table 5. P89LPC9171 Pin description

Symbol	Pin	Type	Description
	TSSOP16		
P1.0 to P1.5		I/O, I [1]	**Port 1:** Port 1 is an 6-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.15.1 "Port configurations" and Table 16 "Static characteristics" for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt trigger inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	10	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Transmitter output for serial port.
P1.1/RXD	9	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Receiver input for serial port.
P1.2/T0/SCL	8	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
		I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
		I/O	**SCL —** I^2C-bus serial clock input/output.
P1.3/$\overline{INT0}$/SDA	7	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
		I	**$\overline{INT0}$ —** External interrupt 0 input.
		I/O	**SDA —** I^2C-bus serial data input/output.
P1.4/$\overline{INT1}$	6	I/O	**P1.4 —** Port 1 bit 4. High current source.
		I	**$\overline{INT1}$ —** External interrupt 1 input.
P1.5/$\overline{RST}$	3	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{RST}$ —** External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode.
P2.2	5	I/O	**Port 2:** P2.2 is a single-bit I/O port with a user-configurable output type. During reset P2.2 latch is configured in the input only mode with the internal pull-up disabled. The operation of the output depends upon the port configuration selected. Refer to Section 7.15 "I/O ports" for details. This pin has Schmitt trigger inputs.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	12	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

[1] Input/output for P1.0 to P1.4. Input for P1.5.

7. Functional description

Remark: Please refer to the P89LPC9151/9161/9171 *User manual* for a more detailed functional description.

7.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

Table 6. Special function registers - P89LPC9151

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	0000 0000
ADCON1	A/D control register 1	97H	ENBI1	ENADCI1	TMM1	EDGE1	ADCI1	ENADC1	ADCS11	ADCS10	00	0000 0000
ADINS	A/D input select	A3H	AIN13	AIN12	AIN11	AIN10	-	-	-	-	00	0000 0000
ADMODA	A/D mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	-	-	-	-	00	0000 0000
ADMODB	A/D mode register B	A1H	CLK2	CLK1	CLK0	INBND0	ENDAC1	-	BSA1	-	00	000x 0000
AD1BH	A/D_0 boundary high register	C4H									FF	1111 1111
AD1BL	A/D_0 boundary low register	BCH									00	0000 0000
AD1DAT0	A/D_0 data register 0	D5H									00	0000 0000
AD1DAT1	A/D_0 data register 1	D6H									00	0000 0000
AD1DAT2	A/D_0 data register 2	D7H									00	0000 0000
AD1DAT3	A/D_0 data register 3	F5H									00	0000 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	-	ENT0	SRST	0	-	DPS	00	0000 00x0
	Bit address		F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	0000 0000
BRGR0[2]	Baud rate generator 0 rate low	BEH									00	0000 0000

Table 6. Special function registers - P89LPC9151

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
BRGR1[2]	Baud rate generator 0 rate high	BFH									00	0000 0000
BRGCON	Baud rate generator 0 control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[2]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	-	CO1	CMF1	00[1]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00[1]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I^2C-bus slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000

Table 6. Special function registers - P89LPC9151

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**	**D8**		
I2CON*	I^2C-bus control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I^2C-bus data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I^2C-bus status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000
		Bit address	**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	0000 0000
		Bit address	**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1*	Interrupt enable 1	E8H	EAD	EST	-	-	-	EC	EKBI	EI2C	00[1]	00x0 0000
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00[1]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/ PSRH	PT1H	PX1H	PT0H	PX0H	00[1]	x000 0000
		Bit address	**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**		
IP1*	Interrupt priority 1	F8H	PAD	PST	-	-	-	PC	PKBI	PI2C	00[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	PADH	PSTH	-	-	-	PCH	PKBIH	PI2CH	00[1]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN _SEL	KBIF	00[1]	xxxx xx00

Table 6. Special function registers - P89LPC9151

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
	Bit address		**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0*	Port 0	80H	-	-	CMPREF /KB5 /CLKIN	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0	[1]	
	Bit address		**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/SDA	T0/SCL	RXD	TXD	[1]	
	Bit address		**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P0M1	Port 0 output mode 1	84H	-	-	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[1]	1111 1111
P0M2	Port 0 output mode 2	85H	-	-	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[1]	0000 0000
P1M1	Port 1 output mode 1	91H	-	-	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[1]	11x1 xx11
P1M2	Port 1 output mode 2	92H	-	-	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[1]	00x0 xx00
PCON	Power control register	87H	SMOD1	SMOD0	-	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	ADPD	I2PD	-	SPD	-	00[1]	0000 0000
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	BOIF	BOF	POF	R_BK	R_WD	R_SF	R_EX	[3]	
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1][6]	011x xx00

Table 6. Special function registers - P89LPC9151

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
RTCH	RTC register high	D2H									00[6]	0000 0000
RTCL	RTC register low	D3H									00[6]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial Port data buffer register	99H									xx	xxxx xxxx
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	-	-	-	-	T0M2	00	xxx0 xxx0
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/$\overline{T}$	T1M1	T1M0	T0GATE	T0C/$\overline{T}$	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	-	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5][6]	

Table 6. Special function registers - P89LPC9151

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4][6]	
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high-impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[3] The RSTSRC register reflects the cause of the P89LPC9151 reset except BOIF bit. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is x011 0000.

[4] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[5] On power-on reset and watchdog reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] The only reset sources that affect these SFRs are power-on reset and watchdog reset.

Table 7. Extended special function registers - P89LPC9151[1]

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
BODCFG	BOD configuration register	FFC8H	-	-	-	-	-	-	BOICFG1	BOICFG0	[2]	
CLKCON	CLOCK Control register	FFDEH	CLKOK	-	-	-	CLKDBL	FOSC2	FOSC1	FOSC0	[3]	
RTCDATH	Real-time clock data register high	FFBFH									00	0000 0000
RTCDATL	Real-time clock data register low	FFBEH									00	0000 0000

[1] Extended SFRs are physically located on-chip but logically located in external data memory address space (XDATA). The MOVX A,@DPTR and MOVX @DPTR,A instructions are used to access these extended SFRs.

[2] The BOICFG1/0 will be copied from UCFG1.5 and UCFG1.3 when power-on reset.

[3] CLKCON register reset value comes from UCFG1 and UCFG2. The reset value of CLKCON.2 to CLKCON.0 come from UCFG1.2 to UCFG1.0 and reset value of CLKDBL bit comes from UCFG2.7.

Table 8. Special function registers - P89LPC9161

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	0000 0000
ADCON1	A/D control register 1	97H	ENBI1	ENADCI1	TMM1	EDGE1	ADCI1	ENADC1	ADCS11	ADCS10	00	0000 0000
ADINS	A/D input select	A3H	AIN13	AIN12	AIN11	AIN10	-	-	-	-	00	0000 0000
ADMODA	A/D mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	-	-	-	-	00	0000 0000
ADMODB	A/D mode register B	A1H	CLK2	CLK1	CLK0	INBND0	ENDAC1	-	BSA1	-	00	000x 0000
AD1BH	A/D_0 boundary high register	C4H									FF	1111 1111
AD1BL	A/D_0 boundary low register	BCH									00	0000 0000
AD1DAT0	A/D_0 data register 0	D5H									00	0000 0000
AD1DAT1	A/D_0 data register 1	D6H									00	0000 0000
AD1DAT2	A/D_0 data register 2	D7H									00	0000 0000
AD1DAT3	A/D_0 data register 3	F5H									00	0000 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	-	ENT0	SRST	0	-	DPS	00	0000 00x0
	Bit address		F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	0000 0000
BRGR0[2]	Baud rate generator 0 rate low	BEH									00	0000 0000

Table 8. Special function registers - P89LPC9161

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
BRGR1[2]	Baud rate generator 0 rate high	BFH									00	0000 0000
BRGCON	Baud rate generator 0 control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[2]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	-	CO1	CMF1	00[1]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	-	CO2	CMF2	00[1]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I^2C-bus slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000