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P89LPC924/925

8-bit microcontrollers with accelerated two-clock 80C51 core
4 kB/8 kB 3 V low-power Flash with 8-bit A/D converter

Rev. 03 — 15 December 2004 **Product data**

1. General description

The P89LPC924/925 are single-chip microcontrollers designed for applications demanding high-integration, low cost solutions over a wide range of performance requirements. The P89LPC924/925 is based on a high performance processor architecture that executes instructions in two to four clocks, six times the rate of standard 80C51 devices. Many system-level functions have been incorporated into the P89LPC924/925 in order to reduce component count, board space, and system cost.

2. Features

2.1 Principal features

- 4 kB/8 kB Flash code memory with 1 kB erasable sectors, 64-byte erasable page size, and single byte erase.
- 256-byte RAM data memory.
- Two 16-bit counter/timers. Each timer may be configured to toggle a port output upon timer overflow or to become a PWM output.
- Real-Time clock that can also be used as a system timer.
- 4-input 8-bit multiplexed A/D converter/single DAC output. Two analog comparators with selectable inputs and reference source.
- Enhanced UART with fractional baud rate generator, break detect, framing error detection, automatic address detection and versatile interrupt capabilities.
- 400 kHz byte-wide I^2C-bus communication port.
- Configurable on-chip oscillator with frequency range and RC oscillator options (selected by user programmed Flash configuration bits). The RC oscillator (factory calibrated to ±1 %) option allows operation without external oscillator components. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz. The RC oscillator option is selectable and fine tunable.
- 2.4 V to 3.6 V V_{DD} operating range. I/O pins are 5 V tolerant (may be pulled up or driven to 5.5 V).
- 15 I/O pins minimum. Up to 18 I/O pins while using on-chip oscillator and reset options.

2.2 Additional features

- 20-pin TSSOP package.
- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- In-Application Programming of the Flash code memory. This allows changing the code in a running application.
- Serial Flash programming allows simple in-circuit production coding. Flash security bits prevent reading of sensitive application programs.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from eight values.
- Low voltage reset (Brownout detect) allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different Power-down reduced power modes. Improved wake-up from Power-down mode (a low interrupt input starts execution). Typical Power-down current is 1 μA (total Power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Oscillator Fail Detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options:
  - quasi-bidirectional,
  - open drain,
  - push-pull,
  - input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC924/925 when internal reset option is selected.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Second data pointer.
- Schmitt trigger port inputs.
- Emulation support.

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
P89LPC924FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
P89LPC925FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

3.1 Ordering options

Table 2: Part options

Type number	Flash memory	Temperature range	Frequency
P89LPC924FDH	4 kB	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC925FDH	8 kB	–40 °C to +85 °C	0 MHz to 18 MHz

4. Block diagram

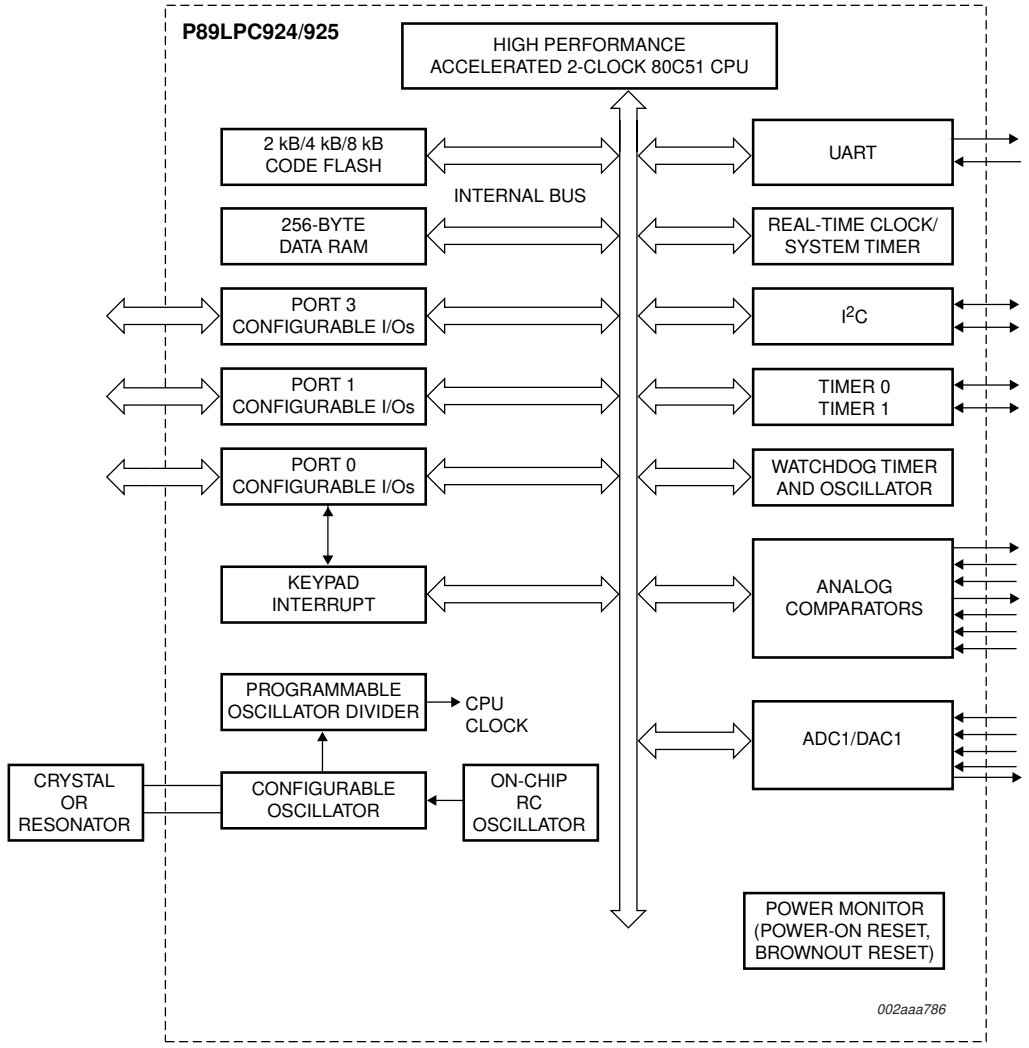

Fig 1. Block diagram.

5. Pinning information

5.1 Pinning

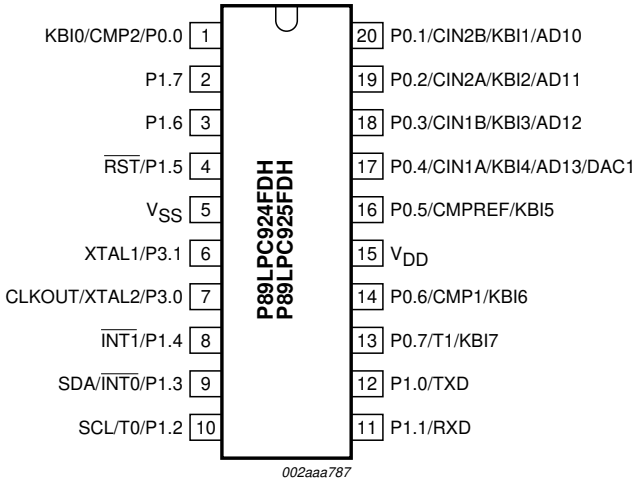

Fig 2. TSSOP20 pin configuration.

5.2 Pin description

Table 3: Pin description

Symbol	Pin	Type	Description
P0.0 - P0.7	1, 20, 19, 18, 17, 16, 14, 13	I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 "Port configurations" and Table 8 "DC electrical characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
	1	I/O	**P0.0** — Port 0 bit 0.
		O	**CMP2** — Comparator 2 output.
		I	**KBI0** — Keyboard input 0.
	20	I/O	**P0.1** — Port 0 bit 1.
		I	**CIN2B** — Comparator 2 positive input B.
		I	**KBI1** — Keyboard input 1.
		I	**AD10** — ADC1 channel 0 analog input.
	19	I/O	**P0.2** — Port 0 bit 2.
		I	**CIN2A** — Comparator 2 positive input A.
		I	**KBI2** — Keyboard input 2.
		I	**AD11** — ADC1 channel 1analog input.
	18	I/O	**P0.3** — Port 0 bit 3.
		I	**CIN1B** — Comparator 1 positive input B.
		I	**KBI3** — Keyboard input 3.
		I	**AD12** — ADC1 channel 2 analog input.
	17	I/O	**P0.4** — Port 0 bit 4.
		I	**CIN1A** — Comparator 1 positive input A.
		I	**KBI4** — Keyboard input 4.
		I	**AD13** — ADC1 channel 3 analog input.
		I	**DAC1** — Digital-to-analog converter output 1.
	16	I/O	**P0.5** — Port 0 bit 5.
		I	**CMPREF** — Comparator reference (negative) input.
		I	**KBI5** — Keyboard input 5.
	14	I/O	**P0.6** — Port 0 bit 6.
		O	**CMP1** — Comparator 1 output.
		I	**KBI6** — Keyboard input 6.
	13	I/O	**P0.7** — Port 0 bit 7.
		I/O	**T1** — Timer/counter 1 external count input or overflow output.
		I	**KBI7** — Keyboard input 7.

Table 3: Pin description...*continued*

Symbol	Pin	Type	Description
P1.0 - P1.7	12, 11, 10, 9, 8, 4, 3, 2	I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.13.1 "Port configurations" and Table 8 "DC electrical characteristics" for details. P1.2 - P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
	12	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Transmitter output for the serial port.
	11	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Receiver input for the serial port.
	10	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
		I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
		I/O	**SCL —** I^2C serial clock input/output.
	9	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
		I	**$\overline{\text{INT0}}$ —** External interrupt 0 input.
		I/O	**SDA —** I^2C serial data input/output.
	8	I/O	**P1.4 —** Port 1 bit 4.
		I	**$\overline{\text{INT1}}$ —** External interrupt 1 input.
	4	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$ —** External Reset input (if selected via FLASH configuration). A LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**
	3	I/O	**P1.6 —** Port 1 bit 6.
	2	I/O	**P1.7 —** Port 1 bit 7.

Table 3: Pin description...*continued*

Symbol	Pin	Type	Description
P3.0 - P3.1	7, 6	I/O	**Port 3:** Port 3 is an 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 "Port configurations" and Table 8 "DC electrical characteristics" for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
	7	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the FLASH configuration.
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the real time clock/system timer.
	6	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the FLASH configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the real time clock/system timer.
V_{SS}	5	I	**Ground:** 0 V reference.
V_{DD}	15	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power Down modes.

[1] Input/Output for P1.0-P1.4, P1.6, P1.7. Input for P1.5.

6. Logic symbol

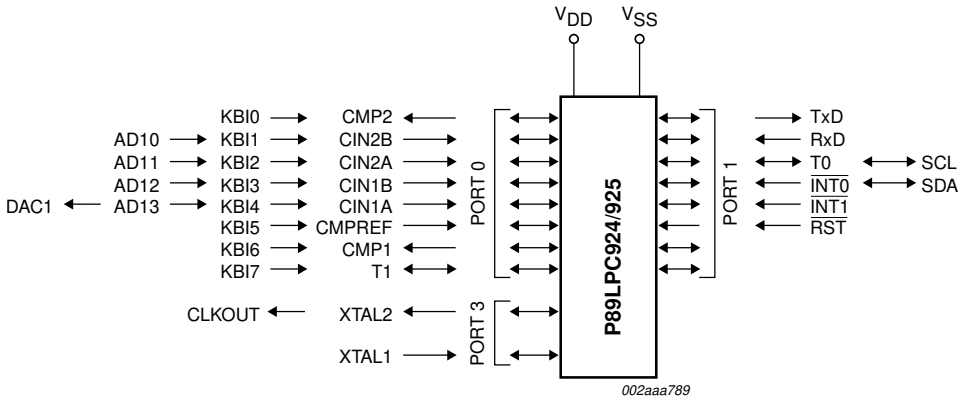

Fig 3. Logic symbol.

7. Special function registers

Remark: Special Function Registers (SFRs) accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

Table 4: Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	00000000
ADCON1	A/D control register 1	97H	ENBI1	ENADCI 1	TMM1	EDGE1	ADCI1	ENADC1	ADCS11	ADCS10	00	00000000
ADINS	A/D input select	A3H	ADI13	ADI12	ADI11	ADI10	-	-	-	-	00	00000000
ADMODA	A/D mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	-	-	-	-	00	00000000
ADMODB	A/D mode register B	A1H	CLK2	CLK1	CLK0	-	ENDAC1	-	BSA1	-	00	000x0000
AD1BH	A/D_1 boundary high register	C4H									FF	11111111
AD1BL	A/D_1 boundary low register	BCH									00	00000000
AD1DAT0	A/D_1 data register 0	D5H									00	00000000
AD1DAT1	A/D_1 data register 1	D6H									00	00000000
AD1DAT2	A/D_1 data register 2	D7H									00	00000000
AD1DAT3	A/D_1 data register 3	F5H									00	00000000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00[1]	000000x0
	Bit address		F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	00000000
BRGR0[2]	Baud rate generator rate LOW	BEH									00	00000000
BRGR1[2]	Baud rate generator rate HIGH	BFH									00	00000000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00	xxxxxx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00[1]	xx000000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00[1]	xx000000
DIVM	CPU clock divide-by-M control	95H									00	00000000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer HIGH	83H									00	00000000
DPL	Data pointer LOW	82H									00	00000000
FMADRH	Program Flash address HIGH	E7H									00	00000000
FMADRL	Program Flash address LOW	E6H									00	00000000

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Table 4: Special function registers...*continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
FMCON	Program Flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	01110000
	Program Flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program Flash data	E5H									00	00000000
I2ADR	I^2C slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	00000000
	Bit address		**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**	**D8**		
I2CON*	I^2C control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x00000x0
I2DAT	I^2C data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register HIGH	DDH									00	00000000
I2SCLL	Serial clock generator/SCL duty cycle register LOW	DCH									00	00000000
I2STAT	I^2C status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	11111000
	Bit address		**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00[1]	00000000
	Bit address		**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1*	Interrupt enable 1	E8H	EAD	EST	-	-	-	EC	EKBI	EI2C	00[1]	00x00000
	Bit address		**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00[1]	x0000000
IP0H	Interrupt priority 0 HIGH	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	PX1H	PT0H	PX0H	00[1]	x0000000
	Bit address		**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**		
IP1*	Interrupt priority 1	F8H	PAD	PST	-	-	-	PC	PKBI	PI2C	00[1]	00x00000
IP1H	Interrupt priority 1 HIGH	F7H	PADH	PSTH	-	-	-	PCH	PKBIH	PI2CH	00[1]	00x00000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxxxx00
KBMASK	Keypad interrupt mask register	86H									00	00000000
KBPATN	Keypad pattern register	93H									FF	11111111
	Bit address		**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		

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Table 4: Special function registers...*continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
P0*	Port 0	80H	T1/KB7	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0		[1]
	Bit address		97	96	95	94	93	92	91	90		
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/ SDA	T0/SCL	RXD	TXD		[1]
	Bit address		B7	B6	B5	B4	B3	B2	B1	B0		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2		[1]
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF	11111111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00	00000000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[1]	11x1xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[1]	00x0xx00
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[1]	xxxxxx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[1]	xxxxxx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	00000000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	ADPD	I2PD	-	SPD	-	00[1]	00000000
	Bit address		D7	D6	D5	D4	D3	D2	D1	D0		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00H	00000000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00H	xx00000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX		[3]
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1][6]	
RTCH	Real-time clock register HIGH	D2H									00[6]	00000000
RTCL	Real-time clock register LOW	D3H									00[6]	00000000
SADDR	Serial port address register	A9H									00	00000000
SADEN	Serial port address enable	B9H									00	00000000
SBUF	Serial Port data buffer register	99H									xx	xxxxxxxx
	Bit address		9F	9E	9D	9C	9B	9A	99	98		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	00000000

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Table 4: Special function registers...*continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	00000000
SP	Stack pointer	81H									07	00000111
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0xxx0
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	00000000
TH0	Timer 0 HIGH	8CH									00	00000000
TH1	Timer 1 HIGH	8DH									00	00000000
TL0	Timer 0 LOW	8AH									00	00000000
TL1	Timer 1 LOW	8BH									00	00000000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	00000000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0		[5] [6]
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK		[4] [6]
WDL	Watchdog load	C1H									FF	11111111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is '0'. If any are written while BRGEN = 1, the result is unpredictable.

[3] The RSTSRC register reflects the cause of the P89LPC924/925 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx110000.

[4] After reset, the value is 111001x1, i.e., PRE2-PRE0 are all '1', WDRUN = 1 and WDCLK = 1. WDTOF bit is '1' after watchdog reset and is '0' after power-on reset. Other resets will not affect WDTOF.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] The only reset source that affects these SFRs is power-on reset.

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8. Functional description

Remark: Please refer to the *P89LPC924/925 User's Manual* for a more detailed functional description.

8.1 Enhanced CPU

The P89LPC924/925 uses an enhanced 80C51 CPU which runs at 6 times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

8.2 Clocks

8.2.1 Clock definitions

The P89LPC924/925 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 4) and can also be optionally divided to a slower frequency (see Section 8.7 "CPU Clock (CCLK) modification: DIVM register").

Note: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output.

PCLK — Clock for the various peripheral devices and is CCLK/2

8.2.2 CPU clock (OSCCLK)

The P89LPC924/925 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the FLASH is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 12 MHz.

8.2.3 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

8.2.4 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

8.2.5 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below**

the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.

8.2.6 Clock output

The P89LPC924/925 supports a user-selectable clock output function on the XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on X1) and if the Real-Time clock is not using the crystal oscillator as its clock source. This allows external devices to synchronize to the P89LPC924/925. This output is enabled by the ENCLK bit in the TRIM register. The frequency of this clock output is $\frac{1}{2}$ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

8.3 On-chip RC oscillator option

The P89LPC924/925 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory pre-programmed value to adjust the oscillator frequency to 7.373 MHz, ±1% at room temperature. End-user applications can write to the Trim register to adjust the on-chip RC oscillator to other frequencies.

8.4 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

8.5 External clock input option

In this configuration, the processor clock is derived from an external source driving the XTAL1/P3.1 pin. The rate may be from 0 Hz up to 18 MHz. The XTAL2/P3.0 pin may be used as a standard port pin or a clock output. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

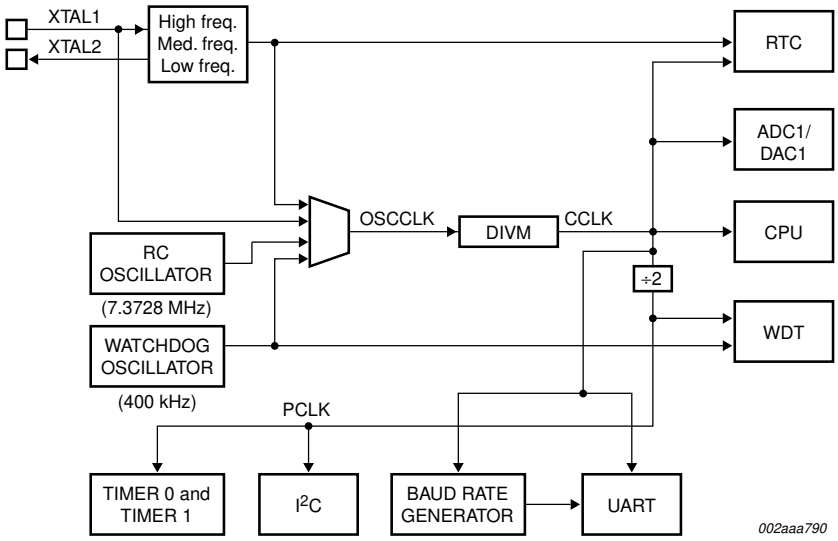

Fig 4. Block diagram of oscillator control.

8.6 CPU Clock (CCLK) wake-up delay

The P89LPC924/925 has an internal wake-up timer that delays the clock until it stabilizes depending to the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60 to 100 μs. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 to 100 μs.

8.7 CPU Clock (CCLK) modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.8 Low power select

The P89LPC924/925 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to ‘1’ to lower the power consumption further. On any reset, CLKLP is ‘0’ allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

8.9 A/D converter

8.9.1 General description

The P89LPC924/925 has an 8-bit, 4-channel multiplexed successive approximation analog-to-digital converter module. A block diagram of the A/D converter is shown in Figure 5. The A/D consists of a 4-input multiplexer which feeds a sample-and-hold circuit providing an input signal to one of two comparator inputs. The control logic in combination with the successive approximation register (SAR) drives a digital-to-analog converter which provides the other input to the comparator. The output of the comparator is fed to the SAR.

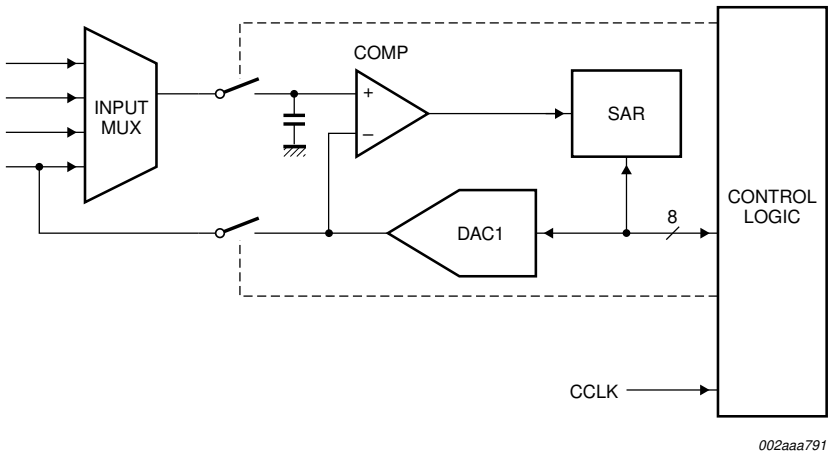

Fig 5. ADC block diagram.

8.9.2 Features

- 8-bit, 4-channel multiplexed input, successive approximation A/D converter.
- Four result registers.
- Six operating modes
  - Fixed channel, single conversion mode
  - Fixed channel, continuous conversion mode
  - Auto scan, single conversion mode
  - Auto scan, continuous conversion mode
  - Dual channel, continuous conversion mode
  - Single step mode
- Three conversion start modes
  - Timer triggered start
  - Start immediately
  - Edge triggered
- 8-bit conversion time of ≥ 3.9 μs at an ADC clock of 3.3 MHz
- Interrupt or polled operation
- Boundary limits interrupt
- DAC output to a port pin with high output impedance
- Clock divider
- Power down mode

8.9.3 A/D operating modes

Fixed channel, single conversion mode: A single input channel can be selected for conversion. A single conversion will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after the conversion completes.

Fixed channel, continuous conversion mode: A single input channel can be selected for continuous conversion. The results of the conversions will be sequentially placed in the four result registers. An interrupt, if enabled, will be generated after every four conversions. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

Auto scan, single conversion mode: Any combination of the four input channels can be selected for conversion. A single conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. If only a single channel is selected this is equivalent to single channel, single conversion mode.

Auto scan, continuous conversion mode: Any combination of the four input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected

channels have been converted. The process will repeat starting with the first selected channel. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continous conversions continue until terminated by the user.

Dual channel, continuous conversion mode: This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the first channel is placed in result register, AD1DAT0. The result of the conversion of the second channel is placed in result register, AD1DAT1. The first channel is again converted and its result stored in AD1DAT2. The second channel is again converted and its result placed in AD1DAT3. An interrupt is generated, if enabled, after every set of four conversions (two conversions per channel).

Single step mode: This special mode allows ‘single-stepping’ in an auto scan conversion mode. Any combination of the four input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the A/D waits for the next start condition. May be used with any of the start modes.

8.9.4 Conversion start modes

Timer triggered start: An A/D conversion is started by the overflow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all A/D operating modes.

Start immediately: Programming this mode immediately starts a conversion. This start mode is available in all A/D operating modes.

Edge triggered: An A/D conversion is started by rising or falling edge of P1.4. Once a conversion has started, additional edge triggers are ignored until the conversion has completed. The edge triggered start mode is available in all A/D operating modes.

8.9.5 Boundary limits interrupt

The A/D converter has both a high and low boundary limit register. After the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion are outside the limit an interrupt will be generated, if enabled. If the conversion result is within the limits, the boundary limits will again be compared after all 8 bits have been converted. An interrupt will be generated, if enabled, if the result is outside the boundary limits. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

8.9.6 DAC output to a port pin with high output impedance

The A/D converter's DAC block can be output to a port pin. In this mode, the AD1DAT3 register is used to hold the value fed to the DAC. After a value has been written to the DAC, the DAC output will appear on the channel 3 pin.

8.9.7 Clock divider

The A/D converter requires that its internal clock source be in the range of 500 kHz to 3.3 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

8.9.8 Power-down and idle mode

In idle mode the A/D converter, if enabled, will continue to function and can cause the device to exit idle mode when the conversion is completed if the A/D interrupt is enabled. In Power-down mode or Total power-down mode, the A/D does not function. If the A/D is enabled, it will consume power. Power can be reduced by disabling the A/D.

8.10 Memory organization

The various P89LPC924/925 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00h:7Fh) accessed via direct or indirect addressing, using instruction other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00h:FFh) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC924/925 has 4 kB/8 kB of on-chip Code memory.

8.11 Data RAM arrangement

The 256 bytes of on-chip RAM are organized as shown in Table 5.

Table 5: On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256

8.12 Interrupts

The P89LPC924/925 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC924/925 supports 13 interrupt sources: A/D converter, external interrupts 0 and 1, timers 0 and 1, serial port Tx, serial port Rx, combined serial port Rx/Tx, brownout detect, watchdog/real-time clock, I^2C, keyboard, and comparators 1 and 2.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

8.12.1 External interrupt inputs

The P89LPC924/925 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC924/925 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.15 “Power reduction modes” for details.

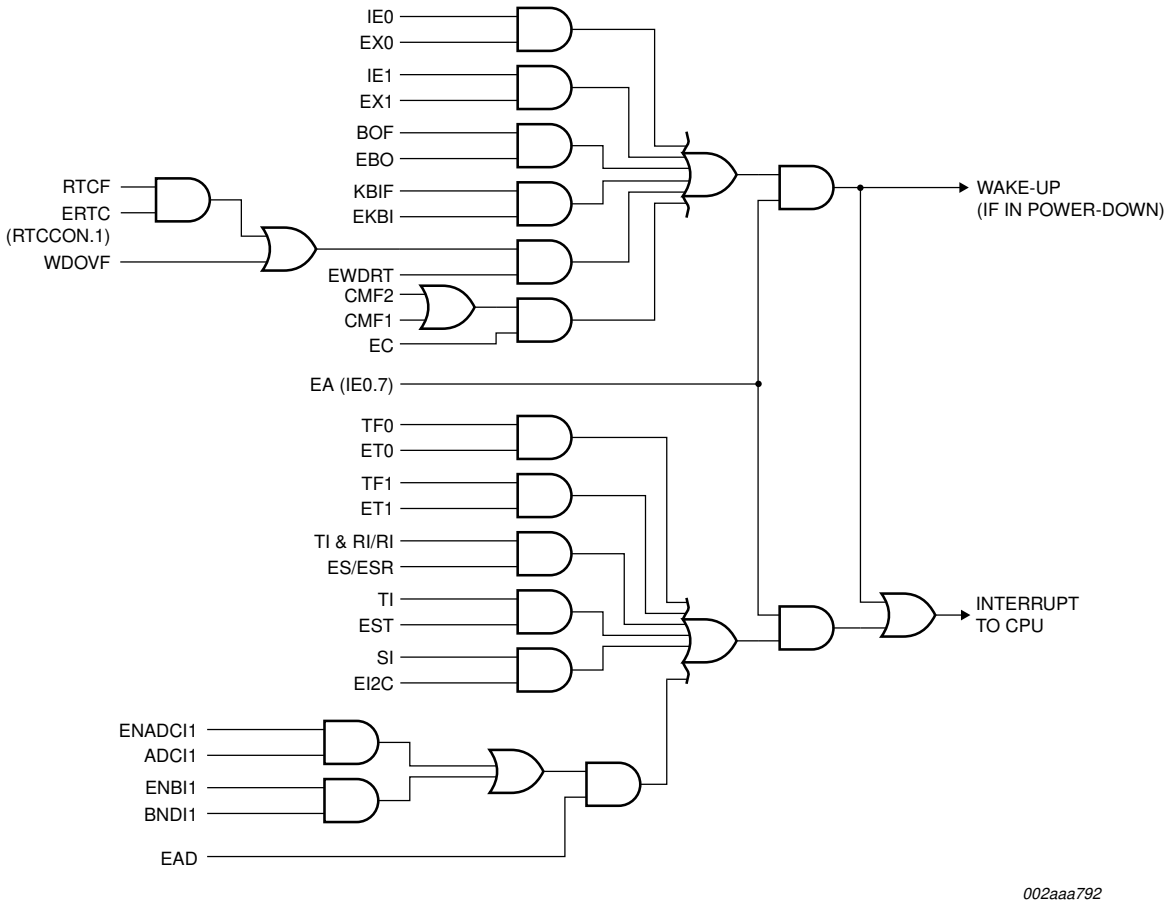

Fig 6. Interrupt sources, interrupt enables, and power-down wake-up sources.

8.13 I/O ports

The P89LPC924/925 has three I/O ports: Port 0, Port 1, and Port 3. Ports 0 and 1 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depend upon the clock and reset options chosen, as shown in Table 6.

Table 6: Number of I/O pins available

Clock source	Reset option	Number of I/O pins (20-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	18
	External $\overline{\text{RST}}$ pin supported[1]	17
External clock input	No external reset (except during power-up)	17
	External $\overline{\text{RST}}$ pin supported[1]	16
Low/medium/high speed oscillator (external crystal or resonator)	No external reset (except during power-up)	16
	External $\overline{\text{RST}}$ pin supported[1]	15

[1] Required for operation above 12 MHz.

8.13.1 Port configurations

All but three I/O port pins on the P89LPC924/925 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

P1.5 ($\overline{RST}$) can only be an input and cannot be configured.

P1.2 (SCL/T0) and P1.3 (SDA/$\overline{INT0}$) may only be configured to be either input-only or open-drain.

8.13.2 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC924/925 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.13.3 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic ‘0’. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.13.4 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt-triggered input that also has a glitch suppression circuit.

8.13.5 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic ‘1’. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt-triggered input that also has a glitch suppression circuit.

8.13.6 Port 0 analog functions

The P89LPC924/925 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high impedance) mode as described in Section 8.13.4.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD1:5 defaults to '0's to enable digital functions.

8.13.7 Additional port features

After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 and are configurable for either input-only or open-drain.

Every output on the P89LPC924/925 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 8 "DC electrical characteristics" for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

8.14 Power monitoring functions

The P89LPC924/925 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on Detect and Brownout detect.

8.14.1 Brownout detection

The Brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a Brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If Brownout detection is enabled, the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{BO} (see Table 8 "DC electrical characteristics"), and is negated when V_{DD} rises above V_{BO}. If the P89LPC924/925 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of Brownout detect, the V_{DD} rise and fall times must be observed. Please see Table 8 "DC electrical characteristics" for specifications.

8.14.2 Power-on detection

The Power-on Detect has a function similar to the Brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where Brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.