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P89LPC952/954

8-bit microcontroller with accelerated two-clock 80C51 core 8 kB/16 kB 3 V byte-erasable flash with 10-bit ADC

Rev. 04 — 24 July 2008 Product data sheet

1. General description

The P89LPC952/954 is a single-chip microcontroller, available in low cost packages, based on a high performance processor architecture that executes instructions in two to four clocks, six times the rate of standard 80C51 devices. Many system-level functions have been incorporated into the P89LPC952/954 in order to reduce component count, board space, and system cost.

2. Features

2.1 Principal features

- 8 kB/16 kB byte-erasable flash code memory organized into 1 kB sectors and 64-byte pages. Single-byte erasing allows any byte(s) to be used as non-volatile data storage.
- 256-byte RAM data memory and a 256-byte auxiliary on-chip RAM.
- 8-input multiplexed 10-bit ADC with window comparator that can generate an interrupt for in or out of range results. Two analog comparators with selectable inputs and reference source.
- Two 16-bit counter/timers (each may be configured to toggle a port output upon timer overflow or to become a PWM output) and a 23-bit system timer that can also be used as a RTC.
- Two enhanced UARTs with a fractional baud rate generator, break detect, framing error detection, and automatic address detection; 400 kHz byte-wide I^2C-bus communication port and SPI communication port.
- High-accuracy internal RC oscillator option, with clock doubler option, allows operation without external oscillator components. The RC oscillator option is selectable and fine tunable. Fast switching between the internal RC oscillator and any oscillator source provides optimal support of minimal power active mode with fast switching to maximum performance.
- 2.4 V to 3.6 V V_{DD} operating range. I/O pins are 5 V tolerant (may be pulled up or driven to 5.5 V).
- 44-pin and 48-pin packages with 40 and 42 I/O pins minimum while using on-chip oscillator and reset options.
- Port 5 has high current sourcing/sinking (20 mA) for all Port 5 pins. All other port pins have high sinking capability (20 mA). A maximum limit is specified for the entire chip.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from eight values.

2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Serial flash In-System Programming (ISP) allows coding while the device is mounted in the end application.
- In-Application Programming (IAP) of the flash code memory. This allows changing the code in a running application.
- Low voltage (brownout) detect allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- On-chip power-on reset allows operation without external reset components. A software reset function is also available.
- Programmable external reset pin (P1.5) configuration options: open drain bidirectional reset input/output, reset input with pull-up, push-pull reset output, input-only port. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets.
- Only power and ground connections are required to operate the P89LPC952/954 when internal reset option is selected.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Schmitt trigger port inputs.
- Second data pointer.
- Extended temperature range.
- Emulation support.

3. Ordering information

Table 1. Ordering information

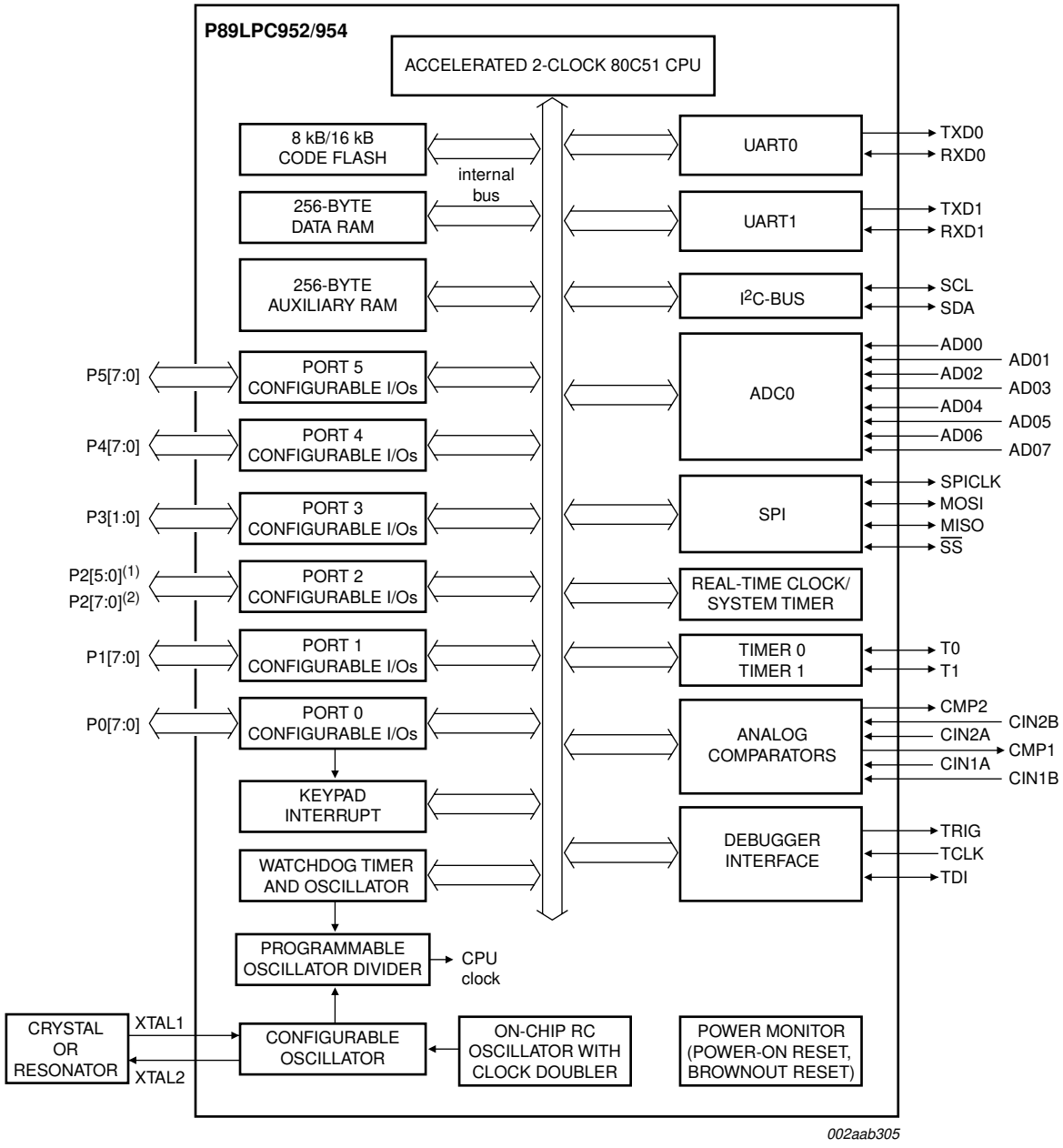
Type number	Package		
	Name	Description	Version
P89LPC952FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
P89LPC952FBD	LQFP44	plastic low profile quad flat package; 44 leads; body 10 × 10 × 1.4 mm	SOT389-1
P89LPC954FA	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
P89LPC954FBD44	LQFP44	plastic low profile quad flat package; 44 leads; body 10 × 10 × 1.4 mm	SOT389-1
P89LPC954FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	Temperature range	Frequency
P89LPC952FA	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC952FBD	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC954FA	16 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC954FBD44	16 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC954FBD48	16 kB	−40 °C to +85 °C	0 MHz to 18 MHz

4. Block diagram

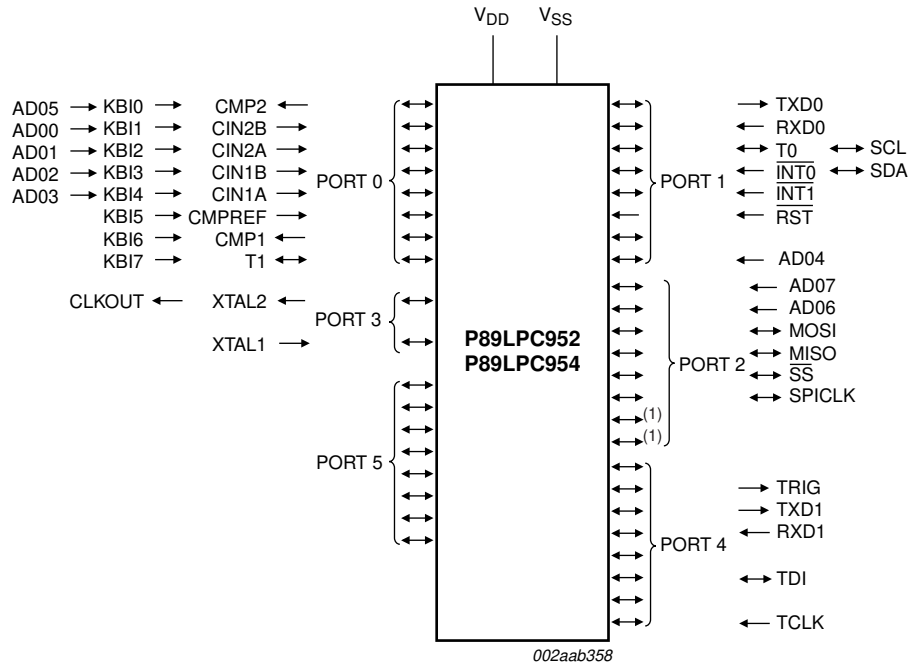


(1) 44-pin package.

(2) 48-pin package.

Fig 1. Block diagram

5. Functional diagram



(1) 48-pin package.

Fig 2. Functional diagram

6. Pinning information

6.1 Pinning

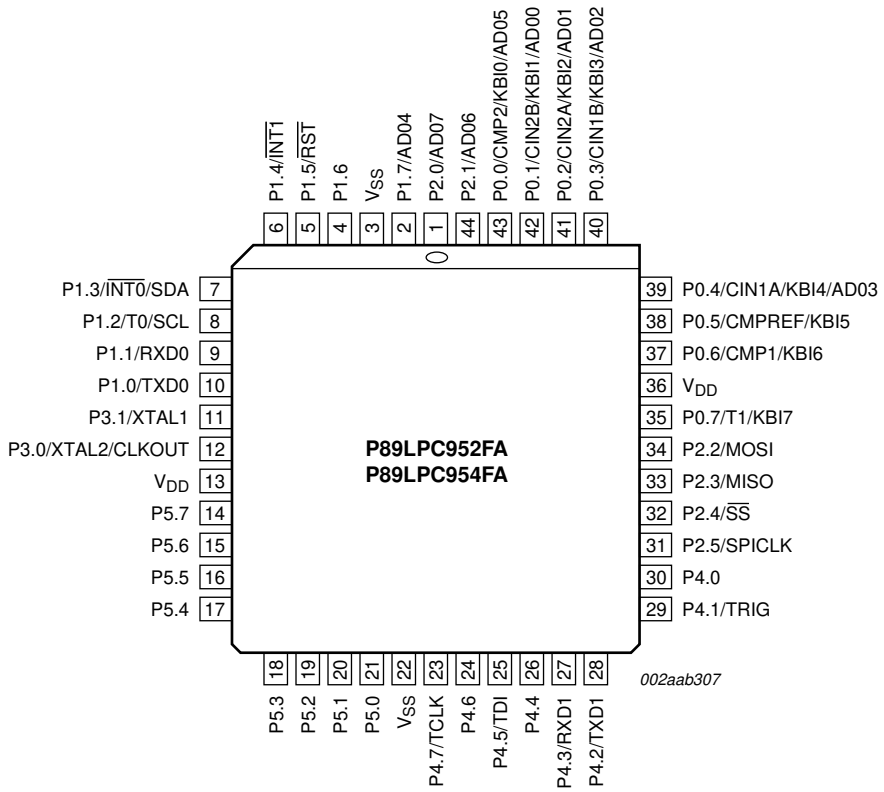


Fig 3. PLCC44 pin configuration

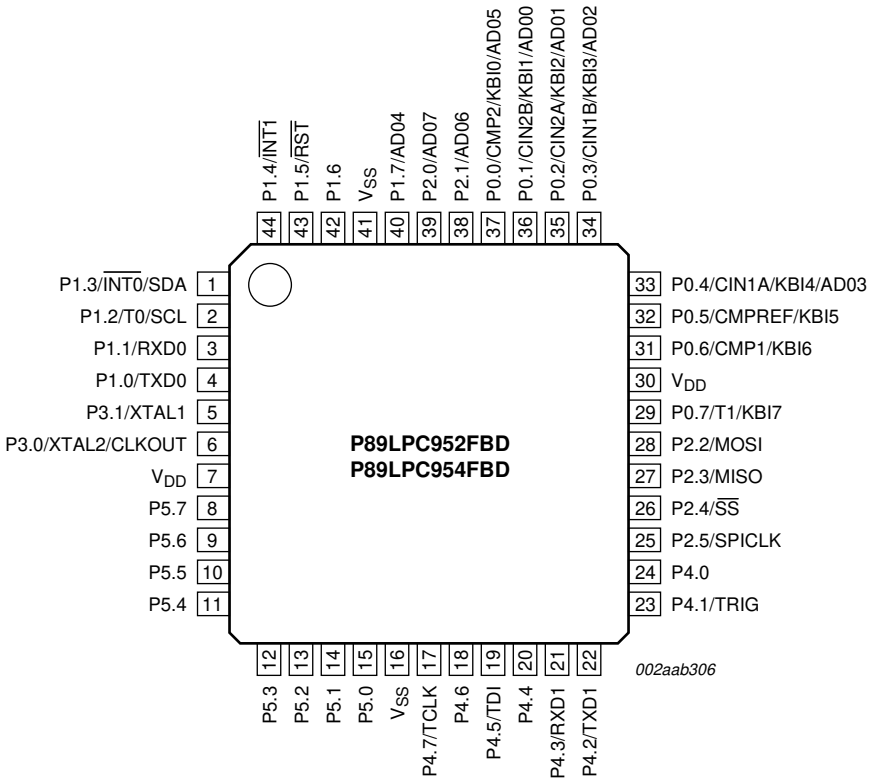


Fig 4. LQFP44 pin configuration

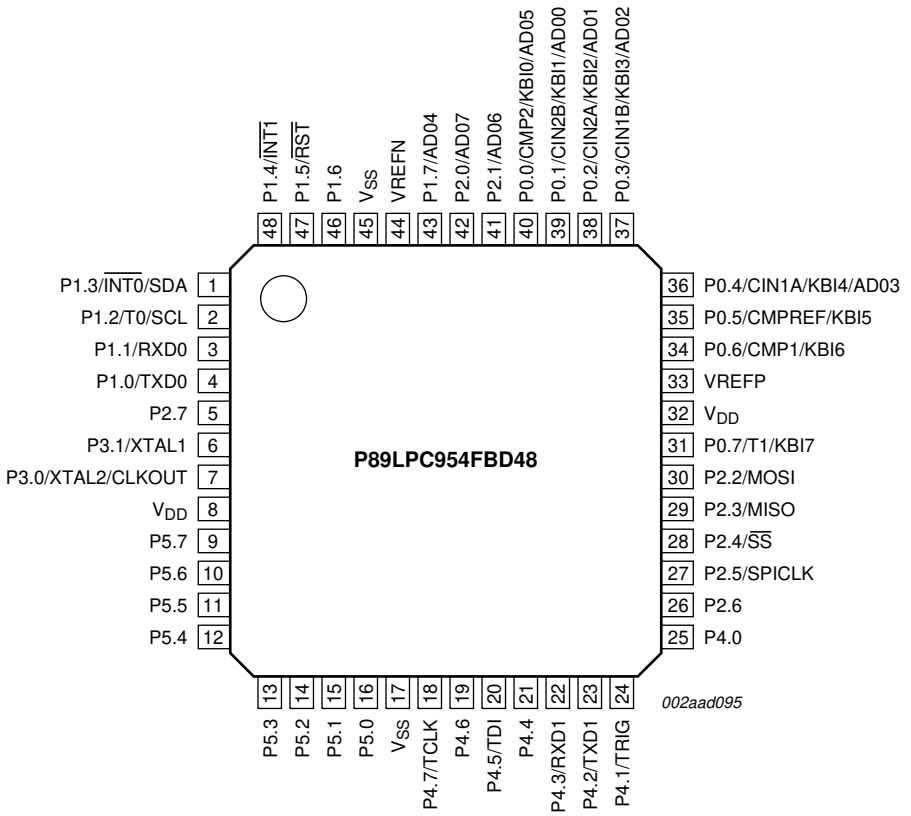


Fig 5. LQFP48 pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P0.0 to P0.7				I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/ KBI0/AD05	40	43	37	I/O	**P0.0** — Port 0 bit 0.
				O	**CMP2** — Comparator 2 output.
				I	**KBI0** — Keyboard input 0.
				I	**AD05** — ADC0 channel 5 analog input.
P0.1/CIN2B/ KBI1/AD00	39	42	36	I/O	**P0.1** — Port 0 bit 1.
				I	**CIN2B** — Comparator 2 positive input B.
				I	**KBI1** — Keyboard input 1.
				I	**AD00** — ADC0 channel 0 analog input.
P0.2/CIN2A/ KBI2/AD01	38	41	35	I/O	**P0.2** — Port 0 bit 2.
				I	**CIN2A** — Comparator 2 positive input A.
				I	**KBI2** — Keyboard input 2.
				I	**AD01** — ADC0 channel 1 analog input.
P0.3/CIN1B/ KBI3/AD02	37	40	34	I/O	**P0.3** — Port 0 bit 3.
				I	**CIN1B** — Comparator 1 positive input B.
				I	**KBI3** — Keyboard input 3.
				I	**AD02** — ADC0 channel 2 analog input.
P0.4/CIN1A/ KBI4/AD03	36	39	33	I/O	**P0.4** — Port 0 bit 4.
				I	**CIN1A** — Comparator 1 positive input A.
				I	**KBI4** — Keyboard input 4.
				I	**AD03** — ADC0 channel 3 analog input.
P0.5/CMPREF/ KBI5	35	38	32	I/O	**P0.5** — Port 0 bit 5.
				I	**CMPREF** — Comparator reference (negative) input.
				I	**KBI5** — Keyboard input 5.

Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P0.6/CMP1/KBI6	34	37	31	I/O	**P0.6** — Port 0 bit 6.
				O	**CMP1** — Comparator 1 output.
				I	**KBI6** — Keyboard input 6.
P0.7/T1/KBI7	31	35	29	I/O	**P0.7** — Port 0 bit 7.
				I/O	**T1** — Timer/counter 1 external count input or overflow output.
				I	**KBI7** — Keyboard input 7.
P1.0 to P1.7				I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.13.1 "Port configurations" and Table 11 "Static characteristics" for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD0	4	10	4	I/O	**P1.0** — Port 1 bit 0.
				O	**TXD0** — Transmitter output for serial port 0.
P1.1/RXD0	3	9	3	I/O	**P1.1** — Port 1 bit 1.
				I	**RXD0** — Receiver input for serial port 0.
P1.2/T0/SCL	2	8	2	I/O	**P1.2** — Port 1 bit 2 (open-drain when used as output).
				I/O	**T0** — Timer/counter 0 external count input or overflow output (open-drain when used as output).
				I/O	**SCL** — I^2C-bus serial clock input/output.
P1.3/$\overline{INT0}$/SDA	1	7	1	I/O	**P1.3** — Port 1 bit 3 (open-drain when used as output).
				I	**$\overline{INT0}$** — External interrupt 0 input.
				I/O	**SDA** — I^2C-bus serial data input/output.
P1.4/$\overline{INT1}$	48	6	44	I/O	**P1.4** — Port 1 bit 4.
				I	**$\overline{INT1}$** — External interrupt 1 input.

Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P1.5/$\overline{\text{RST}}$	47	5	43	I	**P1.5 —** Port 1 bit 5 (input only).
				I	**$\overline{\text{RST}}$ —** External Reset input during power-on or maybe a reset input/output if selected via UCFG1 and UCFG2. When functioning as a reset input or input/output, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. When functioning as a reset output or input/output an internal reset source will drive this pin LOW. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**
P1.6	46	4	42	I/O	**P1.6 —** Port 1 bit 6.
P1.7/AD04	43	2	40	I/O	**P1.7 —** Port 1 bit 7.
				I	**AD04 —** ADC0 channel 4 analog input.
P2.0 to P2.5				I/O	**Port 2:** Port 2 is an 8-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.0/AD07	42	1	39	I/O	**P2.0 —** Port 2 bit 0.
				I	**AD07 —** ADC0 channel 7 analog input.
P2.1/AD06	41	44	38	I/O	**P2.1 —** Port 2 bit 1.
				I	**AD06 —** ADC0 channel 6 analog input.
P2.2/MOSI	30	34	28	I/O	**P2.2 —** Port 2 bit 2.
				I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.3/MISO	29	33	27	I/O	**P2.3 —** Port 2 bit 3.
				I/O	**MISO —** When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{\text{SS}}$	28	32	26	I/O	**P2.4 —** Port 2 bit 4.
				I/O	**$\overline{\text{SS}}$ —** SPI Slave select.

Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P2.5/SPICLK	27	31	25	I/O	**P2.5 —** Port 2 bit 5.
				I/O	**SPICLK —** SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.6	26	-	-	I/O	**P2.6 —** Port 2 bit 6.
P2.7	5	-	-	I/O	**P2.7 —** Port 2 bit 7.
P3.0 to P3.1				I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	7	12	6	I/O	**P3.0 —** Port 3 bit 0.
				O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration.
				O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK -TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer.
P3.1/XTAL1	6	11	5	I/O	**P3.1 —** Port 3 bit 1.
				I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer.
P4.0 to P4.7				I/O	**Port 4:** Port 4 is an 8-bit I/O port with a user-configurable output type. During reset Port 4 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 4 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 4 also provides various special functions as described below:
P4.0	25	30	24	I/O	**P4.0 —** Port 4 bit 0.
P4.1/TRIG	24	29	23	I/O	**P4.1 —** Port 4 bit 1.
				O	**TRIG —** Debugger trigger output.
P4.2/TXD1	23	28	22	I/O	**P4.2 —** Port 4 bit 2.
				O	**TXD1 —** Transmitter output for serial port 1.
P4.3/RXD1	22	27	21	I/O	**P4.3 —** Port 4 bit 3.
				I	**RXD1 —** Receiver input for serial port 1.

Table 3. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	PLCC44	LQFP44		
P4.4	21	26	20	I/O	**P4.4 —** Port 4 bit 4.
P4.5/TDI	20	25	19	I/O	**P4.5 —** Port 4 bit 5.
				I/O	**TDI —** Serial data input/output for debugger interface.
P4.6	19	24	18	I/O	**P4.6 —** Port 4 bit 6.
P4.7/TCLK	18	23	17	I/O	**P4.7 —** Port 4 bit 7.
				I	**TCLK —** Serial clock input for debugger interface.
P5.0 to P5.7				I/O	**Port 5:** Port 5 is an 8-bit I/O port with a user-configurable output type. During reset Port 5 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 5 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.13.1 “Port configurations” and Table 11 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 5 also provides various special functions as described below:
P5.0	16	21	15	I/O	**P5.0 —** Port 5 bit 0. High current source.
P5.1	15	20	14	I/O	**P5.1 —** Port 5 bit 1. High current source.
P5.2	14	19	13	I/O	**P5.2 —** Port 5 bit 2. High current source.
P5.3	13	18	12	I/O	**P5.3 —** Port 5 bit 3. High current source.
P5.4	12	17	11	I/O	**P5.4 —** Port 5 bit 4. High current source.
P5.5	11	16	10	I/O	**P5.5 —** Port 5 bit 5. High current source.
P5.6	10	15	9	I/O	**P5.6 —** Port 5 bit 6. High current source.
P5.7	9	14	8	I/O	**P5.7 —** Port 5 bit 7. High current source.
V_{SS}	17, 45	3, 22	16, 41	I	**Ground:** 0 V reference.
VREFN	44	-	-		negative ADC reference voltage
V_{DD}	8, 32	13, 36	7, 30	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.
VREFP	33	-	-		positive ADC reference voltage

[1] Input/output for P1.0 to P1.4, P1.6, P1.7. Input for P1.5.

7. Functional description

Remark: Please refer to the P89LPC952/954 *User's Manual* for a more detailed functional description.

7.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

Table 4. Special function registers

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		E7	E6	E5	E4	E3	E2	E1	E0		
ACC[1]	Accumulator	E0H									00	0000 0000
AD0CON	ADC0 control register	97H	ENBI0	ENADCI0	TMM0	EDGE0	ADCI0	ENADC0	ADCS01	ADCS00	00	0000 0000
AD0INS	ADC0 input select	A3H	ADI07	ADI06	ADI05	ADI04	ADI03	ADI02	ADI01	ADI00	00	0000 0000
AD0MODA	ADC0 mode register A	C0H	BNDI0	BURST0	SCC0	SCAN0	-	-	-	-	00	0000 0000
AD0MODB	ADC0 mode register B	A1H	CLK2	CLK1	CLK0	-	-	-	-	-	00	000x 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00	0000 00x0
	Bit address		F7	F6	F5	F4	F3	F2	F1	F0		
B[1]	B register	F0H									00	0000 0000
BRGR0_0	Baud rate generator 0 rate low	BEH									00	0000 0000
BRGR1_0	Baud rate generator 0 rate high	BFH									00	0000 0000
BRGCON_0	Baud rate generator 0 control	BDH	-	-	-	-	-	-	SBRGS_0	BRGEN_0	00[3]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00[2]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00[2]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											

Table 4. Special function registers *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I²C-bus slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000
	Bit address		**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**	**D8**		
I2CON[1]	I²C-bus control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I²C-bus data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I²C-bus status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000

Table 4. Special function registers *...continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0[1]	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	0000 0000
		Bit address	**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1[1]	Interrupt enable 1	E8H	-	EST	-	-	ESPI	EC	EKBI	EI2C	00[2]	00x0 0000
IEN2	Interrupt enable 2	D5H	-	-	-	-	EST1	ES1/ESR1	EADC	-	00[2]	00x0 0000
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**		
IP0[1]	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00[2]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/ PSRH	PT1H	PX1H	PT0H	PX0H	00[2]	x000 0000
		Bit address	**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**		
IP1[1]	Interrupt priority 1	F8H	-	PST	-	-	PSPI	PC	PKBI	PI2C	00[2]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	-	PSPIH	PCH	PKBIH	PI2CH	00[2]	00x0 0000
IP2	Interrupt priority 2	D6H	-	-	-	-	PEST1	PES1/ PESR1	PADC	-	00[2]	00x0 0000
IP2H	Interrupt priority 2 high	D7H	-	-	-	-	PEST1H	PES1H/ PESR1H	PADCH	-	00[2]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN _SEL	KBIF	00[2]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0[1]	Port 0	80H	T1/KB7	CMP1 /KB6	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0	[2]	
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1[1]	Port 1	90H	-	-	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/SDA	T0/SCL	RXD0	TXD0	[2]	

Table 4. Special function registers *...continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P2[1]	Port 2	A0H	-	-	SPICLK	$\overline{SS}$	MISO	MOSI	-	-	[2]	
		Bit address	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P3[1]	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2	[2]	
P4	Port 4	B3H	-	TMS	-	-	RXD1	TXD1	TRIG	T3EX	[2]	
P5	Port 5	B4H	T3	-	-	-	-	-	-	-	[2]	
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[2]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[2]	0000 0000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[2]	11x1 xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[2]	00x0 xx00
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)	(P2M1.0)	FF[2]	1111 1111
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)	(P2M2.0)	00[2]	0000 0000
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[2]	xxxx xx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[2]	xxxx xx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	ADPD	I2PD	SPPD	SPD	-	00[2]	0000 0000
		Bit address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW[1]	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX	[4]	

Table 4. Special function registers *...continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[2][7]	011x xx00
RTCH	RTC register high	D2H									00[7]	0000 0000
RTCL	RTC register low	D3H									00[7]	0000 0000
S0ADDR	Serial port address register	A9H									00	0000 0000
S0ADEN	Serial port address enable	B9H									00	0000 0000
S0BUF	Serial Port data buffer register	99H									xx	xxxx xxxx
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
S0CON[1]	Serial port control	98H	SM0_0/FE_0	SM1_00	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00	0000 0000
S0STAT	Serial port extended status register	BAH	DBMOD_0	INTLO_0	CIDIS_0	DBISEL_0	FE_0	BR_0	OE_0	STINT_0	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
S1CON	Serial port 1 control	B6H	SM0_1/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00	0000 0000
S1STAT	Serial port 1 extended status register	D4H	DBMOD_1	INTLO_1	CIDIS_1	DBISEL_1	FE_1	BR_1	OE_1	STINT_1	00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0

Table 4. Special function registers *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		8F	8E	8D	8C	8B	8A	89	88		
TCON[1]	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[6] [7]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[5] [7]	
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] Indicates SFRs that are bit addressable.

[2] All ports are in input only (high-impedance) state after power-up.

[3] BRGR1_0 and BRGR0_0 must only be written if BRGEN_0 in BRGCON_0 SFR is logic 0. If any are written while BRGEN_0 = 1, the result is unpredictable.

[4] The RSTSRC register reflects the cause of the P89LPC952/954 reset. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is xx11 0000.

[5] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[6] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[7] The only reset source that affects these SFRs is power-on reset.

Table 5. Extended special function registers

Name	Description	SFR addr.	Bit functions and addresses		Reset value	
			MSB	LSB	Hex	Binary
ADC0HBND	ADC0 high_boundary register, left (MSB)	FFEFH			FF	1111 1111
ADC0LBND	ADC0 low_boundary register (MSB)	FFEEH			00	0000 0000
AD0DAT0R	ADC0 data register 0, right (LSB)	FFFEH	AD0DAT0[7:0]		00	0000 0000
AD0DAT0L	ADC0 data register 0, left (MSB)	FFFFH	AD0DAT0[9:2]		00	0000 0000
AD0DAT1R	ADC0 data register 1, right (LSB)	FFFCH	AD0DAT1[7:0]		00	0000 0000
AD0DAT1L	ADC0 data register 1, left (MSB)	FFFDH	AD0DAT1[9:2]		00	0000 0000
AD0DAT2R	ADC0 data register 2, right (LSB)	FFFAH	AD0DAT2[7:0]		00	0000 0000
AD0DAT2L	ADC0 data register 2, left (MSB)	FFFBH	AD0DAT2[9:2]		00	0000 0000
AD0DAT3R	ADC0 data register 3, right (LSB)	FFF8H	AD0DAT3[7:0]		00	0000 0000
AD0DAT3L	ADC0 data register 3, left (MSB)	FFF9H	AD0DAT3[9:2]		00	0000 0000
AD0DAT4R	ADC0 data register 4, right (LSB)	FFF6H	AD0DAT4[7:0]		00	0000 0000
AD0DAT4L	ADC0 data register 4, left (MSB)	FFF7H	AD0DAT4[9:2]		00	0000 0000
AD0DAT5R	ADC0 data register 5, right (LSB)	FFF4H	AD0DAT5[7:0]		00	0000 0000
AD0DAT5L	ADC0 data register 5, left (MSB)	FFF5H	AD0DAT5[9:2]		00	0000 0000
AD0DAT6R	ADC0 data register 6, right (LSB)	FFF2H	AD0DAT6[7:0]		00	0000 0000
AD0DAT6L	ADC0 data register 6, left (MSB)	FFF3H	AD0DAT6[9:2]		00	0000 0000
AD0DAT7R	ADC0 data register 7, right (LSB)	FFF0H	AD0DAT7[7:0]			

Table 5. Extended special function registers *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
AD0DAT7L	ADC0 data register 7, left (MSB)	FFF1H	AD0DAT7[9:2]									
BNDSTA0	ADC0 boundary status register	FFEDH										
BRGCON_1	Baud rate generator 1 control	FFB3H	-	-	-	-	-	-	SBRGS_1	BRGEN_1	00[2]	xxxx xx00
BRG0_1	Baud rate generator 1 rate low	FFB4H										
BRG1_1	Baud rate generator 1 rate high	FFB5H										
FREEZE	Peripheral clock freeze	FFD0H	-	-	-	RTC_F	CCU_F	WDT_F	T1_F	T0_F	00	xxx0 0000
P4M1	Port 4 output mode 1	FFB8H	(P4M1.7)	(P4M1.6)	(P4M1.5)	(P4M1.4)	(P4M1.3)	(P4M1.2)	(P4M1.1)	(P4M1.0)	FF[1]	1111 1111
P4M2	Port 4 output mode 2	FFB9H	(P4M2.7)	(P4M2.6)	(P4M2.5)	(P4M2.4)	(P4M2.3)	(P4M2.2)	(P4M2.1)	(P4M2.0)	00[1]	0000 0000
P5M1	Port 5 output mode 1	FFBAH	(P5M1.7)	(P5M1.6)	(P5M1.5)	(P5M1.4)	(P5M1.3)	(P5M1.2)	(P5M1.1)	(P5M1.0)	FF[1]	1111 1111
P5M2	Port 5 output mode 3	FFBBH	(P5M2.7)	(P5M2.6)	(P5M2.5)	(P5M2.4)	(P5M2.3)	(P5M2.2)	(P5M2.1)	(P5M2.0)	00[1]	0000 0000
S1ADDR	Serial port 1 address register	FFB2H									00	0000 0000
S1ADEN	Serial port 1 address enable	FFB1H									00	0000 0000
S1BUF	Serial port 1 data buffer register	FFB0H									xx	xxxx xxxx

[1] Extended SFRs are physically located on-chip but logically located in external data memory address space (XDATA). The MOVX A,@DPTR and MOVX @DPTR,A instructions are used to access these extended SFRs.

[2] BRGR1_1 and BRGR0_1 must only be written if BRGEN_1 in BRGCON_1 SFR is logic 0. If any are written while BRGEN_1 = 1, the result is unpredictable.

7.2 Enhanced CPU

The P89LPC952/954 uses an enhanced 80C51 CPU which runs at six times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

7.3 Clocks

7.3.1 Clock definitions

The P89LPC952/954 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 6) and can also be optionally divided to a slower frequency (see Section 7.8 “CCLK modification: DIVM register”).

Note: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output. The clock doubler option, when enabled, provides an output frequency of 14.746 MHz.

PCLK — Clock for the various peripheral devices and is $^{CCLK}/_{2}$.

7.3.2 CPU clock (OSCCLK)

The P89LPC952/954 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the flash is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source. The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 18 MHz.

7.3.3 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

7.3.4 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

7.3.5 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration. **When using a clock frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using a clock frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device**

in reset when V_{DD} falls below the minimum specified operating voltage. These requirements for clock frequencies above 12 MHz do not apply when using the internal RC oscillator in clock doubler mode.

7.3.6 Clock output

The P89LPC952/954 supports a user-selectable clock output function on the XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on XTAL1) and if the RTC is not using the crystal oscillator as its clock source. This allows external devices to synchronize to the P89LPC952/954. This output is enabled by the ENCLK bit in the TRIM register.

The frequency of this clock output is $\frac{1}{2}$ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

7.4 On-chip RC oscillator option

The P89LPC952/954 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory pre-programmed value to adjust the oscillator frequency to 7.373 MHz ± 1 % at room temperature. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies. When the clock doubler option is enabled (UCFG1.3 = 1), the output frequency is 14.746 MHz. If CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to reduce power consumption. On reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

The requirements in Section 7.3.5 “High speed oscillator option” for configuring P1.5 as an external reset input and using an external reset circuit when the clock frequency is greater than 12 MHz do **not** apply when using the internal RC oscillator’s clock doubler option.

7.5 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

7.6 External clock input option

In this configuration, the processor clock is derived from an external source driving the P3.1/XTAL1 pin. The rate may be from 0 Hz up to 18 MHz. The P3.0/XTAL2 pin may be used as a standard port pin or a clock output.

When using an external clock input frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an external clock input frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage. These requirements for clock frequencies above 12 MHz do not apply when using the internal RC oscillator in clock doubler mode.

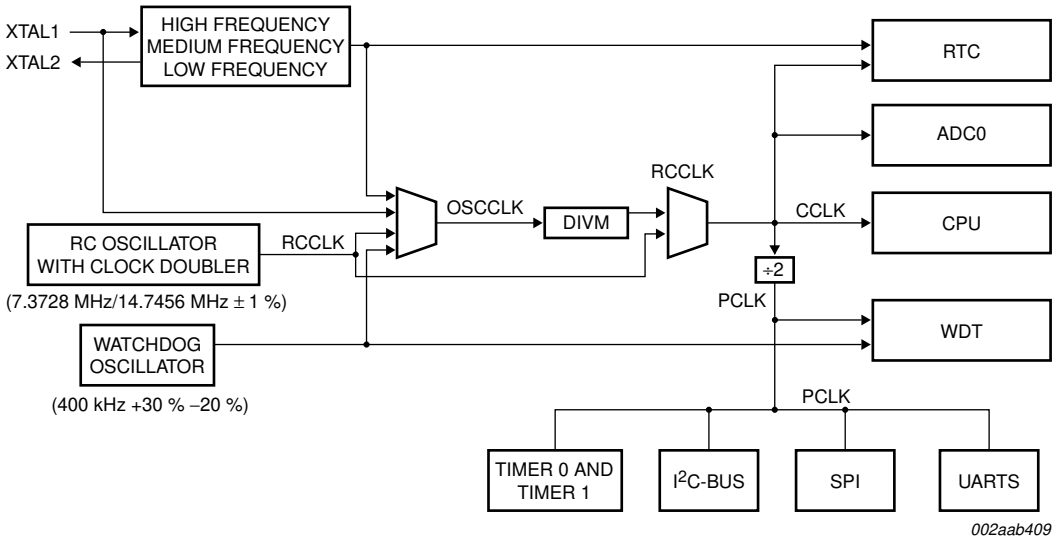


Fig 6. Block diagram of oscillator control

7.7 CCLK wake-up delay

The P89LPC952/954 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 992 OSCCLK cycles plus 60 μs to 100 μs. If the clock source is either the internal RC oscillator, watchdog oscillator, or external clock, the delay is 224 OSCCLK cycles plus 60 μs to 100 μs.

7.8 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

7.9 Low power select

The P89LPC952/954 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to ‘1’ to lower the power consumption further. On any reset, CLKLP is ‘0’ allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.