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P89LPC970/971/972

8-bit microcontroller with accelerated two-clock 80C51 core 2 kB/4 kB/8 kB wide-voltage byte-erasable flash

Rev. 3 — 8 June 2010 Product data sheet

1. General description

The P89LPC970/971/972 is a single-chip microcontroller, available in low cost packages, based on a high performance processor architecture that executes instructions in two to four clocks, six times the rate of standard 80C51 devices. Many system-level functions have been incorporated into the P89LPC970/971/972 in order to reduce component count, board space, and system cost.

2. Features and benefits

2.1 Principal features

- 2 kB/4 kB/8 kB byte-erasable flash code memory organized into 1 kB sectors and 64-byte pages. Single-byte erasing allows any byte(s) to be used as non-volatile data storage.
- 256-byte RAM data memory.
- Two analog comparators with selectable inputs and reference source.
- Five 16-bit counter/timers (each may be configured to toggle a port output upon timer overflow or to become a PWM output).
- A 23-bit system timer that can also be used as real-time clock consisting of a 7-bit prescaler and a programmable and readable 16-bit timer.
- Enhanced UART with a fractional baud rate generator, break detect, framing error detection, and automatic address detection; 400 kHz byte-wide I^2C-bus communication port.
- SPI communication port (pin remap).
- High-accuracy internal RC oscillator option 7.373 MHz calibrated to ±1 %, with clock doubler option, allows operation without external oscillator components. The RC oscillator option is selectable and fine tunable.
- Watchdog timer with separate on-chip oscillator, nominal 400 kHz/25 kHz, calibrated to ±10 % at 400 kHz, requiring no external components. The watchdog prescaler is selectable from eight values.
- Pin remap for UART, I^2C-bus and SPI.
- 2.4 V to 5.5 V V_{DD} operating range.
- Enhanced low voltage (brownout) detect allows a graceful system shutdown when power fails.
- 20-pin TSSOP and DIP packages with 15 I/O pins minimum and up to 18 I/O pins while using on-chip oscillator and reset options.

2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Serial flash In-System Programming (ISP) allows coding while the device is mounted in the end application.
- In-Application Programming (IAP) of the flash code memory. This allows changing the code in a running application.
- Clock switching on the fly among internal RC oscillator, watchdog oscillator, external clock source provides optimal support of minimal power active mode with fast switching to maximum performance.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- Integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Idle mode, Power-down mode and total Power-down mode. In addition, the power consumption can be further reduced in Normal or Idle mode through configuring regulators modes according to the applications.
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A software reset function is also available.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- High current sourcing/sinking (20 mA) on eight I/O pins (P0.3 to P0.7, P1.4, P1.6, P1.7). All other port pins have high sinking capability (20 mA). A maximum limit is specified for the entire chip.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC970/971/972 when internal reset option is selected.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Schmitt trigger port inputs.
- Second data pointer.
- Emulation support.

3. Ordering information

Table 1. Ordering information

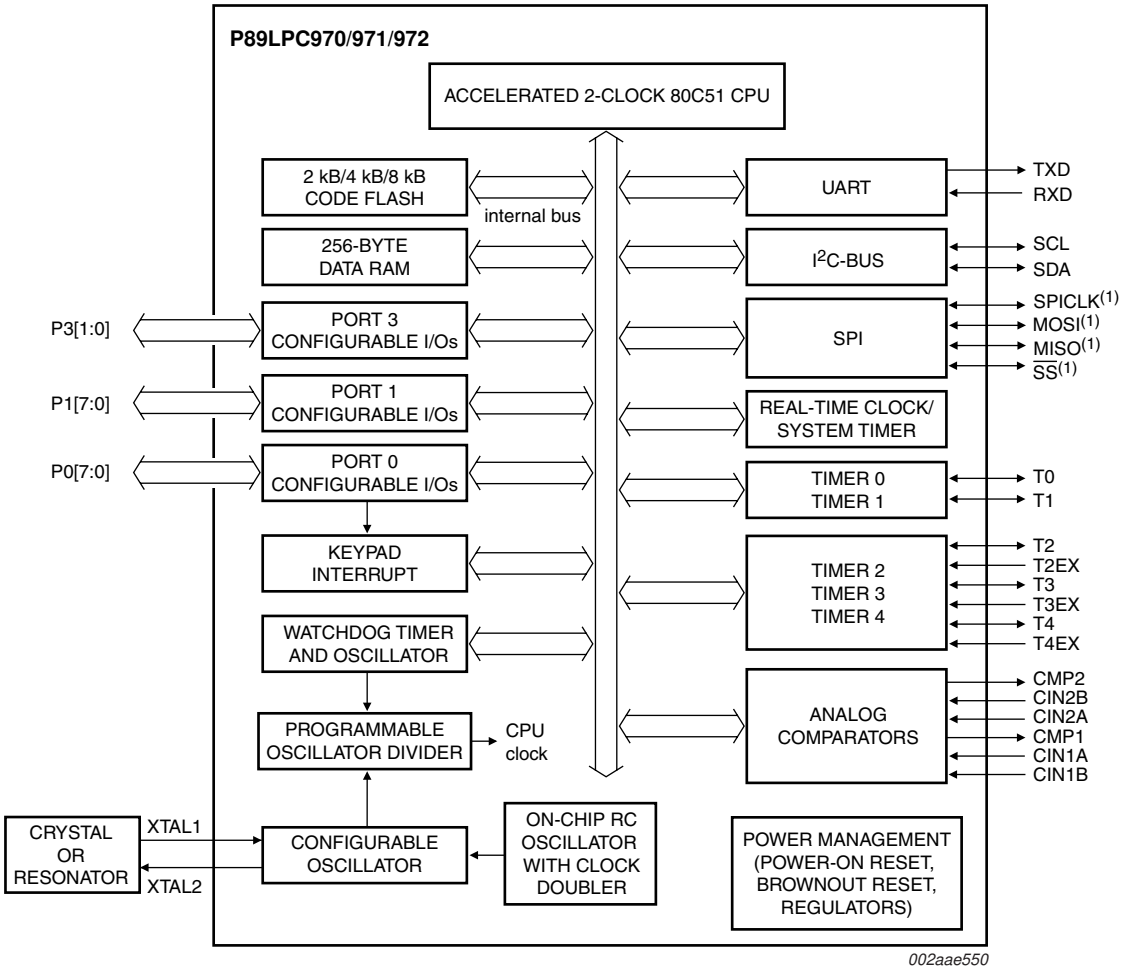
Type number	Package		
	Name	Description	Version
P89LPC970FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
P89LPC971FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
P89LPC972FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
P89LPC972FN	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	Temperature range	Frequency
P89LPC970FDH	2 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC971FDH	4 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC972FDH	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz
P89LPC972FN	8 kB	−40 °C to +85 °C	0 MHz to 18 MHz

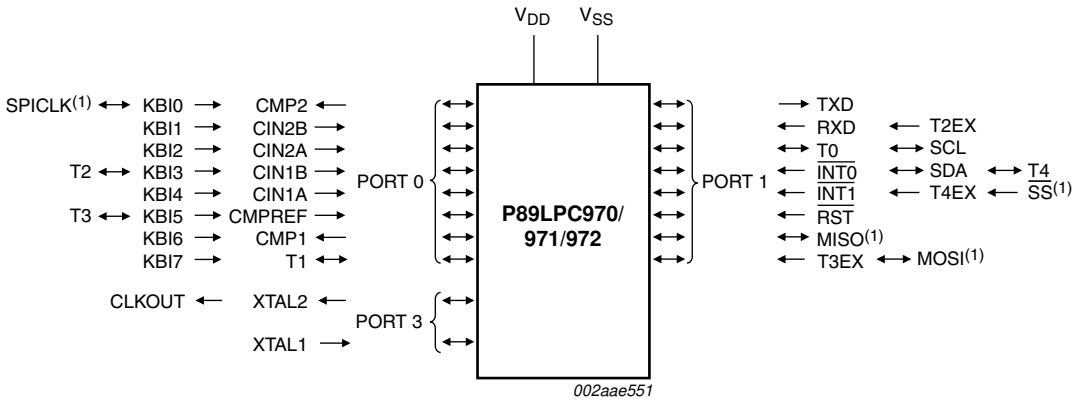
4. Block diagram



(1) For pin remap

Fig 1. Block diagram

5. Functional diagram



(1) For pin remap

Fig 2. Functional diagram

6. Pinning information

6.1 Pinning

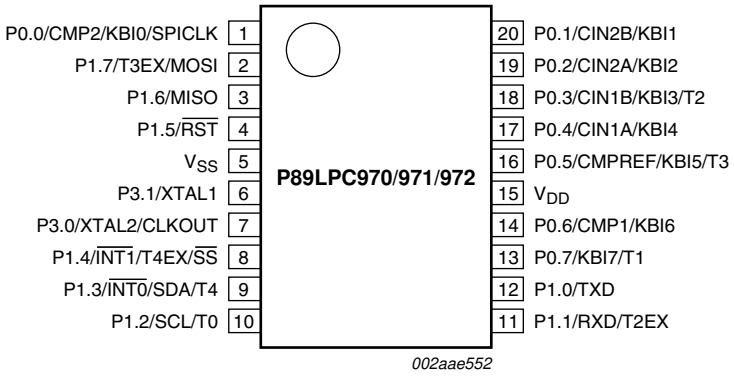


Fig 3. TSSOP20 pin configuration

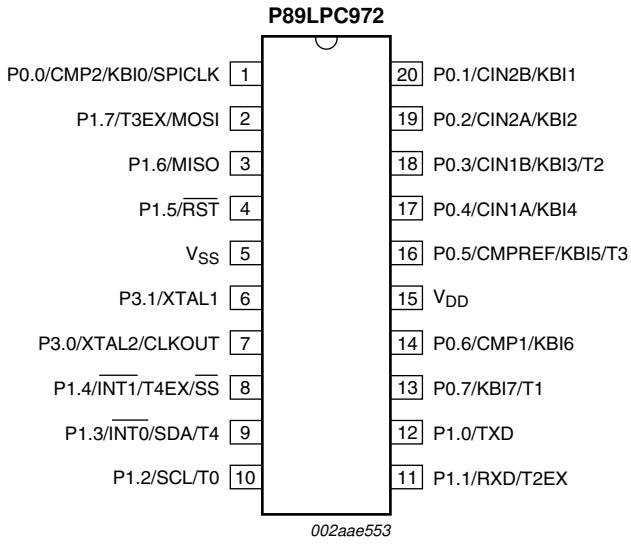


Fig 4. P89LPC972 DIP20 pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
	DIP20, TSSOP20		
P0.0 to P0.7		I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input-only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 "Port configurations" and Table 11 "Static characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt trigger inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/KBI0/ SPICLK	1	I/O	**P0.0** — Port 0 bit 0.
		O	**CMP2** — Comparator 2 output
		I	**KBI0** — Keyboard input 0.
		I/O	**SPICLK** — SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input (pin remap).
P0.1/CIN2B/ KBI1	20	I/O	**P0.1** — Port 0 bit 1.
		I	**CIN2B** — Comparator 2 positive input B.
		I	**KBI1** — Keyboard input 1.
P0.2/CIN2A/ KBI2	19	I/O	**P0.2** — Port 0 bit 2.
		I	**CIN2A** — Comparator 2 positive input A.
		I	**KBI2** — Keyboard input 2.
P0.3/CIN1B/ KBI3/T2	18	I/O	**P0.3** — Port 0 bit 3. High current source.
		I	**CIN1B** — Comparator 1 positive input B.
		I	**KBI3** — Keyboard input 3.
		I/O	**T2** — Timer/counter 2 external count input or overflow output.
P0.4/CIN1A/ KBI4	17	I/O	**P0.4** — Port 0 bit 4. High current source.
		I	**CIN1A** — Comparator 1 positive input A.
		I	**KBI4** — Keyboard input 4.
P0.5/CMPREF/ KBI5/T3	16	I/O	**P0.5** — Port 0 bit 5. High current source.
		I	**CMPREF** — Comparator reference (negative) input.
		I	**KBI5** — Keyboard input 5.
		I/O	**T3** — Timer/counter 3 external count input or overflow output.

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
	DIP20, TSSOP20		
P0.6/CMP1/KBI6	14	I/O	**P0.6 —** Port 0 bit 6. High current source.
		O	**CMP1 —** Comparator 1 output.
		I	**KBI6 —** Keyboard input 6.
P0.7/KBI7/T1	13	I/O	**P0.7 —** Port 0 bit 7. High current source.
		I	**KBI7 —** Keyboard input 7.
		I/O	**T1 —** Timer/counter 1 external count input or overflow output.
P1.0 to P1.7		I/O, I [1]	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input-only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.16.1 “Port configurations” and Table 11 “Static characteristics” for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt trigger inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	12	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Transmitter output for serial port.
P1.1/RXD/T2EX	11	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Receiver input for serial port.
		I	**T2EX —** Timer/counter 2 external capture input.
P1.2/SCL/T0	10	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
		I/O	**SCL —** I^2C-bus serial clock input/output.
		I/O	**T0 —** Timer/counter 0 external count input or overflow output. (open-drain when used as output.)
P1.3/$\overline{INT0}$/SDA/T4	9	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
		I	**$\overline{INT0}$ —** External interrupt 0 input.
		I/O	**SDA —** I^2C-bus serial data input/output.
		I/O	**T4 —** Timer/counter 4 external count input or overflow output.
P1.4/$\overline{INT1}$/T4EX/$\overline{SS}$	8	I/O	**P1.4 —** Port 1 bit 4. High current source.
		I	**$\overline{INT1}$ —** External interrupt 1 input.
		I	**T4EX —** Timer/counter 4 external capture input.
		I	**$\overline{SS}$ —** SPI Slave select input (pin remap).
P1.5/$\overline{RST}$	4	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{RST}$ —** External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode.
P1.6/MISO	3	I/O	**P1.6 —** Port 1 bit 6. High current source.
		I/O	**MISO —** SPI master in slave out. When configured as master, this pin is input, when configured as slave, this pin is output (pin remap).

Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
	DIP20, TSSOP20		
P1.7/T3EX/MOSI	2	I/O	**P1.7 —** Port 1 bit 7. High current source.
		I	**T3EX —** Timer/counter 3 external capture input.
		I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input (pin remap).
P3.0 to P3.1		I/O	**Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input-only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 "Port configurations" and Table 11 "Static characteristics" for details. All pins have Schmitt trigger inputs. Port 3 also provides various special functions as described below:
P3.0/XTAL2/ CLKOUT	7	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration.
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK -TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer.
P3.1/XTAL1	6	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer.
V_{SS}	5	I	**Ground:** 0 V reference.
V_{DD}	15	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

[1] Input/output for P1.0 to P1.4, P1.6, P1.7. Input for P1.5.

7. Functional description

Remark: Please refer to the *P89LPC970/971/972 User manual* for a more detailed functional description.

7.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

Table 4. Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	0000 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00	0000 00x0
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	0000 0000
BRGR0[1]	Baud rate generator 0 rate low	BEH									00	0000 0000
BRGR1[1]	Baud rate generator 0 rate high	BFH									00	0000 0000
BRGCON	Baud rate generator 0 control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[1]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00[2]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00[2]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000

Table 4. Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I²C-bus slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000
		Bit address	**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**	**D8**		
I2CON*	I²C-bus control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I²C-bus data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I²C-bus status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000
		Bit address	**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	0000 0000
		Bit address	**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1*	Interrupt enable 1	E8H	-	EST	-	EXTIM	ESPI	EC	EKBI	EI2C	00[2]	00x0 0000
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00[2]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	PX1H	PT0H	PX0H	00[2]	x000 0000

Table 4. Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	-	PST	-	PXTIM	PSPI	PC	PKBI	PI2C	00[2]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	PXTIMH	PSPIH	PCH	PKBIH	PI2CH	00[2]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[2]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
		Bit address	87	86	85	84	83	82	81	80		
P0*	Port 0	80H	T1/KB7	CMP1/ KB6	CMPREF / KB5/T3	CIN1A/ KB4	CIN1B/ KB3/T2	CIN2A/ KB2	CIN2B/ KB1	CMP2/ KB0	[2]	
		Bit address	97	96	95	94	93	92	91	90		
P1*	Port 1	90H	T3EX	-	$\overline{\text{RST}}$	$\overline{\text{INT1}}$/ T4EX	$\overline{\text{INT0}}$/ SDA/T4	T0/SCL	RXD/ T2EX	TXD	[2]	
		Bit address	B7	B6	B5	B4	B3	B2	B1	B0		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2	[2]	
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[2]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[2]	0000 0000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[2]	11x1 xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[2]	00x0 xx00
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[2]	xxxx xx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[2]	xxxx xx00

Table 4. Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
PCON	Power control register	87H	SMOD1	SMOD0	-	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	I2PD	SPPD	SPD	-	00[2]	0000 0000
PINCON	pin remap control register	CFH	-	-	-	-	-	-	SPI	-	00[2]	0000 0000
PMUCON	Power Management Unit control register	FAH	LPMOD	-	-	-	-	-	-	HCOK		0xxx xxx1
		Bit address	D7	D6	D5	D4	D3	D2	D1	D0		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
PWMD2H	PWM Free Cycle register 2 high byte	AEH									00	0000 0000
PWMD2L	PWM Free Cycle register 2 low byte	AFH									00	0000 0000
PWMD3H	PWM Free Cycle register 3 high byte	E9H									00	0000 0000
PWMD3L	PWM Free Cycle register 3 low byte	EAH									00	0000 0000
PWMD4H	PWM Free Cycle register 4 high byte	AAH									00	0000 0000
PWMD4L	PWM Free Cycle register 4 low byte	ABH									00	0000 0000
RCAP2H	Capture register 2 high byte	FCH									00	0000 0000

Table 4. Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
RCAP2L	Capture register 2 low byte	FBH									00	0000 0000
RCAP3H	Capture register 3 high byte	ECH									00	0000 0000
RCAP3L	Capture register 3 low byte	EBH									00	0000 0000
RCAP4H	Capture register 4 high byte	CAH									00	0000 0000
RCAP4L	Capture register 4 low byte	C9H									00	0000 0000
RSTSRC	Reset source register	DFH	-	BOIF	BORF	POF	R_KB	R_WD	R_SF	R_EX	[3]	
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[2][4]	011x xx00
RTCH	RTC register high	D2H									00[4]	0000 0000
RTCL	RTC register low	D3H									00[4]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial port data buffer register	99H									xx	xxxx xxxx
		Bit address	**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100

Table 4. Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0
		Bit address	**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
T2CON	Timer/Counter 2 control	FFH	PSEL2	ENT2	TIEN2	PWM2	EXEN2	TR2	C/NT2	CP/NRL2	00	0000 0000
TH2	Timer/Counter 2 high byte	FEH									00	0000 0000
TL2	Timer/Counter 2 low byte	FDH									00	0000 0000
T3CON	Timer/Counter 3 control	EFH	PSEL3	ENT3	TIEN3	PWM3	EXEN3	TR3	C/NT3	CP/NRL3	00	0000 0000
TH3	Timer/Counter 3 high byte	EEH									00	0000 0000
TL3	Timer/Counter 3 low byte	EDH									00	0000 0000
T4CON	Timer/Counter 2 control	CDH	PSEL4	ENT4	TIEN4	PWM4	EXEN4	TR4	C/NT4	CP/NRL4	00	0000 0000

Table 4. Special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
TH4	Timer/Counter 4 high byte	CCH									00	0000 0000
TL4	Timer/Counter 4 low byte	CBH									00	0000 0000
TINTF	Timer/Counters 2/3/4 overflow and external flags	CEH	-	-	TF4	EXF4	TF3	EXF3	TF2	EXF2	00	0000 0000
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[4][5]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4][6]	
WDL	Watchdog load	C1H									FF	1111 1111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[2] All ports are in input only (high-impedance) state after power-up.

[3] The RSTSRC register reflects the cause of the P89LPC970/971/972 reset except BOIF bit. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is x011 0000.

[4] The only reset sources that affect these SFRs are power-on reset and watchdog reset.

[5] On power-on reset and watchdog reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

Table 5. Extended special function registers[1]

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
BODCFG	BOD configuration register	FFC8H	-	-	-	-	-	BOICFG2	BOICFG1	BOICFG0	[2]	
CLKCON	Clock control register	FFDEH	CLKOK	-	WDMOD	XTALWD	CLKDBL	FOSC2	FOSC1	FOSC0	[3]	1000 xxxx
CMPREF	Comparator reference register	FFCBH	-	REFS5	REFS4	REFS3	-	REFS2	REFS1	REFS0	00	0000 0000
RTCDATH	Real-time clock data register high	FFBFH									00	0000 0000
RTCDATL	Real-time clock data register low	FFBEH									00	0000 0000

[1] Extended SFRs are physically located on-chip but logically located in external data memory address space (XDATA). The MOVX A,@DPTR and MOVX @DPTR,A instructions are used to access these extended SFRs.

[2] The BOICFG2/1/0 will be copied from UCFG1.5 to UCFG1.3 when power-on reset.

[3] CLKCON register reset value comes from UCFG1. The reset value of CLKCON.2 to CLKCON.0 come from UCFG1.2 to UCFG1.0 and reset value of CLKDBL bit comes from UCFG1.7.

7.2 Enhanced CPU

The P89LPC970/971/972 uses an enhanced 80C51 CPU which runs at six times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

7.3 Clocks

7.3.1 Clock definitions

The P89LPC970/971/972 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 5) and can also be optionally divided to a slower frequency (see Section 7.11 “CCLK modification: DIVM register”).

Remark: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output. The clock doubler option, when enabled, provides an output frequency of 14.746 MHz.

PCLK — Clock for the various peripheral devices and is $^{CCLK}/_{2}$.

7.3.2 CPU clock (OSCCLK)

The P89LPC970/971/972 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the flash is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source.

7.4 Crystal oscillator option

The crystal oscillator option can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 18 MHz. It can be the clock source of OSCCLK and RTC. The low speed oscillator option can be the clock source of the WDT.

7.4.1 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

7.4.2 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

7.4.3 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration.

7.5 Clock output

The P89LPC970/971/972 supports a user-selectable clock output function on the P3.0/XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on XTAL1) and if the RTC and WDT are not using the crystal oscillator as their clock source. This allows external devices to synchronize to the P89LPC970/971/972. This output is enabled by the ENCLK bit in the TRIM register.

The frequency of this clock output is $^1/_2$ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

7.6 On-chip RC oscillator option

The P89LPC970/971/972 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory preprogrammed value to adjust the oscillator frequency to 7.373 MHz ± 1 % at room temperature. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies. When the clock doubler option is enabled (UCFG2.7 = 1), the output frequency is 14.746 MHz. If CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to reduce power consumption. On reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower. When clock doubler option is enabled, BOE0 to BOE2 bits (UCFG1[3:5]) are required to hold the device in reset at power-up until V_{DD} has reached its specified level.

7.7 Watchdog oscillator option

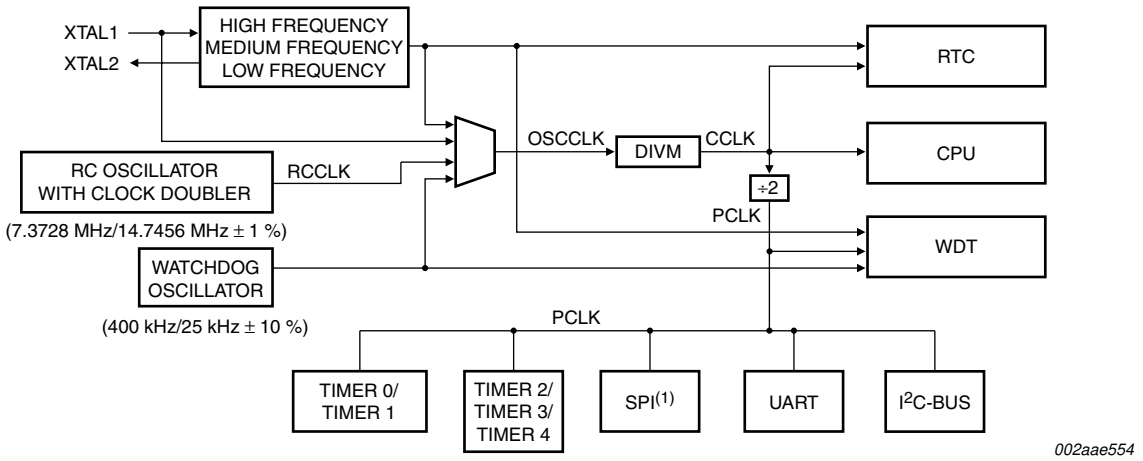
The watchdog has a separate oscillator which provides two options: 400 kHz and 25 kHz. It is calibrated to ±10 % at 400 kHz. The oscillator can be used to save power when a high clock frequency is not needed.

7.8 External clock input option

In this configuration, the processor clock is derived from an external source driving the P3.1/XTAL1 pin. The rate may be from 0 Hz up to 18 MHz. The P3.0/XTAL2/CLKOUT pin may be used as a standard port pin or a clock output. When using an oscillator frequency above 12 MHz, BOE0 to BOE2 bits (UCFG1[3:5]) are required to hold the device in reset at power-up until V_{DD} has reached its specified level.

7.9 Clock source switching on the fly

P89LPC970/971/972 can implement clock switching on any sources of watchdog oscillator, 7 MHz/14 MHz internal RC oscillator, crystal oscillator and external clock input during code is running. CLKOK bit in CLKCON register is used to indicate the clock switch status. CLKOK is cleared when starting clock source switch and set when completed. Notice that when CLKOK is ‘0’, writing to CLKCON register is not allowed.



(1) ±10 % at 400 kHz.

Fig 5. Block diagram of oscillator control

7.10 CCLK wake-up delay

The P89LPC970/971/972 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 1024 OSCCLK cycles plus 60 μs to 100 μs. If the clock source is the internal RC oscillator, the delay is 200 μs to 300 μs. If the clock source is watchdog oscillator or external clock, the delay is 32 OSCCLK cycles.

7.11 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

7.12 Low power select

The P89LPC970/971/972 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to lower the power consumption further. On any reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

7.13 Memory organization

The various P89LPC970/971/972 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- XDATA

  'External' Data or Auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the DPTR, R0, or R1. All or part of this space could be implemented on-chip.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC970/971/972 has 4 kB/8 kB of on-chip Code memory.

7.14 Data RAM arrangement

The 768 bytes of on-chip RAM are organized as shown in Table 6.

Table 6. On-chip data memory usages

Type	Data RAM	Size (bytes)
DATA	Memory that can be addressed directly and indirectly	128
IDATA	Memory that can be addressed indirectly	256
XDATA	Auxiliary (External Data) on-chip memory that is accessed using the MOVX instructions	256

7.15 Interrupts

The P89LPC970/971/972 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC970/971/972 supports 15 interrupt sources: external interrupts 0 and 1, Timers 0 and 1, Timer 2/3/4, serial port TX, serial port RX, combined serial port RX/TX, brownout detect, watchdog/RTC, I^2C-bus, keyboard, comparators 1 and 2, SPI.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1 and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but

not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

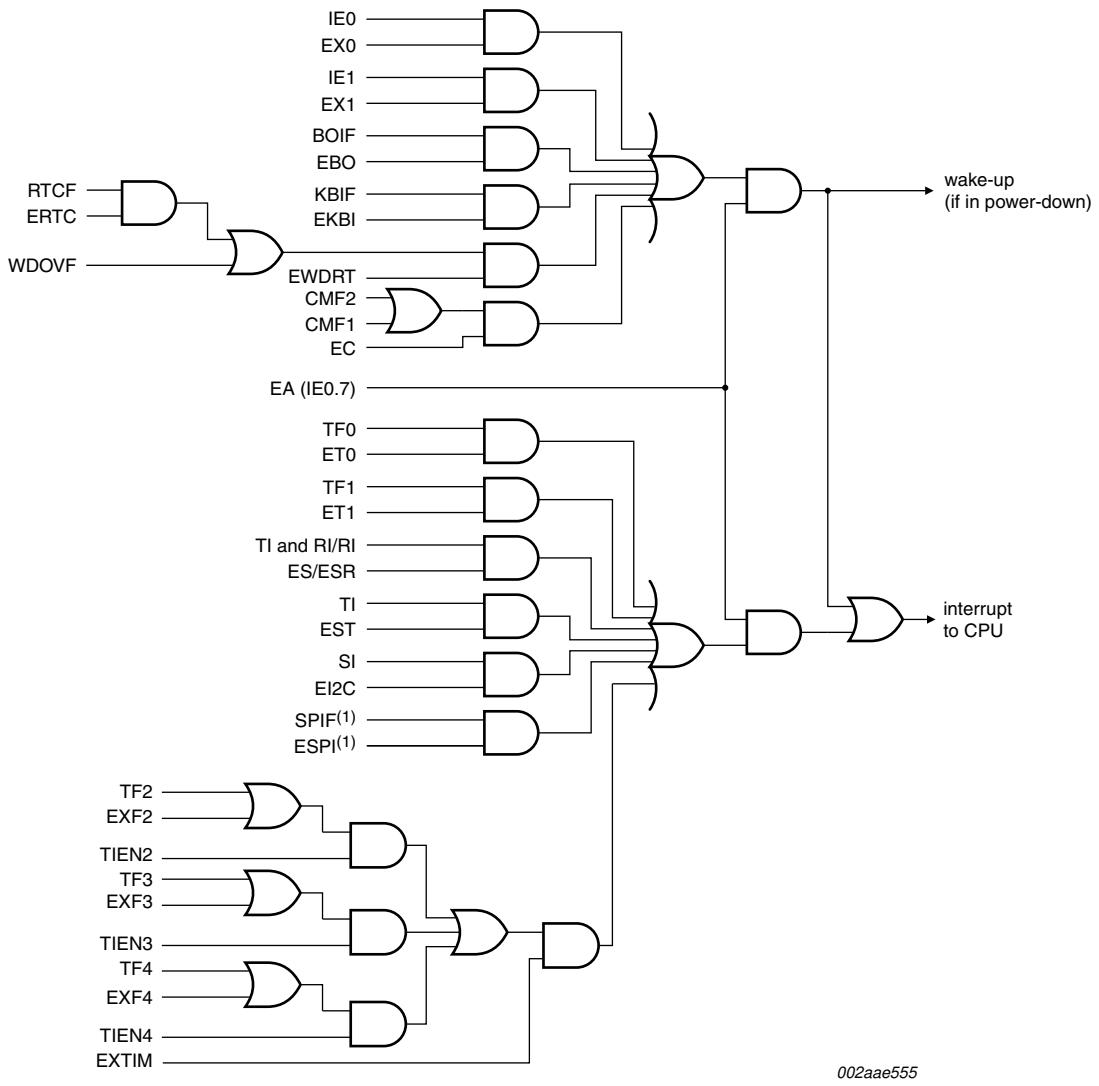
7.15.1 External interrupt inputs

The P89LPC970/971/972 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode, if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC970/971/972 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 7.17.3 “Power reduction modes” for details.



(1) For pin remap.

Fig 6. Interrupt sources, interrupt enables, and power-down wake-up sources

7.16 I/O ports

The P89LPC970/971/972 has four I/O ports: Port 0, Port 1 and Port 3. Ports 0, 1 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depends upon the clock and reset options chosen, as shown in Table 7.

Table 7. Number of I/O pins available

Clock source	Reset option	Number of I/O pins (20-pin package)
On-chip oscillator or watchdog oscillator	no external reset (except during power-up)	18
	external $\overline{\text{RST}}$ pin supported	17
External clock input	no external reset (except during power-up)	17
	external $\overline{\text{RST}}$ pin supported	16
Low/medium/high speed oscillator (external crystal or resonator)	no external reset (except during power-up)	16
	external $\overline{\text{RST}}$ pin supported	15

7.16.1 Port configurations

All but three I/O port pins on the P89LPC970/971/972 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

1. P1.5/$\overline{\text{RST}}$ can only be an input and cannot be configured.
2. P1.2/SCL/T0 and P1.3/$\overline{\text{INT0}}$/SDA/T4 may only be configured to be either input-only or open-drain.

7.16.1.1 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

A quasi-bidirectional port pin has a Schmitt trigger input that also has a glitch suppression circuit.

7.16.1.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt trigger input that also has a glitch suppression circuit.