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Description

The P9242-R is a highly integrated, magnetic induction, wireless power transmitter supporting up to 15W. The system-on-chip operates with an input voltage range of 4.25V to 21V.

The transmitter includes an industry-leading 32-bit ARM® Cortex®-M0 processor offering a high level of programmability while consuming extremely low standby power. The P9242-R features two LED outputs with pre-defined user-programmable blinking patterns, buzzer, and programmable over-current protection supporting a wide range of applications. The I²C serial communication allows the user to read information such as voltage, current, frequency, and fault conditions. The P9242-R includes an under-voltage lockout and thermal management circuit to safe guard the device under fault conditions. Together with the P9221-R receiver (Rx), the P9242-R is a complete wireless power system solution.

The P9242-R is available in a lead-free, space-saving 48-VFQFN package. The product is rated for a -40°C to +85°C operating temperature range.

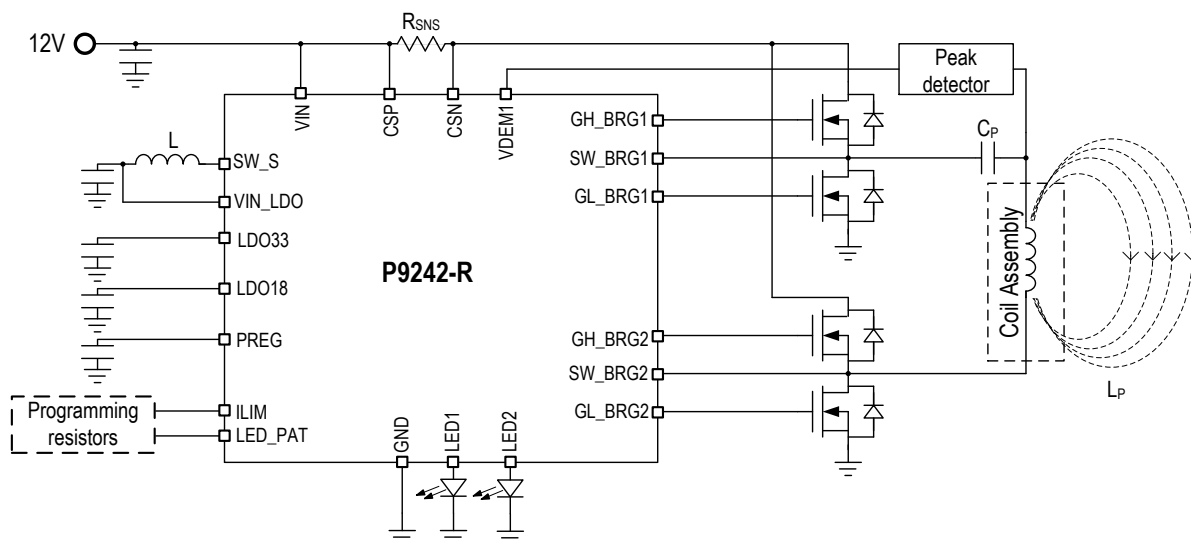
Typical Applications

- Charging pad
- Accessories
- Cradle
- Tablets

Features

- Power transfer up to 15W
- Wide input voltage range: 4.25V to 21V
- WPC-1.2.2 compliant, MP-A2 coil configuration
- Integrated step-down switching regulator
- Embedded 32-bit ARM® Cortex®-M0 processor
- Integrated drivers for external power FETs
- Simultaneous voltage and current demodulation scheme for communication
- Integrated current sense amplifier
- Low standby power
- Dedicated remote temperature sensing
- Programmable current limit
- Power transfer LED indicator
- Foreign objects detection (FOD)
- Pre-defined user-programmable LED pattern
- Active-LOW enable pin for electrical on/off
- Over-current and over-temperature protection
- Supports I²C interface
- -40 to +85°C ambient operating temperature range
- 48-VFQFN (6 × 6 mm) RoHS-compliant package

Basic Application Circuit



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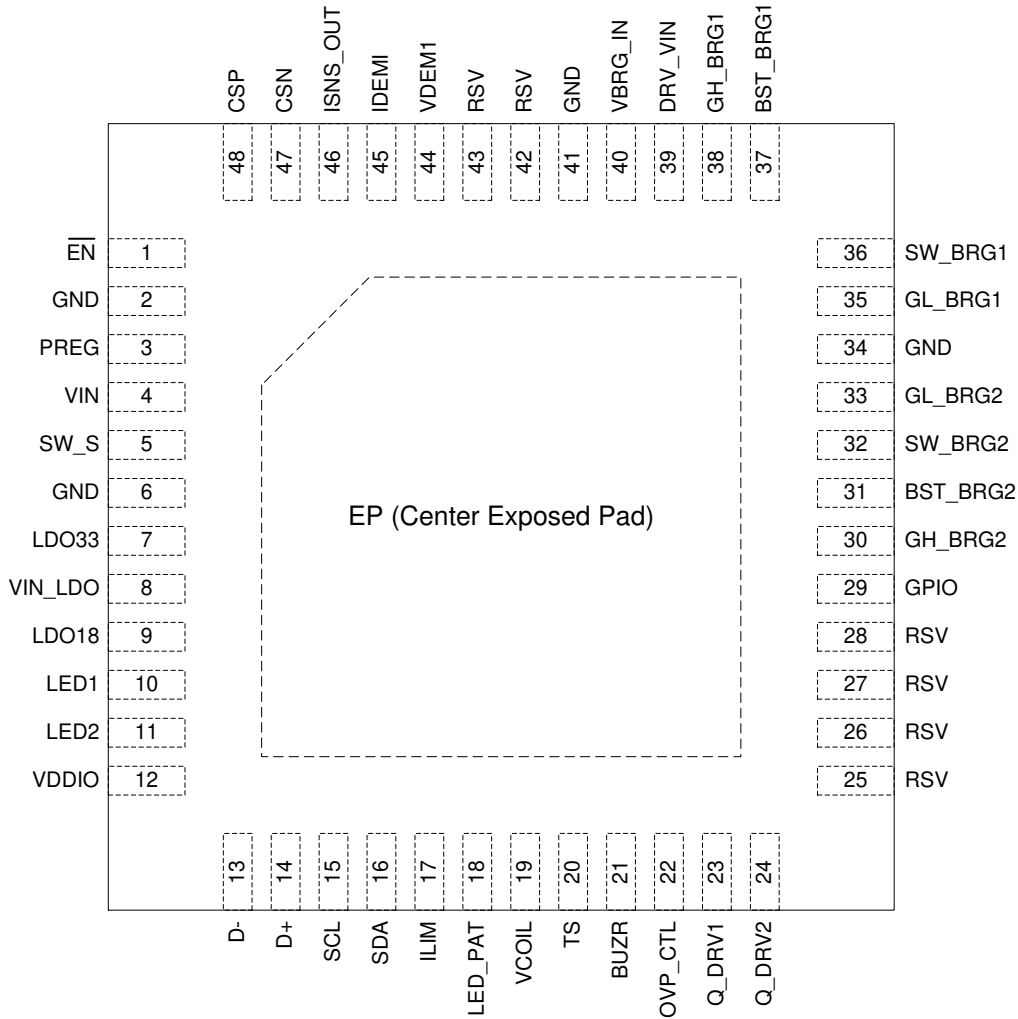
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1. Pin Assignments

Figure 1. Pin Assignments



2. Pin Descriptions

Table 1. Pin Descriptions

Pins	Name	Type	Function
1	EN	Input	Active-LOW enable pin. When connected to logic HIGH, the P9242-R enters the Shut Down Mode, which has a typical current consumption of 25 μ A. When connected to logic LOW, the device is in normal operation.
2, 6, 34, 41, EP	GND	–	Ground connection.
3	PREG	Output	Regulated 5V output used for internal device biasing. Connect a 1 μ F capacitor from this pin to ground. This pin must not be externally loaded.
4	VIN	Input	Input power supply. Connect a 10 μ F capacitor from this pin to ground.
5	SW_S	Output	Step-down regulator's switch node. Connect one of the terminals of the 4.7 μ H inductor to this pin.
7	LDO33	Output	Regulated 3.3V output used for internal device biasing. Connect a 1 μ F capacitor from this pin to ground. This pin should not be externally loaded.
8	VIN_LDO	Input	Linear regulator input power supply. Connected this pin to the 5V output of the step-down regulator.
9	LDO18	Output	Regulated 1.8V output used for internal device biasing. Connect a 1 μ F capacitor from this pin to ground. This pin should not be externally loaded.
10	LED1	Input	Open-drain output. Connect an LED to this pin
11	LED2		Open-drain output. Connect an LED to this pin.
12	VDDIO	Input	Input power supply for internal biasing. This pin must be connected to LDO33.
13	D-	Input	Logic I/O for USB travel adaptor detection.
14	D+	Input	Logic I/O for USB travel adaptor detection.
15	SCL	Input	I ² C interface clock input. Connect a 5.1k Ω pull-up resistor to LDO33 rail.
16	SDA	I/O	I ² C interface data input and data output, connect a 5.1k Ω pull-up resistor to LDO33 rail.
17	ILIM	Input	Programmable over-current limit pin. Connect the center tap of the resistor divider to this pin to set the current-limit threshold. For more information, see section 7.1.
18	LED_PAT	Input	Programmable LED pattern selection. Connect the center tap of the resistor divider to this pin. For more information on various LED blinking patterns, see section 7.8.
19	VCOIL	Input	Input for coil voltage sensing.
20	TS	Input	Remote temperature sensor for over-temperature shutdown. Connect to the NTC thermistor network. If not used, connect to the LDO33 pin through the 10k Ω resistor.
21	BUZR	Output	Buzzer output. Connect a buzzer to this pin.
22	OVP_CTL	I/O	Logic HIGH during power transfer phase used to scale down the voltage to detect over-voltage for VCOIL pin.
23	Q_DRV1	I/O	Control signal for Q factor measurement circuit.
24	Q_DRV2	I/O	Control signal for Q factor measurement circuit.

Pins	Name	Type	Function
25, 26, 27, 28, 42, 43	RSV	Output	Reserved for internal use. Do not connect.
29	GPIO	I/O	General purpose digital I/O pin.
30	GH_BRG2	Output	Gate driver output for the high-side FET of half bridge 2. Connect this pin to a series 12Ω resistor to the respective bridge FET gate.
31	BST_BRG2	Input	Bootstrap pin for half bridge 2. Tie an external capacitor from this pin to the SW_BRG2 pin to generate a drive voltage higher than the input voltage.
32	SW_BRG2	Output	Switch node for half bridge 2.
33	GL_BRG2	Output	Gate driver output for the low-side FET of half bridge 2. Connect this pin to a series 12Ω resistor to the respective bridge FET gate.
35	GL_BRG1	Output	Gate driver output for the low-side FET of half bridge 1. Connect this pin to a series 12Ω resistor to the respective bridge FET gate.
36	SW_BRG1	Output	Switch node for half bridge 1.
37	BST_BRG1	Output	Bootstrap pin for half bridge 1. Tie an external capacitor from this pin to the SW_BRG1 to generate a drive voltage higher than the input voltage.
38	GH_BRG1	Output	Gate driver output for the high-side FET of half bridge 1. Connect this pin to a series 12Ω resistor to the respective bridge FET gate.
39	DRV_VIN	Input	Input power supply for the internal gate drivers. Connect a 10μF capacitor from this pin to ground.
40	VBRG_IN	Input	Bridge voltage input sense.
44	VDEM1	Input	High-pass filter input. Voltage demodulation pin for data packets based on coil voltage variation; transmitted by power receiver.
45	IDEMI	Input	High-pass filter input. Current demodulation pin for data packets based on coil current variation; transmitted by power receiver.
46	ISNS_OUT	Output	Input current sense output.
47	CSN	Input	Low-side input current sense (VBRIDGE).
48	CSP	Input	High-side input current sense (VIN).

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses beyond those listed under “Absolute Maximum Ratings” might cause permanent damage to the P9242-R. Functional operation of the P9242-R at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions for extended periods could affect long-term reliability.

Table 2. Absolute Maximum Ratings

Pins ^[a]	Rating ^[b]	Units
\overline{EN} , VIN, SW_S, VBRG_IN, SW_BRG1, SW_BRG2, CSP, CSN, BST_BRG1, BST_BRG2, GH_BRG1, GH_BRG2	-0.3 to 28	V
PREG, LDO33, VIN_LDO, LED1, LED2, VDDIO, SCL, SDA, ILIM, LED_PAT, VCOIL, TS, BUZR, OVP_CTL, GPIO, D-, D+, Q_DRV1, Q_DRV2, GL_BRG1, GL_BRG2, VDEM1, IDEMI, ISNS_OUT, DRV_VIN	-0.3 to 6	V
LDO18	-0.3 to 2	V

[a] Absolute maximum ratings are not provided for reserved pins (RSV). These pins are not used in the application.

[b] All voltages are referred to ground unless otherwise noted. All GND pins and the exposed pad (EP) connected together.

Table 3. Package Thermal Information

Symbol	Description	VFQFN Rating	Units
θ_{JA}	Thermal Resistance Junction to Ambient ^{[a], [b], [c]}	27.2	°C/W
θ_{JC}	Thermal Resistance Junction to Case ^{[b], [c]}	18.8	°C/W
θ_{JB}	Thermal Resistance Junction to Board ^{[b], [c]}	1.36	°C/W
T_J	Operating Junction Temperature ^{[a], [b]}	-40 to +125	°C
T_A	Ambient Operating Temperature ^{[a], [b]}	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

[a] The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

[b] This thermal rating was calculated on a JEDEC 51-standard 4-layer board with the dimensions 76.2 x 114.3 mm in still air conditions.

[c] Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Table 4. ESD Information

Test Model	Pins	Ratings	Units
HBM	All pins.	±2000	V
CDM	All pins.	±500	V

4. Electrical Characteristics

Table 5. Electrical Characteristics

 Note: $V_{IN} = 5V$, $\overline{EN} = \text{LOW}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at 25°C .

Symbol	Description	Conditions/Notes	Min	Typical	Max	Units
Input Supplies and UVLO						
V_{IN}	Input Operating Range ^[a]		4.25		21	V
V_{IN_UVLO}	Under-Voltage Lockout	V_{IN} rising		4.0		V
V_{IN_UVHYS}	Under-Voltage Hysteresis	V_{IN} falling		0.5		V
I_{IN}	Operating Mode Input Current	Power transfer phase, $V_{in} = 12V$		10		mA
I_{STD_BY}	Standby Mode Current	Periodic ping		1		mA
I_{SHD}	Shut Down Current	$\overline{EN} = V_{IN} = 21V$		25	80	μA
Enable Pin Threshold (\overline{EN})						
V_{IH}	Input Threshold HIGH		2.5			V
V_{IL}	Input Threshold LOW				0.5	V
I_{EN_LKG}	\overline{EN} Pin Input Leakage Current	$V_{\overline{EN}} = 0V$	-1		1	μA
		$V_{\overline{EN}} = 5V$		2.5		μA
Step-Down Regulator^[b] with $C_{OUT} = 33\mu\text{F}$; $L = 4.7\mu\text{H}$						
V_{OUT}	Step-Down Output Voltage	$V_{in} = 12V$	4.5	5	5.5	V
N-Channel MOSFET Drivers						
$t_{LS_ON_OFF}$	Low-Side Gate Driver Rise and Fall Times	$C_{LOAD} = 3nF$; 10% to 90%, 90% to 10%		50	150	ns
$t_{HS_ON_OFF}$	High-Side Gate Driver Rise and Fall Times	$C_{LOAD} = 3nF$; 10% to 90%, 90% to 10%		150	300	ns
Input Current Sense						
V_{SEN_OFST}	Amplifier Output Offset Voltage	Measured at the ISNS_OUT pin; $V_{CSP} = V_{CSN}$		0.6		V
$I_{SEN_ACC_TYP}$ ^[c]	Measured Current Sense Accuracy	$V_{R_ISEN} = 25mV$, $I = 1.25A$		± 3.5		%
Analog to Digital Converter						
N	Resolution			12		Bit
Channel	Number of Channels			10		
V_{IN_FS}	Full Scale Input Voltage			2.4		V

Symbol	Description	Conditions/Notes	Min	Typical	Max	Units
LDO18^[b]						
V _{LDO18}	1.8V LDO Regulator	C _{OUT} = 1μF, V _{VIN_LDO} = 5.5V	1.71	1.8	1.89	V
LDO33^[b]						
V _{LDO33}	3.3V LDO Regulator	C _{OUT} = 1μF, V _{VIN_LDO} = 5.5V	3.15	3.3	3.45	V
PREG						
V _{PREG}	5V LDO Regulator			5		V
Thermal Shutdown						
T _{SD}	Thermal Shutdown	Threshold rising		140		°C
		Threshold falling		120		°C
Analog Input Pins Input Current Leakage (TS, VCOIL)						
I _{LKG}	Leakage Current		-1		1	μA
Open-Drain Pins Output Logic Levels (LED1, LED2, SCL, SDA)						
V _{OH}	Output Logic HIGH		4			V
V _{OL}	Output Logic LOW	I = 8mA			0.5	V
Digital Input/Output Pins Logic Levels						
V _{IH}	Input Voltage HIGH Level		0.7*VDDIO			V
V _{IL}	Input Voltage LOW Level				0.3*VDDIO	V
I _{LKG}	Leakage Current				1	μA
V _{OH}	Output Logic HIGH	I = 8mA, VDDIO = 3.3V	2.4			V
V _{OL}	Output Logic LOW	I = 8mA, VDDIO = 3.3V			0.5	V
I²C Interface (SCL, SDA)						
f _{SCL_SLV}	Clock Frequency	As I ² C slave			400	kHz
C _B	Capacitive Load	For each bus line			100	pF
C _{BIN}	SCL, SDA Input Capacitance			5		pF
I _{LKG}	Input Leakage Current	V = GND and 3.3V	-1		1	μA

[a] The input voltage operating range is dependent upon the type of transmitter power stage (full-bridge, half-bridge) and transmitting coil inductance. WPC specifications should be consulted for appropriate input voltage ranges by end-product type.

[b] Do not externally load. For internal biasing only.

[c] A 20mΩ, 1% or better sense resistor and a 4.7Ω, 1% input filter resistor are required to meet the FOD specification.

5. Typical Performance Characteristics

$V_{IN} = 12.0V$; $\overline{EN} = LOW$. The following performance characteristics were taken using a P9221-R, 15W Wireless Power Receiver (RX) at $T_A = +25^\circ C$ unless otherwise noted.

Figure 2. Efficiency vs. Output Load: $V_{OUT_RX} = 12V$

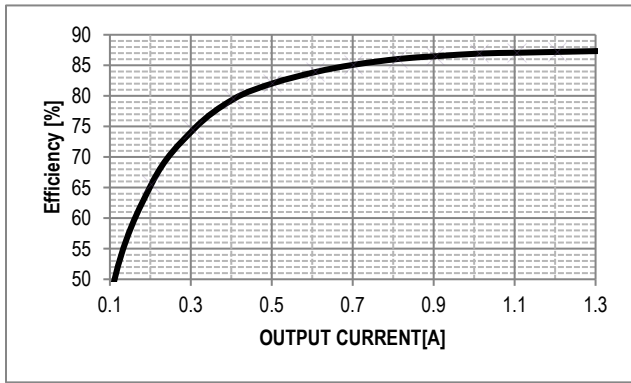


Figure 3. Efficiency vs. Output Load: $V_{OUT_RX} = 9V$

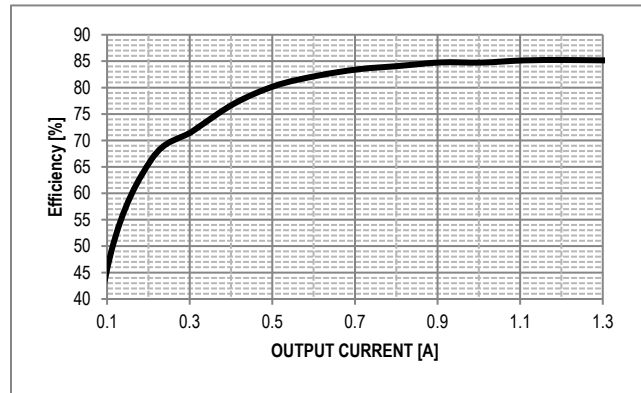


Figure 4. Efficiency vs. Output Load: $V_{OUT_RX} = 5V$

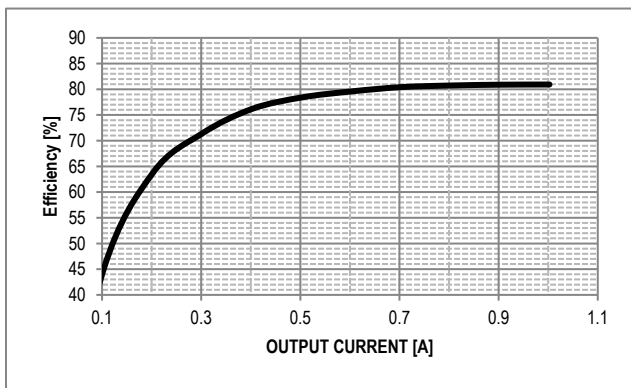


Figure 5. Load Regulation vs. Output Load: V_{CC_5V} in schematic Figure 24

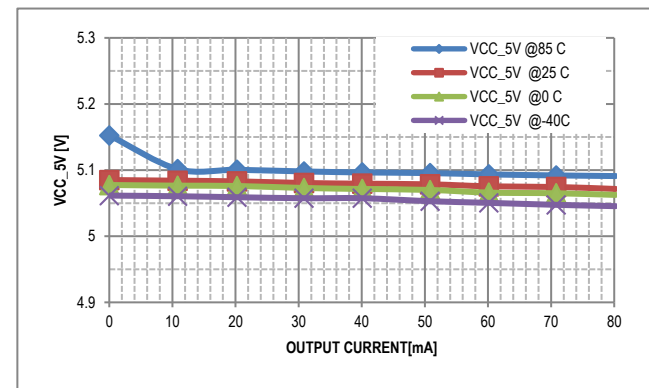


Figure 6. Load Regulation vs. Output Load: LDO33

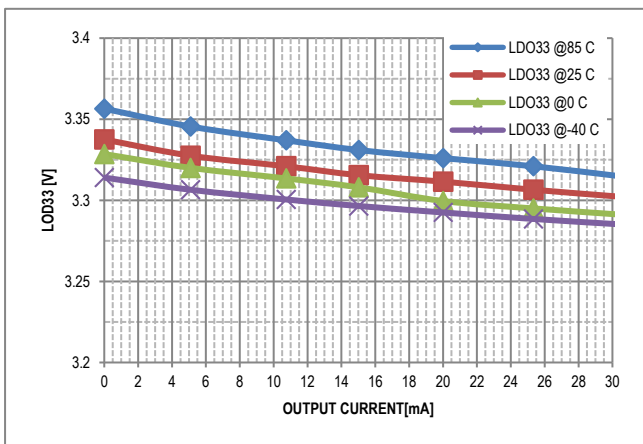


Figure 7. Load Regulation vs. Output Load: LDO18

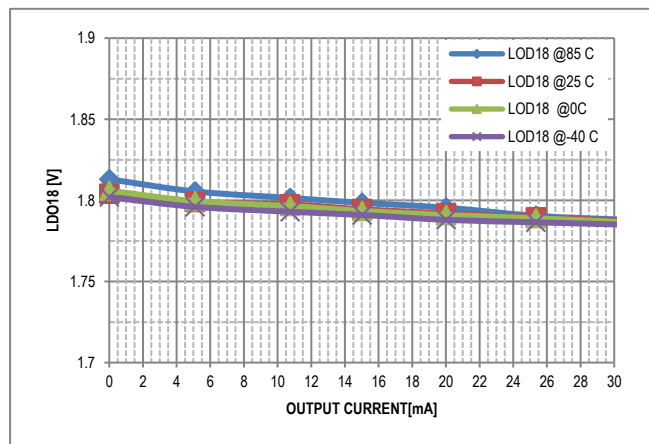


Figure 8. Over-Current Limit vs. V_{ILIM}

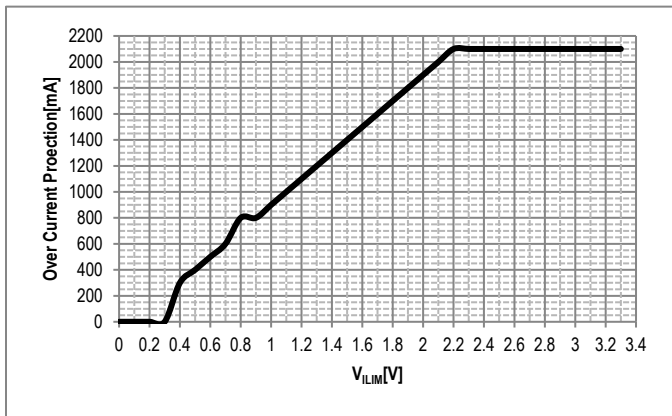


Figure 9. Voltage and Current Signal for Demodulation

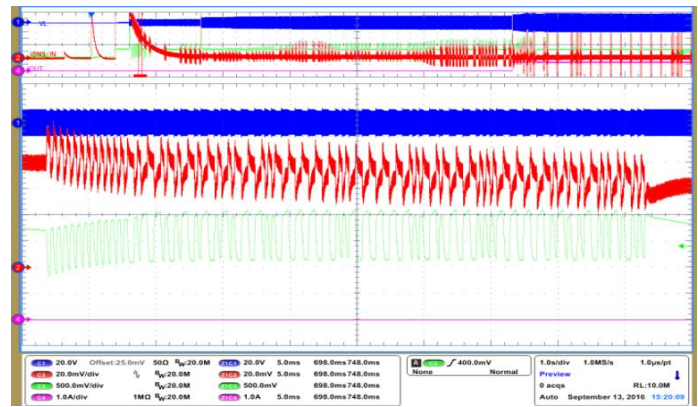


Figure 10. Enable Startup

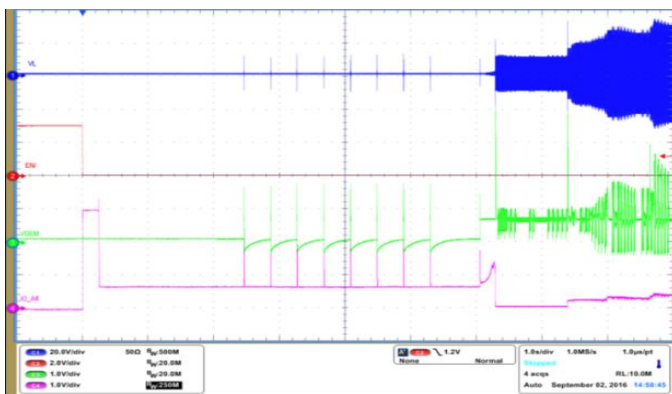


Figure 11. Communication Packet during Rx Load Step from 0 to 1.3A

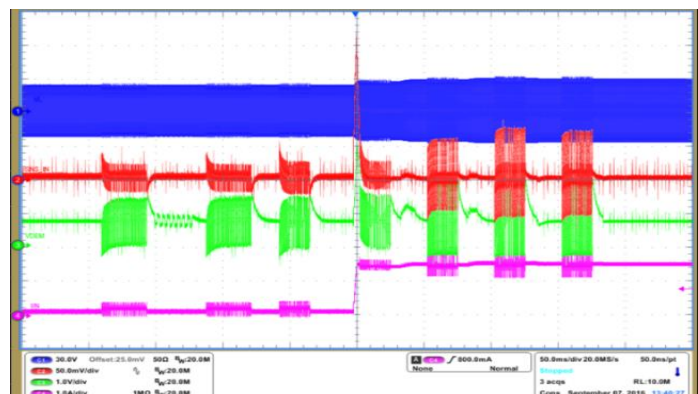
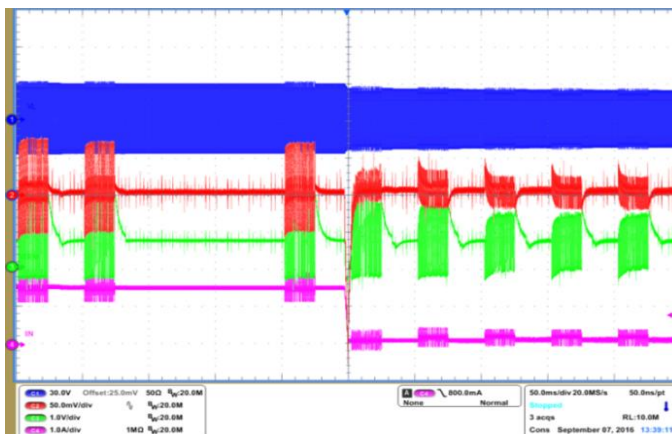
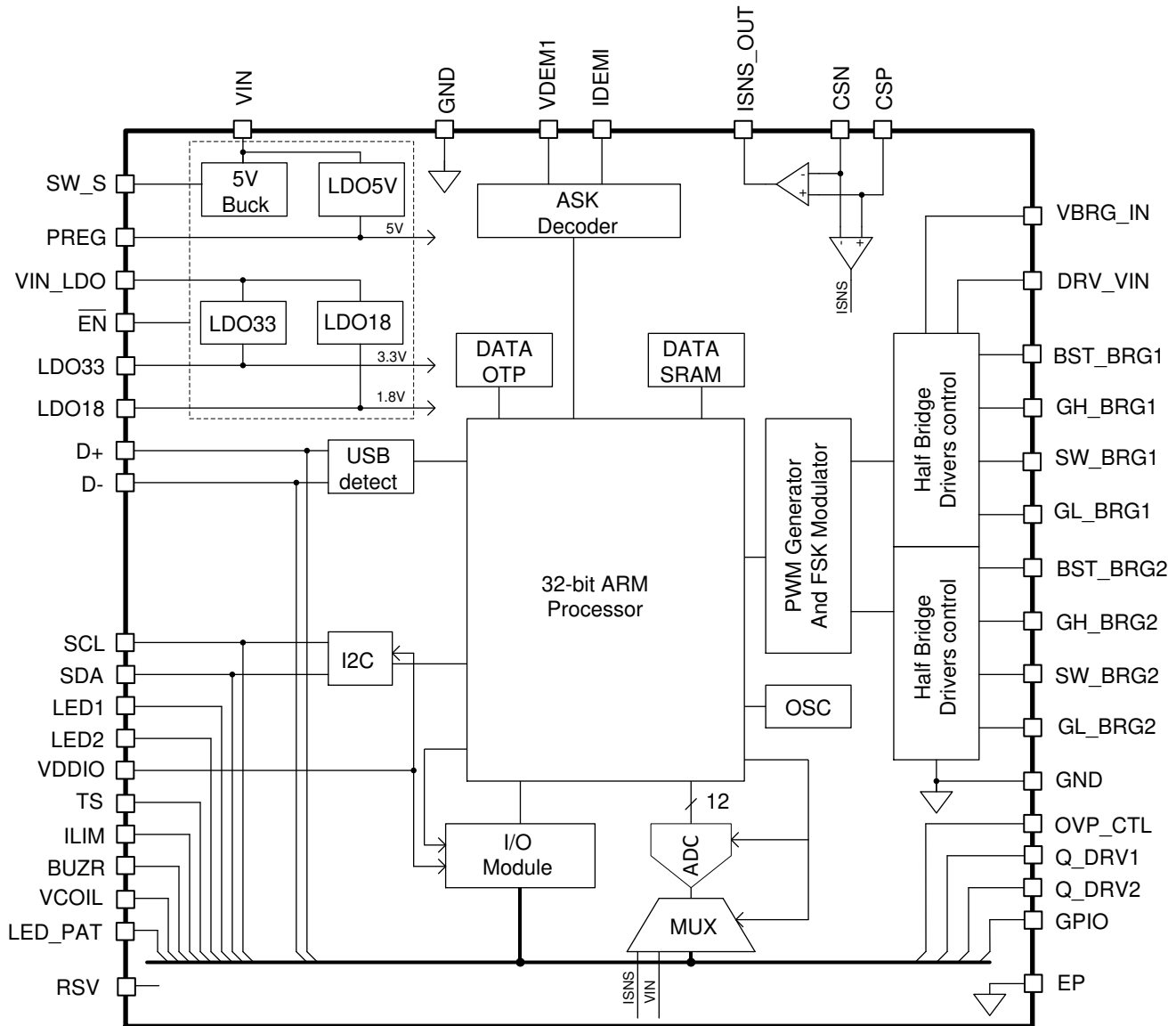


Figure 12. Communication Packet during Rx Load Step from 1.3A to 0



6. Function Block Diagram

Figure 13. Functional Block Diagram



7. Theory of Operation

A wireless power charging system has a base station with one or more transmitters that make power available via DC-to-AC inverter(s) and transmit the power over a strongly-coupled inductor pair to a receiver in a mobile device. The amount of power transferred to the mobile device is controlled by the wireless power receiver by sending communication packets to the transmitter to increase, decrease, or maintain the power level. The communication from receiver to transmitter is purely digital and consists of 1's and 0's that ride on top of the power link that exists between the transmitter (TX) and receiver (RX) coil. Communication from transmitter to receiver is achieved by frequency shift keying (FSK) modulation over the power signal frequency and amplitude shift keying (ASK) is used for the communication protocol from receiver to transmitter.

A feature of the wireless charging system is the fact that when it is not delivering power, the transmitter is in Standby Mode. The transmitter remains in Standby Mode and periodically pings until it detects the presence of a receiver. Once an Extended Power Profile Receiver is detected, such as the P9221-R or equivalent, the transmitter will provide with up to 15W of output power. If a Baseline Power Profile Receiver is present, the transmitter will deliver only up to 5W of output power.

The P9242-R contains features that ensure a high level of functionality and compliance with the WPC requirements, such as a power path that efficiently achieves power transfer, a simple and robust communication demodulation circuit, safety and protection circuits, configuration, and status indication circuits.

7.1 Over-Current Limit – ILIM

The over-current protection (OCP) is designed to protect the half-bridge and wireless receiver unit from becoming exposed to operating conditions that could potentially cause damage or unexpected behavior from the system. The input current is continuously monitored during the power transfer stage. If the input current goes above the OCP threshold of 2.1A (typical), the P9242-R will increase the switching frequency or reduce the duty cycle in order to keep the input current below the OCP value.

7.2 Enable Pin – $\overline{\text{EN}}$

The P9242-R can be disabled by applying a logic HIGH to the $\overline{\text{EN}}$ pin. When the voltage on the $\overline{\text{EN}}$ pin is pulled high, operation is suspended and the P9242-R is placed in the low-current Shut Down Mode. If pulled low, the P9242-R is active.

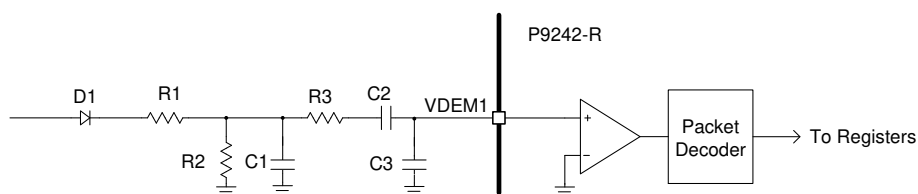
7.3 Buzzer – BUZR

An optional AC-type ceramic buzzer can be connected between the BUZR pin to GND through a current limiting resistor. A short 4kHz “chirp” sound will indicate when the object is detected. Do not connect this pin if the buzzer function is not desired.

7.4 Voltage Demodulation – VDEM1

In order to increase the communication reliability in any load condition, the P9242-R has integrated two demodulation schemes, one based on coil current information and the other based on coil voltage modulation. The voltage mode envelope detector is implemented using a discrete solution as depicted on Figure 14. This simple implementation achieves the envelope detector function low-pass filter as well as the DC filter function.

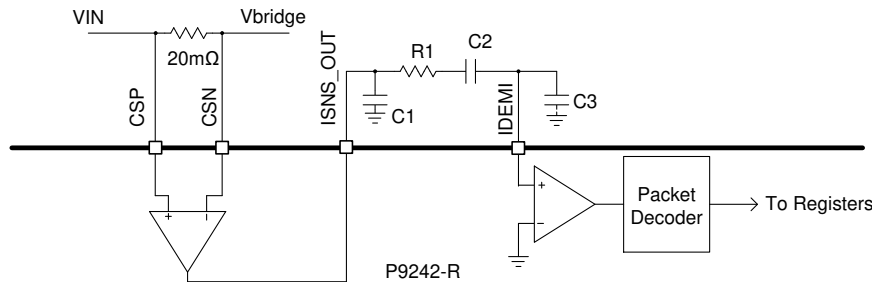
Figure 14. Voltage Mode Envelope Detector



7.5 Current Demodulation – IDEMI

The current-mode detector takes the modulation information from the current sense resistor, which carries the coil current modulation information in addition to the averaged input current. There is an additional discrete low-pass filter and DC filter between the ISNS_OUT and IDEMI pins. The packet decoder block is shared between the voltage-mode and current-mode detectors. The packet decoder selects either voltage-mode or current-mode signals depending upon which produces the best demodulated signal.

Figure 15. Current Mode Envelope Detector



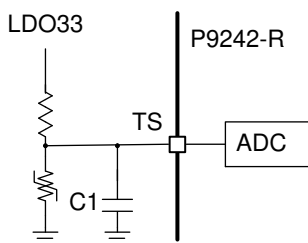
7.6 Thermal Protection

The P9242-R integrates thermal shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down or reset the P9242-R if the die temperature exceeds a threshold to prevent damage resulting from excessive thermal stress that might be encountered under fault conditions. An internal temperature protection block is enabled in the P9242-R that monitors the temperature inside the chip. If the die temperature exceeds 140°C, the chip shuts down and resumes when the internal temperature drops below 120°C.

7.7 External Temperature Sensing – TS

The P9242-R has a temperature sensor input, TS, which can be used to monitor an external temperature by using a thermistor. The built-in comparator's reference voltage was chosen to be 0.6V in the P9242-R, and it is used for monitoring the voltage level on the TS pin.

Figure 16. NTC Thermistor Connection to TS Pin



To disable the thermistor, the TS pin should be connected to the LDO33 pin. Do not leave the TS pin floating.

7.8 LEDs Pattern Selection – LED_PAT

The P9242-R uses two LEDs to indicate the power transfer status, faults and operating modes. LEDs are connected to LED1 and LED2 pins as shown on the typical application schematic Figure 24.

The LED patterns can be programmed by setting the voltage on the LED_PAT pin through the resistor divider R43 and R44 as shown on Figure 24.

Table 6. LED Pattern Selection

Option	Voltage on LED_PAT Pin	LED1/LED2 Pin	Status			
			Standby	Transfer	Complete	Fault
1	Pull-Down or 0.075V	LED1 – GREEN	Off	On	Off	Off
		LED2 – RED	Off	Off	Off	Blink 4Hz
2	0.225V	LED1 – GREEN	On	On	Off	Off
		LED2 – RED	On	Off	Off	Blink 4Hz
3	0.375V	LED1 – GREEN	Off	Blink 1Hz	On	Blink 4Hz
		LED2 – RED	Off	Off	Off	Off
4	0.525V	LED1 – GREEN	Off	On	Off	Blink 4Hz
		LED2 – RED	Off	Off	Off	Off
5	0.675V	LED1 – GREEN	On	Blink 1Hz	On	Off
		LED2 – RED	On	Off	Off	Blink 4Hz
6	0.825V	LED1 – GREEN	Off	Off	On	Off
		LED2 – RED	Off	On	Off	Blink 4Hz
7	0.975V or Pull-Up	LED1 – GREEN	Off	Blink 1Hz	On	Off
		LED2 – RED	Off	Off	Off	Blink 4Hz

7.9 Foreign Object Detection

When metallic objects, such as coins, keys, and paperclips, are exposed to alternating magnetic fields, the eddy current flowing through the object will heat up. The amount of heat generated is a function of the amplitude and frequency of the magnetic field, as well as the characteristics of the object, such as resistivity, size, and shape. In any wireless power system, the heat generated by the eddy current manifests itself as a power loss reducing the overall system efficiency. If appropriate measures are not taken, the heating could lead to unsafe situation.

In Extended Power Profile, there are two stages of foreign object detection (FOD). One is by measuring the system quality factor prior to entering the power transfer phase, and the other is to measure the power loss difference between the received power and the transmitted power during the power transfer phase. Prior to entering the power transfer phase, the P9242-R detects a change in the coil's quality factor (Q-factor) when a wireless power receiver or metal object has been placed on its surface. The transmitter measures the Q-factor and compares it with the reference Q-factor provided by the receiver. If the difference is higher than the reference Q-factor, the P9242 will identify it as FOD and shut down the system.

The second stage of the foreign object detection is during the power transfer where the power loss difference between the received power and transmitted power is constantly measured and compared to the WPC-1.2.2-specified threshold. If the difference is higher than the threshold set by the WPC specification, the system will shut down to avoid over-heating.

7.10 Step-Down Regulator

The input capacitors (C14 and C15 in Figure 24) must be connected as close as possible between the VIN pin and GND pin. Similarly, the output capacitor (C4 and C5 in Figure 24) must be placed close to the inductor and GND. The output voltage is sensed by the VIN_LDO pin; therefore, the connection from the step-down output (VCC_5V; see Figure 24) to the VIN_LDO pin should be made as wide and short as possible to minimize output voltage errors. The step-down regulator is the input voltage to the LDO18 and LDO33 linear regulators and is not recommended for powering an external load.

7.11 Linear Regulators – PREG, LDO33, and LDO18

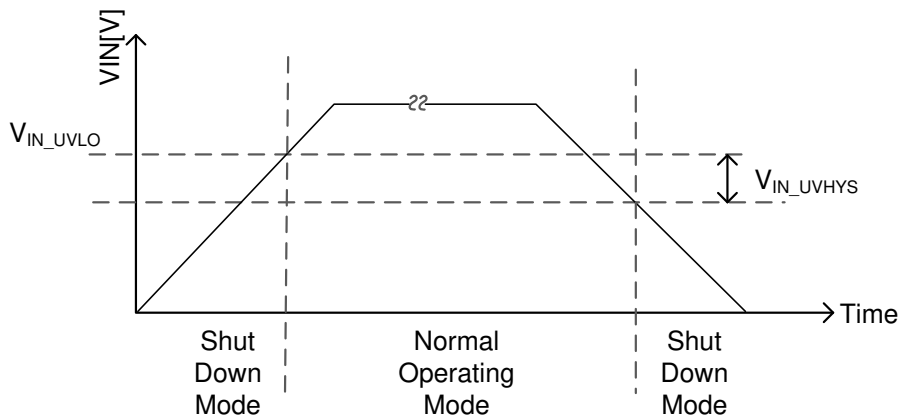
The P9242 has three low-dropout (LDO) regulators used to bias the internal circuitry. The 5V pre-regulator (PREG) provides bias for the entire internal power management. The PREG requires a 1 μ F ceramic bypass capacitor connected from the PREG pin to GND. This capacitor must be placed very close to the PREG pin. The voltage regulator must not be externally loaded.

The LDO33 and LDO18 are used to bias the internal digital circuit. The regulator's input voltage is supplied through the VIN_LDO pin. Both regulators require a 1 μ F ceramic capacitor from the pin to GND. The voltage regulators must not be externally loaded.

7.12 Under-Voltage Lock-Out (UVLO) Protection

The P9242-R has 4V (typical, rising) under-voltage lockout circuit on the VIN pin. To guarantee proper functionality, the voltage on the VIN pin must rise above the UVLO threshold. If the input voltage stays below the UVLO threshold, the P9242-R is in Shut Down Mode.

Figure 17. UVLO Threshold Definition



7.13 LC Resonant Circuit

The LC resonant circuit comprises the series primary resonant coil (L_P) and series capacitance (C_P). The transmitter coil assembly is vendor specific, and it must comply with the WPC recommendation. The WPC recommendations include the self-inductance value, DC resistance (DCR), Q-factor, size, and number of turns.

The P9242-R is designed for an MP-A2 coil configuration using half-bridge and full-bridge inverter topologies to drive the primary coil (L_P) and a series capacitance (C_P). Within the operating frequency range from 110kHz to 145kHz, the assembly of the primary coil and shielding has a self-inductance of $L_P = 10.0\mu\text{H} \pm 10\%$, and the value of the series capacitance is $C_P = 215\text{nF} \pm 5\%$, according to the WPC specification. Near resonance, the voltage developed across the C_P series capacitance could reach 70V peak. High-voltage (100V) COG-type ceramic capacitors are highly recommended for their AC and DC characteristics and temperature stability. The recommended parts are listed on the bill of materials (BOM) in Table 16.

8. Communication Interface

8.1 Modulation/Communication

The WPC-1.2.2 extended power profile specification uses two-way communication for power transfer: receiver-to-transmitter and transmitter-to receiver.

Receiver-to-transmitter communication is accomplished by modulating the load seen by the receiver's coil; the communication is purely digital and symbols 1's and 0's carried on the power signal. Modulation is done with amplitude-shift keying (ASK) modulation using with a bit-rate of 2Kbps. To the transmitter, this appears as an impedance change, which results in measurable variations of the transmitter's coil. The power transmitter demodulates this variation of the coil current or voltage to receive the packets.

Transmitter-to-receiver communication is accomplished by frequency-shift keying (FSK) modulation over the power signal frequency. The power transmitter P9242-R has the means to modulate FSK data from the power signal frequency and use it in order to establish the handshaking protocol with the power receiver.

The P9242-R implements FSK communication when used in conjunction with WPC-compliant receivers, such as the P9221-R. The FSK communication protocol allows the transmitter to send data to the receiver using the power transfer link in the form of modulating the power transfer signal. This modulation appears in the form of a change in the base operating frequency (f_{OP}) to the modulated operating frequency (f_{MOD}) in periods of 256 consecutive cycles. Equation 1 should be used to compute the modulated frequency based on any given operating frequency.

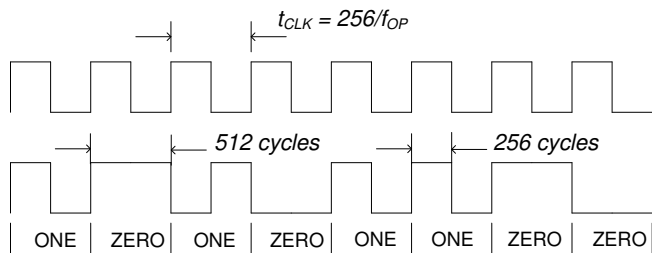
Communication packets are transmitted from transmitter to receiver with less than 1% positive frequency deviation following any receiver-to-transmitter communication packet. The frequency deviation is calculated using Equation 1.

$$f_{MOD} = \frac{60000}{\frac{60000}{f_{OP}} - 3} \text{ [KHz]} \quad \text{Equation 1}$$

Where f_{MOD} is the change in frequency in the power signal frequency; f_{OP} is the base operating frequency of power transfer; and 60,000kHz is the frequency of the internal oscillator responsible for counting the period of the power transfer signal.

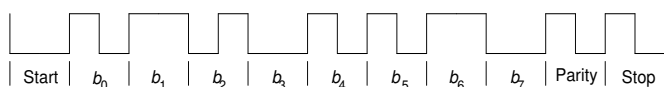
The FSK byte-encoding scheme and packet structure complies with the WPC specification revision 1.2.2. The FSK communication uses a bi-phase encoding scheme to modulate data bits into the power transfer signal. The start bit will consist of 512 consecutive f_{MOD} cycles (or logic '0'). A logic '1' value will be sent by sending 256 consecutive f_{OP} cycles followed by 256 f_{MOD} cycles or vice versa, and a logic '0' is sent by sending 512 consecutive f_{MOD} or f_{OP} cycles.

Figure 18. Example of Differential Bi-phase Encoding for FSK



Each byte will comply with the start, data, parity, and stop asynchronous serial format structure shown in Figure 19:

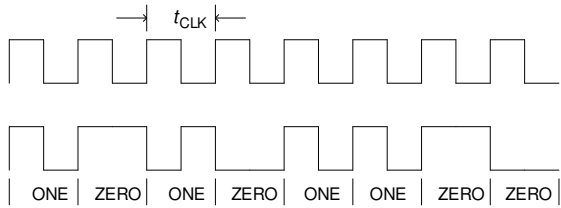
Figure 19. Example of Asynchronous Serial Byte Format for FSK



8.2 Bit Decoding Scheme for ASK

As required by the WPC, the P9242-R uses a differential bi-phase coding scheme to demodulate data bits onto the power signal. A clock frequency of 2kHz is used for this purpose. A logic ONE bit is coded using two narrow transitions, whereas a logic ZERO bit is encoded using one wider transition as shown below:

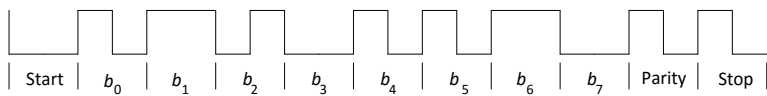
Figure 20. Bit Decoding Scheme



8.3 Byte Decoding for ASK

Each byte in the communication packet comprises 11 bits in an asynchronous serial format, as shown in Figure 21.

Figure 21. Byte Decoding Scheme



Each byte has a start bit, 8 data bits, a parity bit, and a single stop bit.

8.4 Packet Structure

The P9242-R communicates with the base station via communication packets. Each communication packet has the following structure:

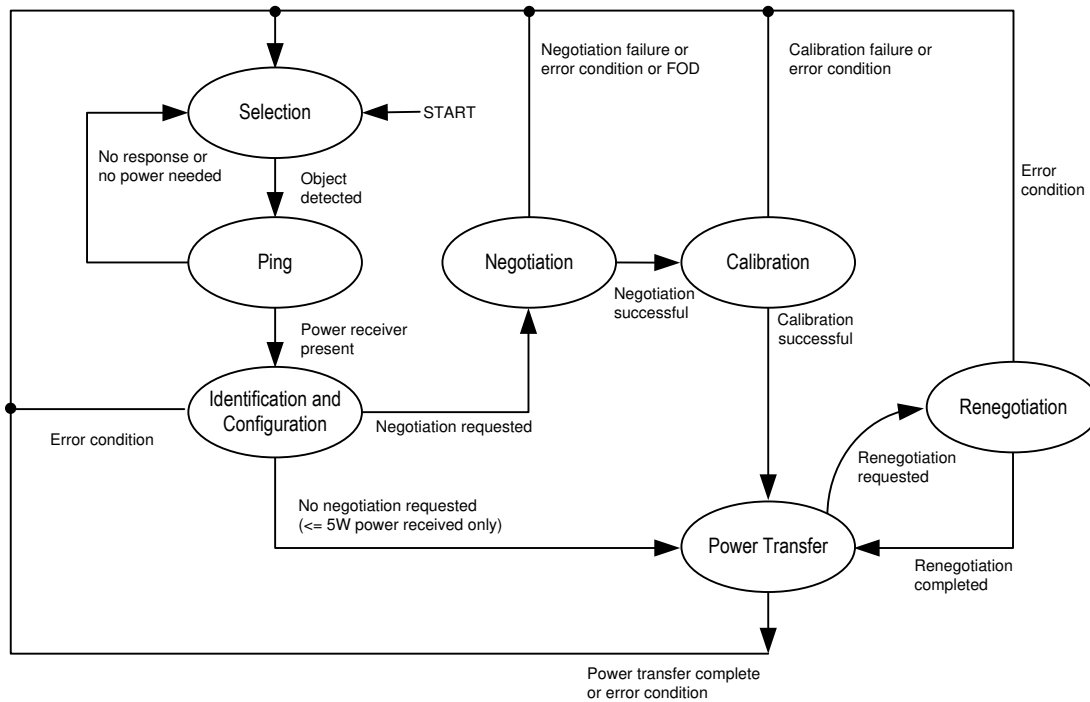
Figure 22. Communication Packet Structure



9. WPC Mode Characteristics

The WPC-1.2.2 extended power profile wireless power specification has a negotiation phase, calibration phase, and renegotiation phase, as shown in Figure 23.

Figure 23. WPC Power Transfer Phases Flow Chart



9.1 Selection Phase

In the selection phase, the power transmitter determines if it will proceed to the ping phase after detecting the placement of an object. In this phase, the power transmitter typically monitors the interface surface for the placement and removal of objects using a small measurement signal. This measurement signal should not wake up a power receiver that is positioned on the interface surface.

9.2 Ping Phase (Digital Ping)

In the ping phase, the power transmitter will transmit power and will detect the response from a possible power receiver. This response ensures the power transmitter that it is dealing with a power receiver rather than some unknown object. When a power receiver is placed on a WPC “Qi” charging pad, it responds to the application of a power signal by rectifying this power signal. When the internal bias voltage is greater than a specific threshold level, then receiver is initiated enabling the WPC communication protocol.

If the power transmitter correctly receives a signal strength packet, the power transmitter proceeds to the identification and configuration phase of the power transfer, maintaining the power signal output.

9.3 Identification and Configuration Phase

The identification and configuration phase is the part of the protocol that the power transmitter executes in order to identify the power receiver and establish a default power transfer contract. This protocol extends the digital ping in order to enable the power receiver to communicate the relevant information.

In this phase, the power transmitter identifies itself and receives information for a default power transfer contract as follows:

- It receives the configuration packet.
- If the power transmitter does not acknowledge the request (does not transmit FSK modulation), the power receiver will assume 5W output power.

9.4 Negotiation Phase

In the negotiation phase, the power receiver negotiates changes to the default power transfer contract. In addition, the power receiver verifies that the power transmitter has not detected a foreign object.

9.5 Calibration Phase

In the calibration phase, the power receiver provides information that the power transmitter can use to improve its ability to detect foreign objects during power transfer.

9.6 Power Transfer Phase

In this phase, the P9242-R controls the power transfer by means of the following control data packets:

- Control Error Packets
- Received Power Packet (RPP, FOD-related)
- End Power Transfer (EPT) Packet

Once the “identification and configuration” phase is completed, the transmitter initiates the power transfer mode. The receiver’s control circuit sends error packets to the transmitter to adjust the rectifier voltage to the level required to maximize the efficiency of the linear regulator and to send to the transmitter the actual received power packet for foreign object detection (FOD) to guarantee safe, efficient power transfer.

In the event of an EPT issued by the application, when the receiver sends EPT packets, the transmitter terminates the power transfer.

10. Functional Registers

The following list of tables is a comprehensive list of address locations, field names, available operations (R or RW), default values, and functional descriptions of all internally accessible registers contained within the P9242-R. The default I²C slave address is 61_{HEX}.

Table 7. State Register

Address and Bits	Register Field Name	R/W	Default	Function and Description
6E0 _{HEX}	System State	R	00 _{HEX}	0 _{DEC} = Startup 1 _{DEC} = Idle 2 _{DEC} = Analog Ping Phase 4 _{DEC} = Digital Ping Phase 5 _{DEC} = WPC Identification 7 _{DEC} = WPC Configuration 8 _{DEC} = Power Transfer Initialization 9 _{DEC} = Power Transfer State 11 _{DEC} = Remove Power 12 _{DEC} = Restart 13 _{DEC} = WPC Negotiation

Table 8. Status Register

Address and Bits	Register Field Name	R/W	Default	Function and Description
6E1 _{HEX}	System Status	R	00 _{HEX}	0 _{DEC} = System Normal 1 _{DEC} = FOD Alarm 2 _{DEC} = EPT Charge Complete 4 _{DEC} = EPT No Response 5 _{DEC} = EPT Internal Fault 6 _{DEC} = Over-Temperature Alarm 7 _{DEC} = Over-Current 9 _{DEC} = EPT Other Rx Fault 10 _{DEC} = Negotiation Fail

Table 9. Read Register – Coil Current

Address and Bits	Register Field Name	R/W	Default	Function and Description
6E2 _{HEX} [7:0]	Coil_current [7:0]	R	-	8 LSB of coil current value in mA.
6E3 _{HEX} [7:0]	Coil_current [15:8]	R	-	8 MSB of coil current value in mA.

Table 10. Read Register – Coil Voltage

Address and Bits	Register Field Name	R/W	Default	Function and Description
6E4 _{HEX} [7:0]	Coil_voltage [7:0]	R	-	8 LSB of coil voltage value in mV.
6E5 _{HEX} [7:0]	Coil_voltage [15:8]	R	-	8 MSB of coil voltage value in mV.

Table 11. Read Register – Remote Temperature Sensing Voltage

$$\text{Sensing Voltage} = \frac{\text{Thermistor ADC Value}[15:0] * 2.4V}{4095}$$

Address and Bits	Register Field Name	R/W	Default	Function and Description
6E8 _{HEX} [7:0]	Thermistor ADC Value [7:0]	R	-	8 LSB of thermistor ADC value.
6E9 _{HEX} [7:0]	Thermistor ADC Value [15:8]	R	-	8 MSB of thermistor ADC value.

Table 12. Read Register – Operating Frequency

$$f_{OP} = \frac{60 \text{ MHz}}{\text{FRE_CNT}[15:0]}$$

Address and Bits	Register Field Name	R/W	Default	Function and Description
6EA _{HEX} [7:0]	FRE_CNT [7:0]	R	-	8 LSB of operating frequency count.
6EB _{HEX} [7:0]	FRQ_CNT [15:8]	R	-	8 MSB of operating frequency count.

Table 13. Read Register – Operating Duty Cycle

$$\text{DUTY CYCLE} = \frac{\text{DUTY_CNT} * 50\%}{255}$$

Address and Bits	Register Field Name	R/W	Default	Function and Description
6EC _{HEX} [7:0]	DUTY_CNT [7:0]	R	-	8 LSB of operating duty count.
6ED _{HEX} [7:0]	DUTY_CNT [15:8]	R	-	8 MSB of operating duty count.

Table 14. Read Register – Full/Half Bridge Status

Address and Bits	Register Field Name	R/W	Default	Function and Description
6EE _{HEX} [7:0]	Full/half bridge status [7:0]	R	-	"0" = Half bridge. "1" = Full bridge.

11. Application Information

11.1 Power Dissipation and Thermal Requirements

The P9242-R is offered in a 48-VFQFN package that has a maximum power dissipation capability of about 1.47W. The maximum power dissipation of the package is determined by the number of thermal vias between the package and the printed circuit board (PCB). The maximum power dissipation of the package is defined by the die's specified maximum operating junction temperature, $T_{J(MAX)}$ of 125°C. The junction temperature rises when the heat generated by the device's power dissipation flow is impeded by the package-to-PCB thermal resistance.

The VFQFN package offers a typical thermal resistance, junction to ambient (θ_{JA}), of 27.2°C/W when the PCB layout design is optimized as described in the *P9242-R Layout Guide* document. The techniques noted in the PCB layout section must be followed when designing the printed circuit board layout. Attention to the placement of the P9242-R and bridge FET packages in proximity to other heat-generating devices in a given application design should also be considered. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing θ_{JA} (in the order of decreasing influence) are PCB characteristics, die/package attached thermal pad size (VFQFN) and thermal vias, and the final system hardware construction. Board designers should keep in mind that the package thermal metric θ_{JA} is impacted by the characteristics of the PCB. Changing the design or configuration of the PCB changes the overall thermal resistivity and the board's heat-sinking efficiency.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design.
- Improving the thermal coupling of the component to the PCB.
- Introducing airflow into the system.

First, the maximum power dissipation for a given situation should be calculated using Equation 2:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}} \quad \text{Equation 2}$$

Where: $P_{D(MAX)}$ = Maximum power dissipation

θ_{JA} = Package thermal resistance (°C/W)

$T_{J(MAX)}$ = Maximum device junction temperature (°C)

T_A = Ambient temperature (°C)

The maximum recommended operating junction temperature ($T_{J(MAX)}$) for the P9242-R is 125°C. The thermal resistance of the 48-pin VFQFN package (NDG48) is optimally $\theta_{JA}=27.2^\circ\text{C/W}$. Operation is specified to a maximum steady-state ambient temperature (T_A) of 85°C. Therefore, the maximum recommended power dissipation is given by the following equation:

$$P_{D(Max)} = (125^\circ\text{C} - 85^\circ\text{C}) / 27.2^\circ\text{C/W} \cong 1.47 \text{ Watt}$$

All the previously mentioned thermal resistances are the values found when the P9242-R is mounted on a standard board of the dimensions and characteristics specified by the JEDEC 51 standard.

11.2 Recommended Coils

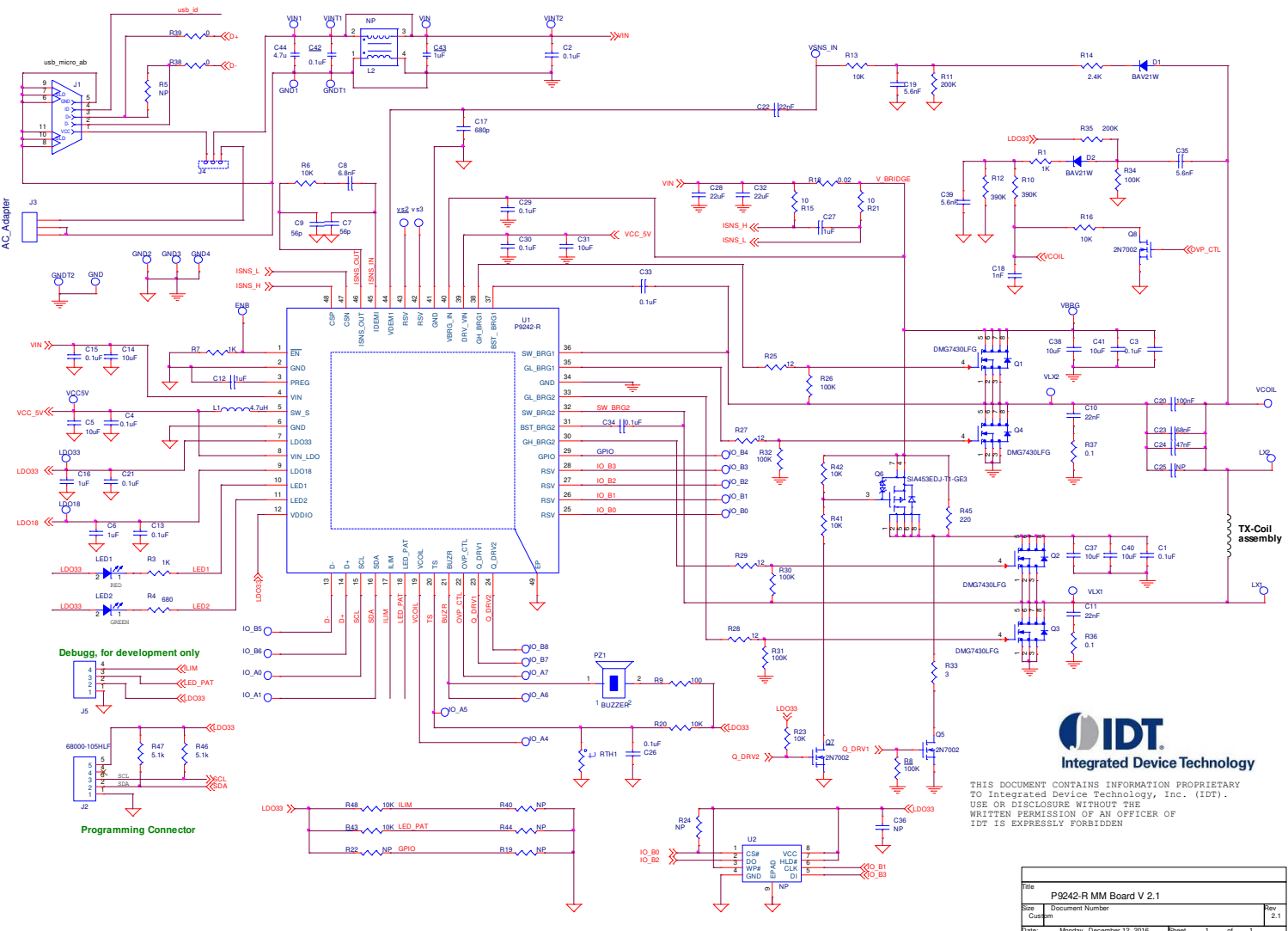
Table 15. Recommended Coil Manufactures

Output Power	Vendor	Part number	Inductance at 100kHz	DCR at 20°C
15W	SUNLORD	SWA53N53H30C11B	10μH	50mΩ
15W	TDK	WT525225-12F2-MA2-G	10.6μH	40mΩ

11.3 Typical Application Schematic

The typical application schematic provides a basic guideline to understanding and building a functional medium-power wireless power transmitter type MP-A2 as described in the WPC specifications. Other components, not shown on the typical application schematic, might be needed in order to comply with other requirements, such as EMC or thermal specifications.

Figure 24. P9242-R Typical Application Schematic



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