Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# Audio, LED Backlight, Power Management, and Control

Product Datasheet

# IDTP95020

## Features

- Quick Turn Customization
- Embedded Microcontroller
  - Master controller during power-up and power-down
  - Power up/down sequence field programmable with external EEPROM
  - Dynamic power management via I²C bus interface
  - Up to 10 general purpose I/Os
  - Housekeeping for IDTP95020 and other devices
- Audio - 4 Channel CODEC with 24-bit resolution
  - Integrated 2.5W mono Class D amplifier with filterless operation
  - Stereo cap-less headphone driver
  - Differential analog audio line inputs
  - Dual mode microphone inputs (analog or DMIC)
- Battery Charger for Li-Ion / Li-Polymer up to 1.5A
  - High efficiency switch-mode EnergyPath™ controller with advanced safety features
  - USB or AC adaptor power input (5V)
  - Programmable current limit
  - Internal 180mΩ ideal diode with external ideal diode controller
- Buck DC-DC PWM converters with PFM mode
  - 2x at 500mA, 0.75V to 3.7V output
  - 1x at 1000mA, 0.75V to 3.7V output
- Boost DC-DC PWM converter
  - 1x at 1.5A peak current, 4.05V to 5.0V output
- 2-ch white LED driver with 2W total output power
  - Two programmable current sinks, 25mA each
  - Voltage limited to rating of external FET and diode
- Linear regulators
  - 3x at 150mA, 0.75V to 3.7V output
  - 4x at 50mA, 0.75V to 3.7V output
  - 1x at 10mA, 3.3V or 3.0V output, always-on
- ADC and Touch Screen Controller
  - 12 bit resolution, Sample rate 62.5kSPS, DNL -1~+2LSB, INL +/-2LSB, on chip 2.5V reference
  - On-chip temperature, charging current, SYS voltage and battery voltage measurement
  - Touch pressure measurement
  - 4-wire Touch Screen interface (shared with GPIO pins and ADC input channels)
- 0°C to 70°C operating temperature range
- 132-ld 10x10x0.85mm dual-row QFN package

## Description

The IDTP95020 is designed to provide maximum flexibility to system designers by providing full customization and programmability. It is a highly integrated single chip device that incorporates an embedded general purpose microcontroller, a high fidelity audio CODEC, full power management functionality, backlight driver, battery charger, touch screen controller, and real time clock, all of which make it an ideal solution for portable consumer devices, such as cellular phone handsets, portable gaming devices, digital media players, and portable navigational devices. The device compact footprint optimizes board area and reduces component count.

The IDTP95020 embedded Microcontroller features 4kB factory-programmable ROM, or the I²C master can load a custom program from an external EEPROM module. The system power-on/power-off sequencing and general system housekeeping could be programmed in internal ROM or external EEPROM. The I²C slave can be used during operation to communicate with the host to accept commands and report status.

The IDTP95020 operates from an adapter or USB power source to deliver power to the system load while charging the battery; up to 1.5A charging current. The input current is limited to the value set by the host for adapter source (up to 2A) or for USB source (100mA or 500mA). The switch-mode EnergyPath™ Battery Charger operates with high efficiency buck regulator to transmit the power to the load with minimal loss.

The IDTP95020 power management features along with the switching regulators and LDOs can provide power for most extremely complex hand-held devices.

The device is offered in a small 132-ld 10x10x0.85mm QFN package and guaranteed to operate over the commercial temperature range 0°C to 70°C.

## Applications

- Smart Phones
- Portable Gaming Device
- Digital Media Players
- Handheld Computers
- Portable Navigational Devices

## Block Diagram

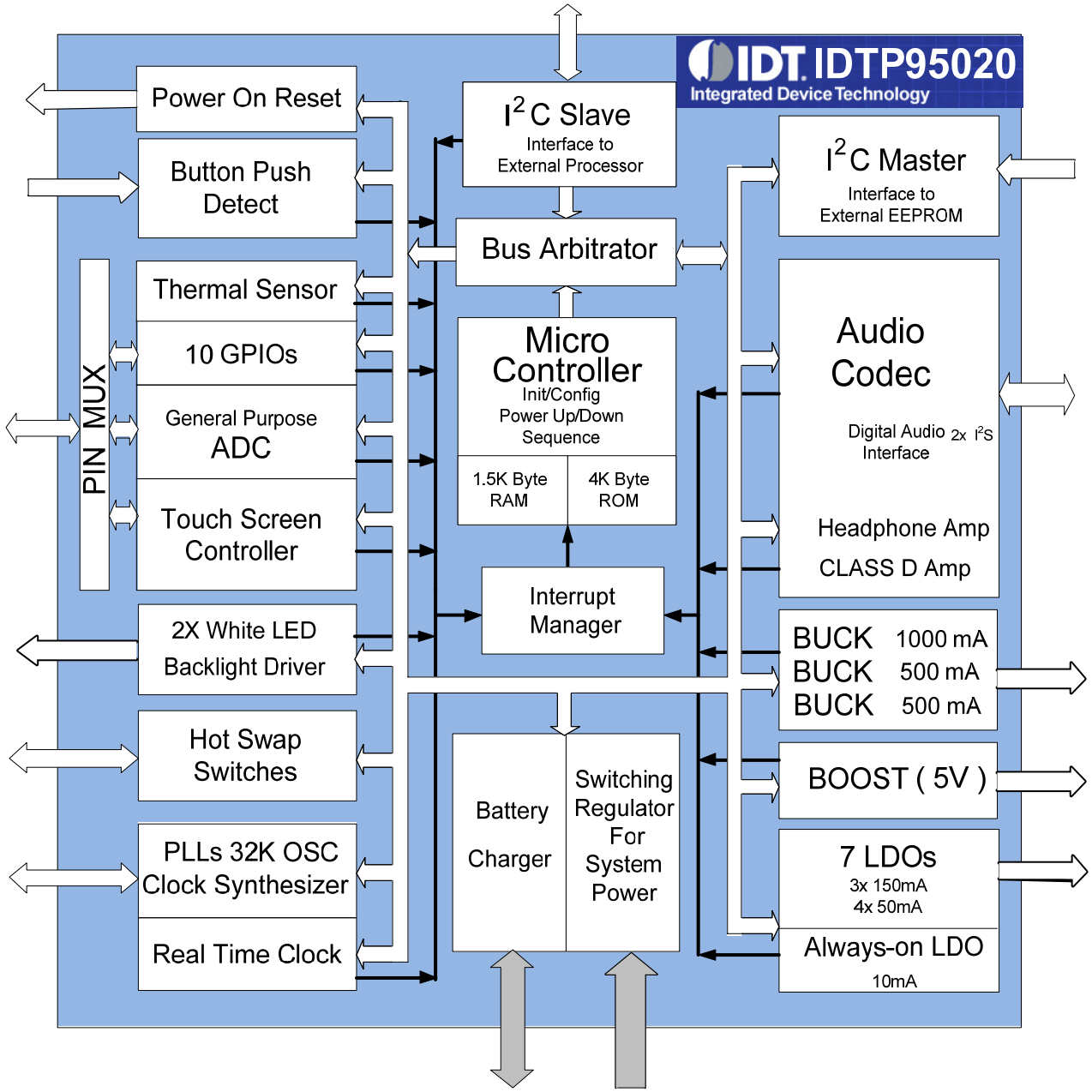


*Figure 1. Simplified Block Diagram*

 

# Table of Contents



 

## Revision History

V1.0 February 2011 – Unreleased Final.

V1.1 June 2011 – Added ESD specifications.

V1.2 June 2011 - Updated ordering part numbers, released Final

 

# ABSOLUTE MAXIMUM RATINGS

Stresses above the ratings listed below can cause permanent damage to the IDTP95020. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

**Table 1. Absolute Maximum Ratings**

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| CHRG_INPUT to CHRG_GND | USB or AC adaptor Charger Input (Transient t < 1ms, Duty Cycle < 1%) | -0.3 | 7 | V |
| CHRG_BAT to DGND | Battery Input Source | -0.3 | 5.5 | V |
| CHRG_SYSVCC to DGND | System VCC Output (Vsys) | -0.3 | 5.5 | V |
| PVDD to PGND | CLASS_D BTL Input Power | -0.3 | 6 | V |
| LDO_IN1, IN2, IN3 to DGND | Input voltage for LDO | -0.3 | 6 | V |
| BUCK500_0_IN to BUCK500_0_GND | BUCK0 Input voltage | -0.3 | 6 | V |
| BUCK500_1_IN to BUCK500_1_GND | BUCK1 Input voltage | -0.3 | 6 | V |
| BUCK1000_IN to BUCK1000_GND | BUCK2 Input voltage | -0.3 | 6 | V |
| FDBK to DGND | BUCK0, 1, 2 feedback voltage | -0.3 | 6 | V |
| LED_BOOST_VIN to LED_BOOST_GND | LED_BOOST Converter gate bias supply | -0.3 | 6 | V |
| LED_BOOST_GATE to LED_BOOST_GND | LED_BOOST Gate Drive to Power FET | -0.3 | LED_BOOST_VIN + 0.3 | V |
| LED_BOOST_VSENSE to LED_BOOST_GND | Voltage Sense Input | -0.3 | LED_BOOST_VIN + 0.3 | V |
| LED_BOOST_ISENSE to LED_BOOST_GND | Current Sense Input | -0.3 | LED_BOOST_VIN + 0.3 | V |
| LED_BOOST_SINK to LED_BOOST_GND | Current Sink for LED String #1 or String #2 | -0.3 | 6 | V |
| BOOST5_OUT to BOOST5_GND | BOOST5 Converter Output | -0.3 | 6 | V |
| BOOST5_SW to BOOST5_GND | BOOST5 Converter Power Switch1 and Switch2 | -0.3 | 6 | V |
| HSPWR to DGND | Hot Swap Switches Power | -0.3 | 6 | V |
| HSCTRL1, HSCTRL2 to DGND | Input voltage for Hot Swap Control | -0.3 | HSPWR + 0.3 | V |
| VDDIO_CK to CKGEN_GND | Power Supply for TCXO_OUT1, TCXO_OUT2 | -0.3 | 2.5 | V |
| TCXO_IN to CKGEN_GND | Input voltage for TCXO_IN | -0.3 | VDD_CKGEN18 + 0.3 | V |
| 32KHZ_CLKIN to CKGEN_GND | Input voltage for 32KHZ_CLK | -0.3 | LDO_LP + 0.3 | V |
| GPIO to DGND | Input voltage for GPIO | -0.3 | CHRG_SYSVCC + 0.3 | V |
| SDA, SCL to DGND | Input voltage for I2C Master or Slave | -0.3 | 6 | V |
| BCLK, WS, SDOUT, SDIN to DGND | Input voltage for I2S channel 1 or 2 | -0.3 | LDO_050_0 + 0.3 | V |
| EX_ROM to DGND | External ROM enable | -0.3 | CHRG_SYSVCC + 0.3 | V |
| AGND, LDO_GND, CKGEN_GND, GND, PGND, BOOST5_GND, BCUCK500_0_GND, BCUCK500_1_GND, BUCK1000_GND, LED_BOOST_GND, CHRG_GND, GND_BAT/ADCGND to DGND | | -0.3 | 0.3 | V |
| $T_J$ | Operating Junction Temperature | | -40 to +125 | °C |
| $T_S$ | Storage Temperature | | -40 to +150 | °C |
| $T_{SOLDER}$ | Soldering Temperature | | 260°C for 10 seconds | °C |
| ESD Rating | (HBM) Human Body Model (all pins except A62, A63, B52, B53) | ±1500 | | V |
| | (HBM) Human Body Model (only pins A62, A63, B52, B53) | ±450 | | |
| | (CDM) Charged Device Model (all pins) | ± 500 | | |
| | (MM) Machine Model (all pins) | ± 200 | | |

 

## ESD Warning

The IDTP95020 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the IDTP95020 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

# RECOMMENDED OPERATING CONDITIONS

**Table 2. Recommended Operating Conditions**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| CHRG_INPUT | USB or AC Adaptor Charger Input | | 4.35 | | 5.5 | V |
| CHRG_BAT | Battery Input Source | When $V_{BAT}$ providing power | 3.0 | | 4.5 | V |
| PVDD | CLASS_D BTL Input Power Supply | | 3.0 | | 5.0 | V |
| LDO_IN1, IN2, IN3 | Input voltage for LDO | | 3.0 | | 5.5 | V |
| BUCK500_0_IN, BUCK500_1_IN, BUCK1000_IN | BUCK0, 1, 2 Input voltage | | 3.0 | | 4.5 | V |
| LED_BOOST_VIN | LED Boost Converter gate bias supply | | 3.0 | | 5.5 | V |
| VDDIO_CK voltage | Power Supply for TCXO_OUT1, TCXO_OUT2 | | 1.1 | | 1.9 | V |
| HSPWR | Hot Swap Switches Power Supply | Do not tie to ground or floating | 3.0 | | 5.5 | V |
| LDO_050_0 | Power Supply for I²C Slave Channel, I²S Channel 1 and 2 | | 1.7 | | 3.6 | V |
| $T_A$ | Ambient Operating Temperature | | 0 | | 70 | °C |
| $T_J$ | Operating Junction Temperature | | -40 | | 125 | °C |
| $\theta_{JA}$ | Maximum Thermal Resistance | Junction to Ambient | | 23.5 | | °C/W |
| $\theta_{JC}$ | Maximum Thermal Resistance | Junction to Case | | 7.6 | | °C/W |
| $\theta_{JB}$ | Maximum Thermal Resistance | Junction to Board | | 0.15 | | °C/W |
| $P_D$ | Maximum Package Power Dissipation | | | 2.3 | | W |

# POWER CONSUMPTION

## Overall Power Consumption

**Table 3. Overall Power Consumption**

| MODE | DESCRIPTION | CHARGE_BAT | TYPICAL CONSUMPTION |
|---|---|---|---|
| Sleep | USB or AC Adaptor is not present, a main battery is present and well-charged. Always on LDO_LP is on, RTC is on and RTC registers are maintained. Wake-up capabilities (Switch Detect Input) are available. | $V_{BAT}$ = 3.8V | 85 * 3.8 = 323 µW |
| Standby | USB or AC Adaptor is not present, a main battery is present and well-charged. Always on LDO_LP is on, all DC-DC Bucks in PFM mode. All LDOs are on, no load. | $V_{BAT}$ = 3.8V | 385 * 3.8 = 1463 µW |
| Touch Controller Standby | USB or AC Adaptor is not present, a main battery is present and well-charged. Always on LDO_LP is on, touch screen controller is on, LDO_050_0 is on. | $V_{BAT}$ = 3.8V | 7.4 * 3.8 = 28.12 mW |

 

## Audio Power Consumption

**Table 4. Audio Power Consumption**

| MODE | CHRG_BAT (V) | LDO_050_0 (V) | VDD_AUDIO18 (V) | VDD_AUDIO33 (V) | PVDD (V) | CHRG_BAT (mA) | PVDD (mA) | TOTAL POWER (mW) |
|---|---|---|---|---|---|---|---|---|
| Playback to 4Ω speaker, sampling at 96 kHz, no signal | 3.3 | 2.3 | 1.5 | 3.0 | 3.0 | 52 | 7 | 192 |
| | 3.8 | 3.3 | 1.8 | 3.3 | 3.3 | 60 | 7 | 252 |
| | 4.2 | 3.6 | 1.8 | 3.6 | 5.0 | 60 | 10 | 302 |
| Playback to 4Ω speaker, sampling at 96 kHz, 0dB FS 1 kHz signal | 3.3 | 2.3 | 1.5 | 3.0 | 3.0 | 53 | 155 | 640 |
| | 3.8 | 3.3 | 1.8 | 3.3 | 3.3 | 61 | 170 | 793 |
| | 4.2 | 3.6 | 1.8 | 3.6 | 5.0 | 61 | 258 | 1546 |
| Playback to 8Ω speaker, sampling at 48 kHz, no signal | 3.3 | 2.3 | 1.5 | 3.0 | 3.0 | 52 | 6 | 190 |
| | 3.8 | 3.3 | 1.8 | 3.3 | 3.3 | 59 | 6 | 244 |
| | 4.2 | 3.6 | 1.8 | 3.6 | 5.0 | 59 | 10 | 298 |
| Playback to 8Ω speaker, sampling at 48 kHz, 0dB FS 1 kHz signal | 3.3 | 2.3 | 1.5 | 3.0 | 3.0 | 52 | 96 | 460 |
| | 3.8 | 3.3 | 1.8 | 3.3 | 3.3 | 60 | 105 | 575 |
| | 4.2 | 3.6 | 1.8 | 3.6 | 5.0 | 60 | 163 | 1067 |
| Playback to 16Ω headphone, sampling at 96 kHz, no signal | 3.3 | 2.3 | 1.5 | 3.0 | 3.0 | 54 | 0 | 178 |
| | 3.8 | 3.3 | 1.8 | 3.3 | 3.3 | 58 | 0 | 220 |
| | 4.2 | 3.6 | 1.8 | 3.6 | 5.0 | 60 | 0 | 252 |
| Playback to 16Ω headphone, sampling at 96 kHz, 0dB FS 1 kHz signal | 3.3 | 1.7 | 1.5 | 3.0 | 3.0 | 120 | 0 | 396 |
| | 3.8 | 3.3 | 1.8 | 3.3 | 3.3 | 133 | 0 | 506 |
| | 4.2 | 3.6 | 1.8 | 3.6 | 5.0 | 135 | 0 | 567 |
| Playback to 16Ω cap-less headphone, sampling at 96 kHz, no signal | 3.3 | 2.3 | 1.5 | 3.0 | 3.0 | 55 | 0 | 182 |
| | 3.8 | 3.3 | 1.8 | 3.3 | 3.3 | 60 | 0 | 228 |
| | 4.2 | 3.6 | 1.8 | 3.6 | 5.0 | 62 | 0 | 260 |
| Playback to 16Ω cap-less headphone, sampling at 96 kHz, 0dB FS 1 kHz signal | 3.3 | 2.3 | 1.5 | 3.0 | 3.0 | 122 | 0 | 403 |
| | 3.8 | 3.3 | 1.8 | 3.3 | 3.3 | 135 | 0 | 513 |
| | 4.2 | 3.6 | 1.8 | 3.6 | 5.0 | 137 | 0 | 576 |
| Stereo playback bypassing ADC and DAC to Class-D 4Ω speaker, no signal | 3.3 | 2.3 | 1.5 | 3.0 | 3.0 | 41 | 7 | 156 |
| | 3.8 | 3.3 | 1.8 | 3.3 | 3.3 | 48 | 7 | 206 |
| | 4.2 | 3.6 | 1.8 | 3.6 | 5.0 | 48 | 10 | 252 |
| Record mode – Stereo Line-In to ADC0 sampling at 96 kHz, no signal | 3.3 | 2.3 | 1.5 | 3.0 | 3.0 | 45 | 0 | 149 |
| | 3.8 | 3.3 | 1.8 | 3.3 | 3.3 | 49 | 0 | 186 |
| | 4.2 | 3.6 | 1.8 | 3.6 | 5.0 | 50 | 0 | 210 |
| Record mode – Analog microphone I/P to ADC1 sampling at 16 kHz, no signal | 3.3 | 2.3 | 1.5 | 3.0 | 3.0 | 43 | 0 | 142 |
| | 3.8 | 3.3 | 1.8 | 3.3 | 3.3 | 47 | 0 | 179 |
| | 4.2 | 3.6 | 1.8 | 3.6 | 5.0 | 47 | 0 | 198 |
| Record mode – Analog microphone I/P to ADC1 sampling at 96 kHz, no signal | 3.3 | 2.3 | 1.5 | 3.0 | 3.0 | 45 | 0 | 149 |
| | 3.8 | 3.3 | 1.8 | 3.3 | 3.3 | 49 | 0 | 186 |
| | 4.2 | 3.6 | 1.8 | 3.6 | 5.0 | 50 | 0 | 210 |

 

# DIGITAL INTERFACES ELECTRICAL CHARACTERISTICS

Unless otherwise specified, typical values at $T_A$ = 25°C, $V_{SYS}$ = 3.8V, $V_{LD0\_LP}$=3.3V, $T_A$ = 0°C to +70°C

## I²C Master Electrical Characteristics

**Table 5. I²C Master Electrical Specifications**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | 0.7x $V_{LD0\_LP}$ | | | V |
| $V_{IL}$ | Input Low Voltage | | -0.3 | | 0.3x $V_{LD0\_LP}$ | V |
| $V_{OL}$ | Output Low Voltage (Open Drain) | IOL = 3 mA | | | 0.4 | V |

## I²C Slave Electrical Characteristics

**Table 6. I²C Slave Electrical Specifications**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{LDO\_050\_0}$ | Input Power Supply | | 1.7 | | 3.6 | V |
| $V_{IH}$ | Input High Voltage | | 0.7x $V_{LDO\_050\_0}$ | | | V |
| $V_{IL}$ | Input Low Voltage | | -0.3 | | 0.3x $V_{LDO\_050\_0}$ | V |
| $V_{OL}$ | Output Low Voltage | IOL = +3 mA | | | 0.4 | V |

## I²S Electrical Characteristics

**Table 7. I²S Electrical Specifications**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{LDO\_050\_0}$ | Input Power Supply | | 1.7 | | 3.6 | V |
| $V_{IH}$ | Input High Voltage | | 0.7x $V_{LDO\_050\_0}$ | | $V_{SYS}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | -0.3 | | 0.3x $V_{LDO\_050\_0}$ | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -1mA, $V_{LDO\_050\_0}$ = 3.3V | 0.9x $V_{LDO\_050\_0}$ | | | V |
| | | $I_{OH}$ = -1mA, $V_{LDO\_050\_0}$ = 2.5V | 0.9x $V_{LDO\_050\_0}$ | | | V |
| | | $I_{OH}$ = -100uA, $V_{LDO\_050\_0}$ = 1.8V | $V_{LDO\_050\_0}$ - 0.2 | | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 1mA | | | 0.1x $V_{LDO\_050\_0}$ | V |

## GPIO Electrical Characteristics

**Table 8. GPIO Electrical Specifications**

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | 0.7x $V_{LD0\_LP}$ | | $V_{SYS}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | -0.3 | | 0.3x $V_{LD0\_LP}$ | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -2mA | 0.9x $V_{SYS}$ | | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2mA | | | 0.1x $V_{SYS}$ | V |

 

# PIN CONFIGURATION AND DESCRIPTION

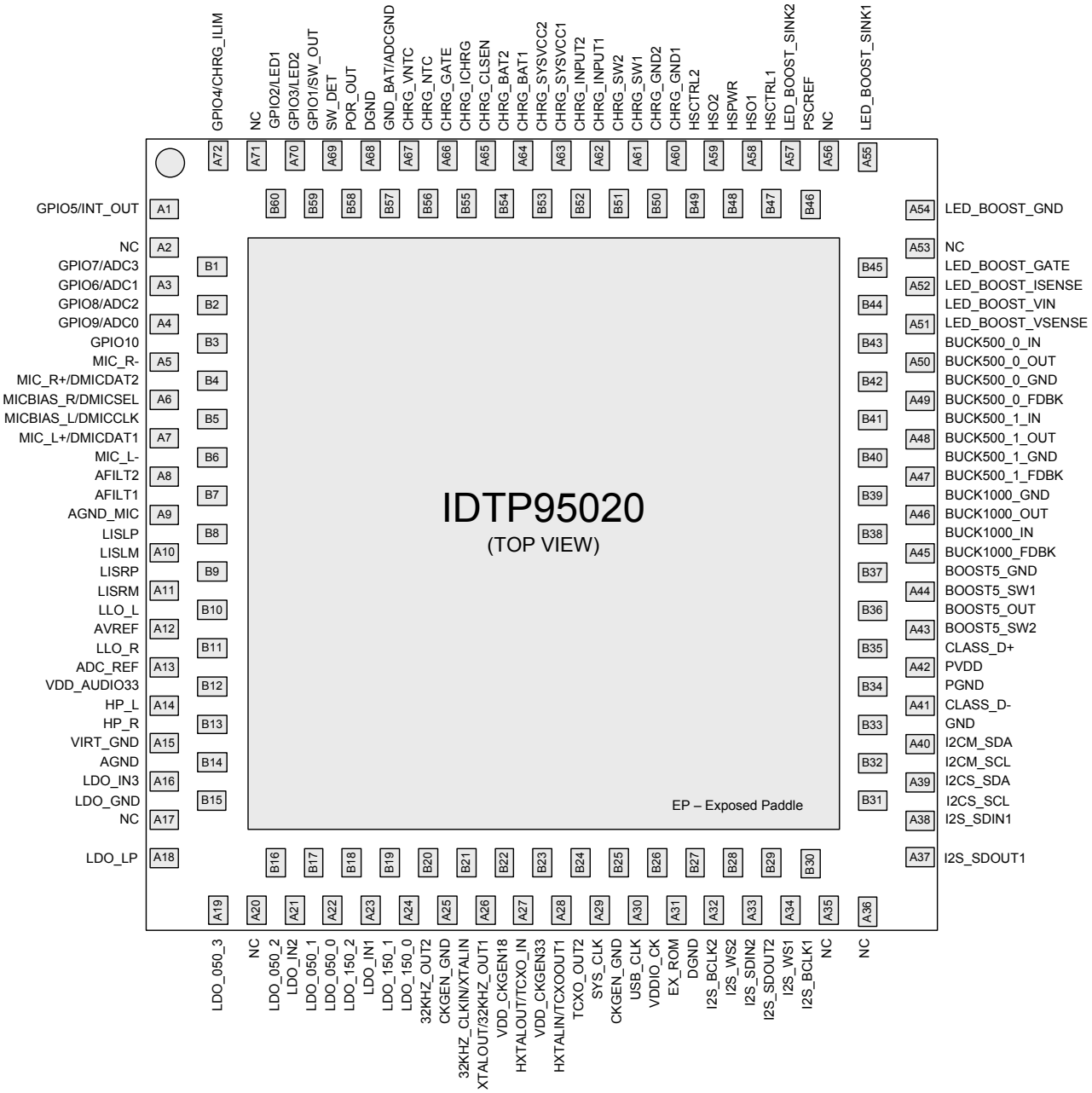


*Figure 2. IDTP95020 Pin Configuration (NGQ132)*

NOTE: All the Buck Converter inputs (BUCK500_0_IN, BUCK500_1_IN, BUCK1000_IN) must be connected to CHRG_SYSVCC1 and CHRG_SYSVCC2.

 

**Table 9 - NQG132 Pin Functions by Pin Number (see Figure 2)**

| MODULE | PIN# | PIN NAME | DESCRIPTION | I/O TYPE |
|---|---|---|---|---|
| **GPIO_TSC** (Also, see pins B57 – A71) | A1 | GPIO5/INT_OUT | GPIO 5: General Purpose I/O # 5 | GPIO |
| | | | INT_OUT : Interrupt Output | |
| | A2 | NC | No Connect | NC |
| | B1 | GPIO7/ADC3 | GPIO 7: General Purpose I/O # 7 | GPIO |
| | | | ADC3 : Auxiliary Input Channel 4 / Y- pin to 4 wire resistive touch screen | |
| | A3 | GPIO6/ADC1 | GPIO 6: General Purpose I/O # 6 | GPIO |
| | | | ADC1 : Auxiliary Input Channel 2 / X- pin to 4-wire resistive touch screen | |
| | B2 | GPIO8/ADC2 | GPIO 8: General Purpose I/O # 8 | GPIO |
| | | | ADC2 : Auxiliary Input Channel 3 / Y+ pin to 4-wire resistive touch screen | |
| | A4 | GPIO9/ADC0/MCLK_IN | GPIO 9: General Purpose I/O # 9 | GPIO |
| | | | ADC0 : Auxiliary Input Channel 1 / X+ pin to 4-wire resistive touch screen | |
| | | | MCLK_IN : Master Clock Input | |
| | B3 | GPIO10 | GPIO 10: General Purpose I/O # 10 | GPIO |
| **AUDIO** | A5 | MIC_R- | MIC_R-: Analog Microphone Differential Stereo Right Inverting Input | A-I |
| | B4 | MIC_R+/DMICDAT2 | MIC_R+: Analog Microphone Differential Stereo Right Non-Inverting Input | A-I |
| | | | DMICDAT2: Digital Microphone 2 Data Input | D-I |
| | A6 | MICBIAS_R/DMICSEL | MICBIAS : Microphone Right Bias | A-O |
| | | | DMICSEL : Digital Microphone Select (Common to both inputs) | D-O |
| | B5 | MICBIAS_L/DMICCLK | MICBIAS : Microphone Left Bias | A-O |
| | | | DMICCLK : Digital Microphone Clock (Common to both inputs) | D-O |
| | A7 | MIC_L+/DMICDAT1 | MIC_L+ : Analog Microphone Differential Stereo Left Non-Inverting Input | A-I |
| | | | DMICDAT1 : Digital Microphone 1 Data Input | D-I |
| | B6 | MIC_L- | MIC_L- : Analog Microphone Differential Stereo Left Inverting Input | A-I |
| | A8 | AFILT2 | Microphone ADC Anti-Aliasing Filter Capacitor #2 | A-I |
| | B7 | AFILT1 | Microphone ADC Anti-Aliasing Filter Capacitor #1 | A-I |
| | A9 | AGND_MIC | Microphone Ground (Analog Ground) | GND |
| | B8 | LISLP | Line Input Stereo Left Non-Inverting | A-I |
| | A10 | LISLM | Line Input Stereo Left Inverting | A-I |
| | B9 | LISRP | Line Input Stereo Right Non-Inverting | A-I |
| | A11 | LISRM | Line Input Stereo Right Inverting | A-I |
| | B10 | LLO_L | Line Level Output, Left | A-O |
| | A12 | AVREF | Analog Reference | A-O |
| | B11 | LLO_R | Line Level Output, Right | A-O |
| | A13 | ADC_REF | ADC Reference Bypass Capacitor | A-I |
| | B12 | VDD_AUDIO33 | Filter Capacitor for Internal 3.3V AUDIO LDO | A-O |
| | A14 | HP_L | Left Headphone Output | A-O |
| | B13 | HP_R | Right Headphone Output | A-O |
| | A15 | VIRT_GND | Virtual Ground for Cap-Less Output | A-O |
| | B14 | AGND | Analog Ground | GND |

 

| MODULE | PIN# | PIN NAME | DESCRIPTION | I/O TYPE |
|---|---|---|---|---|
| LDO | A16 | LDO_IN3 | Input Voltage to LDOs for AUDIO Power (VDD_AUDIO33 and VDD_AUDIO18) | AP-I |
| | B15 | LDO_GND | LDO Ground | GND |
| | A17 | NC | No Connect | NC |
| | A18 | LDO_LP | Always on Low Power LDO Output (Voltage Programmable to 3.0 V or 3.3 V) | AP-O |
| | A19 | LDO_050_3 | 50mA LDO Output #3 (Voltage Range: 0.75-3.7 V) | AP-O |
| | A20 | NC | No Connect | NC |
| | B16 | LDO_050_2 | 50mA LDO Output #2 (Voltage Range: 0.75-3.7 V) | AP-O |
| | A21 | LDO_IN2 | Input Voltage to LDO_050_0, LDO_050_1, LDO_050_2 and LDO_050_3 | AP-I |
| | B17 | LDO_050_1 | 50mA LDO Output #1 (Voltage Range: 0.75-3.7 V) | AP-O |
| | A22 | LDO_050_0 | 50mA LDO Output #0 (Voltage Range: 0.75-3.7 V)<br>Note: This LDO also serves as the internal power source for $I^2S1$, $I^2S2$ and $I^2CS$. The external function of this pin is not affected but the voltage register setting for this LDO will also govern the I/O level for $I^2S1$, $I^2S2$ and $I^2CS$. | AP-O |
| | B18 | LDO_150_2 | 150mA LDO Output #2 (Voltage Range: 0.75-3.7 V) | AP-O |
| | A23 | LDO_IN1 | Input Voltage to LDO_150_0, LDO_150_1 and LDO_150_2 | AP-I |
| | B19 | LDO_150_1 | 150mA LDO Output #1 (Voltage Range: 0.75-3.7 V) | AP-O |
| | A24 | LDO_150_0 | 150mA LDO Output #0 (Voltage Range: 0.75-3.7 V) | AP-O |
| CK_GEN | B20 | 32KHZ_OUT2 | Buffered 32.768kHz Output #2 | D-O |
| | A25 | CKGEN_GND | PLL Analog Ground | GND |
| | B21 | 32KHZ_CLKIN/XTALIN | 32KHZ_CLKIN: External 32.768kHz Clock Input;<br>XTALIN : Input Pin when used with an external crystal | A-I |
| | A26 | XTALOUT/32KHZ_OUT1 | XTALOUT: Output Pin when used with an external crystal<br>32KHZ_OUT1: when XTALIN is connected to a 32kHz input this pin can be a 32kHz Output when CKGEN_PLL_STATUS register, 32KOUT1_EN (bit 4) is set to 1. | A-O |
| | B22 | VDD_CKGEN18 | Filter Capacitor for Internal 1.8V CKGEN LDO | A-IO |
| | A27 | HXTALOUT/TCXO_IN | HXTALOUT: 12 MHz, 13 MHz, 19.2 MHz or 26 MHz output<br>TCXO_IN: External 12 MHz, 13 MHz, 19.2 MHz or 26 MHz clock input | TCXO-D-I |
| | B23 | VDD_CKGEN33 | Filter Capacitor for Internal 3.3V CKGEN LDO | A-IO |
| | A28 | HXTALIN/TCXO_OUT1 | HXTALIN: 12 MHz, 13 MHz, 19.2 MHz, or 26 MHz crystal oscillator input<br>TCXO_OUT1: Buffered HXTALOUT/TCXO_IN Clock Output #1, 32.7638 KHz Output or 24 MHz PLL Output | TCXO-D-O |
| | B24 | TCXO_OUT2 | Buffered HXTALOUT/TXCO_IN Clock Output #2, 12 MHz PLL Output or 48 MHz PLL Output | TCXO-D-O |
| | A29 | SYS_CLK | 12MHz Output or Buffered Output of TCXO_IN | D-O |
| | B25 | CKGEN_GND | PLL Analog Ground | GND |
| | A30 | USB_CLK | 24 MHz or 48 MHz Output | D-O |
| | B26 | VDDIO_CK | Power Supply Input for TCXO_OUT1 and TCXO_OUT2 (1.1V – 1.9V) | AP-I |

 

| MODULE | PIN# | PIN NAME | DESCRIPTION | I/O TYPE |
|---|---|---|---|---|
| I2C_I2S | A31 | EX_ROM | ROM Select. EX_ROM = 1, read contents of external ROM. EX_ROM = 0, read contents of internal ROM into internal shadow memory. | D-I |
| | B27 | DGND | Digital Ground (1) | GND |
| | A32 | I2S_BCLK2 | I²S Bit Clock Channel 2 | D-I |
| | B28 | I2S_WS2 | I²S Word Select (Left/Right) Channel 2 | D-I |
| | A33 | I2S_SDIN2 | I²S Serial Data IN Channel 2 | D-I |
| | B29 | I2S_SDOUT2 | I²S Serial Data OUT Channel 2 | D-O |
| | A34 | I2S_WS1 | I²S Word Select (Left/Right) Channel 1 | D-I |
| | B30 | I2S_BCLK1 | I²S Bit Clock Channel 1 | D-I |
| | A35 | NC | No Connect | NC |
| | A36 | NC | No Connect | NC |
| | A37 | I2S_SDOUT1 | I²S Serial Data OUT Channel 1 | D-O |
| | A38 | I2S_SDIN1 | I²S Serial Data IN Channel 1 | D-I |
| | B31 | I2CS_SCL | I²C Slave clock | I²C -I/O |
| | A39 | I2CS_SDA | I²C Slave data | I²C -O |
| | B32 | I2CM_SCL | I²C Master clock | I²C -O |
| | A40 | I2CM_SDA | I²C Master data | I²C -I/O |
| | B33 | GND | GND : Ground | GND |
| CLASS_D | A41 | CLASS_D- | Class-D Inverting Output | A-O |
| | B34 | PGND | Ground for Class D BTL Power Stage | GND |
| | A42 | PVDD | Input Power for CLASS_D BTL Power Stage | A-I |
| | B35 | CLASS_D+ | Class-D Non-Inverting Output | A-O |
| DC_DC | A43 | BOOST5_SW2 | BOOST5 Converter Power Switch | AP-O |
| | | | Internally connected to pin A44 (BOOST_SW1) | |
| | B36 | BOOST5_OUT | BOOST5 Converter Output | AP-O |
| | A44 | BOOST5_SW1 | BOOST5 Converter Power Switch | AP-O |
| | | | Internally connected to pin A43 (BOOST_SW2) | |
| | B37 | BOOST5_GND | Ground for BOOST5 Power Supply | AP-I |
| | A45 | BUCK1000_FDBK | BUCK2 Converter #2 - Feedback | AP-I |
| | B38 | BUCK1000_IN | BUCK2 Converter #2 - Input | AP-I |
| | A46 | BUCK1000_OUT | BUCK2 Converter Output #2 – 1000mA | AP-O |
| | B39 | BUCK1000_GND | Ground for BUCK2 Converter #2 | GND |
| | A47 | BUCK500_1_FDBK | BUCK1 Converter #1 – Feedback | AP-I |
| | B40 | BUCK500_1_GND | Ground for BUCK1 Converter #1 | GND |
| | A48 | BUCK500_1_OUT | BUCK1 Converter Output #1 - 500mA | AP-O |
| | B41 | BUCK500_1_IN | BUCK1 Converter #1 Input | AP-I |
| | A49 | BUCK500_0_FDBK | BUCK0 Converter #0 feedback | AP-I |
| | B42 | BUCK500_0_GND | Ground for BUCK0 Converter #0 | GND |
| | A50 | BUCK500_0_OUT | BUCK0 Converter Output #0 - 500mA | AP-O |
| | B43 | BUCK500_0_IN | BUCK0 Converter #0 Input | AP-I |
| | A51 | LED_BOOST_VSENSE | LED_BOOST Converter Output Voltage Sense Input to PWM Controller | AP-I |
| | B44 | LED_BOOST_VIN | LED_BOOST Converter GATE BIAS Supply | AP-I |
| | A52 | LED_BOOST_ISENSE | LED_BOOST Converter Output Current Sense Input to PWM Controller | AP-I |
| | B45 | LED_BOOST_GATE | LED_BOOST Converter GATE Drive to Power FET | AP-I |
| | A53 | NC | No Connect | NC |
| | A54 | LED_BOOST_GND | Ground for LED_BOOST | AP-I |
| | A55 | LED_BOOST_SINK1 | LED_BOOST Converter Current Sink for LED String #1 | AP-I |
| | A56 | NC | No Connect | NC |
| | B46 | PSCREF | Power Supply Current Reference | AP-O |
| | A57 | LED_BOOST_SINK2 | LED_BOOST Converter Current Sink for LED String #2 | AP-I |

 

| MODULE | PIN# | PIN NAME | DESCRIPTION | I/O TYPE |
|---|---|---|---|---|
| **HOTSWAP** | B47 | HSCTRL1 | Hot Swap Control Input 1 | D-I |
| | A58 | HSO1 | Hot Swap Output 1 | A-O |
| | B48 | HSPWR | Hot Swap Switches Power Input | AP-I |
| | A59 | HSO2 | Hot Swap Output 2 | A-O |
| | B49 | HSCTRL2 | Hot Swap Control Input 2 | D-I |
| **CHARGER** | A60 | CHRG_GND1 | Pins A60 and B50 are the Power GND Pins for the Switching Regulator in the Charger. Due to their higher current requirement they are internally tied together and must be connected externally at the PC board also. | A-I |
| | B50 | CHRG_GND2 | | A-I |
| | A61 | CHRG_SW1 | Pins A61 and B51connect to the inductor of the switch-mode step-down regulator for the Battery Charger. Due to their higher current requirement they are internally tied together and must be connected externally at the PC board also. | A-O |
| | B51 | CHRG_SW2 | | A-O |
| | A62 | CHRG_INPUT1 | Pins A62 and B52 provide 5V $V_{BUS}$ Input Power from the USB or from an external AC adaptor supply. Due to the pins higher current requirement, they are internally tied together and must be connected externally at the PC board also. | AP-I |
| | B52 | CHRG_INPUT2 | | AP-I |
| | A63 | CHRG_SYSVCC1 | Pins A63 and B53 are System VCC Output ($V_{SYS}$). Due to their higher current requirement they are internally tied together and must be connected externally at the PC board also. | A-O |
| | B53 | CHRG_SYSVCC2 | | A-O |
| | A64 | CHRG_BAT1 | Pins A64 and B64 form the positive battery lead connection to a single cell Li-Ion/Li-Poly battery. Due to their higher current requirement they are internally tied together and must be connected externally at the PC board also. | AP-I/O |
| | B54 | CHRG_BAT2 | | AP-I/O |
| | A65 | CHRG_CLSEN | Input Current Limit Sense/filtering pin for current limit detection | A-I |
| | B55 | CHRG_ICHRG | Current setting. Connect to a current sense resistor | AP-I/O |
| | A66 | CHRG_GATE | Gate Drive for (Optional) External Ideal Diode | A-O |
| | B56 | CHRG_NTC | Thermal Sense, Connect to a battery's thermistor | A-I |
| | A67 | CHRG_VNTC | NTC Power output. This pin provides power to the NTC resistor string. | AP-O |
| | | | This output is automatically CHRG_SYSVCC level but only enabled when NTC measurement is necessary to save power. | |
| | B57 | GND_BAT/ADCGND | GND_BAT and ADCGND: Shared analog ground pin for battery charger and ADC. | GND |
| **GPIO_TSC** | A68 | DGND | Digital Ground | GND |
| | B58 | POR_OUT | Power-On-Reset Output, Active Low | GPIO-OUT |
| | A69 | SW_DET | Switch Detect Input | GPIO |
| | B59 | GPIO1/SW_OUT/ PENDOWN | GPIO 1: General Purpose I/O # 1 | GPIO |
| | | | SW_OUT: Switch Detect Output | |
| | | | PENDOWN: PENDOWN Detect Output | |
| | A70 | GPIO3/LED2 | GPIO 3: General Purpose I/O # 3 | GPIO |
| | | | LED2: Charger LED # 2 Indicates charging complete | |
| | B60 | GPIO2/LED1 | GPIO 2: General Purpose I/O # 2 | GPIO |
| | | | LED1: Charger LED # 1 Indicates charging in progress | |
| | A71 | NC | No Connect | NC |
| | A72 | GPIO4/CHRG_ILIM | GPIO 4: General Purpose I/O # 4<br>CHRG_ILIM: Control the limit of the Charger Pre-Regulator.<br>CHRG_ILIM = 0, limit current to 500mA; CHRG_ILIM = 1, limit current to 1.5A. | GPIO |
| **Thermal** | EP | Exposed Paddle | Exposed paddle (package bottom). Connect to GND. The exposed thermal paddle should be connected to board ground plane. The ground plane should include a large exposed copper pad under the package for thermal dissipation. | GND |

 

# I/O Type Description

**Table 10. I/O Type Description**

| I/O TYPE | DESCRIPTION |
|---|---|
| A-I, A-O and A-IO | **Analog Levels**: Input, Output and Input/Output |
| AP-I, AP-O and AP-I/O | **Power Supply**: Input, Output and Input/Output |
| D-I, D-O | **Digital Levels**: Input, Output<br>Voltage levels are all digital levels (nominally 3.3V) |
| GND | **Ground**: Any connection to Ground |
| GPIO-IN, GPIO-OUT, GPIO | **General Purpose**: Input, Output, Input/Output.<br>Inputs are 3.3V<br>GPIO1, GPIO2, GPIO3 and GPIO5 can be configured as open drain output.<br>GPIO4, GPIO6, GPIO7, GPIO8, GPIO9 and GPIO10 can be configured as CMOS output or open drain output. |
| I2C-I, I2C-O and I2CIO | **I²C**: Input, Output and Input/Output<br>Inputs are CMOS<br>Outputs are open-drain. |
| TCXO-D-I, TCXO-D-O, TCXO-IO | **Clock**: Input, Output, Input/Output<br>Inputs are 1.8V, Outputs are 1.1V to 1.9V |

 

# PRODUCT OVERVIEW

The IDTP95020 is an integrated device that combines a microcontroller, power management, battery charging, touch screen controller, system monitoring, clock synthesis, real time clock and audio functionality. All of these subsystems are configured, monitored and controlled by either the on-chip Microcontroller or by an external controller (Application Processor) over an I²C interface. The external Application Processor can monitor and control functions within the IDTP95020 even with the internal Microcontroller enabled. The registers for the various sub functions allow access from more than one controller through an arbitration mechanism implemented in hardware.

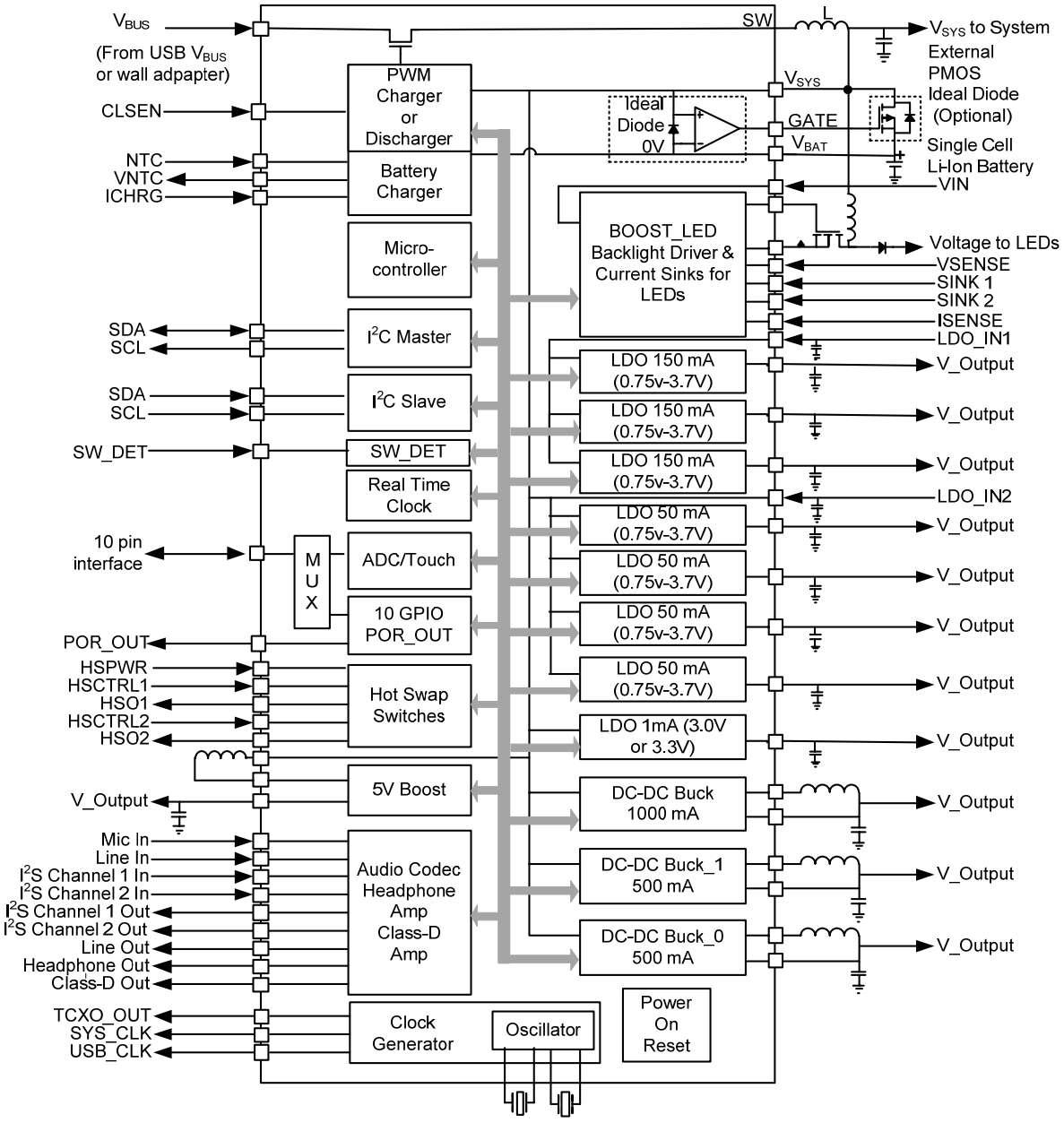


*Figure 3. System Functional Block Diagram*

 

## Functional Modes

There are two primary functional modes for operation: external processor only or simultaneous internal and external processor operation.

***External Processor Control***

In this mode of operation, the external processor can access all internal registers via the I²C interface and receive interrupts via an interrupt pin. The internal Microcontroller can be powered down or clock gated off.

***Combined Internal and External Processor Operation***

In this mode of operation, the Microcontroller in the IDTP95020 will function autonomously or semi-autonomously based on the content of the on-board or external ROM. The external Application Processor may or may not perform additional control functions through the I²C bus interface. Individual time-based or event-based interrupts generated inside the IDTP95020 device may be routed internally or externally to be handled separately. All I²C registers can be simultaneously accessed by either the external Application Processor or the internal Microcontroller. Access to the I²C registers is arbitrated via on-chip hardware arbitration.

## Register Map

All the IDTP95020 control and status registers accessible to the Microprocessor are mapped to a 1024 location address space. This address space maps to:

- 4 x 256 Bytes of I²C pages for the I²C slave interface
- 1024 consecutive addresses in the embedded Microprocessor address space

For easy access from the I²C slave interface (by default 256 Bytes oriented) the first 16 registers of each page are global for all the pages.

Each Module is allocated a consecutive address space.

Register address computation:
Address = Base Address + Offset Address

The Base addresses (for both I²C and embedded µP) are listed in the following table. The Offset addresses are defined in different functional Modules. The offset address is labeled as “Offset Address” in the Module Register definition sections.

**Table 11 – Register Address Global Mapping**

| MODULE | SIZE (BYTES) | BASE ADDRESS (I²C) | BASE ADDRESS (6811 µP) | REGISTER DEFINITION LOCATION | MODULE DESCRIPTION |
|---|---|---|---|---|---|
| Global Registers | 16 | Page-x: 000(0x00) | 0xA000 | Page 146 | Global registers are used by the Access Manager, the first 16 registers of each page are global for all the pages. |
| ACCM | 16 | Page-0: 016(0x10) | 0xA010 | Page 151 | Access manager, including an I²C slave and bus arbiter |
| PCON | 32 | Page-0: 032(0x20) | 0xA020 | Page 133 | Power controller, including registers that control the on/off of the regulators, and control/sense of the GPIO, power states |
| | | | | Page 76 | Clock Generator Registers |
| RTC | 32 | Page-0: 064(0x40) | 0xA040 | Page 79 | Real Time Clock |
| LDO | 32 | Page-0: 096(0x60) | 0xA060 | Page 157 | Linear regulators, including regulators for external and internal usage |
| DC_DC | 16 | Page-0: 128(0x80) | 0xA080 | Page 88 | Switching regulators and Class-D BTL driver consisting of three bucks, one 5V boost , one white LED driver and one Class-D BTL driver |
| CHARGER | 16 | Page-0: 144(0x90) | 0xA090 | Page 62 | Battery Charger, including a dedicated switching buck regulator, an ideal diode, a precision reference and thermal sensor |
| GPT | 16 | Page-0: 160(0xA0) | 0xA0A0 | Page 86 | General purpose timers |
| RESERVED | 16 | Page-0: 176(0xB0) | 0xA0B0 | | RESERVED |

 

| MODULE | SIZE (BYTES) | BASE ADDRESS (I²C) | BASE ADDRESS (6811 μP) | REGISTER DEFINITION LOCATION | MODULE DESCRIPTION |
|---|---|---|---|---|---|
| ADC_TSC | 64 | Page-0: 192(0xC0) | 0xA0C0 | Page 119 | Touch-screen (ADC, pendown detect and switches, temperature and battery voltage monitoring), and GPIOs |
| AUDIO | 240 | Page-1: 000(0x00) | 0xA100 | Page 39 | Audio subsystem, excluding class-D amplifier |
| CLASS_D_DIG | 240 | Page-2: 000(0x00) | 0xA200 | Page 29 | Class-D amplifier digital processing part |
| RESERVED | 240 | Page-3: 000(0x00) | 0xA300 | | RESERVED |

## Byte Ordering and Offset

Most registers are defined within one byte width and occupy one byte in the address space. Some registers occupy more than one byte. Please refer to the individual register descriptions for information on how that register is stored in address space.

## Reserved Bit Fields

Bit fields and Bytes labeled *RESERVED* are reserved for future use. When writing to a register containing some *RESERVED* bits, the user should do a "read-modify-write" such that only the bits which are intended to be written are modified.

NOTE: DO NOT WRITE to registers containing all *RESERVED* bits.

## Register Access Types

**Table 11. Register Access Type Description**

| TYPE | DESCRIPTION |
|---|---|
| RW | Readable and Writeable |
| R | Read only |
| RW1C | Readable and Write 1 to this bit to clear it (for interrupt status) |
| RW1A | Readable and Write 1 to this bit to take actions |

 

# AUDIO MODULE

### *Features*

- 4-ch (2 stereo DACs, 2 stereo ADCs), 24-bit
  - Supports full-duplex stereo audio
  - Provides a mono output
- 2.5W mono speaker amplifier @ 4 ohms and 5V
- Stereo cap-less headphone amplifier
- Two digital microphone inputs
  - Mono or stereo operation
  - Up to 4 microphones in a system
- High performance analog mixer
- 2 adjustable analog microphone bias outputs

### *Description*

The audio system is a low power optimized, high fidelity, 4-channel audio codec with integrated Class D speaker amplifier and cap-less headphone amplifier. It provides high quality HD Audio capability for handheld applications.

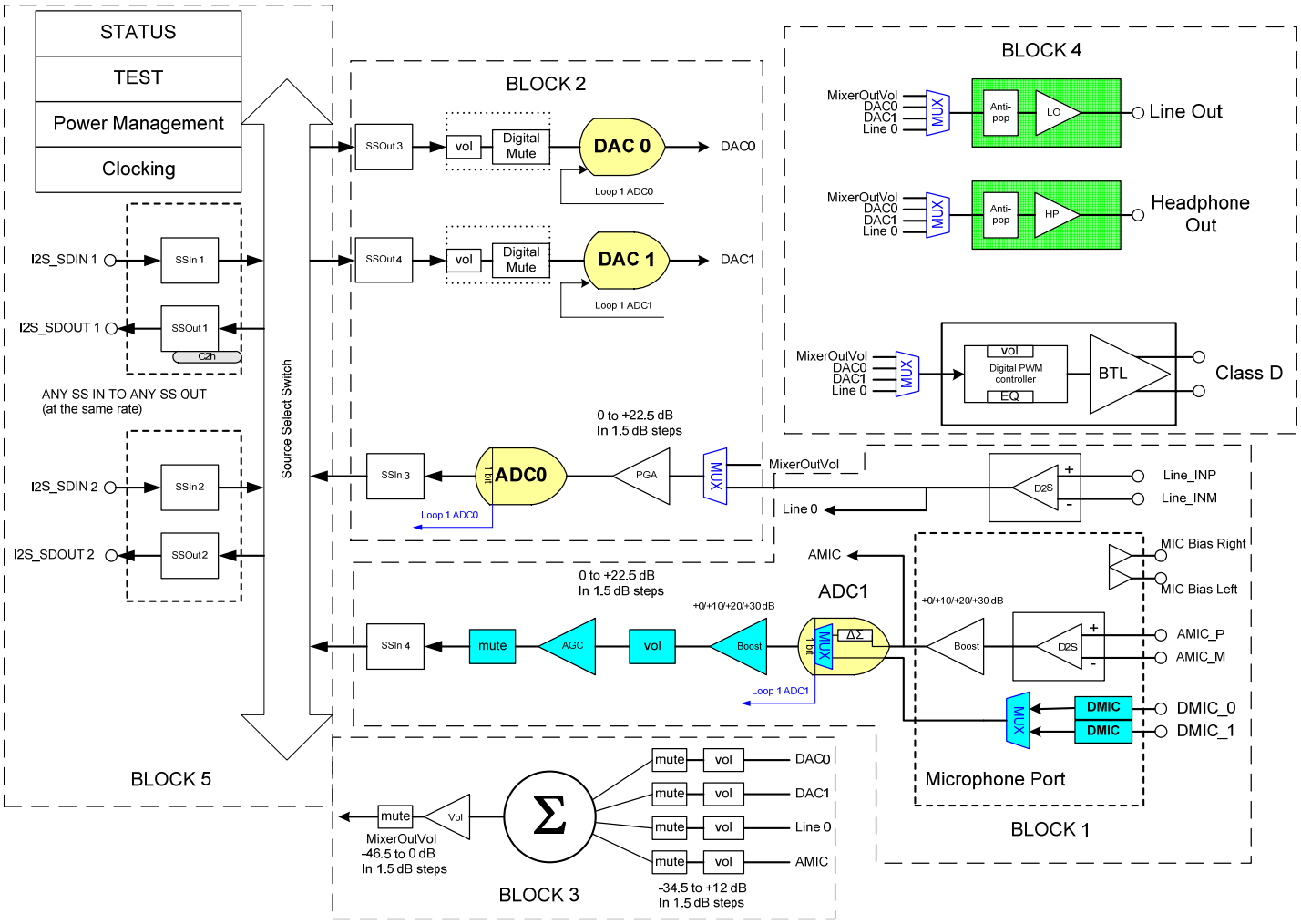


*Figure 4. Audio Block Diagram*

 

## Audio – Pin Definitions

**Table 12. Audio Module Pin Definitions**

| PIN # | PIN_ID | DESCRIPTION |
|---|---|---|
| A5 | MIC_R- | Differential Analog microphone negative input (right channel) |
| B4 | MIC_R+/DMICDAT2 | Differential Analog microphone positive input (right channel) or second digital microphone data input |
| A6 | MICBIAS_R/DMICSEL | Analog microphone supply (right channel) or digital microphone select output (GPO) |
| B5 | MICBIAS_L/DMICCLK | Analog microphone supply (left channel) or digital microphone clock output |
| A7 | MIC_L+/DMICDAT1 | Differential Analog microphone positive input (left channel) or first digital microphone data input |
| B6 | MIC_L- | Differential Analog microphone negative input (left channel) |
| A8 | AFILT2 | ADC filter cap |
| B7 | AFILT1 | ADC filter cap |
| A9 | AGND_MIC | Return path for microphone supply (MICBIAS_L/R ) |
| B8 | LISLP | Differential Analog Line Level positive input (left channel) |
| A10 | LISLM | Differential Analog Line Level negative input (left channel) |
| B9 | LISRP | Differential Analog Line Level positive input (right channel) |
| A11 | LISRM | Differential Analog Line Level negative input (right channel) |
| B10 | LLO_L | Single Ended Line Level Output (Left channel) |
| B11 | LLO_R | Single Ended Line Level Output (Right channel) |
| A12 | AVREF | Analog reference (virtual ground) bypass cap |
| B12 | VDD_AUDIO33 | Filter Capacitor for Internal 3.3V Audio LDO |
| A13 | ADC_REF | ADC reference bypass cap |
| B13 | HP_R | Cap-less headphone output (right channel) |
| A14 | HP_L | Cap-less headphone output (left channel) |
| B14 | AGND | Analog (audio) return |
| A15 | VIRT_GND | Cap-less headphone signal return (virtual ground) |

## Audio – Section Overview

The Audio section is divided into five subsections:

1. Analog Input Buffer and Converter Block
2. DAC, ADC
3. Audio Mixer Block
4. Analog and Class D Output Blocks
5. Sub System Control and Interface Blocks

Note: All register settings are lost when power is removed.

## Audio – Power Up Audio Module

The Audio subsystem is powered by an internal regulator:

- The Audio A/D, D/A converters, Microphone interface and Head phone drivers are powered by an internal 3.3V LDO. The enable/disable control is defined in VDD_AUDIO33 LDO Register (0xA06F).
- The digital processing block is powered by an internal 1.8V LDO. The enable/disable control is defined in VDD_AUDIO18 Register (0xA06E).
- The Class-D driver is powered by the 5V boost converter (connect on the board).

Before enabling power up, pre-configure the Audio clock setting in the PCON MCLK_CFG Register (0xA037). The LDO will automatically assert/de-assert the reset signal for Audio digital when the Audio LDOs are powered up. Audio logic can also be explicitly reset by programming the Audio reset control bit AUDIO_RST, defined in PCON Audio Control Register (0xA038).

The Audio function can be enabled or disabled by the PCON Audio Control Register (0xA038). Disabled Audio will stay in low power state. In disabled mode, the clock is stopped and the Audio registers cannot be accessed, but will retain pre-configured values.

 

## Audio – Analog Performance Characteristics

Unless otherwise specified, typical values at $T_A$ = 25°C, VSYS = 5V, VCC_AUDIO33 = 3.3V, VDD_AUDIO18 = 1.8V, AGND = DGND = 0V, 1 kHz input sine wave, Sample Frequency = 48 kHz, 0 dB = 1 $V_{RMS}$ into 10 kΩ.

**Table 13. Audio Module Analog Performance Characteristics**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Full Scale Input Voltage:** | | | | | |
| All Analog Inputs except Mic (0 dB gain) | | | 1.0 | | Vrms |
| Differential Mic Inputs (+30dB gain) | | | 30.0 | | mVrms |
| Differential Mic Inputs (0 dB gain) | | | 1.0 | | Vrms |
| **Full Scale Output Voltage:** | | | | | |
| Line Input to Line Output | | | 1.0 | | Vrms |
| HP Output | Per channel / 16 ohm load | | 0.707 | | Vrms |
| PCM (DAC) to LINE_OUT | | | 1.0 | | Vrms |
| Headphone output power | Per channel / 16 ohm load | 45 | 50 | 55 | mWpk |
| Analog Frequency Response | ± 1 dB limits. The max frequency response is 40 kHz if the sample rate is 96 kHz or more. | 10 | | 30,000 | Hz |
| **Digital S/N** | The ratio of the rms output level with 1 kHz full scale input to the rms output level with all zeros into the digital input. Measured "A weighted" over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise ratio) – At Line_Out pins. | | | | |
| D/A PCM (DAC) to LINE_OUT | | | 95 | | dB |
| A/D LINE_IN to PCM | | | 90 | | dB |
| Dynamic Range: -60dB signal level | Ratio of Full Scale signal to noise output with -60 dB signal, measured "A weighted" over a 20 Hz to a 20 kHz bandwidth. | | | | |
| LINE_IN to LINE_OUT (direct) | | | 98 | | dB |
| LINE_IN to LINE_OUT (mixer) | | | 95 | | dB |
| LINE_IN to HP (direct) | | | 90 | | dB |
| LINE_IN to HP (mixer) | | | 90 | | dB |
| DAC to LINE_OUT | | | 93 | | dB |
| LINE_IN to A/D | | | 90 | | dB |
| **Total Harmonic Distortion:** | THD+N ratio as defined in AES17 and outlined in AES6id, non-weighted, at 1 kHz. Tested at -3 dB FS or equivalent for analog only paths. 0 dB gain ( PCM data -3 dB FS, analog input set to achieve -3 dB full scale port output level) | | | | |
| LINE_IN to LINE_OUT (direct) | | | 90 | | dB |
| LINE_IN to LINE_OUT (mixer) | | | 80 | | dB |
| DAC to LINE_OUT | | | 85 | | dB |
| DAC to HP (10 KΩ) | | | 80 | | dB |
| DAC to HP (16 Ω) | | | 55 | | dB |
| LINE_IN to ADC | | | 80 | | dB |
| AMIC to ADC | | | 80 | | dB |
| D/A Frequency Response | ± 0.25 dB limits. The D/A freq. response becomes 40 kHz with sampling rates > 96 kHz. At ±3 dB the response range is from 20-22,500 Hz at 48 kHz, or 20-20,000 Hz @ 44.1 kHz or 20-45,000 Hz @ 96 kHz. | 18 | | 22,000 | Hz |
| A/D Frequency Response | | 20 | | 20,000 | Hz |
| Transition Band | Transition band is 40-60% of sample rate. | 19,200 | | 28,800 | Hz |
| Stop Band | Stop band begins at 60% of sample rate | 28,800 | | | Hz |
| Stop Band Rejection | | 85 | | | dB |
| Out-of-Band Rejection | The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output. | 45 | | | dB |

 

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Power Supply Rejection Ratio (1 kHz) | | 70 | | | dB |
| Crosstalk between Input channels | | | | 85 | dB |
| DAC Volume/Gain Step Size | | | 0.75 | | dB |
| ADC/Mixer Volume/Gain Step Size | | | 1.5 | | dB |
| Analog Mic Boost Step Size | | | 10 | | dB |
| Input Impedance | | | 50 | | kΩ |
| Differential Input Impedance | | | 20 | | kΩ |
| Input Capacitance | | | 15 | | pF |
| Mic Bias | | | 2.97 | | V |
| External Load Impedance | | 6 | | | kΩ |

## Audio – Microphone Input Port

The microphone input port supports either analog or digital microphones. The analog and digital modes share pins so only one mode is supported in a typical application.

### *Analog Microphone Input Mode*

The Analog Microphone input path consists of:

- Stereo Differential Input Analog Microphone Buffer
- L/R swap
- Mono or stereo
- Microphone Bias Generator with 2 independent bias outputs.
- Microphone Boost Amplifier with selectable gain of 10, 20, or 30dB

The analog microphone interface provides a stereo differential input for supporting common electret cartridge microphones in a balanced configuration (a single-ended configuration is also supported). A boost amplifier provides up to 30dB of gain to align typical microphone full scale outputs to the ADC input range. The microphone input is then routed to both ADC1 and the analog mixer for further processing. By using the analog mixer the analog microphone input may be routed to ADC0, the line output port or the headphone output port.

### *Digital Microphone Input Mode*

The Digital Microphone input path consists of an input buffer and MUX with the following features:

- One or two microphones per DMICDATx input.
- Mono data sampled during high or low clock level.
- L/R swap
- Versatile DMICSEL output pin for control of digital microphone modules or other external circuitry. (Used primarily to enable/disable microphones that do not support power management using the clock pin.)

The digital microphone interface permits connection of a digital microphone(s) via the DMICDAT1, DMICDAT2, and DMICCLK 3-pin interface. The DMICDAT1 and DMICDAT2 signals are inputs that carry individual channels of digital microphone data to the ADC. In the event that a single microphone is used, the data is ported to both ADC channels. This mode is selected using a register setting and the left time slot is copied to the ADC left and right inputs. The digital microphone input is only available at ADC1.

The DMICCLK output is controllable from 4.704 MHz, 3.528 MHz, 2.352 MHz, 1.176 MHz and is synchronous to the internal master clock (MCLK). The default frequency is 2.352 MHz.

To conserve power, the analog portion of the ADC and the analog boost amplifier will be turned off if the D-mic input is selected. When switching from the digital microphone to an analog input to the ADC, the analog portion of the ADC will be brought back to a full power state and allowed to stabilize before switching from the digital microphone to the analog input in less than 10ms.

 

The IDTP95020 codec supports the following digital microphone configurations:

**Table 14. Valid Digital Mic Configurations**

| MODE | DIGITAL MICS | DATA SAMPLE | INPUT | NOTES |
|---|---|---|---|---|
| 0 | 0 | N/A | N/A | No Digital Microphones (1010 bit pattern sent to ADC to avoid pops) |
| 1 | 2 | Double Edge | DMICDAT1 | Two microphones connected to DMICDAT1. PhAdj settings apply to Left microphone. Right Microphone sampled on opposite phase. DMICDAT2 ignored. |
| 2 | 2 | Double Edge | DMICDAT2 | Two microphones connected to DMICDAT2. PhAdj settings apply to Left microphone. Right Microphone sampled on opposite phase. DMICDAT1 ignored. |
| 3 | 2 | Single Edge | DMICDAT1 and DMICDAT2 | DMICDAT1 used for left data and DMICDAT2 used for right data. |
| 3 | 2 | Double Edge | DMICDAT1 and DMICDAT2 | Two microphones, one on each data input. "Left" microphone used for each channel. Two "Right" microphones may be used by inverting the microphone clock or adjusting the sample phase. |

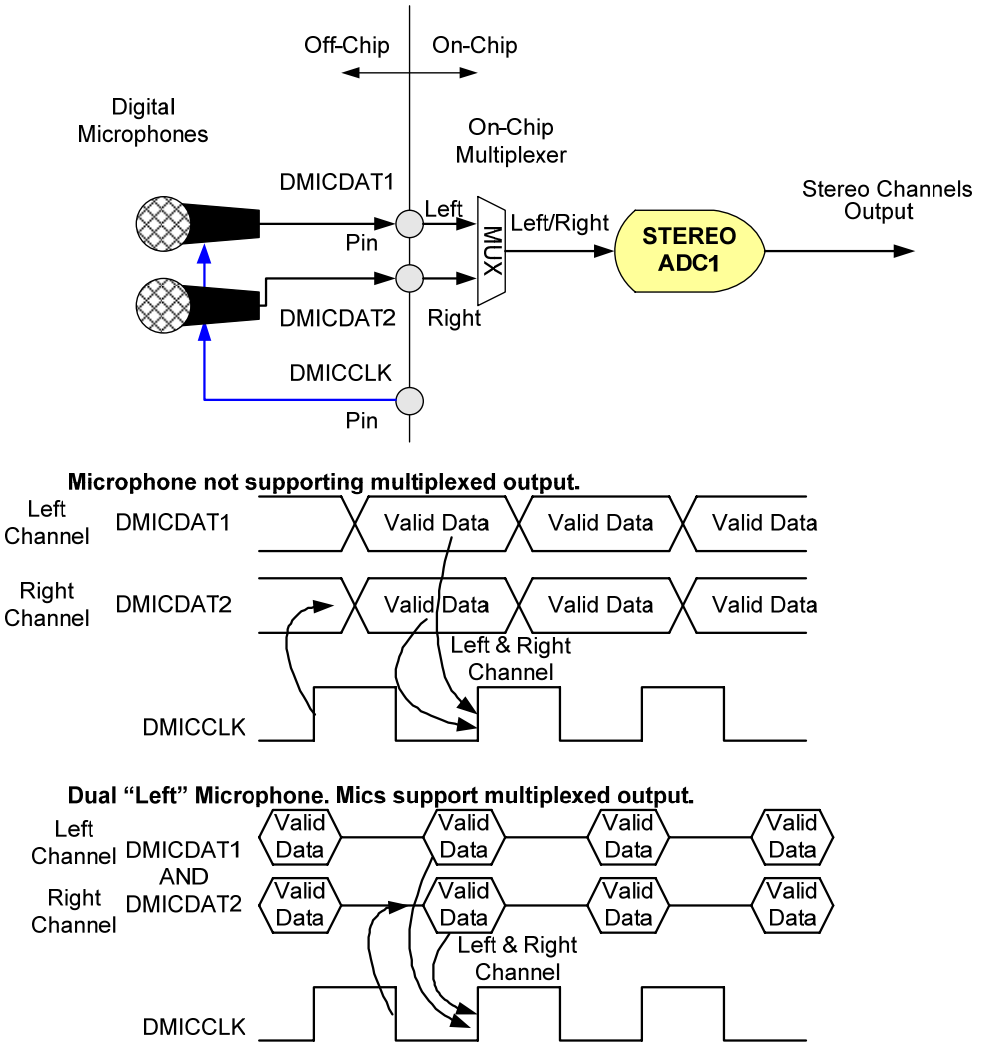


*Figure 5. Stereo Digital Microphone (Mode 3)*

 

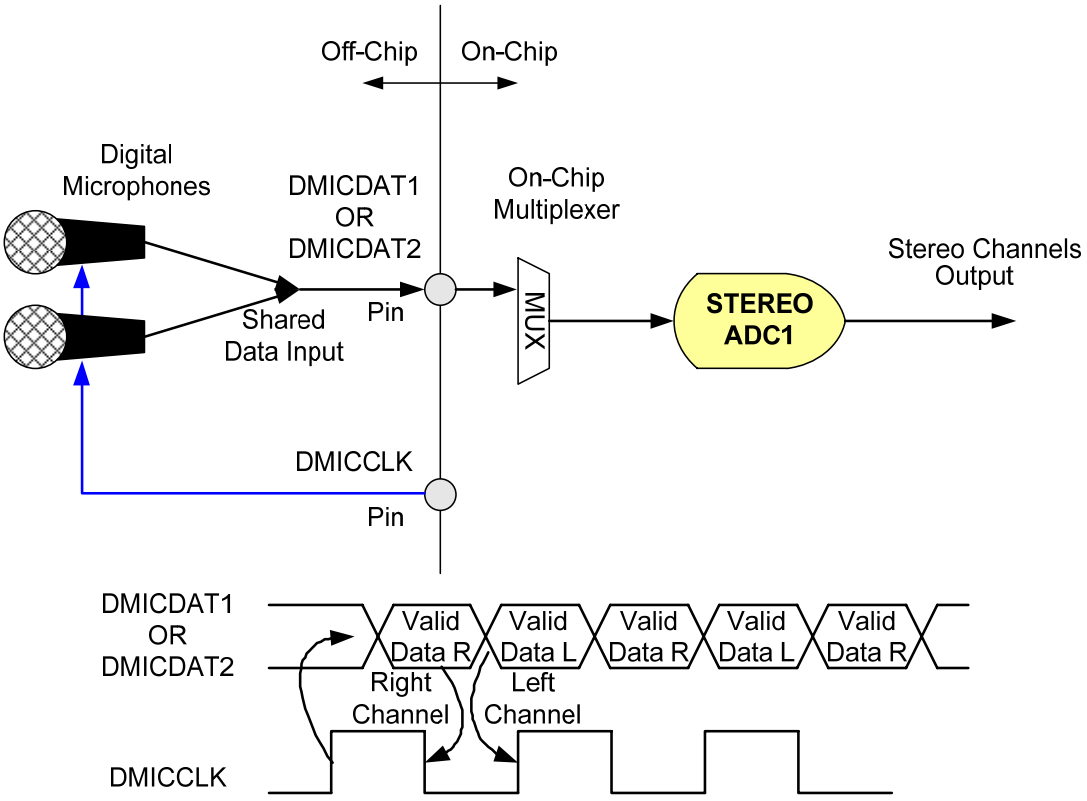


*Figure 6. Stereo Digital Microphone (Mode 1 and 2)*

## Audio – Analog Line Input

The Analog Line Input path consists of a stereo differential input analog buffer that is routed to the analog mixer and ADC0. By using the analog mixer, the analog line input may be routed to ADC0, the line output port or the headphone output port.

## Audio – DAC, ADC

There are 2 stereo DACs and 2 stereo ADCs. All converters support sample rates of 8kHz, 11.025khz, 12kHz, 22.050kHz, 16kHz, 24kHz, 44.1kHz, 48kHz, 88.2kHz, and 96kHz. Word lengths of 16, 20 and 24-bits are selectable.

### *DAC 0/1*

The DAC sample rate and word length are programmed at the I²S input port and the DAC may select either I²S port as the data source.

Digital volume control provides -95.25 dB to 0dB gain in 0.75 dB steps and mute. The output of DAC0 and DAC1 is sent to the analog mixer, the headphone output and the line output.

### *ADC 0/1*

Each ADC includes a high pass filter to remove DC offsets present in the input path. Sample rate, word length, and source ADC are programmed at the I²S output port. If an ADC is selected as the audio data source for more than one audio data sink (I²S output or DAC) then the rates must be programmed the same at all sinks (see Figure 4 blocks 4 and 5). If the rates are not identical, then the highest priority sink will dominate (I2S_SDOUT1, I2S_SDOUT2, DAC0 and DAC1). The other sink will be muted under these circumstances. ADC0 includes an analog amplifier (0-22.5dB gain in 1.5dB steps) and a multiplexer to select between the line input path or the analog mixer output.

Note: There is only 1 L/R clock per I²S I/O port. Therefore, the input and output rates for that port match.

 

## Audio – Automatic Gain Control

The IDTP95020 incorporates digital automatic gain control in the ADC1 record path to help maintain a constant record level for voice recordings. The AGC maintains the recording level by monitoring the output of the ADC and adjusting the Boost (analog for analog microphone path or digital for digital microphone path) and digital record gain to compensate for varying input levels. While the AGC is enabled, the digital record gain and boost register values are ignored.

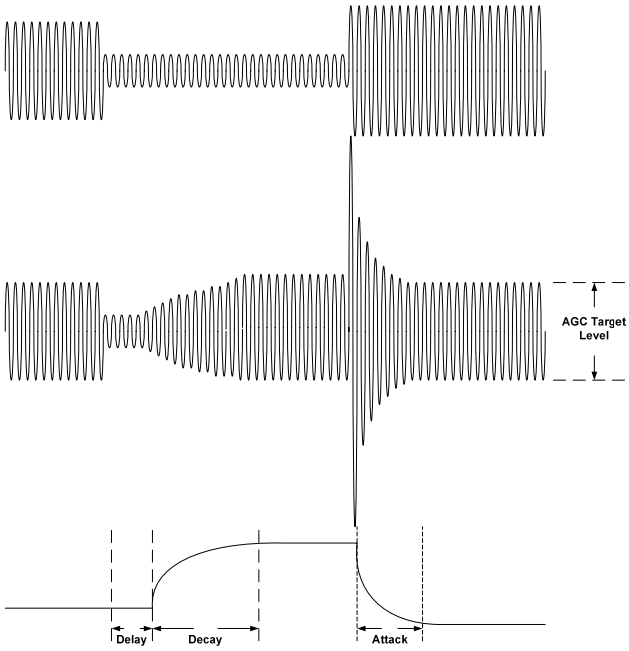


*Figure 7 – Automatic Gain Control*

The AGC target level may be set from -1.5 dB to -22.5 dB relative to the ADC full scale output code in 1.5 dB steps. The maximum gain allowed may be programmed to prevent the AGC from using the entire gain range. The AGC may be applied to either both channels or only the right or left channel. The AGC uses both channels to determine proper record level unless only one channel is selected. When only one channel is enabled, the other channel is ignored and that channel's gain is controlled by its record gain and boost register values.

Delay time is the amount of delay between when the peak record level falls below the target level and when the AGC starts to adjust gain. The delay time may be set from 0 ms to 5.9 seconds in 16 steps. Each step is twice as long as the previous step where 0 is the first step.

Each additional step may be calculated by:

$((8*2^n)/44100)$ seconds

where *n* is the register value from 1 to 15

Decay time is the time that the AGC takes to ramp up across its gain range. The time needed to adjust the recording level depends on the decay time and the amount of gain adjustment needed. If the input level is close to the target level then a relatively small gain adjustment will be needed and will take much less than the programmed decay time. Decay time is adjustable from 23.2 ms to 23.8 seconds and may be calculated as $(2^{n+10}/44100)$ where *n* is the register value from 0 to 10. Register values above 10 set the decay to 23.8 seconds.

Attack time is the time that it takes the AGC to ramp down across its gain range. As with the decay time, the actual time needed to reach the target recording level depends on the attack time and the gain adjustment needed. The attack time is adjustable from 5.8 ms to 5.9 seconds and may be calculated as $(2^{n+8}/44100)$ where *n* is the register value from 0 to 10. Register values above 10 set the decay to 5.9 seconds.

The IDTP95020 also provides a peak limiter function. When the AGC is on, quiet passages will cause the gain to be set to the maximum level allowed. When a large input signal follows a quiet passage, many samples will become clipped as the AGC adjusts the gain to reach the target record level. Long attack times aggravate this situation. To reduce the number of clipped samples the peak limiter will force the attack rate to be as fast as possible (equivalent to zero (0) value in the attack register) until the record level is 87.5% of full scale or less.

To prevent excessive hiss during quiet periods, a signal threshold level may be programmed to prevent the AGC circuit from increasing the gain in the absence of audio. This is often referred to as a 'noise gate' or 'squelch' function. The signal threshold may be programmed from -72 dB FS to -24 dB FS in 1.5 dB increments.

Under some circumstances, it is desirable to force a minimum amount of gain in the record path. When the AGC is in use, the minimum gain may be set from 0 to 30 dB to compensate for microphone sensitivity or other needs.

 

## Audio – Analog Mixer Block

The Audio subsection implements an analog mixing block for use as an input or output mixer.

The Audio Mixer Block consists of:

- Input Volume Controls
- DAC0
- DAC1
- Line Input
- Analog Mic (in analog mic mode only)
- Master Volume Control

The analog mixer has 4 input sources. Each input has an independent volume control that provides gain from -34.5 dB to +12 dB (1.5 dB steps) and mute. After mixing, the output may be attenuated up to 46.5 dB (1.5 dB steps) before being sent to ADC0, the headphone output port and the line output port.

## Audio – Digital Audio Input / Output Interface

The Digital Audio Input/ Output Interface consists of:

- Dual I²S input/output interface with independent bit rate/depth.
- Each I²S input/output pair will operate at same bit rate/depth.

## Audio – Subsystem Clocking

The audio subsystem generates clocks by a PLL inside the audio block. The PLL input is normally from the 48MHz clock from the Clock Generator Module. Optionally, PLL input can be selected from a programmable MCLK from external input (GPIO9 or I2S_BCLK2). MCLK is shared and may be programmed for 64, 128, 256, or 384 times the base rate (44.1 kHz or 48 kHz). The MCLK is used to align the I²S port signals to the host.

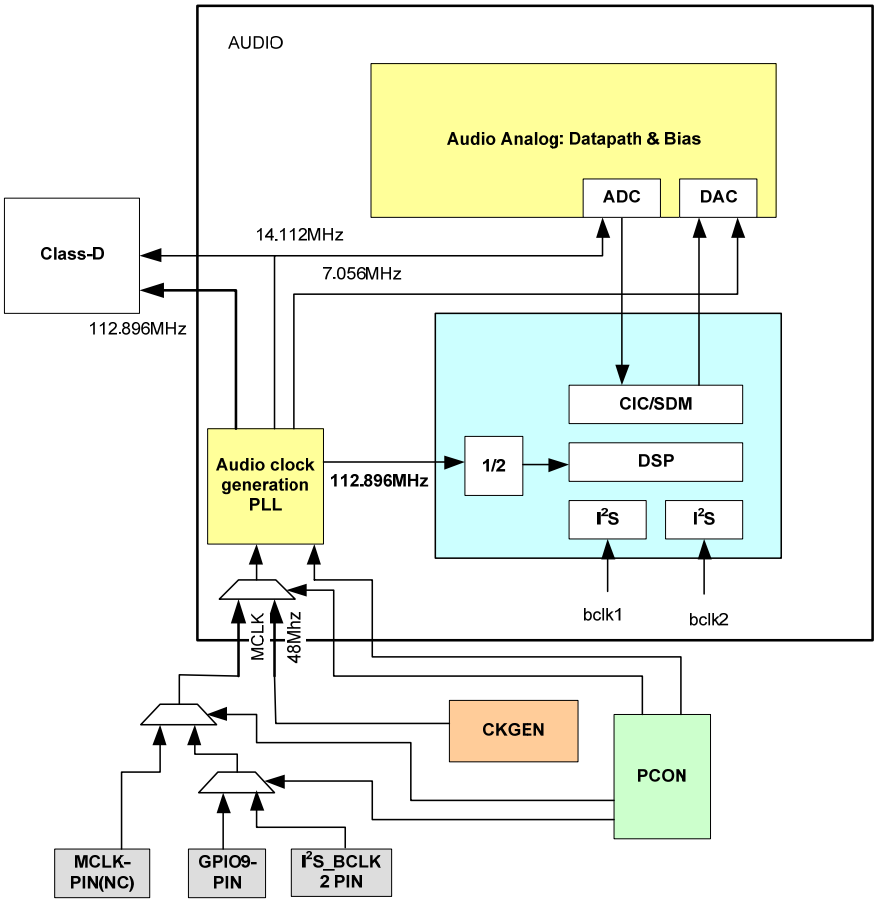


*Figure 8. Audio Subsystem Clock Diagram*

 