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OVERVIEW

The **P95020** is designed to provide maximum flexibility to system designers by providing full customization and programmability. It is the first of a new generation of standardized application-specific controllers that incorporates a general purpose microcontroller, a high fidelity audio CODEC including headphone outputs and a 2.5W Class D audio amplifier, full power management functionality, a touch screen controller and a real time clock all of which are required by portable consumer devices such as cellular phone handsets, portable gaming devices, digital media players, portable navigational devices, etc.

The general purpose microcontroller controls the device power-on/power-off sequencing and can also be used for general system housekeeping.

The P95020 includes two I²C Interfaces, a master for communicating with an external EEPROM and a slave for communicating with the host.

The high fidelity audio CODEC along with headphone outputs and the 2.5 watt Class D audio speaker amplifier comprise a total audio solution for portable applications.

The switch-mode EnergyPath™ Battery Charger operates with its own high efficiency buck regulator to transmit the 2.5 watts available from a USB port to the system with minimal wasted power. It can also handle up to 2A from a wall charger.

Its power management features along with switch-mode converters and LDOs should be sufficient to provide power for even the most complex hand-held devices.

The integrated touch screen controller allows adding touch screen capability to devices at significantly reduced cost.

It also includes IDT's high quality, low power real time clock.

APPLICATIONS

Smart Phones
Portable Gaming Device
Digital Media Players
Portable Navigational Devices

KEY FEATURES

Quick Turn Customization

Embedded Microcontroller

- Master Controller during Power Up & Power-Down
  - Initialization and power sequencing
- Dynamic Power Management via I²C bus interface
- Up to 10 General Purpose I/Os available
- General house keeping for P95020 and other devices

Audio Features

- 4 Channel CODEC with 24-bit resolution and internal registers for status and control
- Integrated 2.5 Watt Mono Class D Amplifier with Filterless Operation.
- Stereo cap-less headphone driver
- Differential Analog Audio Line Inputs
- Dual Mode Microphone Inputs (Analog or DMIC)

Battery Charging Circuit

- Autonomous Li-Ion/Li-Poly charger up to 1.5A
  - Automatic Load Prioritization
  - Advanced Battery Safety features
- High efficiency switch-mode *EnergyPath™ controller
- USB or Wall-mounted Charging
  - Programmable Current Limit
  - Automatic end-of-charge control
- Internal 180 mΩ ideal diode with external ideal diode controller

Power Management Features

- All Converters:
  - Power up/down sequence field reprogrammable with external EEPROM
  - Dynamic voltage scaling
  - Host or I2C output enable / disable
- Buck DC-DC PWM converters with PFM mode
  - Two at 500mA, 0.75V to 3.7V
  - One at 1000mA, 0.75V to 3.7V
- Boost DC-DC converters
  - One at 1.5 A peak on inductor, 4.05V to 5.0V
  - One LED supply with 2 W total output power
    - Two programmable current sinks, @ 25mA each
    - Voltage limited to rating of external FET & diode
- Linear Regulators
  - Three LDOs at 150mA, 0.75V to 3.7V
  - Four LDOs at 50mA, 0.7V to 3.7V
  - One always-on LDO at 10mA, 3.3 or 3.0V

ADC and Touch Screen Controller

- 4-wire touch screen interface
- One direct battery measurement channel
- One direct VSYS measurement channel
- One direct charge current measurement channel
- On-Chip temperature measurement
- Four auxiliary analog input channels (shared with GPIO pins)
- Touch pressure measurement
- Sample rate: 62.5k SPS
- 12 bit resolution, DNL: -1~+2 LSB, INL: +-2
- On-chip 2.5V reference

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BLOCK DIAGRAM

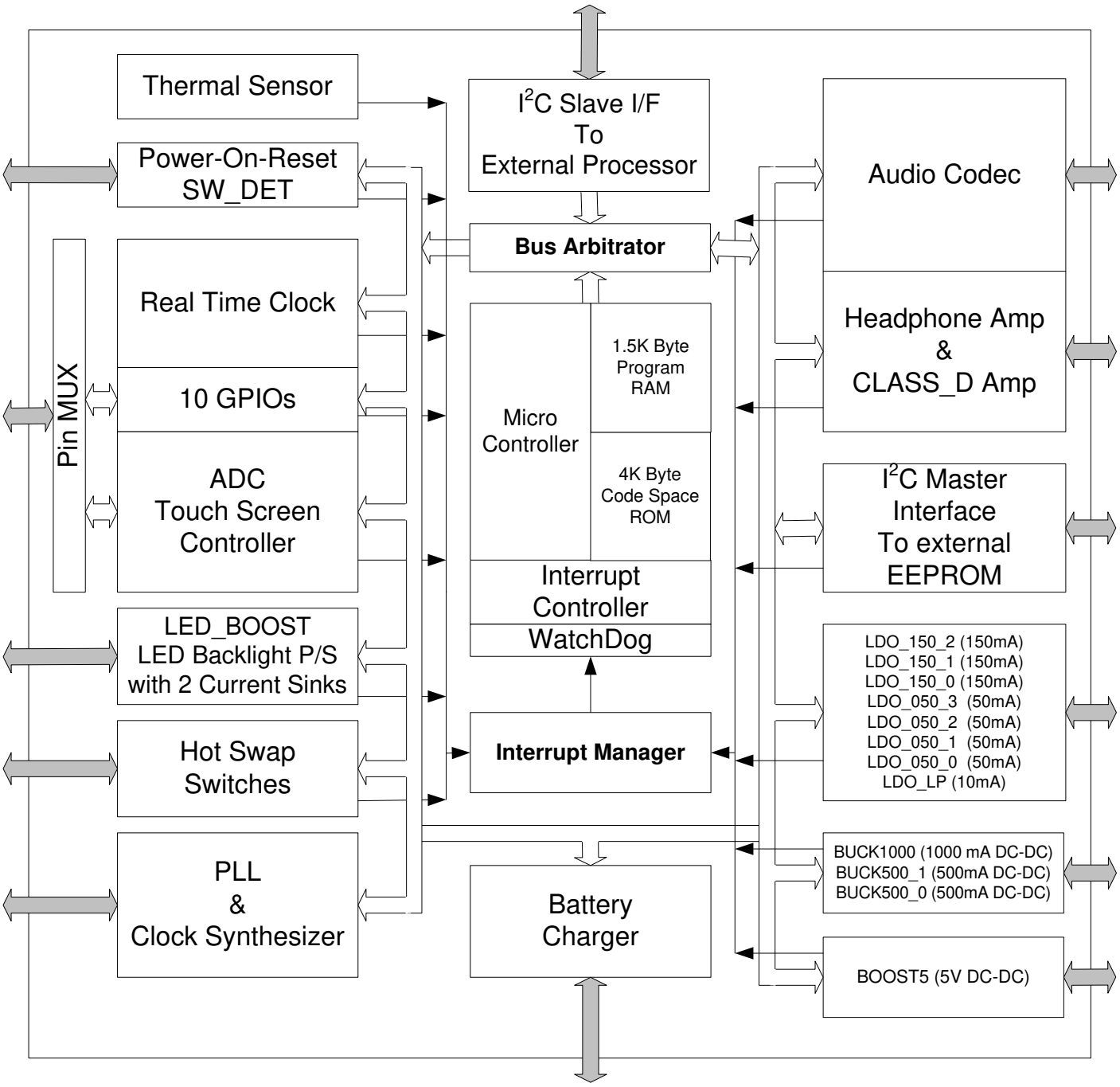

Figure 1 – P95020 Block Diagram.

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TABLE OF CONTENTS

OVERVIEW 1
APPLICATIONS 1
KEY FEATURES 1
BLOCK DIAGRAM 2
PIN ASSIGNMENTS 7
PIN FUNCTIONS BY PIN NUMBER 9
I/O LEVELS BY TYPE 14
ABSOLUTE MAXIMUM RATINGS 15
RECOMMENDED OPERATING CONDITIONS 16
DIGITAL INTERFACES - DC ELECTRICAL CHARACTERISTICS 16
I2C MASTER - ELECTRICAL CHARACTERISTICS 16
I2C SLAVE - ELECTRICAL CHARACTERISTICS 16
I2S - ELECTRICAL CHARACTERISTICS 16
GPIO - ELECTRICAL CHARACTERISTICS 16
AUDIO POWER CONSUMPTION 17
1.0 OVERVIEW 18
1.1 FUNCTIONAL MODES 19
1.2 REGISTER MAP 20
1.3 BYTE ORDERING AND OFFSET 21
1.4 REGISTER ACCESS TYPES 21
1.5 RESERVED BIT FIELDS 21
2.0 AUDIO MODULE 22
2.1 AUDIO - PIN DEFINITIONS 22
2.2 AUDIO - SECTION OVERVIEW 23
2.3 AUDIO - ANALOG PERFORMANCE CHARACTERISTICS 23
2.4 AUDIO - MICROPHONE INPUT PORT 24
2.5 AUDIO - ANALOG LINE INPUT 27
2.6 AUDIO - DAC, ADC 27
2.7 AUDIO - AUTOMATIC GAIN CONTROL 28
2.8 AUDIO - ANALOG MIXER BLOCK 28
2.9 AUDIO - DIGITAL AUDIO INPUT/OUTPUT INTERFACE 29
2.10 AUDIO - REFERENCE VOLTAGE GENERATOR, BUFFER, & FILTERING CAPS 31
2.11 AUDIO - ANALOG AND CLASS D OUTPUT BLOCK 31
2.12 AUDIO - CLASS-D BTL AMPLIFIER 32
2.13 AUDIO CLASS_D - REGISTERS 32
2.14 AUDIO CLASS_D - EQUALIZER COEFFICIENT & PRESCALER RAM (EQRAM) 39
2.15 AUDIO – AUDIO CONTROL REGISTERS 40
3.0 CHARGER MODULE 52
3.1 CHARGER - OVERVIEW 52
3.2 CHARGER – SUB-BLOCKS 52
3.3 CHARGER – DC ELECTRICAL CHARACTERISTICS 53
3.4 CHARGER – TYPICAL PERFORMANCE CHARACTERISTICS 54
3.5 CHARGER - REGISTER ADDRESSES 55
3.6 CHARGER - PRE-REGULATOR 58
3.7 IDEAL DIODE FROM V_{BAT} TO V_{SYS} 59
3.8 CHARGER - CHARGER/DISCHARGER 60
3.9 CHARGER - THERMAL MONITORING 60
3.10 CHARGER - POWER ON RESET 60
4.0 CLOCK GENERATOR MODULE 61
4.1 CKGEN - PIN DEFINITIONS 61
4.2 CKGEN - OSCILLATOR CIRCUIT ELECTRICAL CHARACTERISTICS 62
4.3 CKGEN - PLL CONTROL 63
4.4 CKGEN – OSCILLATOR CIRCUIT 63
4.5 CKGEN - CKGEN POWER SOURCE 63
4.6 CKGEN – CLOCK ACCURACY 63
4.7 CKGEN – CLOCK GENERATOR REGISTERS 64

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5.0 RTC MODULE 66
5.1 RTC - GENERAL DESCRIPTION 66
5.2 RTC - TIMEKEEPER REGISTERS 67
5.3 RTC - DATE REGISTERS 67
5.4 RTC - ALARM REGISTERS 68
5.5 RTC - INTERRUPT REGISTERS 69
5.6 RTC RESERVED REGISTERS 70
6.0 GENERAL PURPOSE TIMERS 71
6.1 GENERAL PURPOSE TIMERS – GENERAL DESCRIPTION 71
6.2 GENERAL PURPOSE TIMERS – REGISTERS 71
7.0 DC_DC MODULE 74
8.0 2MHz, 500mA & 1000mA SYNCHRONOUS BUCK REGULATORS 75
8.1 BUCK1000 & BUCK500 - PIN DEFINITIONS 76
8.2 BUCK1000 & BUCK500 - ELECTRICAL CHARACTERISTICS 76
8.3 BUCK CONVERTERS – TYPICAL PERFORMANCE CHARACTERISTICS 77
8.4 BUCK1000 & BUCK500 - REGISTER ADDRESSES 79
8.5 BUCK1000 & BUCK500 - ENABLING & DISABLING 80
8.6 BUCK1000 & BUCK500 - APPLICATIONS INFORMATION 81
9.0 HIGH EFFICIENCY 10 LED BOOST CONVERTER AND SINKS 83
9.1 LED_BOOST - ELECTRICAL CHARACTERISTICS 84
9.2 LED_BOOST – TYPICAL PERFORMANCE CHARACTERISTICS 84
9.3 LED_BOOST - REGISTER SETTINGS 85
9.4 LED_BOOST - ENABLING & DISABLING 86
9.5 LED_BOOST – Over-Voltage Protection 87
9.6 LED_BOOST – Over-Current Limiter 87
9.7 LED_BOOST - APPLICATIONS INFORMATION 87
10.0 BOOST5 – 1.5A, SYNCHRONOUS PWM BOOST CONVERTER 89
10.1 BOOST5 - ELECTRICAL CHARACTERISTICS 90
10.2 BOOST5 - REGISTER SETTINGS 90
10.3 BOOST5 - ENABLING & DISABLING 91
10.4 OUTPUT DIODE 92
10.5 BOOST5 - APPLICATIONS INFORMATION 92
11.0 CLASS_D BTL POWER OUTPUT STAGE 93
11.1 CLASS_D - ELECTRICAL CHARACTERISTICS 93
11.2 CLASS_D – TYPICAL PERFORMANCE CHARACTERISTICS 94
11.3 CLASS_D – REGISTER SETTINGS 94
11.4 CLASS_D - AUDIO INTERFACE AND DECODE 95
11.5 CLASS_D - SHORT CIRCUIT PROTECTION CIRCUITRY 95
11.6 CLASS_D - APPLICATIONS INFORMATION 95
12.0 TSC MODULE - ADC AND TOUCH SCREEN CONTROLLER 96
12.1 ADC AND TOUCH SCREEN CONTROLLER ELECTRICAL CHARACTERISTICS 97
12.2 ADC AND TOUCH SCREEN CONTROLLER PIN DEFINITIONS 97
12.3 ADC AND TOUCH SCREEN CONTROLLER OPERATION 97
12.4 ADC AND TOUCH SCREEN CONTROLLER REGISTERS 100
13.0 PCON MODULE – POWER CONTROLLER AND GENERAL PURPOSE I/O 107
13.1 GPIO PIN DEFINITIONS 107
13.2 POWER STATES 107
13.3 POWER SEQUENCING BY EMBEDDED MICROCONTROLLER 107
13.4 POWER ON RESET OUTPUT (POR_OUT) 108
13.5 POWER SWITCH DETECTOR (SW_DET) 108
13.6 GPIO GENERAL DESCRIPTION 108
13.7 PCON REGISTERS 108
14.0 HOTSWAP MODULE 113
14.1 HOT SWAP (LOAD SWITCHES) – ELECTRICAL CHARACTERISTICS 113
14.2 HOTSWAP – TYPICAL PERFORMANCE CHARACTERISTICS 114
14.3 HOTSWAP – PIN DEFINITIONS 115
14.4 PCON REGISTER - HOTSWAP CONFIGURATION 115
15.0 I2C_I2S MODULE 116
15.1 I2C_I2S - PIN DEFINITIONS 116
15.2 I²C SLAVE 116
15.3 INTERRUPT DISPATCHER 117

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15.4 ACCESS ARBITER 117
15.5 DIGITAL AUDIO DATA SERIAL INTERFACE 117
15.6 I2C_I2S – INTERFACE TIMING 118
15.7 GLOBAL REGISTER SETTINGS (I²C-page 0) 120
15.8 ACCM REGISTERS 123
16.0 LDO MODULE 124
16.1 LDO - PIN DEFINITIONS 125
16.2 LDO - LDO_150 & LDO_050 ELECTRICAL CHARACTERISTICS 125
16.3 LDO – TYPICAL PERFORMANCE CHARACTERISTICS 126
16.4 LDO - LDO_LP - ELECTRICAL CHARACTERISTICS 127
16.5 LDO - LIST OF ALL LDOS 127
16.6 LDO – REGISTER SETTINGS 127
17.0 EMBUP – EMBEDDED MICROCONTROLLER SUBSYSTEM & I/O 131
17.1 OVERVIEW 131
17.2 FUNCTIONAL DESCRIPTION 131
17.3 ON-CHIP RAM & ROM 131
17.4 I²C SLAVE INTERFACE 131
17.5 PERIPHERALS 132
17.6 INTERRUPT CONTROLLER 132
18.0 APPLICATIONS INFORMATION 133
18.1 EXTERNAL COMPONENTS 133
18.2 DIGITAL LOGIC DECOUPLING CAPACITORS 133
18.3 CLASS_D CONSIDERATIONS 133
18.4 SERIES TERMINATION RESISTORS 133
18.5 I²C EXTERNAL RESISTOR CONNECTION 133
18.6 CRYSTAL LOAD CAPACITORS 133
18.7 PCB LAYOUT CONSIDERATIONS 133
18.8 POWER DISSIPATION AND THERMAL REQUIREMENTS 133
18.9 TYPICAL BLOCK PERFORMANCE CHARACTERISTICS GRAPHS 133
18.10 APPLICATIONS REFERENCE DESIGN(S) 134
19.0 SOLDERING PROFILE 134
20.0 PACKAGE OUTLINE DRAWING 134
20.1 LLG124 PACKAGE OUTLINE 134
20.2 NQG132 PACKAGE OUTLINE (Exposed Die Paddle Size D2 = E2 = 5.5 mm) 135
21.0 ORDERING INFORMATION 135

TABLE OF FIGURES

Figure 1 – P95020 Block Diagram. 2
Figure 2 – P95020 Pinout Diagram (LLG124) 7
Figure 3 – P95020 Pinout (NGQ132) 8
Figure 4 – Overall System Functional Diagram. 18
Figure 5 – Audio Block Diagram 22
Figure 6 –Stereo Digital Microphone (Mode 3) 26
Figure 7 –Stereo Digital Microphone (Mode 1 & 2) 27
Figure 8 – Automatic Gain Control 28
Figure 9 – Charger Block Diagram 52
Figure 10 – Pre-Regulator Efficiency vs Load Current VBUS = 5.0V, VSYS = 3.7V 54
Figure 11– Pre-Regulator Load Regulation VBUS = 5.0V, VSYS = 3.7V 55
Figure 12 – Battery Charge Current vs Temperature 55
Figure 13 – V_{SYS} Regulation Curve (Tracking V_{BAT}) 59
Figure 14 – Clock Generator Block Diagram 61
Figure 15 DC_DC Block Diagram 74
Figure 16 – BUCK500 / BUCK1000 Block Diagram 76
Figure 17 – BUCK500 DC-DC Regulator Efficiency vs Load Current PWM Mode 78
Figure 18 – BUCK1000 DC-DC Regulator Efficiency vs Load Current PWM Mode 78
Figure 19 – BUCK500 DC-DC Regulator Efficiency vs Load Current PFM Mode 79
Figure 20 – BUCK500 or BUCK 1000 Applications Diagram 81
Figure 21 – White LED Boost & Sink Driver Block Diagram 83

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Figure 22 – LED Boost Efficiency vs Load Current (two srings of 10 LEDs) 84
Figure 23 – LED Boost Efficiency vs VIN (two srings of 10 LEDs) 85
Figure 24 – LED_BOOST Application Schematic 87
Figure 25 – BOOST5 Block Diagram 89
Figure 26 – BOOST5 Applications Diagram 92
Figure 27 – Clss D BTL Efficiency vs Outpout Power (4 ohm speaker) 94
Figure 28 – ADC & Touchscreen Controller Block Diagram 96
Figure 29 – Hotswap Block Diagram 113
Figure 30 – Hotswap #1 ON Resistance vs Temperature 114
Figure 31 – Hotswap #2 ON Resistance vs Temperature 114
Figure 32 – I^2C Read / Write Operation 117
Figure 33 – LDO_050 / LDO_150 Block Diagram 124
Figure 34 – LDO_050_n 50mA LDO Load Regulation 126
Figure 35 – LDO_150_n 150mA LDO Load Regulation 126
Figure 36 - Top level Interrupt routing 132
Figure 37 – Power Derating Curve (Typical) 133

LIST OF TABLES

Table 1 – LLG124 Pin Functions by Pin Number (See Figure 2) 9
Table 2 - NQG132 Pin Functions by Pin Number (see Figure 3) 11
Table 3 – Register Address Global Mapping 20
Table 4 - Valid Digital Mic Configurations 25
Table 5 - MCLK Rate selection: MCLK_DIV2: MCLK_RATE 29
Table 6 – MCLK/Sample Rate 30
Table 7 - EQRAM Addresses 39
Table 8 – Register 0xA090 (0x90) Current Limit (I_LIM) Settings Bits [2:0] 56
Table 9 – Register 0xA091, (0x91) Charging Maximum Voltage (CHG_VOL) Settings, Bits [5:4] 56
Table 10 – Register 0xA091, (0x91) Charging Current Limit via Sense Resistor (CHG_CUR) Settings, Bits [3:0] 56
Table 11 – Register 0xA092 (0x92) Charging Termination Time (CHG_TERM) Settings Bits [1:0] 56
Table 12 – Register 0xA093 (0x93) Battery Recovery Charge Current Control Settings Bits [7:5] 57
Table 13 – Register 0xA093, (0x93) Battery Good Voltage Threshold Settings, Bits [4:3] 57
Table 14 – Register 0xA095, (0x95) Current Charger Mode Settings, Bits [4:3] 57
Table 15 - Crystal Specifications 63
Table 16 - Alarm mask bits 66
Table 17 – DC-DC Block Registers (Including the CLASS_D BTL Power Bridge) 74
Table 18 – BUCK500_0, BUCK500_1 and BUCK1000 Register Addresses 79
Table 19 – Output Voltage Register Settings, Bits [6:0] 79
Table 20 – Control Register Cycle by Cycle Current Limit (I_LIM) Settings for Bits [3:2] [Note] 80
Table 21 – Interoperability of enabling/disabling methods vs. loading default values. 80
Table 22 – Register 0xA086 (0x86) IOUT Current Settings for Bits [4:0], Half Scale and Full Scale 85
Table 23 – Interoperability of enabling/disabling methods vs. loading default values. 86
Table 24 – Register 0xA088 Output Voltage Bit Setting [4:0] 90
Table 25 – Register 0xA089 (0x89) Peak Current Limit (I_LIM) Settings Bits [3:2] 91
Table 26 – Interoperability of enabling/disabling methods vs. loading default values. 91
Table 27 – Peak Short Circuit Detect Level Settings for Bits [3:2] 94
Table 28 – I2C Interface Timing 118
Table 29 – I2S Interface Timing 119
Table 30 - Interrupt Source Mapping 122
Table 31 – Control Register Current Limit (I_LIM) Settings for Bits [1:0] 128

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PIN ASSIGNMENTS

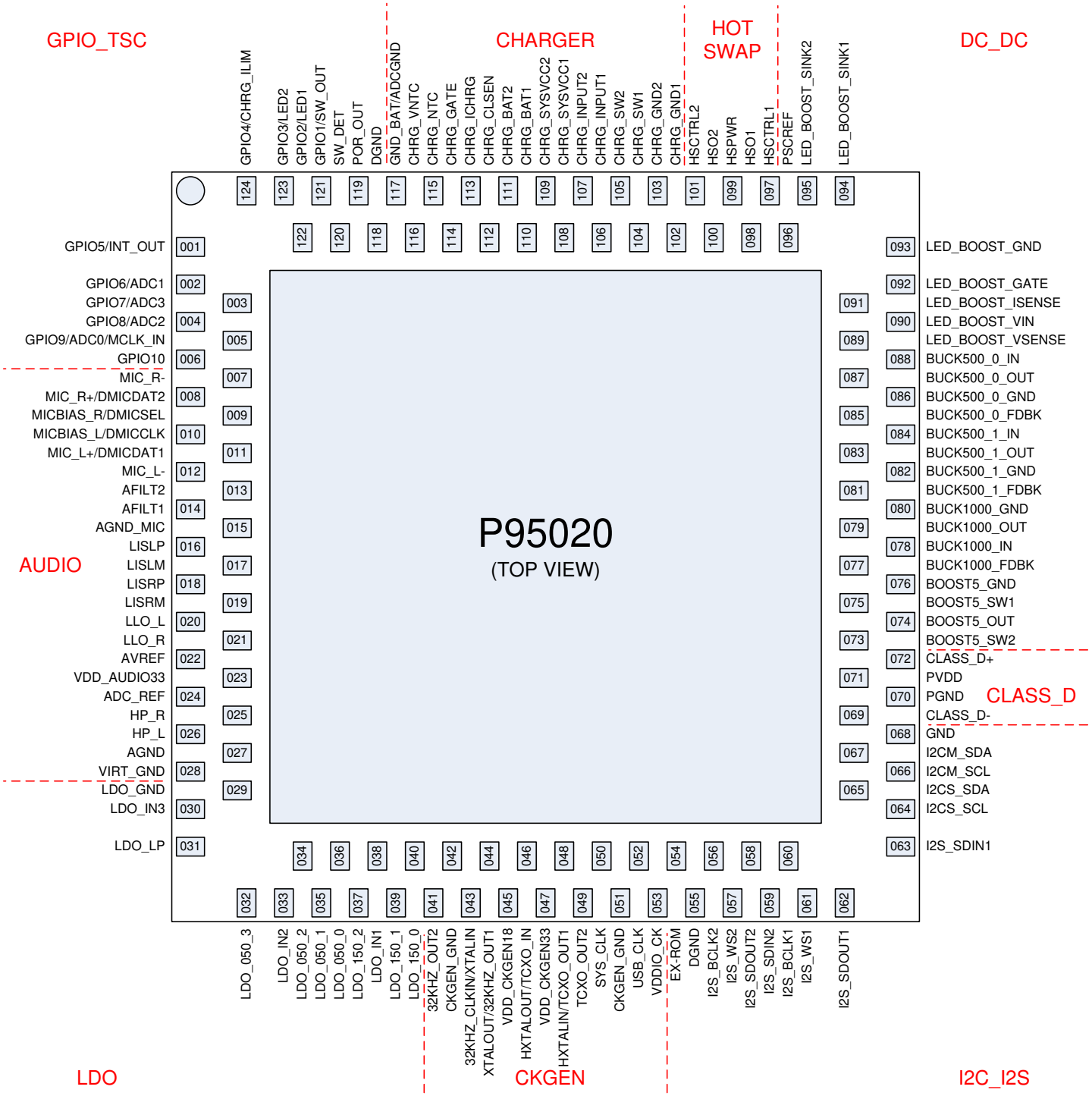

Figure 2 – P95020 Pinout Diagram (LLG124)

NOTES:

1. All the Buck Converter inputs (BUCK500_0_IN, BUCK500_1_IN, BUCK1000_IN) must be connected to CHRG_SYSVCC1 and CHRG_SYSVCC2.
2. LLG124 package is available upon request.

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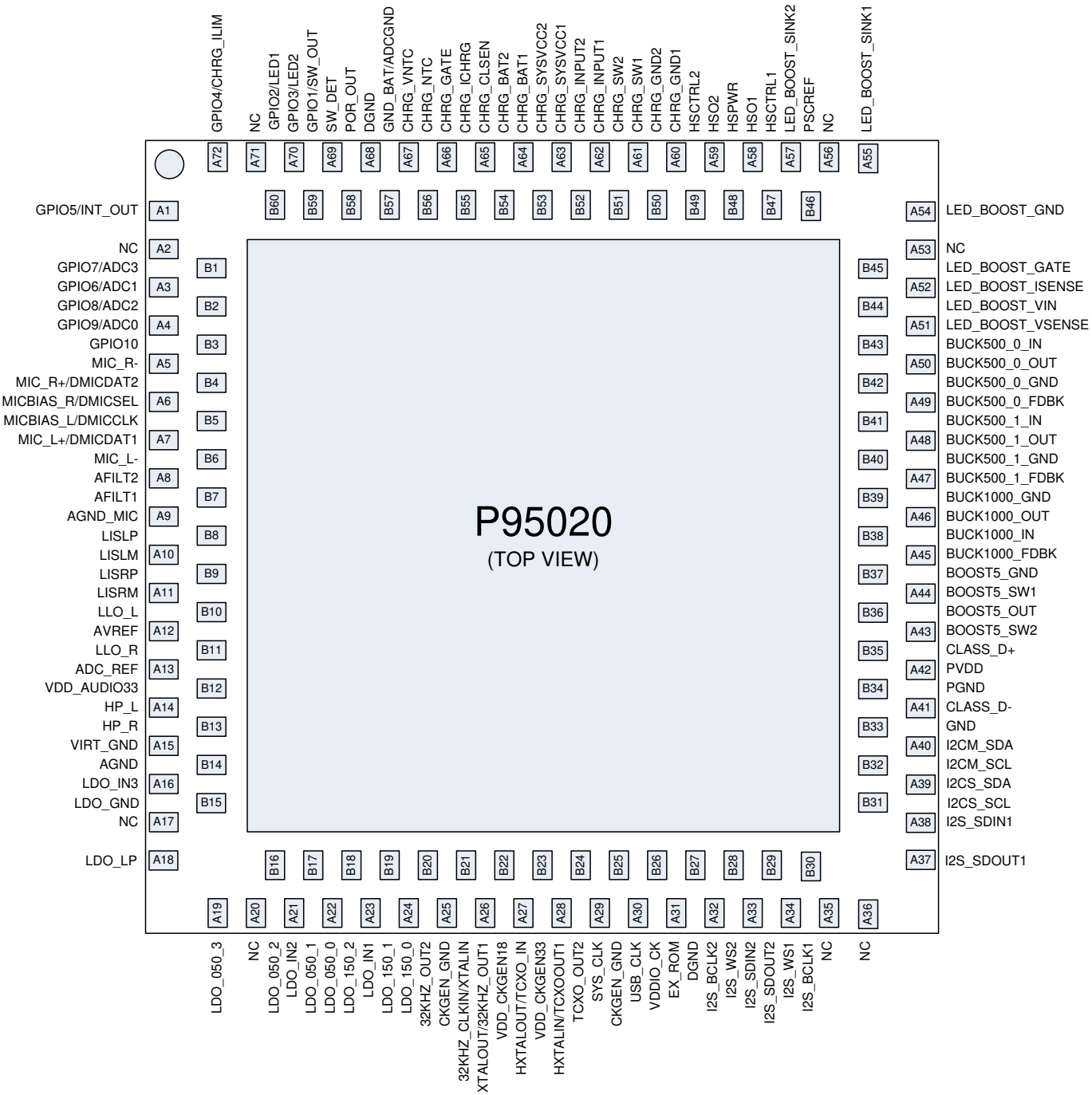

Figure 3 – P95020 Pinout (NGQ132)

NOTES:

All the Buck Converter inputs (BUCK500_0_IN, BUCK500_1_IN, BUCK1000_IN) must be connected to CHRG_SYSVCC1 and CHRG_SYSVCC2.

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PIN FUNCTIONS BY PIN NUMBER

Table 1 – LLG124 Pin Functions by Pin Number (See Figure 2)

MODULE	PIN #	PIN NAME	DESCRIPTION	I/O TYPE
GPIO_TSC (*See Pins 117-124 also)*	1	GPIO5/INT_OUT	GPIO 5: General Purpose I/O # 5 INT_OUT : Interrupt Output	GPIO
	2	GPIO6/ADC1	GPIO 6: General Purpose I/O # 6 ADC1 : Auxiliary Input Channel 2 / X- pin to 4-wire resistive touch-screen	GPIO
	3	GPIO7/ADC3	GPIO 7: General Purpose I/O # 7 ADC3 : Auxiliary Input Channel 4 / Y- pin to 4-wire resistive touch-screen	GPIO
	4	GPIO8/ADC2	GPIO 8: General Purpose I/O # 8 ADC2 : Auxiliary Input Channel 3 / Y+ pin to 4-wire resistive touch-screen	GPIO
	5	GPIO9/ADC0/MCLK_IN	GPIO 9: General Purpose I/O # 9 ADC0 : Auxiliary Input Channel 1 / X+ pin to 4-wire resistive touch-screen MCLK_IN : Master Clock Input	GPIO
	6	GPIO10	GPIO 10: General Purpose I/O # 10	GPIO
	7	MIC_R-	MIC_R-: Analog Microphone Differential Stereo Right Inverting Input	A-I
	8	MIC_R+/DMICDAT2	MIC_R+: Analog Microphone Differential Stereo Right Non-Inverting Input DMICDAT2: Digital Microphone 2 Data Input	A-I D-I
	9	MICBIAS_R/DMICSEL	MICBIAS : Microphone Right Bias DMICSEL : Digital Microphone Select (Common to both inputs)	A-O D-O
	10	MICBIAS_L/DMICCLK	MICBIAS : Microphone Left Bias DMICCLK : Digital Microphone Clock (Common to both inputs)	A-O D-O
	11	MIC_L+/DMICDAT1	MIC_L+ : Analog Microphone Differential Stereo Left Non-Inverting Input DMICDAT1 : Digital Microphone 1 Data Input	A-I D-I
	12	MIC_L-	MIC_L- : Analog Microphone Differential Stereo Left Inverting Input	A-I
	13	AFILT2	Microphone ADC Anti-Aliasing Filter Capacitor #2	A-I
	14	AFILT1	Microphone ADC Anti-Aliasing Filter Capacitor #1	A-I
	15	AGND_MIC	Microphone Ground (Analog Ground)	GND
	16	LISLP	Line Input Stereo Left Non-Inverting	A-I
	17	LISLM	Line Input Stereo Left Inverting	A-I
	18	LISRP	Line Input Stereo Right Non-Inverting	A-I
	19	LISRM	Line Input Stereo Right Inverting	A-I
	20	LLO_L	Line Level Output, Left	A-O
	21	LLO_R	Line Level Output, Right	A-O
	22	AVREF	Analog Reference	A-O
	23	VDD_AUDIO33	Filter Capacitor for Internal 3.3V AUDIO LDO	A-O
	24	ADC_REF	ADC Reference Bypass Capacitor	A-I
	25	HP_R	Right Headphone Output	A-O
	26	HP_L	Left Headphone Output	A-O
	27	AGND	Line Out Ground (Analog Ground)	GND
AUDIO	28	VIRT_GND	Virtual Ground for Cap-Less Output	A-O
	29	LDO_GND	LDO Ground	GND
	30	LDO_IN3	Input Voltage to LDOs for AUDIO Power (VDD_AUDIO33 & VDD_AUDIO18)	AP-I
	31	LDO_LP	Always on Low Power LDO Output (Voltage Programmable to 3.0 V or 3.3 V)	AP-O
	32	LDO_050_3	50mA LDO Output #3 (Voltage Range: 0.75-3.7 V)	AP-O
	33	LDO_IN2	Input Voltage to LDO_050_0, LDO_050_1, LDO_050_2 & LDO_050_3	AP-I
	34	LDO_050_2	50mA LDO Output #2 (Voltage Range: 0.75-3.7 V)	AP-O
	35	LDO_050_1	50mA LDO Output #1 (Voltage Range: 0.75-3.7 V)	AP-O
	36	LDO_050_0	50mA LDO Output #0 (Voltage Range: 0.75-3.7 V) Note: This LDO also serves as the internal power source for I2S1, I2S2 and I2CS. The external function of this pin is not affected but the voltage register setting for this LDO will also govern the I/O level for I2S1, I2S2 and I2CS.	AP-O
	37	LDO_150_2	150mA LDO Output #2 (Voltage Range: 0.75-3.7 V)	AP-O
	38	LDO_IN1	Input Voltage to LDO_150_0, LDO_150_1, & LDO_050_2	AP-I
	39	LDO_150_1	150mA LDO Output #1 (Voltage Range: 0.75-3.7 V)	AP-O
LDO	40	LDO_150_0	150mA LDO Output #0 (Voltage Range: 0.75-3.7 V)	AP-O
	41	32KHZ_OUT2	Buffered 32.768kHz Output #2	D-O
	42	CKGEN_GND	PLL Analog Ground	GND
CKGEN	43	32KHZ_CLKIN/XTALIN	32KHZ_CLKIN: External 32.768kHz Clock Input; XTALIN : Input Pin when used with an external crystal	A-I

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MODULE	PIN #	PIN NAME	DESCRIPTION	I/O TYPE
	44	XTALOUT/32KHZ_OUT1	XTALOUT: Output Pin when used with an external crystal 32KHZ_OUT1: when XTALIN is connected to a 32kHz input this pin can be a 32kHz Output when CKGEN_PLL_STATUS register, 32KOUT1_EN (bit 4) is set to 1.	A-O
	45	VDD_CKGEN18	Filter Capacitor for Internal 1.8V CKGEN LDO	A-IO
	46	HXTALOUT/TCXO_IN	HXTALOUT: 12 MHz, 13 MHz, 19.2 MHz or 26 MHz crystal oscillator output TCXO_IN: External 12 MHz, 13 MHz, 19.2 MHz or 26 MHz Clock Input	TCXO-D-I
	47	VDD_CKGEN33	Filter Capacitor for Internal 3.3V CKGEN LDO	A-IO
	48	HXTALIN/TCXO_OUT1	HXTALIN: 12 MHz, 13 MHz, 19.2 MHz, or 26 MHz crystal oscillator input TCXO_OUT1: Buffered HXTALOUT/TCXO_IN Clock Output #1, 32.7638 KHz Output, 24 MHz PLL Output	TCXO-D-O
	49	TCXO_OUT2	Buffered HXTALOUT/TXCO_IN Clock Output #2, 12 MHz PLL Output, 24MHz PLL Output	TCXO-D-O
	50	SYS_CLK	12MHz Output or Buffered Output of TCXO_IN	D-O
	51	CKGEN_GND	PLL Analog Ground	GND
	52	USB_CLK	24 MHz or 48 MHz Output	D-O
	53	VDDIO_CK	Power Supply Input for TCXO_OUT1 and TCXO_OUT2 (1.1V – 1.9V)	AP-I
	54	EX_ROM	ROM Select. EX_ROM = 1, read contents of external ROM. EX_ROM = 0, read contents of internal ROM into internal shadow memory.	D-I
	55	DGND	Digital Ground	GND
	56	I2S_BCLK2	I²S Bit Clock Channel 2	D-I
	57	I2S_WS2	I²S Word Select (Left/Right) Channel 2	D-I
	58	I2S_SDOUT2	I²S Serial Data OUT Channel 2	D-O
	59	I2S_SDIN2	I²S Serial Data IN Channel 2	D-I
	60	I2S_BCLK1	I²S Bit Clock Channel 1	D-I
	61	I2S_WS1	I²S Word Select (Left/Right) Channel 1	D-I
	62	I2S_SDOUT1	I²S Serial Data OUT Channel 1	D-O
	63	I2S_SDIN1	I²S Serial Data IN Channel 1	D-I
	64	I2CS_SCL	I²C Slave clock	I2C-I/O
	65	I2CS_SDA	I²C Slave data	I2C-O
	66	I2CM_SCL	I²C Master clock	I2C-O
	67	I2CM_SDA	I²C Master data	I2C-I/O
I2C_I2S	68	GND	GND : Ground	GND
	69	CLASS_D-	Class-D Inverting Output	A-O
	70	PGND	Ground for Class D BTL Power Stage	GND
	71	PVDD	Input Power for CLASS_D BTL Power Stage	A-I
CLASS_D	72	CLASS_D+	Class-D Non-Inverting Output	A-O
	73	BOOST5_SW2	BOOST5 Converter Power Switch Internally connected to pin 075 (BOOST_SW1)	AP-O
	74	BOOST5_OUT	BOOST5 Converter Output	AP-O
	75	BOOST5_SW1	BOOST5 Converter Power Switch Internally connected to pin 073 (BOOST_SW2)	AP-O
	76	BOOST5_GND	Ground for BOOST5 Power Supply	AP-I
	77	BUCK1000_FDBK	BUCK2 Converter #2 -Feedback	AP-I
	78	BUCK1000_IN	BUCK2 Converter #2 - Input	AP-I
	79	BUCK1000_OUT	BUCK2 Converter Output #2 – 1000mA	AP-O
	80	BUCK1000_GND	Ground for BUCK2 Converter #2	GND
	81	BUCK500_1_FDBK	BUCK1 Converter #1 – Feedback	AP-I
	82	BUCK500_1_GND	Ground for BUCK1 Converter #1	GND
	83	BUCK500_1_OUT	BUCK1 Converter Output #1 - 500mA	AP-O
	84	BUCK500_1_IN	BUCK1 Converter #1 Input	AP-I
	85	BUCK500_0_FDBK	BUCK0 Converter #0 feedback	AP-I
	86	BUCK500_0_GND	Ground for BUCK0 Converter #0	GND
	87	BUCK500_0_OUT	BUCK0 Converter Output #0 - 500mA	AP-O
	88	BUCK500_0_IN	BUCK0 Converter #0 Input	AP-I
	89	LED_BOOST_VSENSE	LED_BOOST Converter Output Voltage Sense Input to PWM Controller	AP-I
	90	LED_BOOST_VIN	LED_BOOST Converter GATE BIAS Supply	AP-I
	91	LED_BOOST_ISENSE	LED_BOOST Converter Output Current Sense Input to PWM Controller	AP-I
	92	LED_BOOST_GATE	LED_BOOST Converter GATE Drive to Power FET	AP-I
	93	LED_BOOST_GND	Ground for LED_BOOST	AP-I
	94	LED_BOOST_SINK1	LED_BOOST Converter Current Sink for LED String #1	AP-I
	95	LED_BOOST_SINK2	LED_BOOST Converter Current Sink for LED String #2	AP-I
DC_DC	96	PSCREF	Power Supply Current Reference	AP-O
	97	HSCTRL1	Hot Swap Control Input 1	D-I
	98	HSO1	Hot Swap Output 1	A-O
	99	HSPWR	Hot Swap Switches Power Input	AP-I
	100	HSO2	Hot Swap Output 2	A-O
HOTSWAP	101	HSCTRL2	Hot Swap Control Input 2	D-I

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MODULE	PIN #	PIN NAME	DESCRIPTION	I/O TYPE
	102	CHRG_GND1	Pins 102 & 103 are the Power GND Pins for the Switching Regulator in the Charger. Due to their higher current requirement they are internally tied together & must be connected externally at the PC board also.	A-I
	103	CHRG_GND2		A-I
	104	CHRG_SW1	Pins 104 and 105 connect to the inductor of the switch-mode step-down regulator for the Battery Charger. Due to their higher current requirement they are internally tied together & must be connected externally at the PC board also.	A-O
	105	CHRG_SW2		A-O
	106	CHRG_INPUT1	Pins 106 and 107 provide 5V V_{BUS} Input Power from the USB or from an external wall mounted external supply. Due to their higher current requirement they are internally tied together & must be connected externally at the PC board also.	AP-I
	107	CHRG_INPUT2		AP-I
	108	CHRG_SYSVCC1	Pins 108 and 109 are System VCC Output (V_{SYS}). Due to their higher current requirement they are internally tied together & must be connected externally at the PC board also.	A-O
	109	CHRG_SYSVCC2		A-O
	110	CHRG_BAT1	Pins 110 and 111 form the positive battery lead connection to a single cell Li-Ion/Li-Poly battery. Due to their higher current requirement they are internally tied together & must be connected externally at the PC board also.	AP-I/O
	111	CHRG_BAT2		AP-I/O
	112	CHRG_CLSEN	Input Current Limit Sense/filtering pin for current limit detection	A-I
	113	CHRG_ICHRG	Current setting. Connect to a current sense resistor	AP-I/O
	114	CHRG_GATE	Gate Drive for (Optional) External Ideal Diode	A-O
	115	CHRG_NTC	Thermal Sense, Connect to a battery's thermistor	A-I
CHARGER	116	CHRG_VNTC	NTC Power output. This pin provides power to the NTC resistor string. This output is automatically CHRG_SYSVCC level but only enabled when NTC measurement is necessary to save power.	AP-O
GPIO_TSC (*See Pins 001-006 also)*	117	GND_BAT/ADCGND	GND_BAT & ADCGND: Shared analog ground pin for battery charger and ADC.	GND
	118	DGND	Digital Ground	GND
	119	POR_OUT	Power-On-Reset Output, Active Low	GPIO-OUT
	120	SW_DET	Switch Detect Input	GPIO
	121	GPIO1/SW_OUT/PENDOWN	GPIO 1: General Purpose I/O # 1 SW_OUT: Switch Detect Output PENDOWN: PENDOWN Detect Output	GPIO
	122	GPIO2/LED1	GPIO 2**:** General Purpose I/O # 2 LED1**:** Charger LED # 1 Indicates charging in progress	GPIO
	123	GPIO3/LED2	GPIO 3**:** General Purpose I/O # 3 LED2: Charger LED # 2 Indicates charging complete	GPIO
	124	GPIO4/CHRG_ILIM	GPIO 4**:** General Purpose I/O # 4 CHRG_ILIM**:** Control the current limit of the Charger Pre-Regulator. CHRG_ILIM = 0, limit current to 500mA; CHRG_ILIM = 1, limit current to 1.5A	GPIO

Table 2 - NQG132 Pin Functions by Pin Number (see Figure 3)

MODULE	PIN #	PIN NAME	DESCRIPTION	I/O TYPE
GPIO_TSC *(See Pins B57 – A71 also)*	A1	GPIO5/INT_OUT	GPIO 5: General Purpose I/O # 5 INT_OUT : Interrupt Output	GPIO
	A2	NC	No Connect	NC
	B1	GPIO7/ADC3	GPIO 7: General Purpose I/O # 7 ADC3 : Auxiliary Input Channel 4 / Y- pin to 4 wire resistive touch screen	GPIO
	A3	GPIO6/ADC1	GPIO 6: General Purpose I/O # 6 ADC1 : Auxiliary Input Channel 2 / X- pin to 4-wire resistive touch screen	GPIO
	B2	GPIO8/ADC2	GPIO 8: General Purpose I/O # 8 ADC2 : Auxiliary Input Channel 3 / Y+ pin to 4-wire resistive touch screen	GPIO
	A4	GPIO9/ADC0/MCLK_IN	GPIO 9: General Purpose I/O # 9 ADC0 : Auxiliary Input Channel 1 / X+ pin to 4-wire resistive touch screen MCLK_IN : Master Clock Input	GPIO
	B3	GPIO10	GPIO 10: General Purpose I/O # 10	GPIO
AUDIO	A5	MIC_R-	MIC_R-: Analog Microphone Differential Stereo Right Inverting Input	A-I
	B4	MIC_R+/DMICDAT2	MIC_R+: Analog Microphone Differential Stereo Right Non-Inverting Input DMICDAT2: Digital Microphone 2 Data Input	A-I D-I
	A6	MICBIAS_R/DMICSEL	MICBIAS : Microphone Right Bias DMICSEL : Digital Microphone Select (Common to both inputs)	A-O D-O
	B5	MICBIAS_L/DMICCLK	MICBIAS : Microphone Left Bias DMICCLK : Digital Microphone Clock (Common to both inputs)	A-O D-O
	A7	MIC_L+/DMICDAT1	MIC_L+ : Analog Microphone Differential Stereo Left Non-Inverting Input DMICDAT1 : Digital Microphone 1 Data Input	A-I D-I

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MODULE	PIN #	PIN NAME	DESCRIPTION	I/O TYPE
	B6	MIC_L-	MIC_L- : Analog Microphone Differential Stereo Left Inverting Input	A-I
	A8	AFILT2	Microphone ADC Anti-Aliasing Filter Capacitor #2	A-I
	B7	AFILT1	Microphone ADC Anti-Aliasing Filter Capacitor #1	A-I
	A9	AGND_MIC	Microphone Ground (Analog Ground)	GND
	B8	LISLP	Line Input Stereo Left Non-Inverting	A-I
	A10	LISLM	Line Input Stereo Left Inverting	A-I
	B9	LISRP	Line Input Stereo Right Non-Inverting	A-I
	A11	LISRM	Line Input Stereo Right Inverting	A-I
	B10	LLO_L	Line Level Output, Left	A-O
	A12	AVREF	Analog Reference	A-O
	B11	LLO_R	Line Level Output, Right	A-O
	A13	ADC_REF	ADC Reference Bypass Capacitor	A-I
	B12	VDD_AUDIO33	Filter Capacitor for Internal 3.3V AUDIO LDO	A-O
	A14	HP_L	Left Headphone Output	A-O
	B13	HP_R	Right Headphone Output	A-O
	A15	VIRT_GND	Virtual Ground for Cap-Less Output	A-O
	B14	AGND	Analog Ground	GND
LDO	A16	LDO_IN3	Input Voltage to LDOs for AUDIO Power (VDD_AUDIO33 & VDD_AUDIO18)	AP-I
	B15	LDO_GND	LDO Ground	GND
	A17	NC	No Connect	NC
	A18	LDO_LP	Always on Low Power LDO Output (Voltage Programmable to 3.0 V or 3.3 V)	AP-O
	A19	LDO_050_3	50mA LDO Output #3 (Voltage Range: 0.75-3.7 V)	AP-O
	A20	NC	No Connect	NC
	B16	LDO_050_2	50mA LDO Output #2 (Voltage Range: 0.75-3.7 V)	AP-O
	A21	LDO_IN2	Input Voltage to LDO_050_0, LDO_050_1, LDO_050_2 & LDO_050_3	AP-I
	B17	LDO_050_1	50mA LDO Output #1 (Voltage Range: 0.75-3.7 V)	AP-O
	A22	LDO_050_0	50mA LDO Output #0 (Voltage Range: 0.75-3.7 V) Note: This LDO also serves as the internal power source for I2S1, I2S2 and I2CS. The external function of this pin is not affected but the voltage register setting for this LDO will also govern the I/O level for I2S1, I2S2 and I2CS.	AP-O
	B18	LDO_150_2	150mA LDO Output #2 (Voltage Range: 0.75-3.7 V)	AP-O
	A23	LDO_IN1	Input Voltage to LDO_150_0, LDO_150_1 & LDO_150_2	AP-I
	B19	LDO_150_1	150mA LDO Output #1 (Voltage Range: 0.75-3.7 V)	AP-O
	A24	LDO_150_0	150mA LDO Output #0 (Voltage Range: 0.75-3.7 V)	AP-O
CK_GEN	B20	32KHZ_OUT2	Buffered 32.768kHz Output #2	D-O
	A25	CKGEN_GND	PLL Analog Ground	GND
	B21	32KHZ_CLKIN/XTALIN	32KHZ_CLKIN: External 32.768kHz Clock Input; XTALIN : Input Pin when used with an external crystal	A-I
	A26	XTALOUT/32KHZ_OUT1	XTALOUT: Output Pin when used with an external crystal 32KHZ_OUT1: when XTALIN is connected to a 32kHz input this pin can be a 32kHz Output when CKGEN_PLL_STATUS register, 32KOUT1_EN (bit 4) is set to 1.	A-O
	B22	VDD_CKGEN18	Filter Capacitor for Internal 1.8V CKGEN LDO	A-IO
	A27	HXTALOUT/TCXO_IN	HXTALOUT: 12 MHz, 13 MHz, 19.2 MHz or 26 MHz output TCXO_IN: External 12 MHz, 13 MHz, 19.2 MHz or 26 MHz clock input	TCXO-D-I
	B23	VDD_CKGEN33	Filter Capacitor for Internal 3.3V CKGEN LDO	A-IO
	A28	HXTALIN/TCXO_OUT1	HXTALIN: 12 MHz, 13 MHz, 19.2 MHz, or 26 MHz crystal oscillator input TCXO_OUT1: Buffered HXTALOUT/TCXO_IN Clock Output #1, 32.7638 KHz Output or 24 MHz PLL Output	TCXO-D-O
	B24	TCXO_OUT2	Buffered HXTALOUT/TXCO_IN Clock Output #2, 12 MHz PLL Output or 48 MHz PLL Output	TCXO-D-O
	A29	SYS_CLK	12MHz Output or Buffered Output of TCXO_IN	D-O
	B25	CKGEN_GND	PLL Analog Ground	GND
	A30	USB_CLK	24 MHz or 48 MHz Output	D-O
	B26	VDDIO_CK	Power Supply Input for TCXO_OUT1 and TCXO_OUT2 (1.1V – 1.9V)	AP-I
I2C_I2S	A31	EX_ROM	ROM Select. EX_ROM = 1, read contents of external ROM. EX_ROM = 0, read contents of internal ROM into internal shadow memory.	D-I
	B27	DGND	Digital Ground (1)	GND
	A32	I2S_BCLK2	I²S Bit Clock Channel 2	D-I
	B28	I2S_WS2	I²S Word Select (Left/Right) Channel 2	D-I
	A33	I2S_SDIN2	I²S Serial Data IN Channel 2	D-I
	B29	I2S_SDOUT2	I²S Serial Data OUT Channel 2	D-O
	A34	I2S_WS1	I²S Word Select (Left/Right) Channel 1	D-I
	B30	I2S_BCLK1	I²S Bit Clock Channel 1	D-I
	A35	NC	No Connect	NC
	A36	NC	No Connect	NC

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MODULE	PIN #	PIN NAME	DESCRIPTION	I/O TYPE
	A37	I2S_SDOUT1	I²S Serial Data OUT Channel 1	D-O
	A38	I2S_SDIN1	I²S Serial Data IN Channel 1	D-I
	B31	I2CS_SCL	I²C Slave clock	I2C-I/O
	A39	I2CS_SDA	I²C Slave data	I2C-O
	B32	I2CM_SCL	I²C Master clock	I2C-O
	A40	I2CM_SDA	I²C Master data	I2C-I/O
	B33	GND	GND : Ground	GND
CLASS_D	A41	CLASS_D-	Class-D Inverting Output	A-O
	B34	PGND	Ground for Class D BTL Power Stage	GND
	A42	PVDD	Input Power for CLASS_D BTL Power Stage	A-I
	B35	CLASS_D+	Class-D Non-Inverting Output	A-O
DC_DC	A43	BOOST5_SW2	BOOST5 Converter Power Switch Internally connected to pin A44 (BOOST_SW1)	AP-O
	B36	BOOST5_OUT	BOOST5 Converter Output	AP-O
	A44	BOOST5_SW1	BOOST5 Converter Power Switch Internally connected to pin A43 (BOOST_SW2)	AP-O
	B37	BOOST5_GND	Ground for BOOST5 Power Supply	AP-I
	A45	BUCK1000_FDBK	BUCK2 Converter #2 - Feedback	AP-I
	B38	BUCK1000_IN	BUCK2 Converter #2 - Input	AP-I
	A46	BUCK1000_OUT	BUCK2 Converter Output #2 – 1000mA	AP-O
	B39	BUCK1000_GND	Ground for BUCK2 Converter #2	GND
	A47	BUCK500_1_FDBK	BUCK1 Converter #1 – Feedback	AP-I
	B40	BUCK500_1_GND	Ground for BUCK1 Converter #1	GND
	A48	BUCK500_1_OUT	BUCK1 Converter Output #1 - 500mA	AP-O
	B41	BUCK500_1_IN	BUCK1 Converter #1 Input	AP-I
	A49	BUCK500_0_FDBK	BUCK0 Converter #0 feedback	AP-I
	B42	BUCK500_0_GND	Ground for BUCK0 Converter #0	GND
	A50	BUCK500_0_OUT	BUCK0 Converter Output #0 - 500mA	AP-O
	B43	BUCK500_0_IN	BUCK0 Converter #0 Input	AP-I
	A51	LED_BOOST_VSENSE	LED_BOOST Converter Output Voltage Sense Input to PWM Controller	AP-I
	B44	LED_BOOST_VIN	LED_BOOST Converter GATE BIAS Supply	AP-I
	A52	LED_BOOST_ISENSE	LED_BOOST Converter Output Current Sense Input to PWM Controller	AP-I
	B45	LED_BOOST_GATE	LED_BOOST Converter GATE Drive to Power FET	AP-I
	A53	NC	No Connect	NC
	A54	LED_BOOST_GND	Ground for LED_BOOST	AP-I
	A55	LED_BOOST_SINK1	LED_BOOST Converter Current Sink for LED String #1	AP-I
	A56	NC	No Connect	NC
	B46	PSCREF	Power Supply Current Reference	AP-O
	A57	LED_BOOST_SINK2	LED_BOOST Converter Current Sink for LED String #2	AP-I
HOTSWAP	B47	HSCTRL1	Hot Swap Control Input 1	D-I
	A58	HSO1	Hot Swap Output 1	A-O
	B48	HSPWR	Hot Swap Switches Power Input	AP-I
	A59	HSO2	Hot Swap Output 2	A-O
	B49	HSCTRL2	Hot Swap Control Input 2	D-I
CHARGER	A60	CHRG_GND1	Pins A60 & B50 are the Power GND Pins for the Switching Regulator in the Charger. Due to their higher current requirement they are internally tied together & must be connected externally at the PC board also.	A-I
	B50	CHRG_GND2		A-I
	A61	CHRG_SW1	Pins A61 & B51connect to the inductor of the switch-mode step-down regulator for the Battery Charger. Due to their higher current requirement they are internally tied together & must be connected externally at the PC board also.	A-O
	B51	CHRG_SW2		A-O
	A62	CHRG_INPUT1	Pins A62 & B52 provide 5V V_{BUS} Input Power from the USB or from an external wall mounted external supply. Due to their higher current requirement they are internally tied together & must be connected externally at the PC board also.	AP-I
	B52	CHRG_INPUT2		AP-I
	A63	CHRG_SYSVCC1	Pins A63 & B53 are System VCC Output (V_{SYS}). Due to their higher current requirement they are internally tied together & must be connected externally at the PC board also.	A-O
	B53	CHRG_SYSVCC2		A-O
	A64	CHRG_BAT1	Pins A64 & B64 form the positive battery lead connection to a single cell Li-Ion/Li-Poly battery. Due to their higher current requirement they are internally tied together & must be connected externally at the PC board also.	AP-I/O
	B54	CHRG_BAT2		AP-I/O
	A65	CHRG_CLSEN	Input Current Limit Sense/filtering pin for current limit detection	A-I
	B55	CHRG_ICHRG	Current setting. Connect to a current sense resistor	AP-I/O
	A66	CHRG_GATE	Gate Drive for (Optional) External Ideal Diode	A-O
	B56	CHRG_NTC	Thermal Sense, Connect to a battery's thermistor	A-I
	A67	CHRG_VNTC	NTC Power output. This pin provides power to the NTC resistor string. This output is automatically CHRG_SYSVCC level but only enabled when NTC measurement is necessary to save power.	AP-O

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MODULE	PIN #	PIN NAME	DESCRIPTION	I/O TYPE
	B57	GND_BAT/ADCGND	GND_BAT & ADCGND: Shared analog ground pin for battery charger and ADC.	GND
GPIO_TSC	A68	DGND	Digital Ground	GND
	B58	POR_OUT	Power-On-Reset Output, Active Low	GPIO-OUT
	A69	SW_DET	Switch Detect Input	GPIO
	B59	GPIO1/SW_OUT/PENDOWN	GPIO 1: General Purpose I/O # 1 SW_OUT: Switch Detect Output PENDOWN: PENDOWN Detect Output	GPIO
	A70	GPIO3/LED2	GPIO 3**:** General Purpose I/O # 3 LED2: Charger LED # 2 Indicates charging complete	GPIO
	B60	GPIO2/LED1	GPIO 2**:** General Purpose I/O # 2 LED1**:** Charger LED # 1 Indicates charging in progress	GPIO
	A71	NC	No Connect	NC
	A72	GPIO4/CHRG_ILIM	GPIO 4**:** General Purpose I/O # 4 CHRG_ILIM: Control the limit of the Charger Pre-Regulator. CHRG_ILIM = 0, limit current to 500mA; CHRG_ILIM = 1, limit current to 1.5A.	GPIO

I/O LEVELS BY TYPE

I/O TYPE	DESCRIPTION
A-I, A-O & A-IO	**Analog Levels**: Input, Output & Input/Output
AP-I, AP-O & AP-I/O	**Power Supply**: Input, Output & Input/Output
D-I, D-O	**Digital Levels**: Input, Output Voltage levels are all digital levels (nominally 3.3V)
GND	**Ground**: Any connection to Ground
GPIO-IN, GPIO-OUT, GPIO	**General Purpose**: Input, Output, Input/Output. Inputs are 3.3V Outputs are V_{SYS} with open-drain capable
I2C-I, I2C-O & I2CIO	**I²C**: Input, Output & Input/Output Inputs are CMOS Outputs are open-drain.
TCXO-D-I, TCXO-D-O, TCXO-IO	**Clock**: Input, Output, Input/Output Inputs are 1.8V, Outputs are 1.1V to 1.9V

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ABSOLUTE MAXIMUM RATINGS

Stresses above the ratings listed below can cause permanent damage to the P95020. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
CHRG_INPUT to CHRG_GND	USB or Wall Charger Input	Transient t < 1ms, Duty Cycle < 1%	-0.3	7	V
CHRG_BAT to DGND	Battery Input Source		-0.3	5.5	V
CHRG_SYSVCC to DGND	System VCC Output (Vsys)		-0.3	5.5	V
PVDD to PGND	CLASS_D BTL Input Power		-0.3	6	V
LDO_IN1, IN2, IN3 to DGND	Input voltage for LDO		-0.3	6	V
BUCK500_0_IN to BUCK500_0_GND	BUCK0 Input voltage		-0.3	6	V
BUCK500_1_IN to BUCK500_1_GND	BUCK1 Input voltage		-0.3	6	V
BUCK1000_IN to BUCK1000_GND	BUCK2 Input voltage		-0.3	6	V
FDBK to DGND	BUCK0, 1, 2 feedback voltage		-0.3	6	V
LED_BOOST_VIN to LED_BOOST_GND	LED_BOOST Converter gate bias supply		-0.3	6	V
LED_BOOST_GATE to LED_BOOST_GND	LED_BOOST Converter Gate Drive to Power FET		-0.3	LED_BOOST_VIN + 0.3	V
LED_BOOST_VSENSE to LED_BOOST_GND	Voltage Sense Input		-0.3	LED_BOOST_VIN + 0.3	V
LED_BOOST_ISENSE to LED_BOOST_GND	Current Sense Input		-0.3	LED_BOOST_VIN + 0.3	V
LED_BOOST_SINK to LED_BOOST_GND	Current Sink for LED String #1 or String #2		-0.3	6	V
BOOST5_OUT to BOOST5_GND	BOOST5 Converter Output		-0.3	6	V
BOOST5_SW to BOOST5_GND	BOOST5 Converter Power Switch1 and Switch2		-0.3	6	V
HSPWR to DGND	Hot Swap Switches Power		-0.3	6	V
HSCTRL1, HSCTRL2 to DGND	Input voltage for Hot Swap Control		-0.3	HSPWR + 0.3	V
VDDIO_CK to CKGEN_GND	Power Supply for TCXO_OUT1, TCXO_OUT2		-0.3	2.5	V
TCXO_IN to CKGEN_GND	Input voltage for TCXO_IN		-0.3	VDD_CKGEN18 + 0.3	V
32KHZ_CLKIN to CKGEN_GND	Input voltage for 32KHZ_CLK		-0.3	LDO_LP + 0.3	V
GPIO to DGND	Input voltage for GPIO		-0.3	CHRG_SYSVCC + 0.3	V
SDA, SCL to DGND	Input voltage for I2C Master or Slave		-0.3	CHRG_SYSVCC + 0.3	V
BCLK, WS, SDOUT, SDIN to DGND	Input volatge for I2S channel 1 or 2		-0.3	LDO_050_0 + 0.3	V
EX_ROM to DGND	External ROM enable		-0.3	CHRG_SYSVCC + 0.3	V
AGND, LDO_GND, CKGEN_GND, GND, PGND, BOOST5_GND, BCUCK500_0_GND, BCUCK500_1_GND, BUCK1000_GND, LED_BOOST_GND, CHRG_GND, GND_BAT/ADCGND to DGND			-0.3	0.3	V
T_A	Operating Ambient Temperature			-40 to +85	°C
T_J	Operating Junction Temperature			-40 to +125	°C
T_S	Storage Temperature			-40 to +150	°C
T_{SOLDER}	Soldering Temperature			260°C for 10 seconds	-

ESD: The P95020 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the P95020 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
CHRG_INPUT	USB or Wall Charger Input		4.35V		5.5V	V
CHRG_BAT	Battery Input Source	When Vbat providing power	3.0V		4.5V	V
PVDD	CASS_D BTL Input Power Supply		3.0V		5.0V	V
LDO_IN1, IN2, IN3	Input voltage for LDO		3.0V		5.5V	V
BUCK500_0_IN, BUCK500_1_IN, BUCK1000_IN	BUCK0, 1, 2 Input voltage		3.0V		4.5V	V
LED_BOOST_VIN	LED Boost Converter gate bias supply		3.0V		5.5V	V
VDDIO_CK voltage	Power Supply for TCXO_OUT1, TCXO_OUT2		1.1V		1.9V	V
HSPWR	Hot Swap Switches Power Supply	Do not tie to ground or floating	3.0V		5.5V	V
LDO_050_0	Power Supply for I2C Slave Channel, I2S Channel 1 and 2		1.7V		3.6V	V
T_A	Ambient Operating Temperature		-40		85	°C
T_J	Operating Junction Temperature		-40		125	°C

DIGITAL INTERFACES - DC ELECTRICAL CHARACTERISTICS

I2C MASTER - ELECTRICAL CHARACTERISTICS

Unless otherwise specified, typical values at T_A =25C, V_{SYS} = 3.8V, V_{LD0_LP}=3.3V, T_A = -40°C to +85°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage		0.7x V_{LD0_LP}		V_{SYS} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.3x V_{LD0_LP}	V
V_{OL}	Output Low Voltage (Open Drain)	IOL = 3 mA			0.4	V

I2C SLAVE - ELECTRICAL CHARACTERISTICS

Unless otherwise specified, typical values at T_A =25C, V_{SYS} = 3.8V, T_A = -40°C to +85°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{LDO_050_0}$	Input Power Supply		1.7		3.6	V
V_{IH}	Input High Voltage		0.7x $V_{LDO_050_0}$		V_{SYS} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.3x $V_{LDO_050_0}$	V
V_{OL}	Output Low Voltage	IOL = +3 mA			0.4	V

I2S - ELECTRICAL CHARACTERISTICS

Unless otherwise specified, typical values at T_A =25C, V_{SYS} = 3.8V, T_A = -40°C to +85°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{LDO_050_0}$	Input Power Supply		1.7		3.6	V
V_{IH}	Input High Voltage		0.7x $V_{LDO_050_0}$		V_{SYS} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.3x $V_{LDO_050_0}$	V
V_{OH}	Output High Voltage	I_{OH} = -1mA, $V_{LDO_050_0}$ = 3.3V	0.9x $V_{LDO_050_0}$			V
		I_{OH} = -1mA, $V_{LDO_050_0}$ = 2.5V	0.9x $V_{LDO_050_0}$			V
		I_{OH} = -100uA, $V_{LDO_050_0}$ = 1.8V	$V_{LDO_050_0}$ - 0.2			V
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.1x $V_{LDO_050_0}$	V

GPIO - ELECTRICAL CHARACTERISTICS

Unless otherwise specified, typical values at T_A =25C, V_{SYS} = 3.8V, V_{LD0_LP}=3.3V, T_A = -40°C to +85°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage		0.7x V_{LD0_LP}		V_{SYS} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.3x V_{LD0_LP}	V
V_{OH}	Output High Voltage	I_{OH} = -2mA	0.9x V_{SYS}			V
V_{OL}	Output Low Voltage	I_{OL} = 2mA			0.1x V_{SYS}	V

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OVERALL POWER CONSUMPTION

MODE	DESCRIPTION	CHARGE_BAT	TYPICAL CONSUMPTION
Sleep	USB or Wall Adaptor is not present, a main battery is present and well-chaged. Always on LDO_LP is on, RTC is on and RTC registers are maintained. Wake-up capabilities (Switch Detect Input) are available.	Vbat = 3.8V	TBD
Standby	USB or Wall Adaptor is not present, a main battery is present and well-chaged. Always on LDO_LP is on, all DC-DC Bucks in PFM mode. All LDO's are on, no load.	Vbat = 3.8V	TBD
Touch Controller Standby	USB or Wall Adaptor is not present, a main battery is present and well-charged. Always on LDO_LP is on, touch screen controller is on, LDO_050_0 is on.	Vbat = 3.8V	TBD

AUDIO POWER CONSUMPTION

MODE	CHRG_BAT (V)	LDO_050_0 (V)	VDD_AUDIO18 (V)	VDD_AUDIO33 (V)	PVDD (V)	CHRG_BAT (mA)	PVDD (mA)	Total Power (mW)
Playback to 4Ω speaker, sampling at 96 kHz, no signal	3.3	2.3	1.5	3.0	3.0	52	7	192
	3.8	3.3	1.8	3.3	3.3	60	7	252
	4.2	3.6	1.8	3.6	5.0	60	10	302
Playback to 4Ω speaker, sampling at 96 kHz, 0dB FS 1 kHz signal	3.3	2.3	1.5	3.0	3.0	53	155	640
	3.8	3.3	1.8	3.3	3.3	61	170	793
	4.2	3.6	1.8	3.6	5.0	61	258	1546
Playback to 8Ω speaker, sampling at 48 kHz, no signal	3.3	2.3	1.5	3.0	3.0	52	6	190
	3.8	3.3	1.8	3.3	3.3	59	6	244
	4.2	3.6	1.8	3.6	5.0	59	10	298
Playback to 8Ω speaker, sampling at 48 kHz, 0dB FS 1 kHz signal	3.3	2.3	1.5	3.0	3.0	52	96	460
	3.8	3.3	1.8	3.3	3.3	60	105	575
	4.2	3.6	1.8	3.6	5.0	60	163	1067
Playback to 16Ω headphone, sampling at 96 kHz, no signal	3.3	2.3	1.5	3.0	3.0	54	0	178
	3.8	3.3	1.8	3.3	3.3	58	0	220
	4.2	3.6	1.8	3.6	5.0	60	0	252
Playback to 16Ω headphone, sampling at 96 kHz, 0dB FS 1 kHz signal	3.3	1.7	1.5	3.0	3.0	120	0	396
	3.8	3.3	1.8	3.3	3.3	133	0	506
	4.2	3.6	1.8	3.6	5.0	135	0	567
Playback to 16Ω cap-less headphone, sampling at 96 kHz, no signal	3.3	2.3	1.5	3.0	3.0	55	0	182
	3.8	3.3	1.8	3.3	3.3	60	0	228
	4.2	3.6	1.8	3.6	5.0	62	0	260
Playback to 16Ω cap-less headphone, sampling at 96 kHz, 0dB FS 1 kHz signal	3.3	2.3	1.5	3.0	3.0	122	0	403
	3.8	3.3	1.8	3.3	3.3	135	0	513
	4.2	3.6	1.8	3.6	5.0	137	0	576
Stereo playback bypassing ADC and DAC to Class-D 4Ω speaker, no signal	3.3	2.3	1.5	3.0	3.0	41	7	156
	3.8	3.3	1.8	3.3	3.3	48	7	206
	4.2	3.6	1.8	3.6	5.0	48	10	252
Record mode – Stereo Line-In to ADC0 sampling at 96 kHz, no signal	3.3	2.3	1.5	3.0	3.0	45	0	149
	3.8	3.3	1.8	3.3	3.3	49	0	186
	4.2	3.6	1.8	3.6	5.0	50	0	210
Record mode – Analog microphone I/P to ADC1 sampling at 16 kHz, no signal	3.3	2.3	1.5	3.0	3.0	43	0	142
	3.8	3.3	1.8	3.3	3.3	47	0	179
	4.2	3.6	1.8	3.6	5.0	47	0	198
Record mode – Analog microphone I/P to ADC1 sampling at 96 kHz, no signal	3.3	2.3	1.5	3.0	3.0	45	0	149
	3.8	3.3	1.8	3.3	3.3	49	0	186
	4.2	3.6	1.8	3.6	5.0	50	0	210

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1.0 OVERVIEW

The P95020 is an integrated device that combines a microcontroller, power management, battery charging, touch screen controller, system monitoring, clock synthesis, real time clock and audio functionality. All of these subsystems are configured, monitored and controlled by either the on-chip Microcontroller or by an external controller (Application Processor) over an I²C interface. The external Application Processor can monitor and control functions within P95020 even when the internal Microcontroller is enabled. The registers for the various sub functions allow access from more than one controller through an arbitration mechanism implemented in hardware.

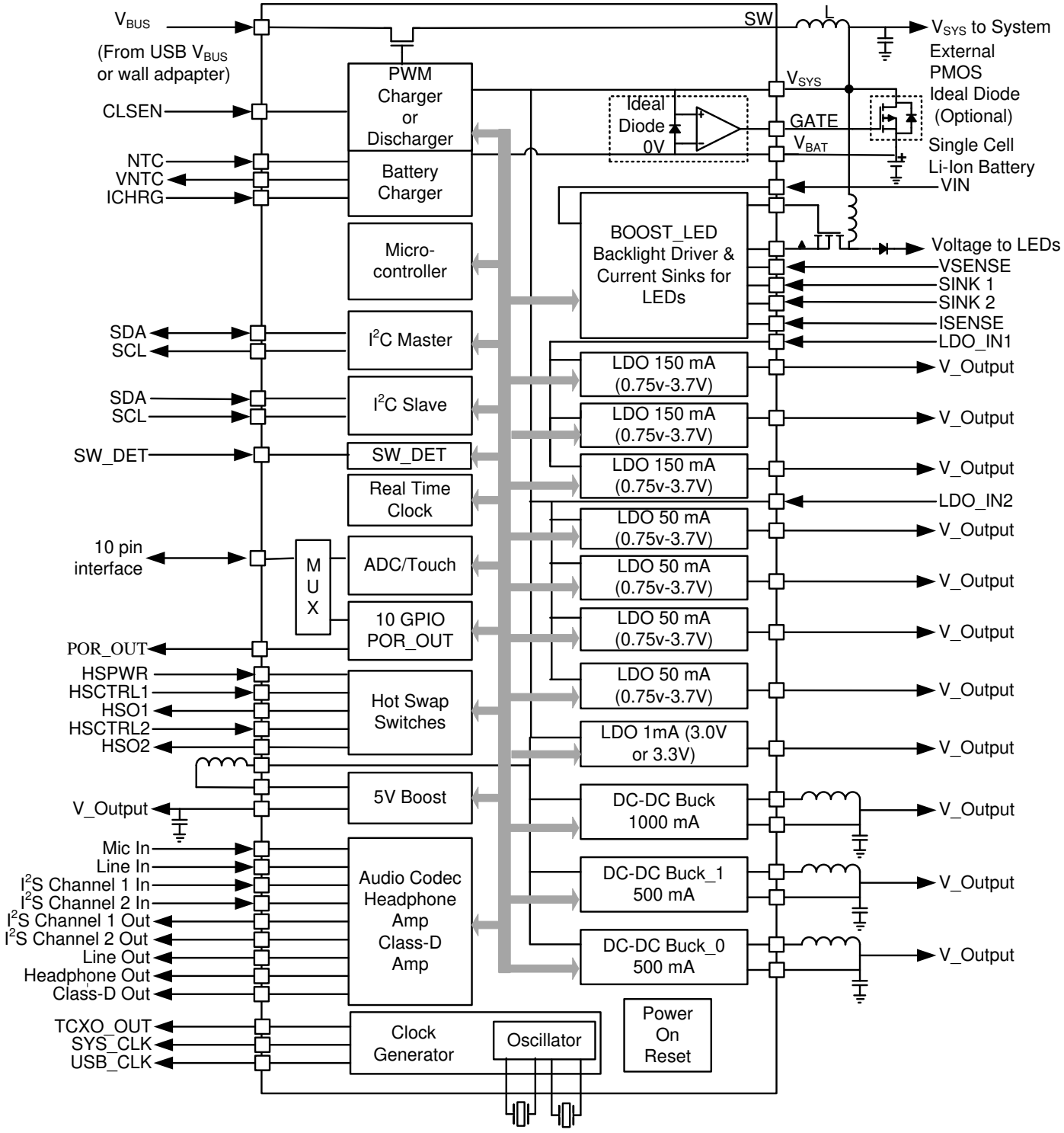

Figure 4 – Overall System Functional Diagram.

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1.1 FUNCTIONAL MODES

There are two primary functional modes for operation: external processor only or simultaneous internal and external processor operation.

External Processor Control

In this mode of operation the external processor can access all internal registers via the I²C interface and receive interrupts via an interrupt pin, and the internal Microcontroller can be powered down or clock gated off.

Combined Internal and External Processor Operation

In this mode of operation the Microcontroller in the P95020 will function autonomously or semi-autonomously based on the content of the on-board or external ROM. The external Application Processor may or may not perform additional control functions through the I²C bus interface. Individual time-based or event-based interrupts generated inside the P95020 device may be routed internally or externally to be handled separately. All I²C registers can be simultaneously accessed by either the external Application Processor or the internal Microcontroller. Access to the I^2C registers is arbitrated via on-chip hardware arbitration.

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1.2 REGISTER MAP

All the P95020 control and status registers accessible to the Microprocessor are mapped to a 1024 location address space. This address space maps to:

4 x 256 Bytes of I²C pages for the I²C slave interface

1024 consecutive addresses in the embedded Microprocessor address space

For easy access from the I²C slave interface (by default 256 Bytes oriented) the first 16 registers of each page are global for all the pages.

Each Module is allocated a consecutive address space.

Register address computation: Address = Base Address + Offset Address

The Base addresses (for both I²C and embedded uP) are listed in the following table. The Offset addresses are defined in different functional Modules. The offset address is labeled as "Offset Address" in the Module Register definition sections.

Table 3 – Register Address Global Mapping

Module	Size (Bytes)	Base Address (I²C)	Base Address (6811 µP)	Register Definition Location	Module Description
Global Registers	16	Page-x: 000(0x00)	0xA000	Page 120 Section 15.7	Global registers are used by the Access Manager, the first 16 registers of each page are global for all the pages.
ACCM	16	Page-0: 016(0x10)	0xA010	Page 123 Section 15.8	Access manager, including an I²C slave and bus arbiter
PCON	32	Page-0: 032(0x20)	0xA020	Page 108 Section 13.7.1	Power controller, including registers that control the on/off of the regulators, and control/sense of the GPIO, power states
				Page 64 Section 4.7	Clock Generator Registers
RTC	32	Page-0: 064(0x40)	0xA040	Page 67 Section 5.2	Real Time Clock
LDO	32	Page-0: 096(0x60)	0xA060	Page 127 Section 16.6	Linear regulators, including regulators for external and internal usage
DC_DC	16	Page-0: 128(0x80)	0xA080	Page 74 Section 7.0	Switching regulators and Class-D BTL driver consisting of three bucks, one 5V boost , one white LED driver and one Class-D BTL driver
CHARGER	16	Page-0: 144(0x90)	0xA090	Page 55 Section 3.5	Battery Charger, including a dedicated switching buck regulator, an ideal diode, a precision reference and thermal sensor
GPT	16	Page-0: 160(0xA0)	0xA0A0	Page 71 Section 6.2	General purpose timers
RESERVED	16	Page-0: 176(0xB0)	0xA0B0		RESERVED
ADC_TSC	64	Page-0: 192(0xC0)	0xA0C0	Page 100 Section 12.4	Touch-screen (ADC, pendown detect and switches, temperature and battery voltage monitoring), and GPIOs
AUDIO	240	Page-1: 000(0x00)	0xA100	Page 40 Section 2.15	Audio subsystem, excluding class-D amplifier
CLASS_D_DIG	240	Page-2: 000(0x00)	0xA200	Page 32 Section 2.13	Class-D amplifier digital processing part
RESERVED	240	Page-3: 000(0x00)	0xA300		RESERVED

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1.3 BYTE ORDERING AND OFFSET

Most registers are defined within one byte width and occupy one byte in the address space. Some registers occupy more than one byte. Please refer to the individual register descriptions for information on how that register is stored in address space.

1.4 REGISTER ACCESS TYPES

TYPE	MEANING
RW	Readable and Writeable
R	Read only
RW1C	Readable and Write 1 to this bit to clear it (for interrupt status)
RW1A	Readable and Write 1 to this bit to take actions

1.5 RESERVED BIT FIELDS

Bit fields and Bytes labeled *RESERVED* are reserved for future use. When writing to a register containing some *RESERVED* bits, the user should do a “read-modify-write” such that only the bits which are intended to be written are modified.

DO NOT WRITE to registers containing all *RESERVED* bits.

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2.0 AUDIO MODULE

FEATURES

- 4 Channels (2 stereo DACs and 2 stereo ADCs) with 24-bit resolution
  - Supports full-duplex stereo audio
  - Provides a mono output
- 2.5W mono speaker amplifier @ 4 ohms and 5V
- Stereo cap-less headphone amplifier
- Two digital microphone inputs
  - Mono or stereo operation
  - Up to 4 microphones in a system
- High performance analog mixer
- 2 adjustable analog microphone bias outputs

DESCRIPTION

The audio system is a low power optimized, high fidelity, 4-channel audio codec with integrated Class D speaker amplifier, cap-less headphone amplifier. It provides high quality HD Audio capability for handheld applications.

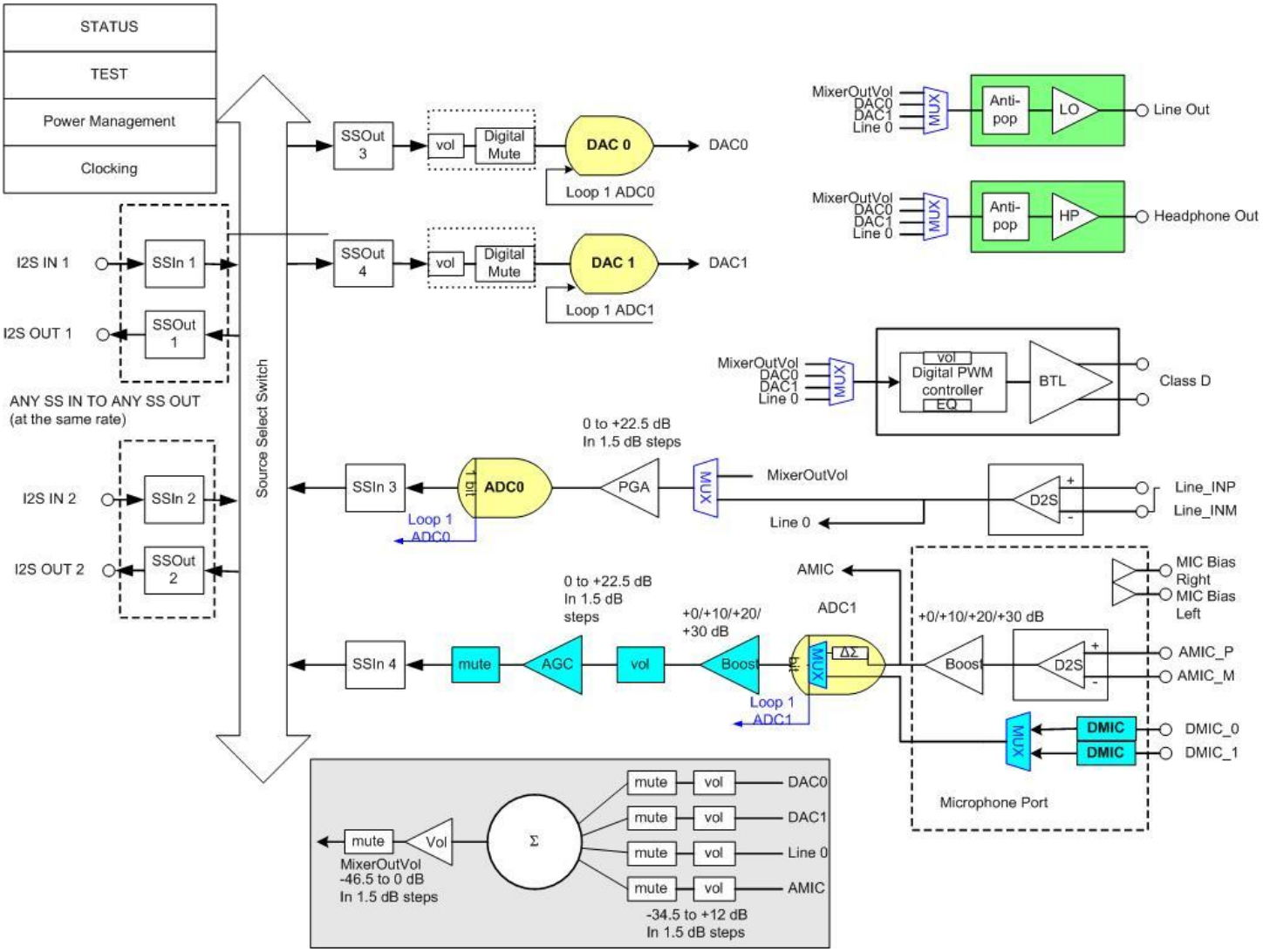

Figure 5 – Audio Block Diagram

2.1 AUDIO - PIN DEFINITIONS

Pin #	PIN_ID	DESCRIPTION
007	MIC_R-	Differential Analog microphone negative input (right channel)
008	MIC_R+/DMICDAT2	Differential Analog microphone positive input (right channel) or second digital microphone data input
009	MICBIAS_R/DMICSEL	Analog microphone supply (right channel) or digital microphone select output (GPO)
010	MICBIAS_L/DMICCLK	Analog microphone supply (left channel) or digital microphone clock output
011	MIC_L+/DMICDAT1	Differential Analog microphone positive input (left channel) or first digital microphone data input

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012	MIC_L-	Differential Analog microphone negative input (left channel)
013	AFILT2	ADC filter cap
014	AFILT1	ADC filter cap
015	AGND_MIC	Return path for microphone supply (MICBIAS_L/R)
016	LISLP	Differential Analog Line Level positive input (left channel)
017	LISLM	Differential Analog Line Level negative input (left channel)
018	LISRP	Differential Analog Line Level positive input (right channel)
019	LISRM	Differential Analog Line Level negative input (right channel)
020	LLO_L	Single Ended Line Level Output (Left channel)
021	LLO_R	Single Ended Line Level Output (Right channel)
022	AVREF	Analog reference (virtual ground) bypass cap
023	VDD_AUDIO33	Filter Capacitor for Internal 3.3V Audio LDO
024	ADC_REF	ADC reference bypass cap
025	HP_R	Cap-less headphone output (right channel)
026	HP_L	Cap-less headphone output (left channel)
027	AGND	Analog (audio) return
028	VIRT_GND	Cap-less headphone signal return (virtual ground)

2.2 AUDIO - SECTION OVERVIEW

The Audio section can be divided into seven subsections.

Analog Input Buffer & Converter Block
DAC, ADC
Audio Mixer Block
Analog and Class D Output Blocks
Sub System Control and Interface Blocks
Note: All register settings are lost when power is removed.

2.3 AUDIO - ANALOG PERFORMANCE CHARACTERISTICS

Unless otherwise specified, typical values at T_A =25C, VSYS = 5V, T_A = -40°C to +85°C,
(VCC_AUDIO33 = 3.3V, VDD_AUDIO18 = 1.8V, AGND = DGND = 0V, T_A = 25 ° C; 1 kHz input sine wave, Sample Frequency = 48 kHz, 0 dB = 1 V_{RMS} into 10 KΩ)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Full Scale Input Voltage:					
All Analog Inputs except Mic (0 dB gain)			1.0		V rms
Differential Mic Inputs (+30dB gain)			30.0		mV rms
Differentail Mic Inputs (0 dB gain)			1.0		V rms
Full Scale Output Voltage:					
Line Input to Line Output			1.0		V rms
HP Output	Per channel / 16 ohm load		0.707		V rms
PCM (DAC) to LINE_OUT			1.0		V rms
Headphone output power	Per channel / 16 ohm load	45	50	55	mWpk
Analog Frequency Response	± 1 dB limits. The max frequency response is 40 kHz if the sample rate is 96 kHz or more.	10		30,000	Hz
Digital S/N	The ratio of the rms output level with 1 kHz full scale input to the rms output level with all zeros into the digital input. Measured “A weighted” over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise ratio) – At Line_Out pins.				
D/A PCM (DAC) to LINE_OUT			95		dB
A/D LINE_IN to PCM			90		dB
Dynamic Range: -60dB signal level	Ratio of Full Scale signal to noise output with -60 dB signal, measured “A weighted” over a 20 Hz to a 20 kHz bandwidth.				
LINE_IN to LINE_OUT (direct)			98		dB
LINE_IN to LINE_OUT (mixer)			95		dB
LINE_IN to HP (direct)			90		dB

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LINE_IN to HP (mixer)			90		dB
DAC to LINE_OUT			93		dB
LINE_IN to A/D			90		dB
Total Harmonic Distortion:	THD+N ratio as defined in AES17 and outlined in AES6id, non-weighted, at 1 kHz. Tested at -3 dB FS or equivalent for analog only paths. 0 dB gain (PCM data -3 dB FS, analog input set to achieve -3 dB full scale port output level)				
LINE_IN to LINE_OUT (direct)			90		dB
LINE_IN to LINE_OUT (mixer)			80		dB
DAC to LINE_OUT			85		dB
DAC to HP (10 KΩ)			80		dB
DAC to HP (16 Ω)			55		dB
LINE_IN to ADC			80		dB
AMIC to ADC			80		dB
D/A Frequency Response	± 0.25 dB limits. The D/A freq. response becomes 40 kHz with sampling rates > 96 kHz. At ±3 dB the response range is from 20-22,500 Hz at 48 kHz, or 20-20,000 Hz @ 44.1 kHz or 20-45,000 Hz @ 96 kHz.	18		22,000	Hz
A/D Frequency Response		20		20,000	Hz
Transition Band	Transition band is 40-60% of sample rate.	19,200		28,800	Hz
Stop Band	Stop band begins at 60% of sample rate	28,800			Hz
Stop Band Rejection		85			dB
Out-of-Band Rejection	The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.	45			dB
Power Supply Rejection Ratio (1 kHz)		70			dB
Crosstalk between Input channels				85	dB
DAC Volume/Gain Step Size			0.75		dB
ADC/Mixer Volume/Gain Step Size			1.5		dB
Analog Mic Boost Step Size			10		dB
Input Impedance			50		K
Differential Input Impedance			20		K
Input Capacitance			15		pF
Mic Bias			2.97		V
External Load Impedance		6			kΩ

2.4 AUDIO - MICROPHONE INPUT PORT

The microphone input port supports either analog or digital microphones. The analog and digital modes share pins so only one mode is supported in a typical application.

2.4.1 AUDIO - Analog Microphone Input mode

The Analog Microphone input path consists of:

Stereo Differential Input Analog Microphone Buffer

- L/R swap
- Mono or stereo
- Microphone Bias Generator with 2 independent bias outputs.
- Microphone Boost Amplifier with selectable gain of 10, 20, or 30dB

The analog microphone interface provides a stereo differential input for supporting common electret cartridge microphones in a balanced configuration (a single-ended configuration is also supported). A boost amplifier provides up to 30dB of gain to align typical microphone full scale outputs to the ADC input range. The microphone input is then routed

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to both ADC1 and the analog mixer for further processing. By using the analog mixer the analog microphone input may be routed to ADC0, the line output port or the headphone output port.

2.4.2 AUDIO - Digital Microphone Input mode

The Digital Microphone Input path consists of:

Digital Microphone input buffer and MUX with the following features:

- One or two microphones per DMICDATx input.
- Mono data sampled during high or low clock level.
- L/R swap
- Versatile DMICSEL output pin for control of digital microphone modules or other external circuitry. (Used primarily to enable/disable microphones that do not support power management using the clock pin.)

The digital microphone interface permits connection of a digital microphone(s) via the DMICDAT1, DMICDAT2, and DMICCLK 3-pin interface. The DMICDAT1 and DMICDAT2 signals are inputs that carry individual channels of digital microphone data to the ADC. In the event that a single microphone is used, the data is ported to both ADC channels. This mode is selected using a register setting and the left time slot is copied to the ADC left and right inputs. The digital microphone input is only available at ADC1.

The DMICCLK output is controllable from 4.704 MHz, 3.528 MHz, 2.352 MHz, 1.176 MHz and is synchronous to the internal master clock (MCLK). The default frequency is 2.352 MHz.

To conserve power, the analog portion of the ADC and the analog boost amplifier will be turned off if the D-mic input is selected. When switching from the digital microphone to an analog input to the ADC, the analog portion of the ADC will be brought back to a full power state and allowed to stabilize before switching from the digital microphone to the analog input. This should take less than 10mS.

The P95020 codec supports the following digital microphone configurations:

Table 4 - Valid Digital Mic Configurations

MODE	DIGITAL MICS	DATA SAMPLE	INPUT	NOTES
0	0	N/A	N/A	No Digital Microphones (1010 bit pattern sent to ADC to avoid pops)
1	2	Double Edge	DMICDAT1	Two microphones connected to DMICDAT1. PhAdj settings apply to Left microphone. Right Microphone sampled on opposite phase. DMICDAT2 ignored.
2	2	Double Edge	DMICDAT2	Two microphones connected to DMICDAT2. PhAdj settings apply to Left microphone. Right Microphone sampled on opposite phase. DMICDAT1 ignored.
3	2	Single Edge	DMICDAT1 and DMICDAT2	DMICDAT1 used for left data and DMICDAT2 used for right data.
3	2	Double Edge	DMICDAT1 and DMICDAT2	Two microphones, one on each data input. “Left” microphone used for each channel. Two “Right” microphones may be used by inverting the microphone clock or adjusting the sample phase.

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