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PAC1932/3/4

Multi-Channel DC Power/Energy Monitor with Accumulator

Features

- High-Side Current Monitor with 2, 3 or 4 Channels
  - 100 mV full scale range for current sense voltage,16 bit resolution
  - Selectable bidirectional current sense capability, -100 mV to +100 mV range, 16 bit two's complement (signed) data format
  - External sense resistor sets full scale current range
  - Very low input current simplifies routing
- Wide Bus Voltage Range for Voltage Monitor
  - 0V to 32V input common-mode voltage
  - 16 bit resolution for voltage measurements, 14 bits are used for power calculations
- Real Time Auto-Calibration of Offset and Gain Errors for Voltage and Current, No User Adjustment Required
- 1% Power Measurement Accuracy over a Wide Dynamic Range
- On-Chip Accumulation of 28-bit Power Results for Energy Measurement
  - 48-bit power accumulator register for recording accumulated power data
  - 24 bit Accumulator Count
  - User programmable sampling rates of 8, 64, 256 and 1024 samples per second
  - 17 minutes of power data accumulation minimum at 1024 S/s
  - Over 36 hours of power data accumulation minimum at 8 S/s
- 2.7V to 5.5V Supply Operation
  - Separate V_{DD} I/O pin for digital I/O
  - 1.62-5.5V capable SMBus and digital I/O
  - SMBus 3.0 and I^2C Fast Mode Plus (1Mb/S)
- SMBus Address – 16 Options, set with Resistor
- No Input Filters Required
- ALERT Features that can be Enabled:
  - ALERT on accumulator overflow
  - ALERT on Conversion Complete
- 4x4x0.5 mm UQFN Package
- 2.225x2.17 mm WLCSP Package
  - WLCSP available for PAC1934 only
  - Contact Marketing for other options

Applications

- Embedded Computing
- Networking
- FPGA Systems
- Automotive
- Low voltage/High Power – AI, GPU
- Industrial
- Linux Applications
- Notebook and Tablet Computing
- Cloud, Linux and Server Computing

Computing Platform Support

- Windows® 10 Driver
- Linux Driver
- Python Script

Description

The PAC1932/3/4 are two, three and four-channel power and energy monitoring devices. A high-voltage multiplexer sequentially connects the inputs to a bus voltage monitor and current sense amplifier that feed high-resolution ADCs. Digital circuitry performs power calculations and energy accumulation.

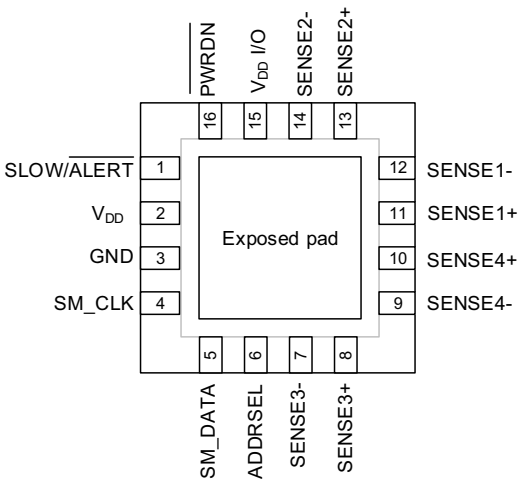
This enables energy monitoring with integration periods from 1 ms up to 36 hours or longer. Bus voltage, sense resistor voltage and accumulated proportional power are stored in registers for retrieval by the system master or Embedded Controller.

The sampling rate and energy integration period can be controlled over SMBus or I^2C. Active channel selection, one-shot measurements and other controls are also configurable by SMBus or I^2C.

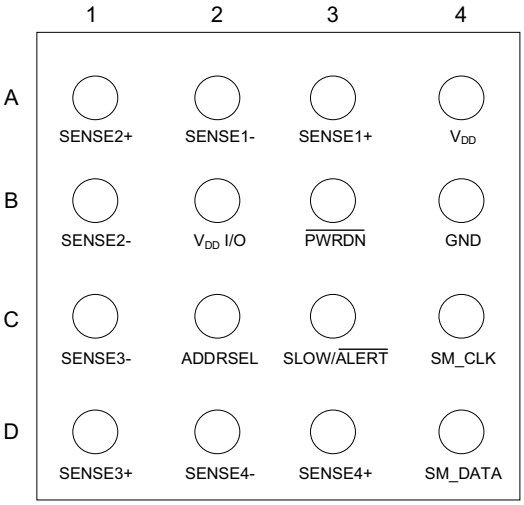
The PAC1932/3/4 device family uses real time calibration to minimize offset and gain errors. No input filters are required for this device.

Package Types

PAC1932/3/4 – Top View
4x4x 0.5 mm UQFN*

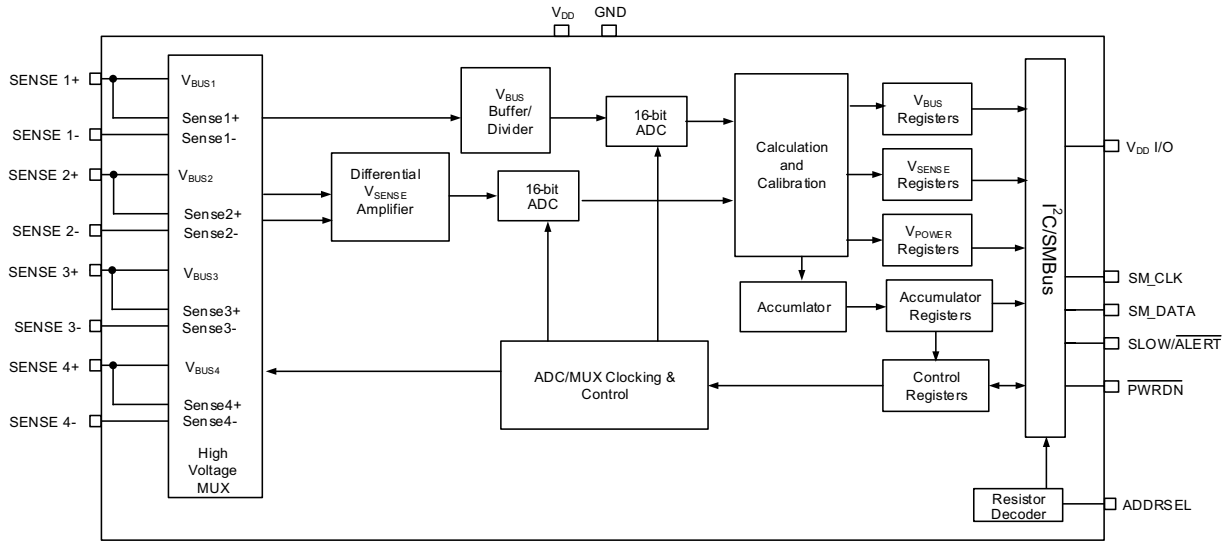


PAC1934 – Top View
2.225x2.17 mm WLCSP



*Includes Exposed Thermal Pad; see Table 3-1.

Device Block Diagram



Note: For PAC1932, channels 3 and 4 are inactive.
For PAC1933, channel 4 is inactive.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Electrical Specifications

Absolute Maximum Ratings(†)

V_{DD} pin ..... -0.3 to 6.0V

Voltage on SENSE- and SENSE+ pins ..... -0.3 to 40V

Voltage on any other pin to GND ..... GND -0.3 to +6.0V

Voltage between Sense pins (|(SENSE+ – SENSE-)|) ..... 500 mV

Input current to any pin except V_{DD} ..... ±100 mA

Output short-circuit current ..... Continuous

Junction to Ambient (θ_{J-A}) ..... +78°C/W

Operating Ambient Temperature Range ..... -40 to +150°C

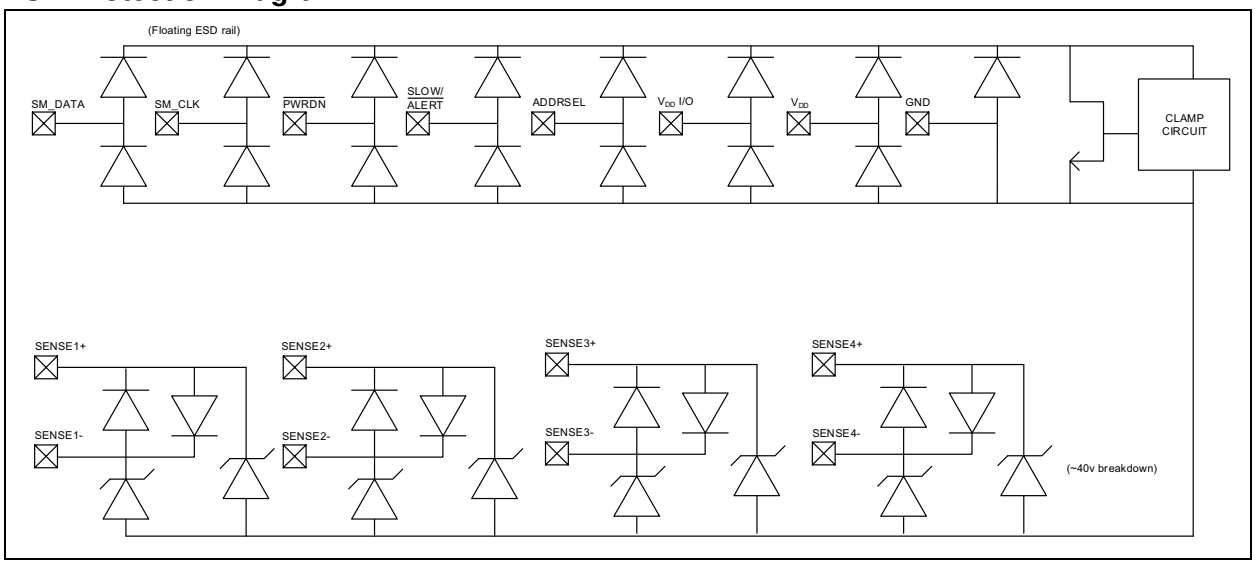
Storage Temperature Range ..... -55 to +150°C

ESD Rating – all pins – HBM 4000V

ESD Rating – all pins – CDM 2000V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

ESD Protection Diagram



This diagram represents the ESD protection circuitry on the PAC1934. The SENSE pins are allowed to be at 32V if V_{DD} is at zero. The back-to-back diodes between the Sense+ and Sense- pins have 1 kΩ resistors in series with them.

For PAC1932 and PAC1933, some of the SENSE pins are not electrically connected inside. These unconnected pins should be grounded.

TABLE 1-1: DC CHARACTERISTICS

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, $V_{DD\ I/O}$= 1.62V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C V_{DD} = $V_{DD\ I/O}$ = 3.3V, V_{BUS} = 32V, V_{SENSE} = (SENSE+ – SENSE-) = 0V

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Supply						
V_{DD} Range	V_{DD}	2.7	—	5.5	V	
$V_{DD\ I/O}$ Range	V_{DD} I/O	1.62	—	5.5	V	
V_{DD} Pin Active Current	I_{DD}	—	585	675	µA	1024 Samples/s All IDD specifications are the same for PAC1932/3/4
V_{DD} Pin Active Current	$I_{DD\ SLOW}$	—	16	—	µA	4 channels enabled, 8 Samples/s
Minimum V_{DD} Rise Rate	$V_{DD\_RISE\_MIN}$	—	0.05	—	V/ms	0 to 5V in 100 ms
Maximum V_{DD} Rise Rate	V_{DD_RISE}	—	1000	—	V/ms	0 to 5V in 5 µs
V_{DD} Sleep Current	I_{DD_SLEEP}	—	5	—	µA	Sleep State
V_{DD} Power-Down Current	I_{DD_PWRDN}	—	0.1	—	µA	Power-Down State
$V_{DD\ I/O}$ Current	$I_{DD\ I/O}$	—	—	2	µA	All States
Analog Input Characteristics						
V_{BUS} Voltage Range	V_{BUS}	–0.2V	—	32	V	Common mode range for SENSE+ and SENSE- pins, referenced to ground (negative range not tested in production)
V_{SENSE} Differential Input Voltage Range	V_{SENSE_DIF}	–100	—	100	mV	
SENSE+, SENSE- Pin Input Current	I_{SENSE+}, I_{SENSE-}	–7	0	7	µA	V_{SENSE}+ = V_{SENSE}- = 32V (Input current is the combined current for the two pins)
SENSE+, SENSE- Pin Input current	I_{SENSE+}, I_{SENSE-}	–1	0	1	µA	V_{SENSE}+ = 6V, V_{SENSE}- = 5.9V
V_{SENSE} Measurement Accuracy						
V_{SENSE} Gain Accuracy	$V_{SENSE\_GAIN\_ERR}$	—	±0.2 ±1	±0.9	% %	At +25°C typical, -40 to +85°C
V_{SENSE} Offset Accuracy, referenced to input	$V_{BUS\_OFFSET\_ERR}$	—	±0.02 ±0.2	±0.1	mV mV	At +25C° typical, -40 to +85°C
V_{SENSE} – Unidirectional Currents						
V_{SENSE} ADC Resolution	V_{SENSE_RES}	—	—	16	Bits	Straight Binary for unidirectional currents
V_{SENSE} Full Scale Range	V_{SENSE_FSR}	0	—	100	mV	Unidirectional currents
V_{SENSE} LSB Step Size	V_{SENSE_LSB}	—	1.5	—	µV	Unidirectional currents
V_{SENSE} – Bidirectional Currents						
V_{SENSE} ADC Resolution	V_{SENSE_RES}	—	—	16	bits	16-bit two's complement (signed)
V_{SENSE} Full Scale Range	V_{SENSE_FSR}	-100	—	100	mV	Bidirectional currents

TABLE 1-1: DC CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, $V_{DD\ I/O}$= 1.62V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C V_{DD} = $V_{DD\ I/O}$ = 3.3V, V_{BUS} = 32V, V_{SENSE} = (SENSE+ – SENSE-) = 0V

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{SENSE} LSB Step Size	V_{SENSE_LSB}	—	3	—	µV	Bidirectional currents
V_{BUS} Measurement Accuracy						
V_{BUS} Gain Accuracy	$V_{BUS\_GAIN\_ERR}$	—	±0.02 ±0.2	±0.5	% %	At +25°C typical, -40 to +85°C
V_{BUS} Offset Accuracy, referenced to input	$V_{BUS\_OFFSET\_ERR}$	—	±1 ±2	—	LSB LSB	At +25°C typical, -40 to +85°C
V_{BUS} – Unipolar Voltages						
V_{BUS} ADC Resolution	V_{BUS_RES}	—	—	16	bits	Straight Binary for unidirectional currents
V_{BUS} Unipolar Full-Scale Range	V_{BUS_FSR}	0	—	32	V	Unipolar voltage
V_{BUS} LSB Step Size	V_{BUS_LSB}	—	488	—	µV	FSR = 32V, 16-bit resolution
V_{BUS} – Bipolar Voltages						
V_{BUS} ADC Resolution	V_{BUS_RES}	—	—	16	bits	16-bit two's complement (signed) numbers are reported for V_{BUS} measurement result
V_{BUS} Bipolar Full-Scale Range	V_{BUS_FSR}	–32	—	32	V	Mathematical scaling. Physics limits the negative input voltage to -0.2V
V_{BUS} LSB Step Size	V_{BUS_LSB}	—	976	—	µV	Bipolar voltages

TABLE 1-1: DC CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, $V_{DD\ I/O}$= 1.62V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C V_{DD} = $V_{DD\ I/O}$ = 3.3V, V_{BUS} = 32V, V_{SENSE} = (SENSE+ – SENSE-) = 0V						
Characteristic	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Power Accumulator Accuracy						
Accumulator Error	$_{ACC\_Err}$	—	0.2	—	%	V_{SENSE} = 97 mV
Accumulator Error	$_{ACC\_Err}$	—	0.2	—	%	V_{SENSE} = 10 mV
Accumulator Error	$_{ACC\_Err}$	—	1	—	%	V_{SENSE} = 1 mV
Accumulator Error	$_{ACC\_Err}$	—	3	—	%	V_{SENSE} = 100 µV
Accumulator Error	$_{ACC\_Err}$	—	5	—	%	V_{SENSE} = 50 µV
Active Mode Timing						
Pull-Up Voltage Range	V_{PULLUP}	1.62	—	5.5	V	Pull-up voltage for I^2C/SMBus pins and digital I/O pins. Set by V_{DD} I/O.
Time to First Communications	t_{INT_T}	—	14.25	—	ms	
Transition From Sleep State to Start of Conversion Cycle	$t_{SLEEP\_TO\_ACTIVE}$	—	3	—	ms	
Digital I/O Pins (SM_CLK, SM_DATA, SLOW/$\overline{\text{ALERT}}$, $\overline{\text{PWRDN}}$)						
Input High Voltage	V_{IH}	V_{DD} I/O x 0.7	—	—	V	
Input Low Voltage	V_{IL}	—	—	V_{DD} I/O x 0.3	V	
Output Low Voltage	V_{OL}	—	—	0.4	V	Sinking 8 mA for the $\overline{\text{ALERT}}$ pin and 20 mA for the SMCLK pin
Leakage Current	I_{LEAK}	–1	—	+1	µA	

TABLE 1-2: SMBUS MODULE SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 32V; Typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 32V, V_{SENSE} = (SENSE+ – SENSE-) = 0V, V_{DD} I/O = 1.62V to 5.5V						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SMBus Interface						
Input Capacitance	C_{IN}	—	4	10	pF	Not tested in production
SMBus Timing						
Clock Frequency	f_{SMB}	.010	—	1	MHz	No minimum if Time-Out is not enabled.
Spike Suppression	t_{SP}	0	—	50	ns	
Bus Free Time Stop to Start	t_{BUF}	0.5	—	—	µs	Per SMBus 3.0
Hold Time after Repeated Start Condition	$t_{HD:STA}$	0.26	—	—	µs	Per SMBus 3.0
Repeated Start Condition Setup Time	$t_{SU:STA}$	0.26	—	—	µs	Per SMBus 3.0
Setup Time: Stop	$t_{SU:STO}$	0.26	—	—	µs	Per SMBus 3.0
Setup Time: Start	$t_{SU:STA}$	0.26	—	—	µs	
Data Hold Time	$t_{HD:DAT}$	0	—	—	µs	
Data Setup Time	$t_{SU:DAT}$	50	—	—	ns	Per SMBus 3.0 (**Note**)
Clock Low Period	t_{LOW}	0.5	—	—	µs	Per SMBus 3.0
Clock High Period	t_{HIGH}	0.26	—	50	µs	
Clock/Data Fall Time	t_{FALL}	—	—	120	ns	Not tested in production
Clock/Data Rise Time	t_{RISE}	—	—	120	ns	Not tested in production
Capacitive Load	C_{LOAD}	—	—	550	pF	Per bus line, C_{LOAD} not tested in production
SLOW Pin Pulse Width	SLOWpw	—	100	—	µs	Pulses narrower than 100 µS may not be detected

Note: A device must internally provide a hold time of at least 300 ns for the SM_DATA signal (with respect to the $V_{IH(min)}$ of the SM_CLK signal) to bridge the undefined region of the falling edge of SM_CLK.

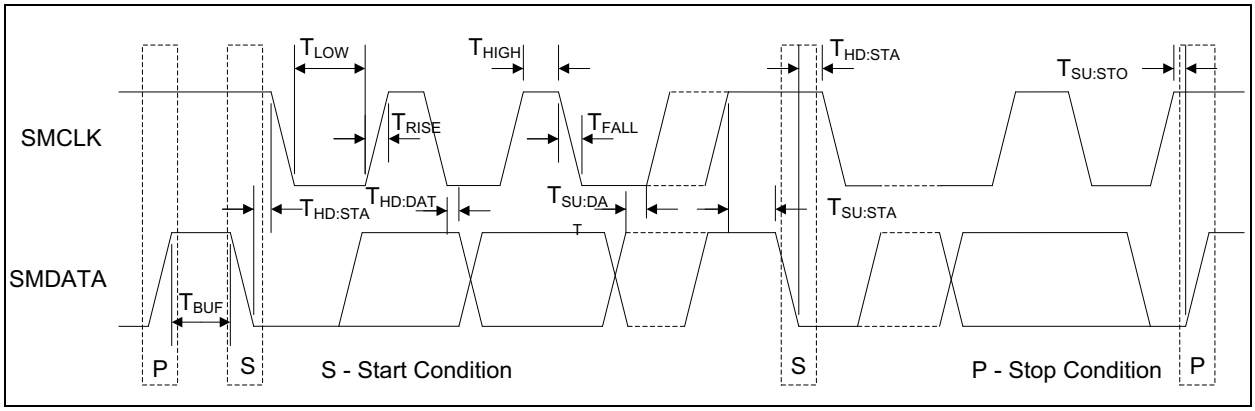


FIGURE 1-1: *SMBus Timing.*

NOTES:

2.0 TYPICAL OPERATING CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 3.3V, V_{SENSE} = (SENSE+ – SENSE-) = 0V, V_{DD} I/O = 1.62 to 5.5V.

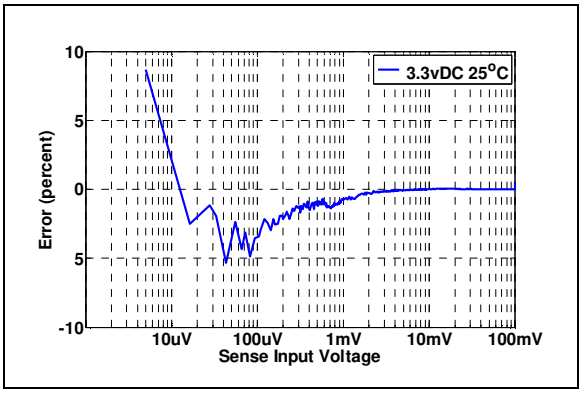


FIGURE 2-1: *V_{SENSE} Error vs. V_{SENSE} Input Voltage.*

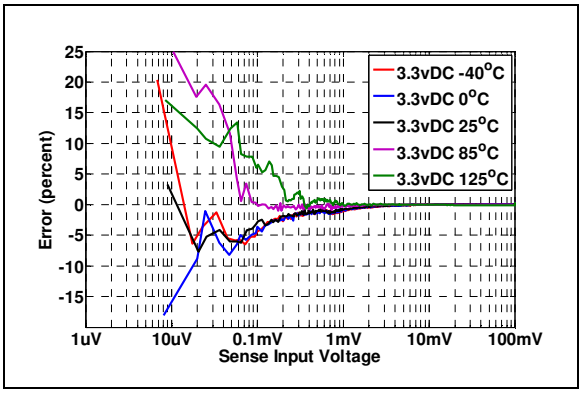


FIGURE 2-4: *V_{SENSE} Error vs. V_{SENSE} Input Voltage and Temperature.*

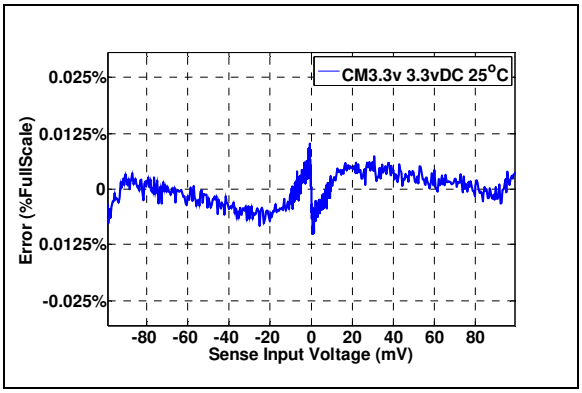


FIGURE 2-2: *V_{SENSE} Error vs. V_{SENSE} Input Voltage Bidirectional Mode.*

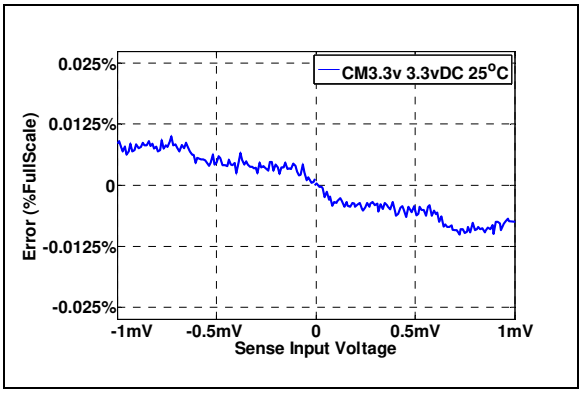


FIGURE 2-5: *V_{SENSE} Error vs. V_{SENSE} Input Voltage Bidirectional Mode (Zoom View).*

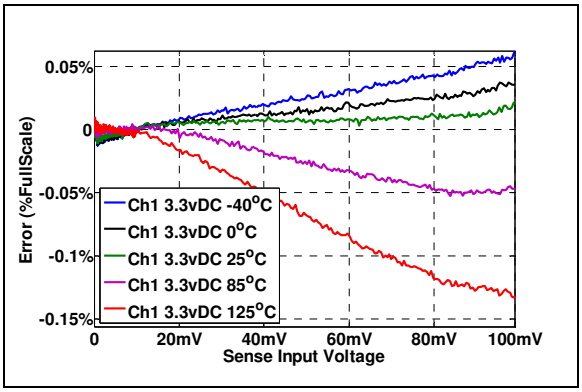


FIGURE 2-3: *V_{SENSE} Error vs. V_{SENSE} Input Voltage vs. Temperature.*

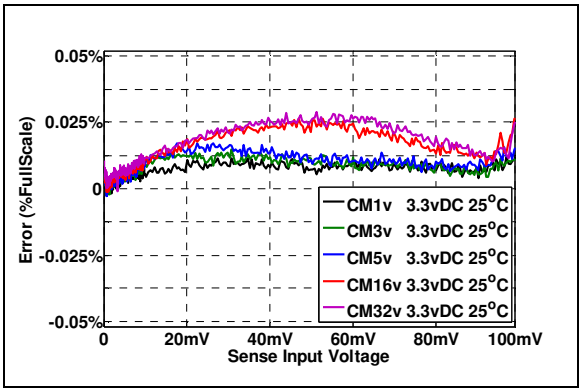


FIGURE 2-6: *V_{SENSE} Error vs. V_{SENSE} and Common Mode.*

Note: Unless otherwise indicated, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 3.3V, V_{SENSE} = (SENSE+ – SENSE-) = 0V, V_{DD} I/O = 1.62 to 5.5V.

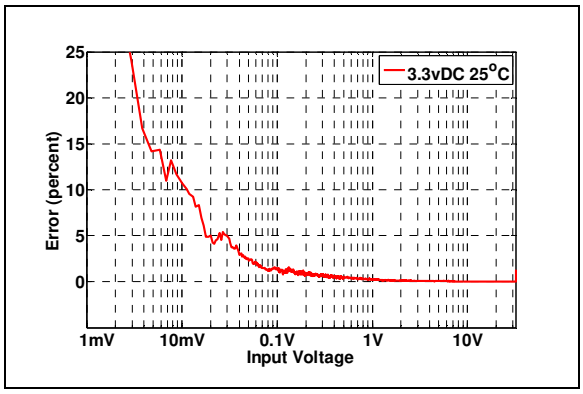


FIGURE 2-7: *V_{BUS} Error vs. V_{BUS} Input Voltage.*

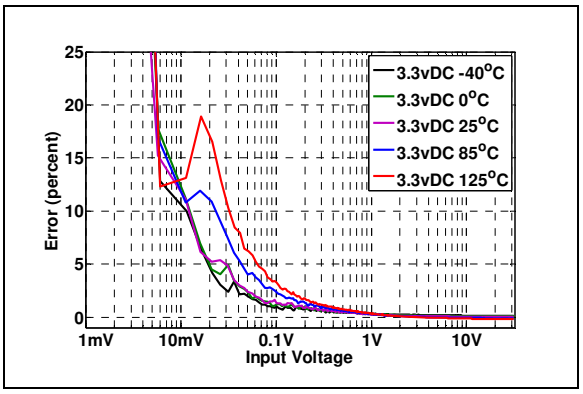


FIGURE 2-10: *V_{BUS} Error vs. V_{BUS} Input Voltage vs. Temperature.*

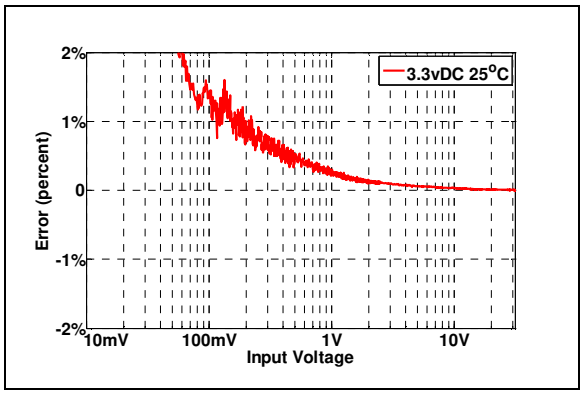


FIGURE 2-8: *V_{BUS} Error vs. V_{BUS} Input Voltage (Zoom View).*

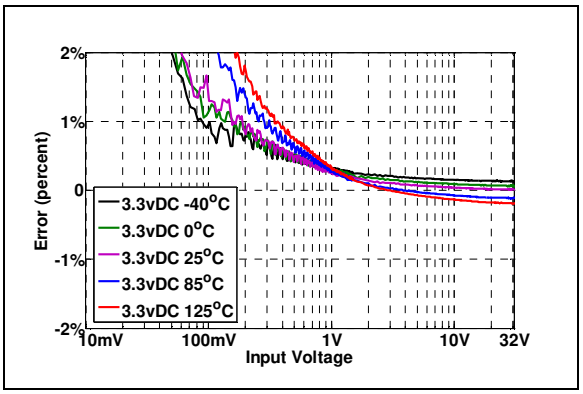


FIGURE 2-11: *V_{BUS} Error vs. V_{BUS} Input Voltage vs. Temperature (Zoom View).*

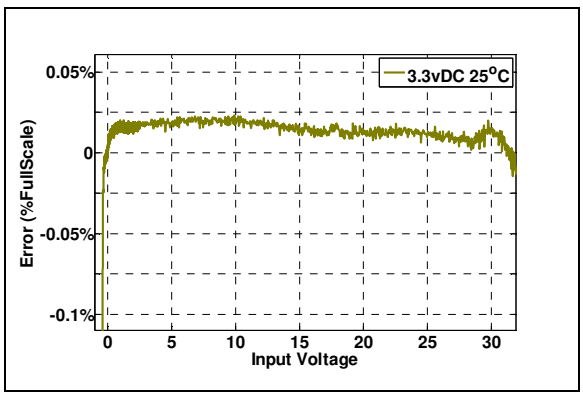


FIGURE 2-9: *V_{BUS} Error vs. V_{BUS} Input Voltage.*

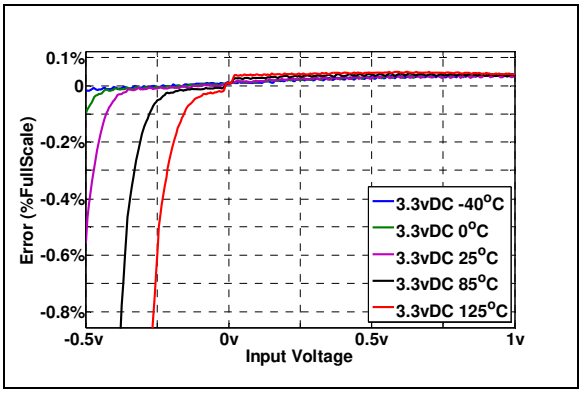


FIGURE 2-12: *V_{BUS} Error vs. V_{BUS} Input Voltage vs. Temperature (Bipolar Voltage Mode).*

Note: Unless otherwise indicated, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 3.3V, V_{SENSE} = (SENSE+ – SENSE-) = 0V, V_{DD} I/O = 1.62 to 5.5V.

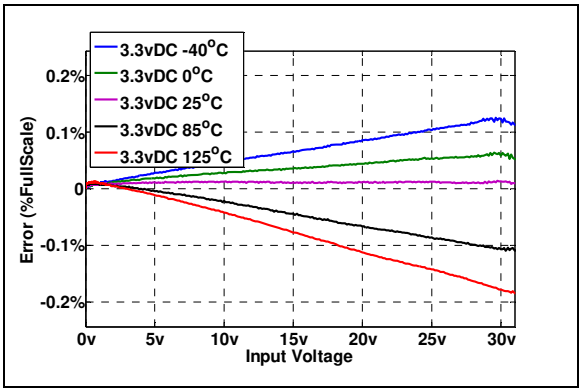


FIGURE 2-13: *V_{BUS} Error vs. V_{BUS} Input Voltage vs. Temperature.*

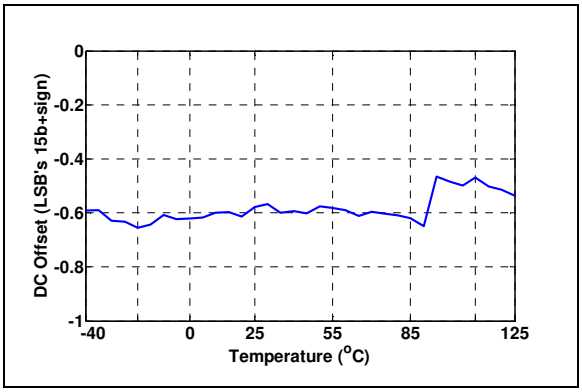


FIGURE 2-16: *Input Offset for V_{BUS} Measurements vs. Temperature.*

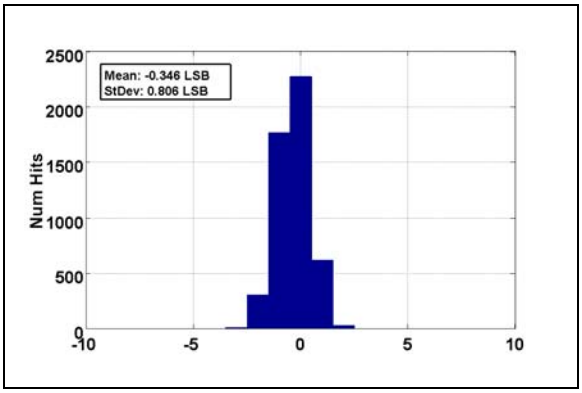


FIGURE 2-14: *Zero Input Histogram for V_{BUS} (LSBs, 8X Average Results, Total Population 5,000 devices).*

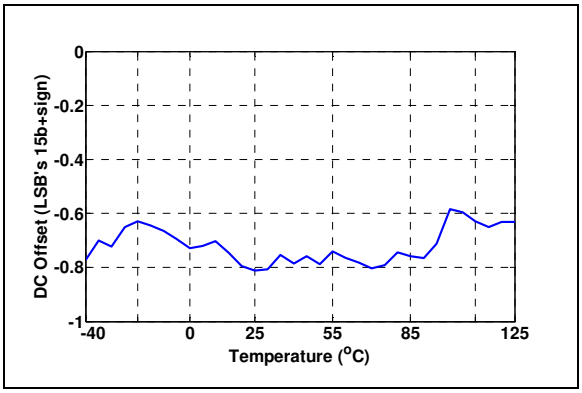


FIGURE 2-17: *Input Offset for V_{SENSE} Measurements vs. Temperature.*

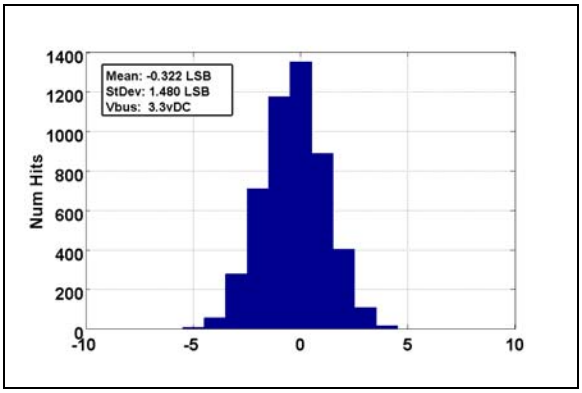


FIGURE 2-15: *Zero Input Histogram for V_{SENSE} (LSBs, 8X Average Results, Total Population 5,000 Devices).*

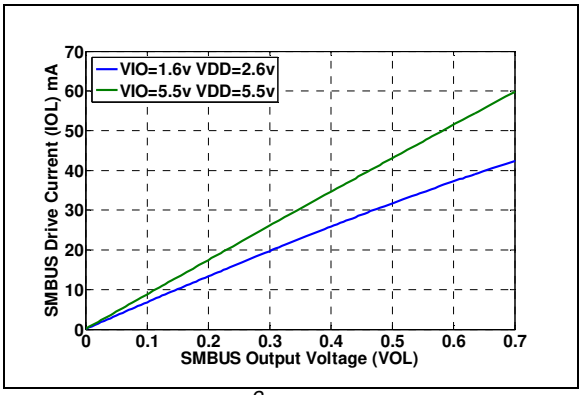


FIGURE 2-18: *I^2C/SMBus Drive Current vs. V_{OL}.*

Note: Unless otherwise indicated, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 3.3V, V_{SENSE} = (SENSE+ – SENSE-) = 0V, V_{DD} I/O = 1.62 to 5.5V.

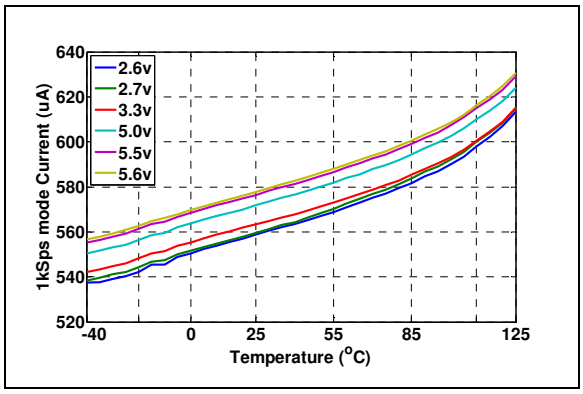


FIGURE 2-19: *I_{DD} vs. Temperature and Supply at 1024 Samples/Second.*

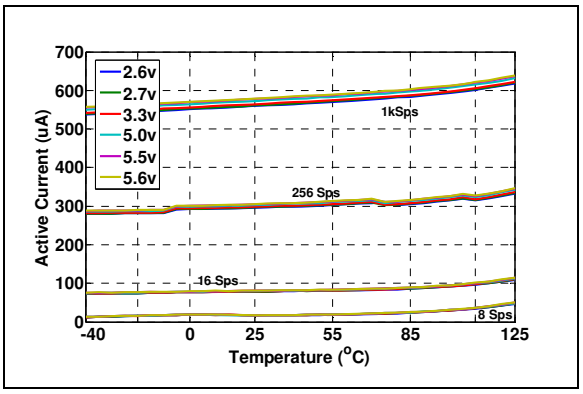


FIGURE 2-22: *I_{DD} vs.Temperature, V_{DD}, and Sample Rate.*

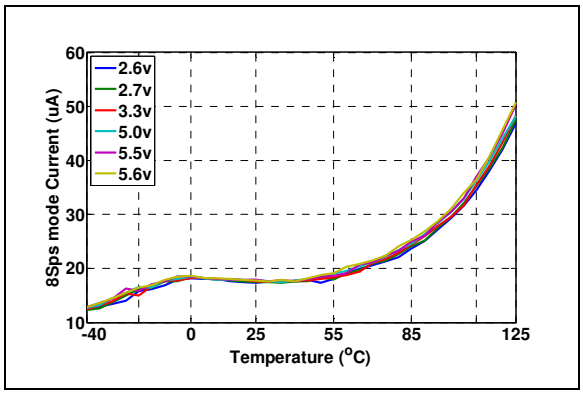


FIGURE 2-20: *I_{DD} in SLOW Mode vs. Temperature and V_{DD}.*

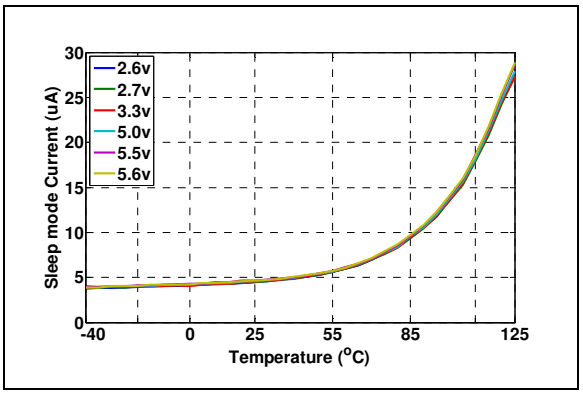


FIGURE 2-23: *I_{DD} in SLEEP Mode vs. Temperature and V_{DD}.*

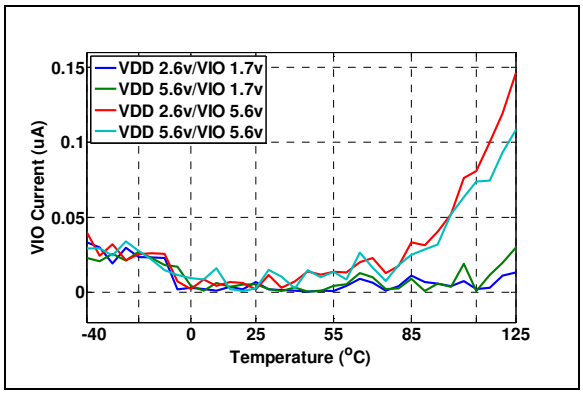


FIGURE 2-21: *I_{DD} for V_{DD} I/O Pin vs. Temperature and V_{DD}.*

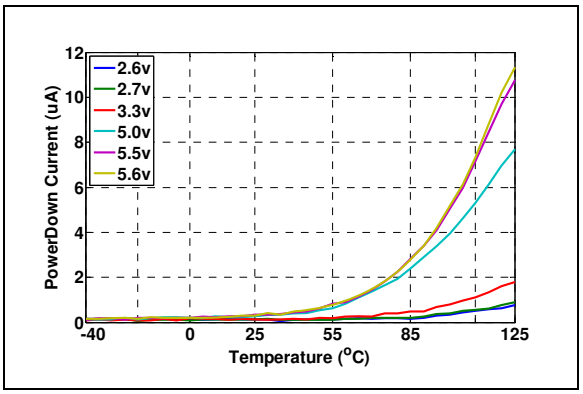


FIGURE 2-24: *I_{DD} in Power Down Mode vs. Temperature and V_{DD}.*

Note: Unless otherwise indicated, maximum values are at T_A = -40°C to +85°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 32V; typical values are at T_A = +25°C, V_{DD} = 3.3V, V_{BUS} = 3.3V, V_{SENSE} = (SENSE+ – SENSE-) = 0V, V_{DD} I/O = 1.62 to 5.5V.

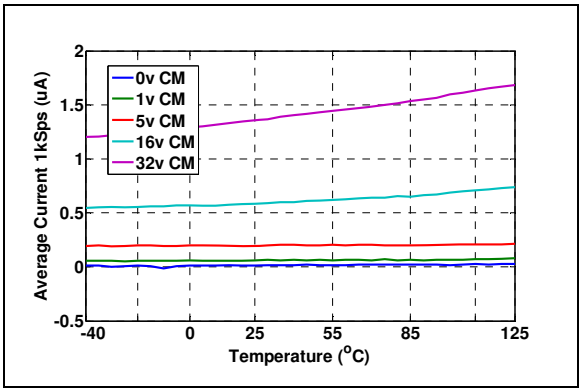


FIGURE 2-25: *V_{SENSE} Input Current – Active Mode, 1024 Samples/Second.*

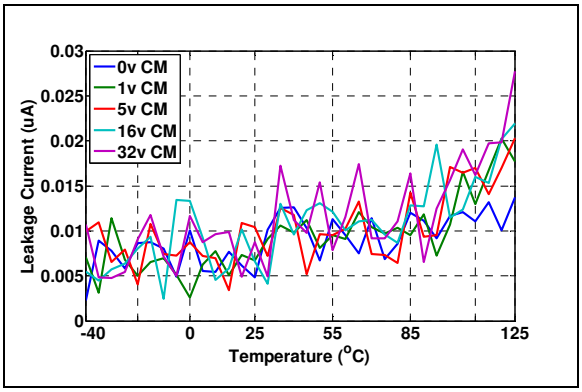


FIGURE 2-28: *V_{SENSE} Input Leakage Current vs. V_{DD} and Temperature.*

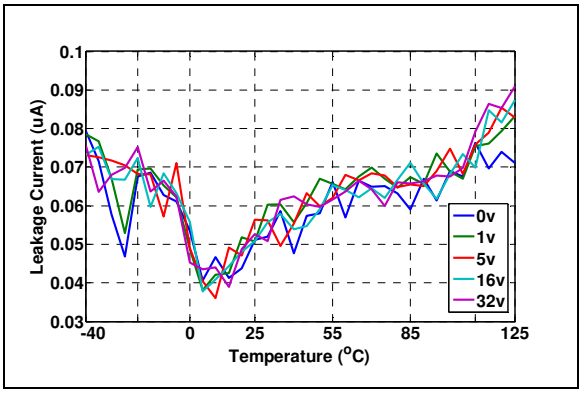


FIGURE 2-26: *V_{BUS} Input Leakage Current vs. V_{DD} and Temperature.*

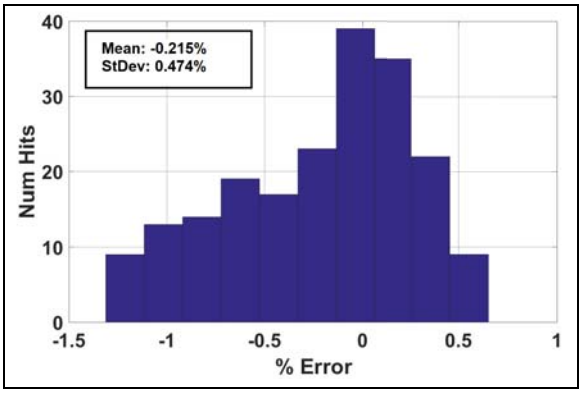


FIGURE 2-29: *Clock Frequency Error -40°C to +85°C. Total Population 200 Devices.*

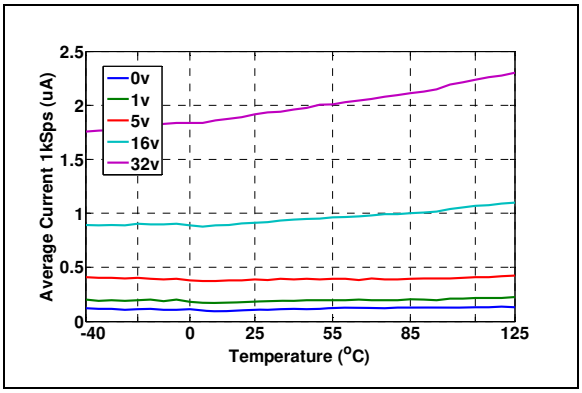


FIGURE 2-27: *V_{BUS} Input Current – Active Mode, 1024 Samples/Second.*

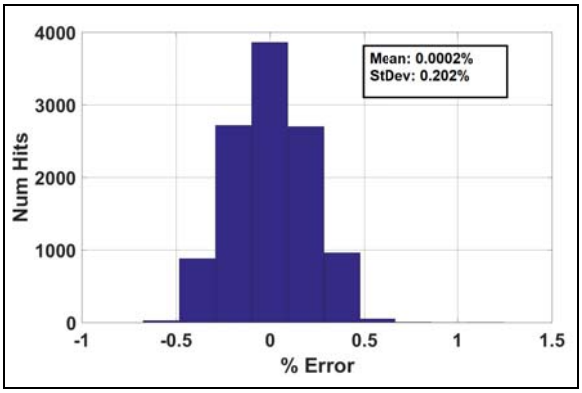


FIGURE 2-30: *Clock Frequency Error at 30°C. Total Population 11,189 Devices.*

Figure 2-31 shows the equivalent circuitry for the input channels of the PAC193X devices. ESD protection diodes include two 40V breakdown diodes. Input leakage current is very low (no DC bias current). The switched capacitor sampling circuits shown as a switch with equivalent series resistance and sampling capacitor. The switches work at 1024 samples per second (SPS) maximum, independent of sampling rate (at 8 SPS, the device is sleeping in between samples). Input impedance for each input is about 32 MΩ.

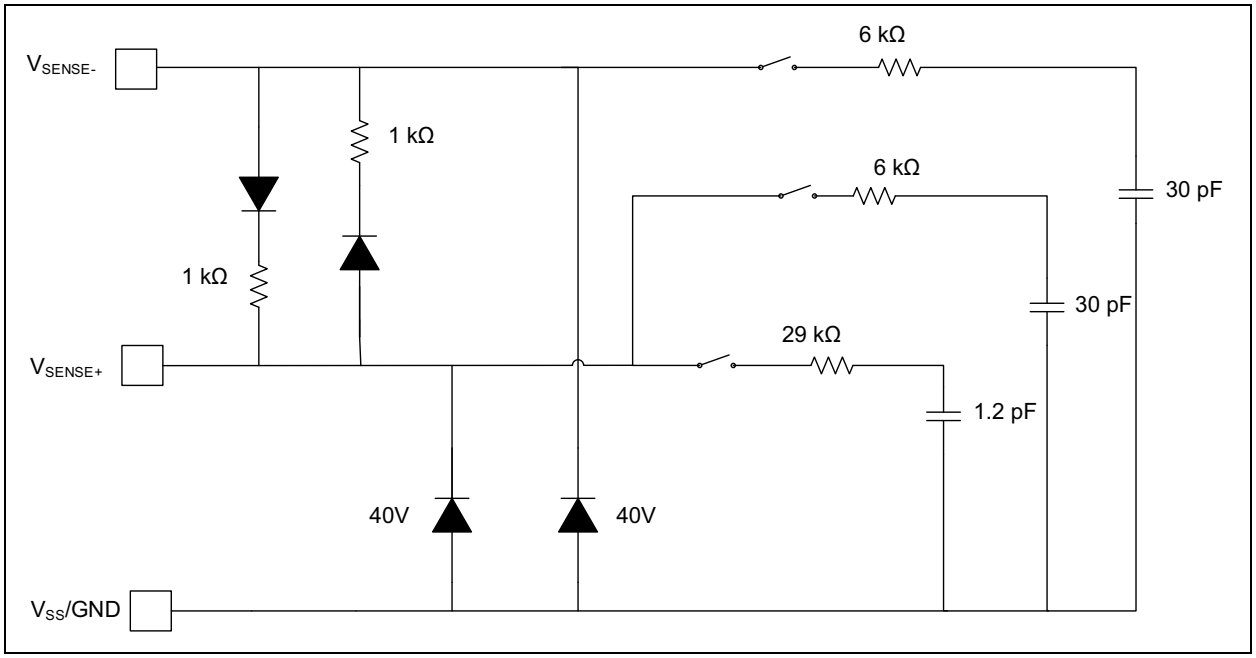


FIGURE 2-31: *Equivalent Input Circuits for PAC193X Devices.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in **Table 3-1**.

TABLE 3-1: PIN DESCRIPTIONS

QFN	WLCSP16	Symbol	Pin Type	Description
1	C3	SLOW/$\overline{\text{ALERT}}$	Digital I/O pin	Voltage range is set by V_{DD} I/O pin. Default function is SLOW, may be programmed to function as $\overline{\text{ALERT}}$ pin (Open Collector when functioning as $\overline{\text{ALERT}}$, requires pull-up resistor to V_{DD} I/O).
2	A4	V_{DD}	Power for IC	Positive power supply voltage.
3	B4	GND	Ground pin	Ground for the IC.
4	C4	SM_CLK	SMBus clock input	Clock Input pin.
5	D4	SM_DATA	SMBus data I/O	Open drain requires pull-up resistor to V_{DD} I/O.
6	C2	ADDRSEL	Analog I/O pin	Address selection for the SMBus Slave address.
7	C1	SENSE3-(1)	32V analog pin	0-32V range, connect to load side of sense resistor.
8	D1	SENSE3+(1)	32V analog pin	0-32V range, connect to supply side of sense resistor.
9	D2	SENSE4-(1)	32V analog pin	0-32V range, connect to load side of sense resistor.
10	D3	SENSE4+(1)	32V analog pin	0-32V range, connect to supply side of sense resistor.
11	A3	SENSE1+	32V analog pin	0-32V range, connect to supply side of sense resistor.
12	A2	SENSE1-	32V analog pin	0-32V range, connect to load side of sense resistor.
13	A1	SENSE2+	32V analog pin	0-32V range, connect to supply side of sense resistor.
14	B1	SENSE2-	32V analog pin	0-32V range, connect to load side of sense resistor.
15	B2	V_{DD} I/O	Sets V_{IH} reference for digital I/O	Digital power reference level for digital I/O.
16	B3	$\overline{\text{PWRDN}}$	Digital input pin	Voltage range is set by V_{DD} I/O pin. Active low puts the device in power-down state (all circuitry is powered down including SMBus).
17	—	EP	N/C	The Exposed pad is not electrically connected.

Note 1: For PAC1932, pins 7,8,9,10 are not connected inside and should be grounded.
For PAC1933, pins 9 and 10 are not connected inside and should be grounded.

3.1 SenseN+/SenseN– (N=1,2,3,4)

These two pins form the differential input for measuring voltage across a sense resistor in the application. The positive input (SenseN+) also acts as the input pin for bus voltage.

3.2 Ground (GND)

System ground.

3.3 SMBus Data (SM_DATA)

This is the bi-directional SMBus data pin. This pin is open drain, and requires a pull-up resistor to V_{DD} I/O.

3.4 SMBus Clock (SM_CLK)

This is the SMBus clock input pin.

3.5 Positive Power Supply Voltage (V_{DD})

Power supply input pin for the device. 2.7-5.5V range, bypass with 100 nF ceramic capacitor to ground near the IC.

3.6 Digital Power Reference Voltage ($V_{DD\ I/O}$)

Connect this pin to the power supply voltage for the digital controller driving the SMBus pins and digital input pins for the device, 1.62V-5.5V. Bypass with 100 nF ceramic capacitor to ground near the IC. This pin does not supply power, instead it acts as the V_{IH} reference.

3.7 Address Selection (ADDR_SEL)

Connect a resistor from this pin to ground to select SMBus address.

3.8 Enable Pin ($\overline{\text{PWRDN}}$)

Power down input pin for the device, active low.

3.9 SLOW/$\overline{\text{ALERT}}$

In default mode, if this pin is forced high, sampling rate is forced to eight samples/second. When it is forced low, the sampling rate is 1024 samples/second unless a different sample rate has been programmed.This pin may be programmed to act as the $\overline{\text{ALERT}}$ pin, in $\overline{\text{ALERT}}$ mode the pin needs a pull-up resistor to V_{DD} I/O.

3.10 Exposed Thermal Pad Pin (EP)

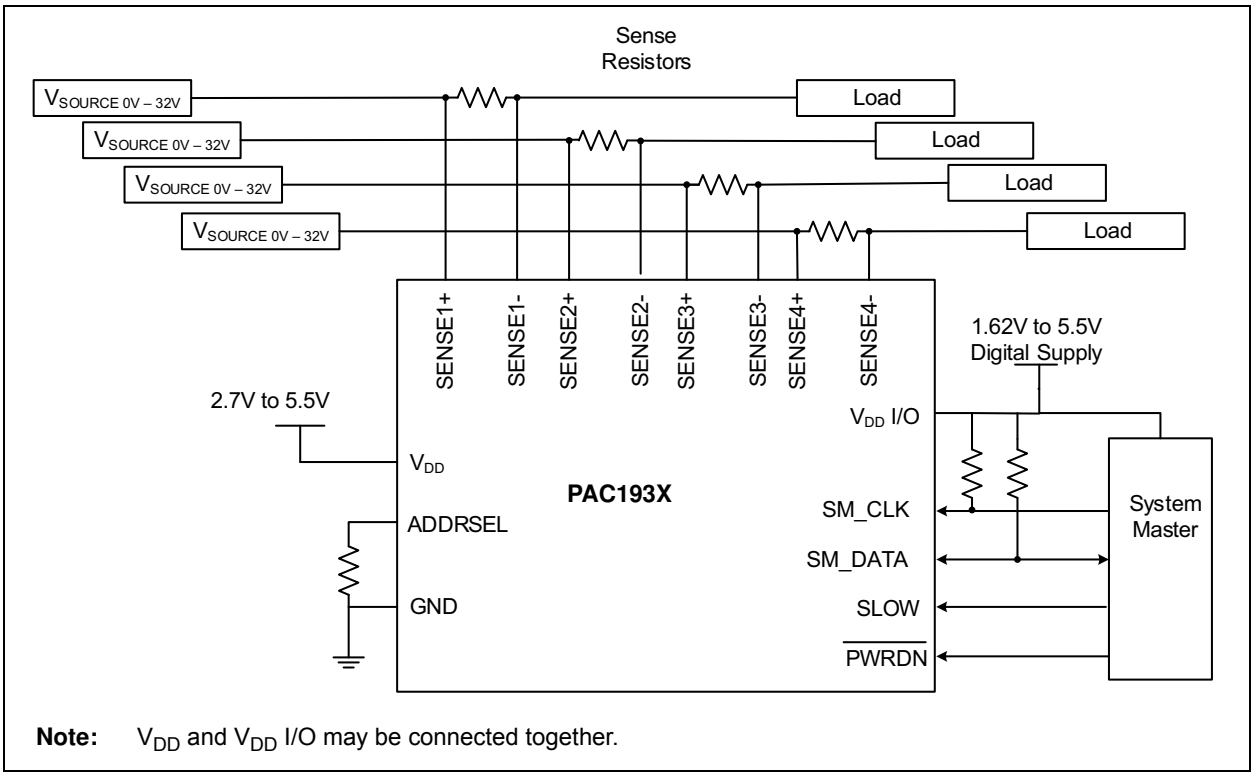
The Exposed pad is not electrically connected. It is recommended that you connect it to ground.

4.0 GENERAL DESCRIPTION

The PAC1934 is a four-channel, bidirectional, high-side current-sensing device with precision voltage measurement capabilities, DSP for power calculation and a power accumulator. PAC1932 and PAC1933 are two and three channel versions of the PAC1934. These devices measure the voltage developed across an external sense resistor (V_{SENSE}) to represent the high-side current of a battery or voltage regulator. The PAC1932/3/4 also measures the SENSE+ pin voltages (V_{BUS}). Both V_{BUS} and V_{SENSE} are converted to digital results by a 16-bit ADC, and the digital results are multiplied to give V_{POWER}. The V_{POWER} results are accumulated on-chip, which enables energy measurement over the accumulation period.

The PAC1932/3/4 has an I^2C/SMBus interface for digital control and reading results. It also has digital supply reference V_{DD} I/O that is to be connected to the same supply as the digital master for the I^2C/SMBUS, enabling digital I/O voltages as low as 1.62V.

A system diagram is shown in **Figure 4-1**.



Note: V_{DD} and V_{DD} I/O may be connected together.

FIGURE 4-1: *PAC1932/3/4 System Diagram.*

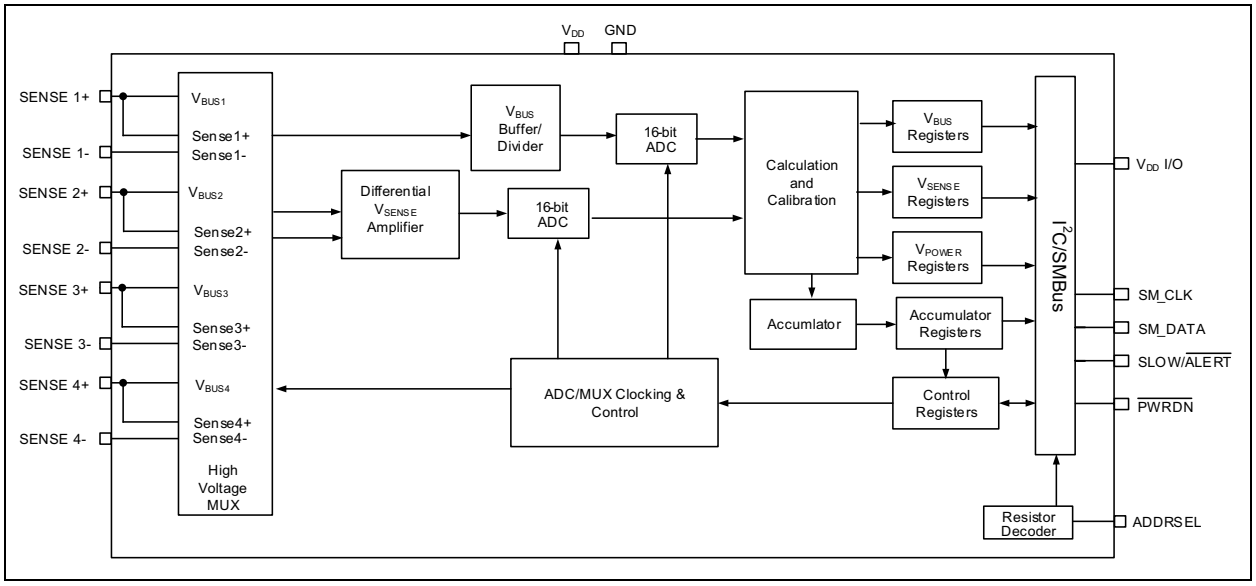


FIGURE 4-2: *PAC1932/3/4 Functional Block Diagram.*

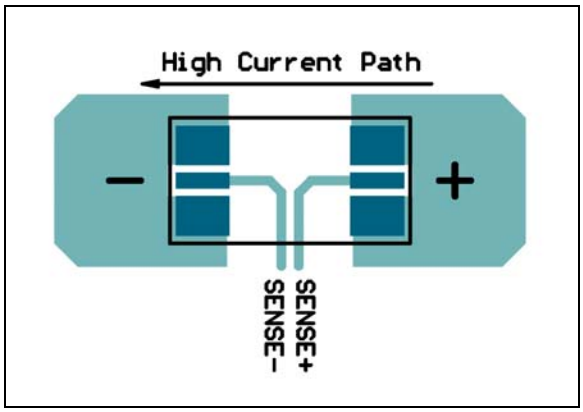


FIGURE 4-3: *PCB Pattern for Sense Resistor.*

Figure 4-3 shows the recommended PCB pattern for sense resistor with wide metal for the high-current path. The drawing shows metal, solder paste openings and resistor outline. V_{SOURCE} connects to the +terminal of the high-current path, and the load connects to the -terminal of the high-current path. Sense+ and Sense- have a Kelvin connection to the current sense resistor to ensure that no metal with high current is included in the V_{SENSE} measurement path. Sense+ and Sense- are shown as a differential pair, route them as a differential pair to the Sense inputs at the chip.

4.1 Detailed Description

A high-voltage multiplexer connects the input pins to the V_{BUS} and V_{SENSE} amplifiers. The amplifier outputs are sampled simultaneously for each channel, converted by 16 bit ADCs and processed for gain and offset error correction. After each conversion, V_{BUS} and V_{SENSE} are multiplied together to give V_{POWER}.

An internal oscillator and digital control signals control the two ADCs and the mux. The mux sequentially connects each channel's amplifiers to the ADC inputs.

The PAC1932/3/4 measures the source-side voltage, V_{BUS}, and the voltage V_{SENSE} across an external current sense resistor, R_{SENSE}.

4.1.1 INITIAL OPERATION AND ACTIVE STATE

After POR and a start-up sequence, the device is in the Active state and begins sampling the inputs sequentially. Voltage and current are sampled for all active channels and power is calculated and accumulated. All active channels are sampled at 1024 samples/second by default. Sample rates of 256, 64 or eight samples/second may be programmed over I^2C or SMBus. If the SLOW pin is asserted the sample rate is eight samples per second. For sampling rates lower than 1024 samples/second, the device is in Sleep mode for a portion of the conversion cycle, which results in lower power dissipation. If fewer than four channels are active, power is also reduced.

To read accumulator data and reset the accumulators, the REFRESH command is used. To read the voltage, current, power and accumulator data without resetting the accumulators, the REFRESH_V command is used. Changes to the Control register (01h) are activated by sending either REFRESH or REFRESH_V. When a new value is written to the Control register (01h), the new values take effect at the end of the next round-robin sampling cycle following the next REFRESH or REFRESH_V command.

4.1.2 REFRESH COMMAND

The master sends the REFRESH command after changing the Control register and/or before reading accumulator data from the device. The master controls the accumulation period in this manner.

The readable registers for the V_{BUS}, V_{SENSE}, Power, accumulator outputs and accumulator count are updated by the REFRESH command and the values will be static until the next REFRESH command. These readable registers will be stable within 1 mS from sending the REFRESH command, and may be read by the master at any time up until the next REFRESH command is sent. The internal accumulator values and accumulator count will be reset by the REFRESH command, but the sampling of the inputs, data conversion and power integration is not interrupted and will continue as determined by the settings in the Control register.

Changes written to the control and configuration registers take effect 1 mS after a REFRESH command is sent. Any new commands written within this 1 mS window will be ignored and NACKed to indicate that they are ignored.

The values for V_{BUS} and V_{SENSE} measurement results and Power calculation results respond to the REFRESH command in the same fashion as the accumulators and accumulator count. The readable registers will be stable within 1 mS from sending the REFRESH command and may be read by the master at any time. The internal values continue to be updated according to the sampling plan determined by the settings in the Control register. The results that are sent to the readable registers for V_{BUS}, V_{SENSE} and Power are the values from the most recent complete conversion cycle. See **Register 6-1** REFRESH Command (Address 00h).

4.1.3 REFRESH_G COMMAND

The REFRESH_G is identical in every respect to the REFRESH command, but it is used with the I^2C General Call address (0000 000). This allows the system to issue a REFRESH command to all of the PAC1932/3/4 devices in the system with a single command. Then the data from this REFRESH_G command may be read device-by-device to capture a snapshot of the system power and energy for all devices. See **Register 6-12** REFRESH_G Command (Address 1Eh). Note that the REFRESH_G command can also be used with a valid Slave address but in this case only the device with this Slave address will receive the command. In other words it has the same properties as the REFRESH command with the possibility of being compatible with the I^2C General Call address.

4.1.4 REFRESH_V COMMAND

If the user wants to read V_{SENSE} and V_{BUS} results, the most recent Power calculation, and/or the accumulator values and count without resetting the accumulators, the REFRESH_V command may be sent. Sending the REFRESH_V command and waiting 1 mS ensures that the V_{SENSE}, V_{BUS}, Power, accumulator and accumulator count values will be stable when read by the master. The sampling of the inputs, data conversion and power integration are not interrupted and will continue as determined by the settings in the Control register. The data in these readable registers will remain stable until the next REFRESH or REFRESH_V command. The internal accumulator values and accumulator count are unaffected by the REFRESH_V command.

Note that the REFRESH_V command may also be used to activate changes to the Control register, just like the REFRESH command, except with the REFRESH_V command changes to the Control register will be enacted without resetting the accumulators or accumulator count. See **Register 6-13** REFRESH_V Command (Address 1Fh).

4.1.5 SLEEP STATE

The SLEEP state is a lower power state than the Active state. While in this state, the device will draw a supply current of I_{SLEEP} from the V_{DD} pin. The device automatically goes to this state between conversion cycles when sampling rates lower than 1,024 samples/second are selected, or if fewer than four channels are active. All digital states and data are retained in the SLEEP state. The device can also be put in the Sleep state by setting the SLEEP bit followed by a REFRESH or REFRESH_V command, and sampling will resume when the SLEEP bit is cleared followed by a REFRESH of REFRESH_V command. The device does not go into SLEEP state based on any other condition such as static conditions on the SMBus pins. If SMBus Timeout is enabled, it is supported in SLEEP mode or ACTIVE mode.

4.1.6 POWER-DOWN STATE

The Power-Down state is entered by pulling the $\overline{\text{PWRDN}}$ pin low. In this state, all circuits on the chip including the SMBus pins are inactive, and the device is in a state of minimum power dissipation.

In the Power-Down state, no data is retained in the chip (neither register configuration nor measurement data). When the $\overline{\text{PWRDN}}$ pin is pulled high, integration, measurement and accumulation will begin using the default register settings, as described in **Section 4.1.1 "Initial Operation and Active State"**. The first measurement data may be requested by a REFRESH or REFRESH_V command 20 ms after the $\overline{\text{PWRDN}}$ pin is pulled high.

4.1.7 PROGRAMMING THE SAMPLE RATE AND THE SLOW PIN

The default sampling rate after power-up is 1024 samples/second. Sampling rates of 256, 64 or 8 samples/second may be programmed in the **Register 6-2** CTRL Register (Address 01h). Any time a new sample rate is programmed, it does not take effect until a REFRESH, REFRESH_G, or REFRESH_V command is received. When any of these REFRESH commands are received, any round-robin sampling cycle in progress will complete before the new sampling rate takes effect. For example, if the user is sampling at 8 SPS and program a new sample rate, it may take up to 125 mS for the new sample rate to take effect and for all the sample rate related registers (like CTRL_ACT) to show their updated values.

If one of these lower sample rates is used, power dissipation is reduced. The round-robin sampling and conversion cycle is exactly the same, but the device goes into the sleep state between conversion cycles. See **Section 2.0 "Typical Operating Curves"**.

If the SLOW pin is pulled high, the device will sample at eight samples/second. No matter what the programmed sample rate, this new SLOW sample rate will take effect on the next conversion cycle (if a round-robin conversion cycle is in process when the SLOW pin goes high, that conversion cycle will complete before the SLOW sample rate takes effect.)

If the device is programmed for Single Shot mode, and the SLOW pin is asserted, the first sampling will begin within 125 ms after the SLOW pin is asserted.

If the device is in the Sleep state, asserting the SLOW pin will not cause sampling to start.

Whenever the SLOW pin changes state, a limited REFRESH or REFRESH_V command may be executed by the chip hardware (default is REFRESH). Like any other REFRESH command, this resets the accumulators and accumulator count for a REFRESH command, and updates the readable registers for either REFRESH or REFRESH_V. These are limited REFRESH commands because no programmed changes to the Control or Status registers take effect (Control and Status registers means registers 01h, 1Ch, 1Dh, and 20h-26h). The readable registers are stable with the new values within 1 ms of the SLOW pin transition.

The Slow register enables selection of REFRESH or REFRESH_V on the SLOW pin transitions, which allows this function to be disabled for either edge, and also tracks both the state of the SLOW pin and transitions on the SLOW pin. See **Register 6-14**, SLOW (Address 20h).

This is the default functionality of the SLOW pin, but it may be reconfigured to function as an $\overline{\text{ALERT}}$ pin (see paragraph **Section 4.4 "Alert Functionality"**). If the SLOW pin is configured to serve as an $\overline{\text{ALERT}}$ pin, the slower sampling rate of eight samples/second is only available by programming the Control register 01h.

4.2 Conversion Cycles

A conversion cycle for the device consists of analog-to-digital conversion being complete for all channels (including the real-time calibration that is part of each conversion cycle). Immediately following the data conversion, the power results are calculated for that channel and the power value is added to the accumulator. Averaged values for V_{SENSE} and V_{BUS} are also updated internally as part of each conversion cycle.

Data conversion and processing is performed for each active channel in sequential fashion until all active channels have been converted, completing the conversion cycle for the device. The sequential sampling of each channel, along with the calculation time and any sleep time needed to set the overall sampling rate, is referred to as a round-robin sampling period.

4.3 Conversion Cycle Controls

4.3.1 REDUCING THE NUMBER OF CHANNELS TO BE SAMPLED

Program **Register 6-10** CHANNEL_DIS and SMBus (Address 1Ch) to reduce the number of channels that are active. The sample rate is unaffected, but power dissipation is reduced very slightly if some channels are disabled. Any or all channels may be disabled; if all channels are disabled, the device goes into Sleep mode. When a channel is disabled due to register programming in the PAC1934 or due to factory programming on the PAC1932 and PAC1933, the auto incrementing pointer will skip these channels by default (see **Section 5.5 "Auto-Incrementing Pointer"**).

4.3.2 SINGLE SHOT MODE

The Control register also allows the device to operate in Single Shot mode. In Single Shot mode, all active channels will sample and convert once, followed by results being calculated. The accumulator and accumulator count operate the same as for continuous conversion mode, accumulating each single shot power calculation and incrementing the accumulator count. The conversion cycle will start when the REFRESH command (or REFRESH_V or REFRESH_G) is sent.

After the single shot measurements and calculations are complete, the device will go into Sleep mode. A REFRESH, REFRESH_G or REFRESH_V command may be sent to read the data. The user needs to wait 3 ms after the REFRESH command before commanding another Single Shot conversion by means of sending one of the REFRESH commands. This is because a 1 ms delay is required between REFRESH commands, and coming out of Sleep requires 2 ms.

4.4 Alert Functionality

The Alert functionality can serve two purposes: to notify the system that a conversion cycle for all active channels is complete, or to notify the system that the accumulator or accumulator count has overflowed.

4.4.1 USING THE ALERT FUNCTION

To use the ALERT function, configure the SLOW pin to function as ALERT using **Register 6-2** CTRL Register (Address 01h). For this configuration, the ALERT pin must have a pull-up to V_{DD} I/O (it will function as an open drain output). If a pull-up resistor is attached to the pin for Alert functionality, the device will power up in Slow mode. Any of the four sample rates can be programmed using **Register 6-2** CTRL Register (Address 01h).

The Alert function for Accumulator Overflow can also be used without reconfiguring the SLOW pin, by monitoring the OVF bit in **Register 6-2** CTRL Register (Address 01h).

4.4.2 ALERT AFTER COMPLETE CONVERSION

Register 6-2 has an ALERT_CC bit that can be used to enable the ALERT_CC function. If this bit is set, the ALERT pin will go low for 5 µS after each complete conversion cycle is complete.

4.4.3 ALERT ON ACCUMULATOR OVERFLOW

If the ALERT function is enabled, and any of the accumulators or the accumulator count overflows, the ALERT pin may be used to notify the system. To enable this trigger for the ALERT pin, bit 1 in the **Register 6-2** CTRL Register (Address 01h) must be set. Note that the OVF bit in the **Register 6-2** CTRL Register (Address 01h) will be set when these overflows occur.

4.4.4 CLEARING ALERT AND OVF

When the Alert function has been tripped by accumulator or accumulator count overflow, it will remain asserted until a REFRESH command is received. REFRESH_G will also clear the OVF bit and the Alert function, but REFRESH_V will not.

4.5 Voltage Measurement

The V_{BUS} voltage for each channel is measured by the SENSE+ pin for each channel. A high-voltage multiplexer is connected to each SENSE+ pin, and the multiplexer sequentially connects each SENSE+ input to and ADC for conversion. The result is stored in a 16-bit V_{BUS} results register and the 14 MSBs are multiplied by the V_{SENSE} number for the V_{POWER} results value. The V_{POWER} results are accumulated in the accumulator.

Full-Scale Voltage (FSV) is 32V by default. The device may be programmed for bipolar V_{BUS} measurements. in this bipolar mode, the mathematical range for negative V_{BUS} numbers is -32V, the actual range is limited to about -200mV due to physical factors. This bipolar capability for V_{BUS} enables accurate offset measurement and correction. For bipolar operation, the 16-bit V_{BUS} result is a two's complement (signed) number.

The measured voltage at SENSE+ can be calculated using **Equation 4-1**.

EQUATION 4-1: BUS VOLTAGE

$$V_{Source} = 32V \times \frac{V_{BUS}}{Denominator}$$

Where:

V_{SOURCE}	=	The measured voltage on the SENSE+ pin
V_{BUS}	=	The value read from the V_{BUS} results registers
Denominator	=	2^{16} for unipolar measurements
	=	2^{15} for bipolar measurements

4.6 Current Measurement

The PAC1932/3/4 device family includes high-side current sensing circuits. These circuits measure the voltage (V_{SENSE}) induced across a fixed external current sense resistor (R_{SENSE}) and store the voltage as a 16-bit number in the V_{SENSE} Results registers.

The PAC1932/3/4 current sensing operates with a Full-Scale Range (FSR) of 100 mV in unidirectional mode (default).

When sensing unidirectional currents (the default mode), the ADC results are presented in straight binary format. For bidirectional current sensing, the ADC results are in two's complement (signed) format. For bipolar current measurements, the range is ±100 mV, but use FSR = 100 mV in the equations that follow. For best accuracy on current values near zero, it is recommended to use the bidirectional current mode and 8x average current results.

4.7 Selecting R_{SENSE} Values

R_{SENSE} can easily be calculated if you know the maximum current you want to sense, as shown in **Equation 4-2**.

Consider that you may need to select a value for IMax that includes current peaks well beyond your nominal current.

EQUATION 4-2: CALCULATING R_{SENSE}

$$Rsense = \frac{FSR}{IMax}$$

Where:

FSR	=	Full Scale V_{SENSE} voltage input
R_{SENSE}	=	External R_{SENSE} resistor value
IMax	=	Maximum current to measure

Full-Scale Current (FSC) can be calculated from **Equation 4-3**.

EQUATION 4-3: FULL-SCALE CURRENT

$$FSC = \frac{100\ mV}{R_{SENSE}}$$

Where:

FSC	=	Full-scale current
R_{SENSE}	=	External sense resistor value

The actual current through R_{SENSE} can then be calculated using **Equation 4-4**.

EQUATION 4-4: SENSE CURRENT

$$I_{SENSE} = FSC \times \frac{V_{SENSE}}{Denominator}$$

Where:

I_{SENSE}	=	Actual bus current
FSC	=	Full-scale current value (from **Equation 4-3**)
V_{SENSE}	=	The value read from the V_{SENSE} results registers
Denominator	=	2^{16} for unipolar measurements
	=	2^{15} for bipolar measurements

4.8 ADC Measurements, Offset, and 8x Averaging

The PAC1932/3/4 is primarily desired for energy measurements where many power readings are accumulated. This is inherently an averaging process. Individual voltage and current measurements can also benefit from averaging to reduce noise and offset. Averaged values are internally calculated for V_{BUS} and V_{SENSE}, with a rolling average of the most recent eight values present in the VBUSn_AVG (**Register 6-7**) and VSENSEn_AVG (**Register 6-6**) registers. The average is updated internally after every conversion cycle. The readable registers are updated with REFRESH, REFRESH_V, or REFRESH_G commands like all the other readable results registers. These averaged results may be used for the most accurate, lowest noise and lowest offset measurements.

The ADC channels use a special offset canceling technique. If the user observes the unaveraged results for near-zero values of V_{BUS} and V_{SENSE}, they may observe a cyclical pattern of offset variation. The user may think this is noise, but in fact it is due to internal circuitry switching through different permutations of offset cancellation circuitry. This small variation in unaveraged offset is canceled in the 8x averaged result. It is also canceled in the Power Accumulator results. The overall effect is offset that is consistently very close to zero LSB over supply and temperature variations.

The offset canceling technique is illustrated in **Figure 4-4**. It is very difficult to accurately observe, as it is a challenge to read the data from every conversion cycle. The effect of capturing data points at a rate that does not correspond exactly to the internal sampling rate of the PAC1932/3/4 can make these permutations appear less periodic and deterministic than they are inside the chip. The data conversion uses one of the permute positions 1-4 for each input on each conversion, cycling through all four permutations in four conversions. When averaged the Permute Enabled result shown below is realized, evenly distributed around zero.

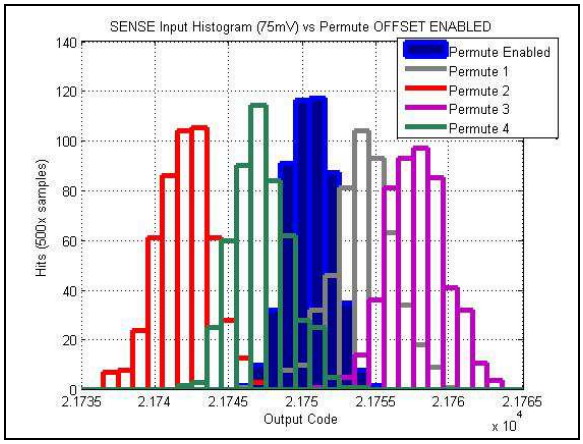


FIGURE 4-4: *Illustration of the Four Permute Combinations that the ADC Cycles through and the Resulting Low Average Offset. Each Bin Represents One Code.*

Results from both the V_{BUS} and V_{SENSE} ADCs are 17b two's complement (signed) internally. There is an additional bit of resolution that is not accessible from the results register. The NEG_PWR (Address 1Dh) register determines whether the conversion results are reported in the readable registers as unipolar or bipolar numbers. Using bipolar numbers can give more accurate results for very small numbers that may actually be negative for some readings, in addition to measuring bidirectional currents (charging/discharging) and voltages that can dip below ground.

Averaged values are also calculated for V_{BUS} and V_{SENSE}. A rolling average of the most recent eight values is present in the VBUSn_AVG (**Register 6-7**) and VSENSEn_AVG (**Register 6-6**) registers. These registers require eight conversion cycles after POR before they represent an accurate value, they are updated after every conversion cycle. The readable registers are updated with REFRESH, REFRESH_V or REFRESH_G commands like all the other readable results registers.

4.9 Power and Energy

The Full-Scale Range for Power depends on the external sense resistor used, as shown in Equation 4-5.

EQUATION 4-5: POWER FSR CALCULATION

$$PowerFSR = (100\ mV/R_{SENSE}\Omega) \times 32V$$
$$= 3.2V^2/R_{SENSE}\Omega$$

Where:

$R_{SENSE}\Omega$ = External R_{SENSE} resistor value
100 mV = Full-Scale V_{SENSE} voltage input
32V = Full-Scale V_{BUS} voltage input

The device implements Power measurements by multiplying V_{BUS} and the V_{SENSE} to give a result V_{POWER}. V_{POWER} values are used to calculate Proportional Power as shown in Equation 4-6. The Proportional Power is the fractional portion of Power FSR measured in one sample. Bipolar mode is where V_{BUS} is bipolar mode, V_{BUS} is bidirectional mode, or both V_{BUS} and V_{SENSE} are bipolar/bidirectional.

EQUATION 4-6: PROPORTIONAL POWER CALCULATION

$$P_{PROP} = \frac{Vpower}{Denominator}$$

Where:

Denominator = 2^{28} (unipolar mode)
= 2^{27} (bipolar mode)

To calculate the actual power from the Proportional Power, multiply by the Power FSR as shown in Equation 4-7. This Actual Power number is the power measured in one sample.

EQUATION 4-7: POWER CALCULATION

$$P_{actual} = PowerFSR \times P_{PROP}$$

These V_{POWER} results are digitally accumulated on chip, and stored in the VACCUM registers.

The energy calculation Equations 4-8 and 4-9 use a different denominator term depending on unipolar or bipolar mode. Bipolar mode for energy applies when bipolar/bidirectional mode is used for V_{BUS} and/or V_{SENSE}. Equation 4-8 shows how to realize this using the Accumulator results, Accumulator count and the accumulation period, T. In this equation, T must be known from a system clock time stamp or other accurate indicator of the total accumulation period.

EQUATION 4-8: ENERGY CALCULATION

$$Energy = \frac{V(accum)}{Denominator} \times (PwrFSR) \times \frac{T}{AccCount}$$

Where:

Denominator = 2^{28} (unipolar mode)
= 2^{27} (bipolar mode)

EQUATION 4-9: ENERGY CALCULATION

$$Energy = \frac{V(accum)}{Denominator} \times \frac{(PwrFSR)}{f_S}$$

Where:

Denominator = 2^{28} (unipolar mode)
= 2^{27} (bipolar mode)

Equation 4-9 shows how to calculate energy using the accumulated power and the sampling rate, f_S.

4.9.1 ADDITIONAL ACCUMULATOR INFORMATION

The math for the Power calculation and accumulation inside the chip is always done in two's complement math, no matter what the user sets the output registers to show. V_{BUS} and V_{SENSE} are 17-bit two's complement (signed) numbers internally. V_{POWER} is the product of V_{SENSE} multiplied by the 14 MSBs of V_{BUS}, and this is a 31 bit two's complement result (signed) internally. In some cases this results in a Power result that is not identical to the product of the V_{BUS} results register multiplied by the V_{SENSE} register. However, the Power result from the Power results register is more accurate than the product of the V_{BUS} register multiplied by the V_{SENSE} register in these cases, as explained below.

If V_{SENSE} and V_{BUS} are both programmed to be unsigned (unipolar) in register NEG_PWR (Address 1Dh), 16b without sign are exported to V_{BUS} and V_{SENSE} results registers.

If V_{BUS} is programmed to be signed (bipolar) in **Register 6-11** NEG_PWR (Address 1Dh), the corresponding data is truncated to 16-bit two's complement (signed) for the readable results register.

If V_{SENSE} is programmed to be signed (bipolar) in register NEG_PWR (Address 1Dh), the corresponding results register value is truncated to 16-bit two's complement (signed), but the power calculation uses 17-bit two's complement (signed). Therefore, a mismatch is possible between an externally calculated power value (V_{BUS} times V_{SENSE}) and the actual power value calculated internally to the chip. The internally calculated (and accumulated) value is more accurate than the externally calculated value in every case.

The continuous power integration periods (also called the energy accumulation period) can range from ~1ms to many hours, depending on the number of samples per second selected via SMBus. The number of samples is limited by the size of the Accumulator Count register to 16,777,216 (2^{24}). This count corresponds to about 273 minutes at 1024 samples/second, or 582 hours at eight samples/second. This Accumulator Count can overflow, and it will not reset when it overflows.

When the accumulation registers reach their maximum value, this is called accumulator overflow. The accumulator outputs remain at their maximum value; they do not roll over. The user can calculate the worst-case time to roll over and read them at or before that time or use the built in Alert functions to detect rollover and read them at that time.

Worst-case accumulator overflow time can be calculated assuming that every measurement that is accumulated is a full-scale number. Since the power numbers are 28 bits, and the accumulator is 48 bits, 2^{20} samples can be accumulated before overflow if they are all full-scale values. For most applications, they will not all be full-scale numbers; this is especially true if V_{BUS} is not 32V. If V_{BUS} is a lower number, the maximum number of full-scale samples that can be accumulated is scaled by $32V/V_{BUS}$. This limitation can limit the accumulation period before overflow to 17 minutes at 1024 samples/second, or 36 hours at eight samples/second, if most values are near full-scale. The Accumulator Count limit described above will still limit the total number of samples to 2^{24}.