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PAC5210

Power Application Controller ™

Multi-Mode Power Manager™

Configurable Analog Front End™

Application Specific Power Drivers™

ARM® Cortex™-M0 Controller Core

active-semi®
Solutions for Sustainability

www.active-semi.com

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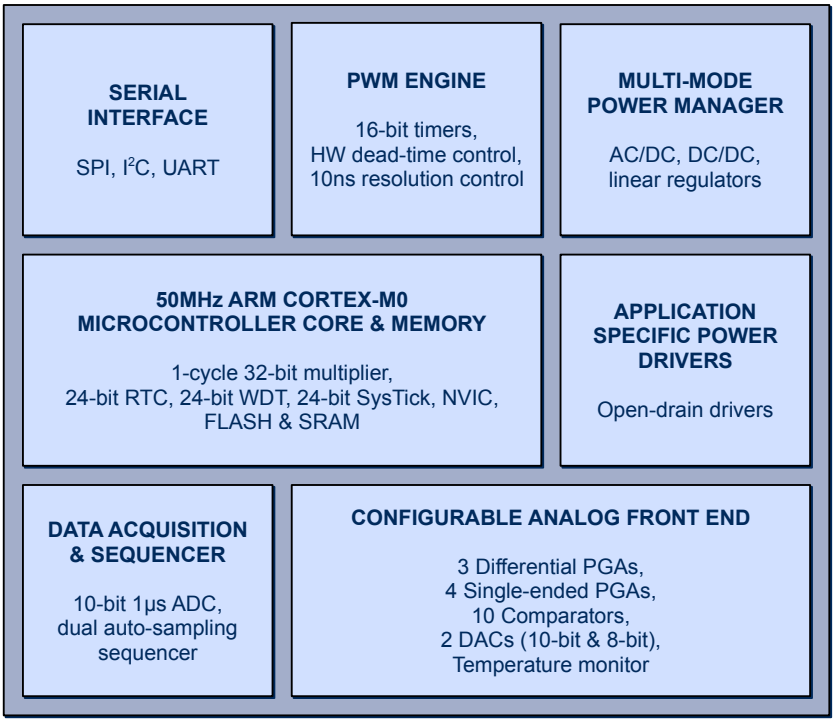
1. GENERAL DESCRIPTION

The PAC5210 belongs to Active-Semi's broad portfolio of full-featured Power Application Controller™ (PAC) products that are highly optimized for controlling and powering next generation smart energy appliances, devices, and equipment. These application controllers integrate a 50MHz ARM® Cortex™-M0 32-bit microcontroller core with Active-Semi's proprietary and patent-pending Multi-Mode Power Manager™, Configurable Analog Front End™, and Application Specific Power Drivers™ to form the most compact microcontroller-based power and general purpose application systems ranging from digital power supply to motor control. The PAC5210 microcontroller features up to 32kB of embedded FLASH and 8kB of SRAM memory, a high-speed 10-bit 1µs analog-to-digital converter (ADC) with dual auto-sampling sequencers, 5V/3.3V I/Os, flexible clock sources, timers, a versatile 14-channel PWM engine, and several serial interfaces.

The Multi-Mode Power Manager (MMPM) provides “all-in-one” efficient power management solution for multiple types of power sources. It features a configurable multi-mode switching supply controller capable of operating in buck, flyback, or boost mode, and up to four linear regulated voltage supplies. The Application Specific Power Drivers (ASPD) is medium voltage level open drain driver for general purpose driving. The Configurable Analog Front End (CAFE) comprises differential programmable gain amplifiers, single-ended programmable gain amplifiers, comparators, digital-to-analog converters, and I/Os for programmable and inter-connectible signal sampling, feedback amplification, and sensor monitoring of multiple analog input signals. Together, these modules and microcontroller enable a wide range of compact applications with highly integrated power management, driving, feedback, and control for DC supply up to 52V and for line AC supply.

Figure 1-1. Power Application Controller

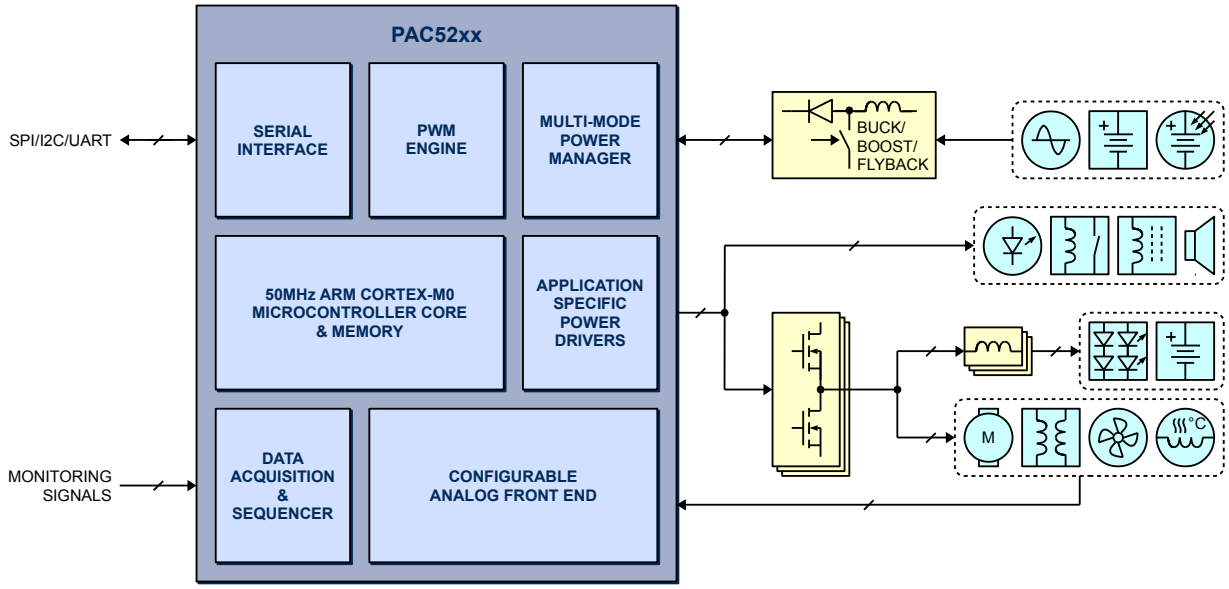


The PAC5210 is available in a 56-pin 8x8 TQFN package. The PAC family includes a range of part numbers optimized to work with different targeted primary applications.

2. PAC FAMILY APPLICATIONS

- General purpose high-voltage system controllers
- Home appliances
- Power tools
- Motor controllers
- LED lighting controllers
- Uninterruptible power supply (UPS)
- Solar micro-inverters
- Wireless power controllers
- Digital power controllers
- Industrial applications

Figure 2-1. Simplified Application Diagram



3. PRODUCT SELECTION SUMMARY

Table 3-1. Product Selection Summary

PART NUMBER	PIN PKG	POWER MANAGER		CONFIGURABLE ANALOG FRONT END					APPLICATION SPECIFIC POWER DRIVERS			MICROCONTROLLER						PRIMARY APPLICATION
		INPUT VOLTAGE	MULTI-MODE SW	DIFF-PGA	PGA	COMPARATOR	DAC	ADC CHANNEL	POWER DRIVER	PWM CHANNEL	FAULT PROTECT	SPEED (MHz)	FLASH (kB)	SRAM (kB)	GPIO	INTERFACE	XTAL	
PAC5210	56-pin 8x8 TQFN	5.2-52V	Y	3	4	10	2	11	3 OD (23V/40mA)	14	Int + 2 Ext	50	32	8	37	SPI I^2C UART SWD	Y	IPM control or general purpose control

Notes: DIFF-PGA = differential programmable gain amplifier, GD = gate driver, HS = high-side , LS = low-side, OD = open-drain driver, PGA = programmable gain amplifier, UHV = ultra-high-voltage.

4. ORDERING INFORMATION

Table 4-1. Ordering Information

PART NUMBER[1]	TEMPERATURE RANGE	PACKAGE	PINS	PACKING
PAC5210QS	-40°C to 105°C	TQFN88-56	56 + Exposed Pad	Tray

[1] For the latest packaging and ordering information please see http://www.active-semi.com/ or contact us under sales@active-semi.com .

5. PAC5210 FEATURES

- Proprietary Multi-Mode Power Manager
  - Multi-mode switching supply controller configurable as high-voltage or ultra-high-voltage buck, AC/DC or flyback
  - DC supply up to 52V or line AC input
  - 4 linear regulators with power and hibernate management
  - Power and temperature monitor, warning, and fault detection
- Proprietary Configurable Analog Front End
  - 10 analog front end I/O pins
  - 3 differential programmable gain amplifiers
  - 4 single-ended programmable gain amplifiers
  - 10 comparators
  - 2 DACs (10-bit and 8-bit)
- Proprietary Application Specific Power Drivers
  - 3 open-drain drivers
  - Configurable delays and fast fault protection
- 50MHz ARM Cortex-M0 32-bit microcontroller core
  - Fast single cycle 32-bit x 32-bit multiplier
  - 24-bit SysTick timer
  - Nested vectored interrupt controller (NVIC) with 20 external interrupts
  - Wake-up interrupt controller allowing power-saving sleep modes
  - Clock-gating allowing low power operation
- 32kB FLASH and 8kB SRAM memory
- 10-bit 1µs ADC with multi-input/multi-sample control engine
  - 11 ADC inputs including input from configurable analog front end
- 3.3V I/Os
  - 4 general purpose I/O with tri-state and dedicated analog input to ADC
- True 5V I/Os
  - 23 general purpose I/Os with tri-state, pull-up and pull-down and dedicated I/O supply
  - Configurable between true 5V and 3.3V I/Os
- Flexible clock and PLL from internal 2% oscillator, ring oscillator, external clock, or crystal
- 9 timing generators
  - Four 16-bit timers with up to 16 PWM/CC blocks and 7 independent dead-time controllers
  - 24-bit watchdog timer
  - 4s or 8s watchdog timer
  - 24-bit real time clock
  - 24-bit SysTick timer
  - Wake-up timer for sleep modes from 0.125s to 8s
- SPI, I^2C, and UART communication interfaces
- SWD debug interface with interface disable function

6. ABSOLUTE MAXIMUM RATINGS

Table 6-1. Absolute Maximum Ratings

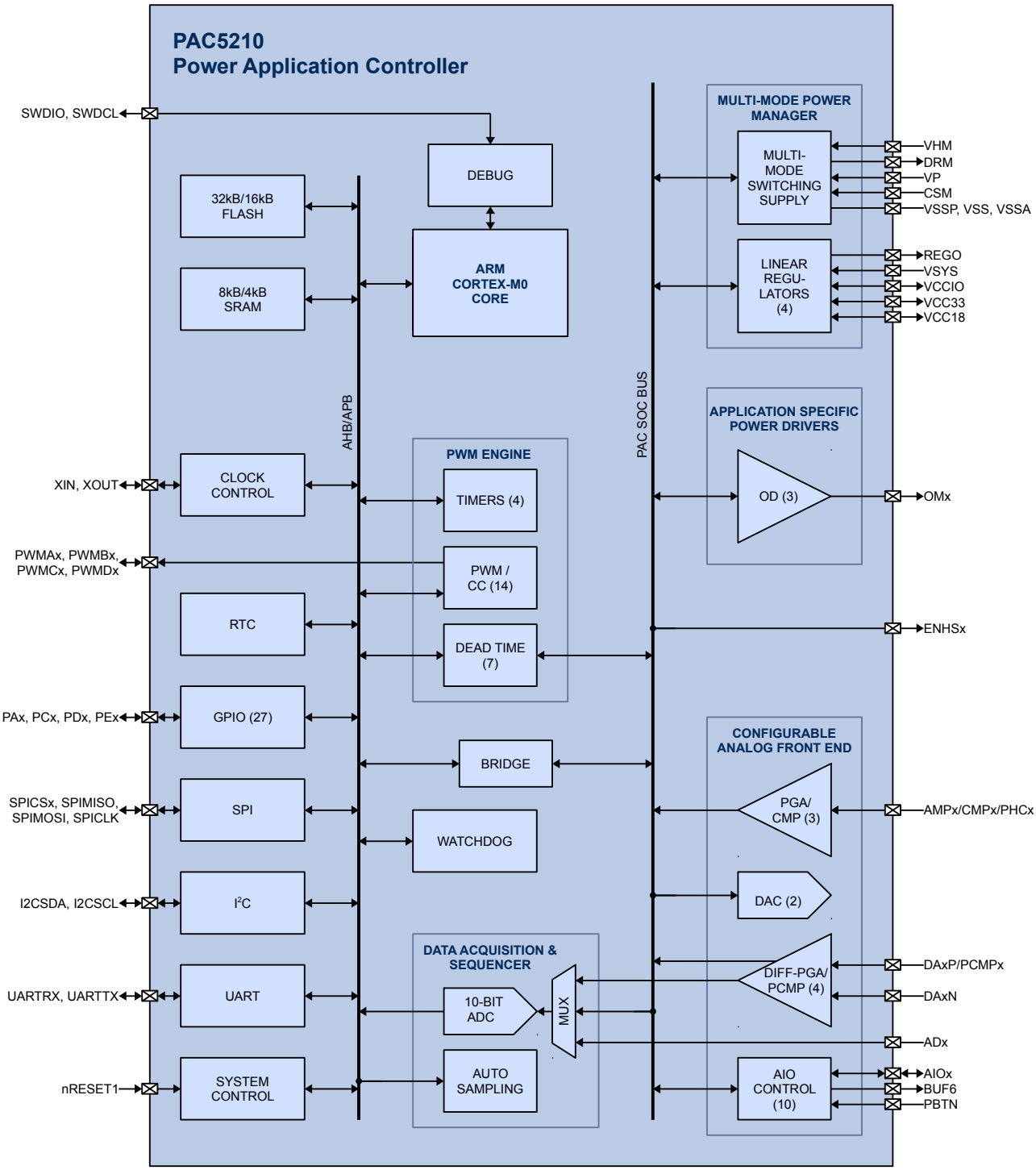
(Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

PARAMETER		VALUE	UNIT
VHM, DRM to VSSP		-0.3 to 54	V
VP to VSS		-0.3 to 20	V
CSM, REGO to VSS		-0.3 to V_P + 0.3	V
VSYS, AIO6/.. to VSS		-0.3 to 6	V
VCC33 to VSS		-0.3 to 4.1	V
VCC18 to VSS		-0.3 to 2.5	V
AIOx/.. (except AIO6/..), VCCIO, ENHS1, ENHS2 to VSS		-0.3 to V_{SYS} + 0.3	V
PAx/.., PDx/.., PEx/.. to VSS		-0.3 to V_{CCIO} + 0.3	V
XIN, XOUT to VSS		-0.3 to V_{CC18} + 0.3	V
PCx/.. to VSSA		-0.3 to V_{CC33} + 0.3	V
OMx to VSSP		-0.3 to 24	V
VSSP, VSSA to VSS		-0.3 to 0.3	V
VSS, VSYS, DRM, REGO, OMx RMS current[1]		0.2	A_{RMS}
VSSP RMS current[1]		0.4	A_{RMS}
VP RMS current[1]		0.6	A_{RMS}
Operating temperature range		-40 to 105	°C
Electrostatic discharge (ESD)	Human body model (JEDEC)	2	kV
	Charge device model (JEDEC)	1	kV
	Machine model (JEDEC)	200	V

[1] Peak current can be 10 times higher than RMS value for pulses shorter than 10µs.

7. ARCHITECTURAL BLOCK DIAGRAM

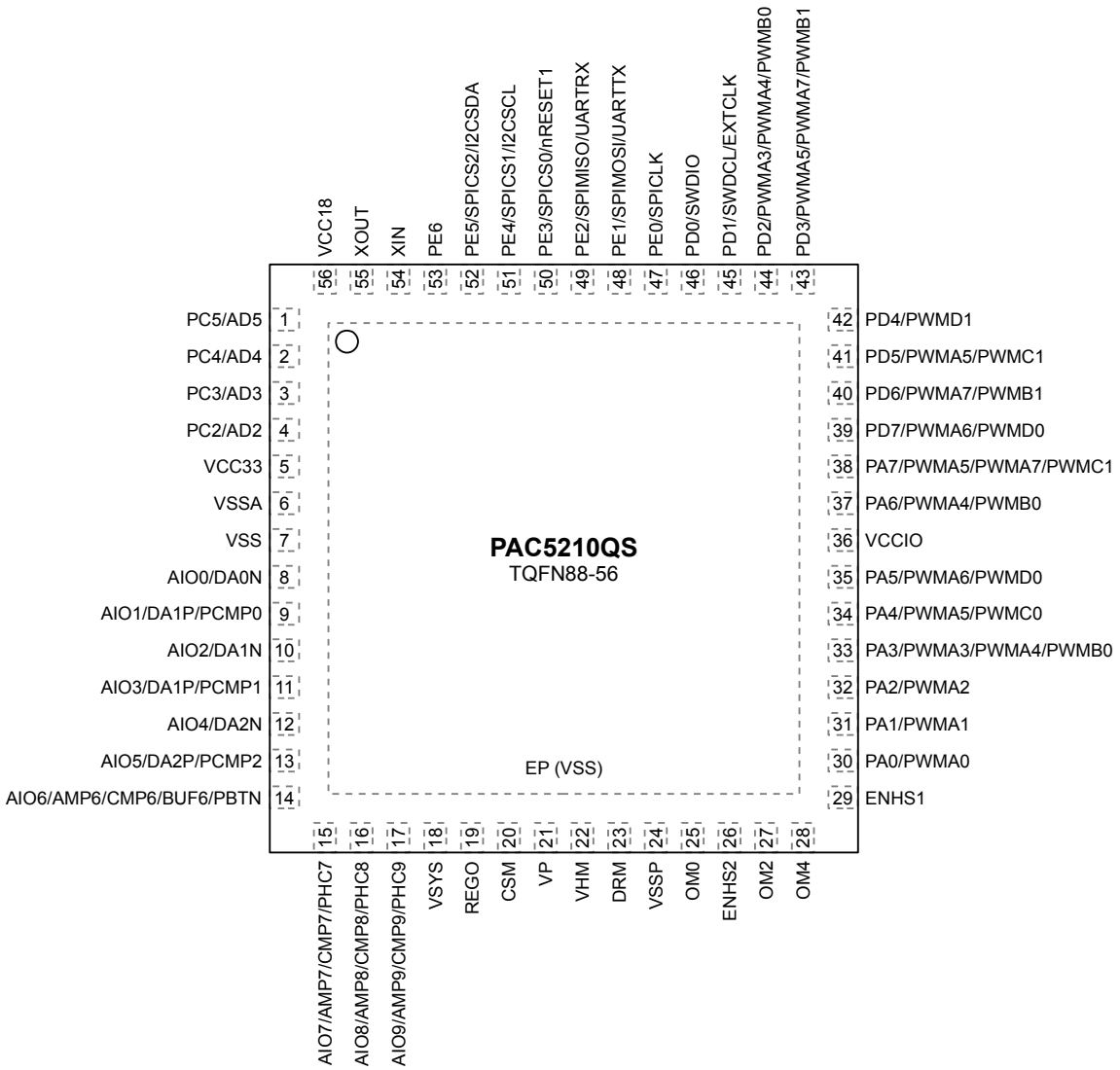
Figure 7-1. Architectural Block Diagram



8. PIN CONFIGURATION

8.1. PAC5210QS

Figure 8-1. PAC5210QS Pin Configuration (TQFN88-56 Package)



9. PIN DESCRIPTION

Table 9-1. Multi-Mode Power Manager and System Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
CSM	20	Analog	Switching supply current sense input. Connect to the positive side of the current sense resistor.
DRM	23	Analog	Switching supply driver output. Connect to the base or gate of the external power NPN or n-channel MOSFET. See *PAC51xx/52xx User Guide* and application notes.
EP (VSS)	EP	Power	Exposed pad. Must be connected to V_{SS} in a star ground configuration. Connect to a large PCB copper area for power dissipation heat sinking.
REGO	19	Power	System regulator output. Connect to V_{SYS} directly or through an external power-dissipating resistor.
VCC18	56	Power	Internally generated 1.8V core power supply. Connect a 2.2µF or higher value ceramic capacitor from V_{CC18} to V_{SSA}. See Figure 9-1. Power Supply Bypass Capacitor Routing below.
VCC33	5	Power	Internally generated 3.3V power supply. Connect a 2.2µF or higher value ceramic capacitor from V_{CC33} to V_{SSA}. See PCB layout note below.
VCCIO	53	Power	Internally generated digital I/O power supply. Connect a 4.7µF or higher value ceramic capacitor from V_{CCIO} to V_{SSA}. See Figure 9-1. Power Supply Bypass Capacitor Routing below.
VHM	22	Power	Switching supply controller supply input. Connect a 1µF or higher value ceramic capacitor, or a 0.1µF ceramic capacitor in parallel with a 10µF or higher electrolytic capacitor from V_{HM} to V_{SSP}. This pin requires good capacitive bypassing to V_{SSP}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin. See Figure 9-1. Power Supply Bypass Capacitor Routing below.
VP	21	Power	Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 0.1µF ceramic capacitor from V_P pin to V_{SS} for voltage loop stabilization. This pin requires good capacitive bypassing to V_{SS}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin. See See Figure 9-1. Power Supply Bypass Capacitor Routing below.
VSS	7	Power	Ground.
VSSA	6	Power	Analog ground. Connect to V_{SS} in a star ground configuration.
VSSP	24	Power	Power ground. Connect to V_{SS} in a star ground configuration.
VSYS	18	Power	5V system power supply. Connect a 4.7µF or higher value ceramic capacitor from V_{SYS} to V_{SSP}. See Figure 9-1. Power Supply Bypass Capacitor Routing below.
XIN	54	Analog	Crystal oscillator driver input. Leave floating if unused.
XOUT	55	Analog	Crystal oscillator driver output. Leave floating if unused.

Table 9-2. Configurable Analog Front End Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
AIO0/DA0N	8	AIO0	I/O	Analog front end I/O 0.
		DA0N	Analog	Differential PGA 0 negative input.
AIO1/DA0P/PCMP0	9	AIO1	I/O	Analog front end I/O 1.
		DA0P	Analog	Differential PGA 0 positive input.
		PCMP0	Analog	Protection comparator input 0.
AIO2/DA1N	10	AIO2	I/O	Analog front end I/O 2.
		DA1N	Analog	Differential PGA 1 negative input.
AIO3/DA1P/PCMP1	11	AIO3	I/O	Analog front end I/O 3.
		DA1P	Analog	Differential PGA 1 positive input.
		PCMP1	Analog	Protection comparator input 1.
AIO4/DA2N	12	AIO4	I/O	Analog front end I/O 4.
		DA2N	Analog	Differential PGA 2 negative input.
AIO5/DA2P/PCMP2	13	AIO5	I/O	Analog front end I/O 5.
		DA2P	Analog	Differential PGA 2 positive input.
		PCMP2	Analog	Protection comparator input 2.
AIO6/AMP6/CMP6/BUF6/PBTN	14	AIO6	I/O	Analog front end I/O 6.
		AMP6	Analog	PGA input 6.
		CMP6	Analog	Comparator input 6.
		BUF6	Analog	Buffer output 6.
		PBTN	Analog	Push button input.
AIO7/AMP7/CMP7/PHC7	15	AIO7	I/O	Analog front end I/O 7.
		AMP7	Analog	PGA input 7.
		CMP7	Analog	Comparator input 7.
		PHC7	Analog	Phase comparator input 7.
AIO8/AMP8/CMP8/PHC8	16	AIO8	I/O	Analog front end I/O 8.
		AMP8	Analog	PGA input 8.
		CMP8	Analog	Comparator input 8.
		PHC8	Analog	Phase comparator input 8.
AIO9/AMP9/CMP9/PHC9	17	AIO9	I/O	Analog front end I/O 9.
		AMP9	Analog	PGA input 9.
		CMP9	Analog	Comparator input 9.
		PHC9	Analog	Phase comparator input 9.

Table 9-3. Application Specific Power Drivers Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
ENHS1	29	O	Protection group 1 control output.
ENHS2	26	O	Protection group 2 control output.
OM0	25	OD	Medium-voltage open-drain driver 0.
OM2	27	OD	Medium-voltage open-drain driver 2.
OM4	28	OD	Medium-voltage open-drain driver 4.

Table 9-4. I/O Ports Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
PA0/PWMA0	30	PA0	I/O	I/O port A0.
		PWMA0	I/O	Timer A PWM/capture 0.
PA1/PWMA1	31	PA1	I/O	I/O port A1.
		PWMA1	I/O	Timer A PWM/capture 1.
PA2/PWMA2	32	PA2	I/O	I/O port A2.
		PWMA2	I/O	Timer A PWM/capture 2.
PA3/PWMA3/PWMA4/PWMB0	33	PA3	I/O	I/O port A3.
		PWMA3	I/O	Timer A PWM/capture 3.
		PWMA4	I/O	Timer A PWM/capture 4.
		PWMB0	I/O	Timer B PWM/capture 0.
PA4/PWMA5/PWMC0	34	PA4	I/O	I/O port A4.
		PWMA5	I/O	Timer A PWM/capture 5.
		PWMC0	I/O	Timer C PWM/capture 0.
PA5/PWMA6/PWMD0	35	PA5	I/O	I/O port A5.
		PWMA6	I/O	Timer A PWM/capture 6.
		PWMD0	I/O	Timer D PWM/capture 0.
PA6/PWMA4/PWMB0	37	PA6	I/O	I/O port A6.
		PWMA4	I/O	Timer A PWM/capture 4.
		PWMB0	I/O	Timer B PWM/capture 0.
PA7/PWMA5/PWMA7/PWMC1	38	PA7	I/O	I/O port A7.
		PWMA5	I/O	Timer A PWM/capture 5.
		PWMA7	I/O	Timer A PWM/capture 7.
		PWMC1	I/O	Timer C PWM/capture 1.
PC2/AD2	4	PC2	I/O	I/O port C2.
		AD2	Analog	ADC input 2.
PC3/AD3	3	PC3	I/O	I/O port C3.
		AD3	Analog	ADC input 3.
PC4/AD4	2	PC4	I/O	I/O port C4.
		AD4	Analog	ADC input 4.
PC5/AD5	1	PC5	I/O	I/O port C5.
		AD5	Analog	ADC input 5.

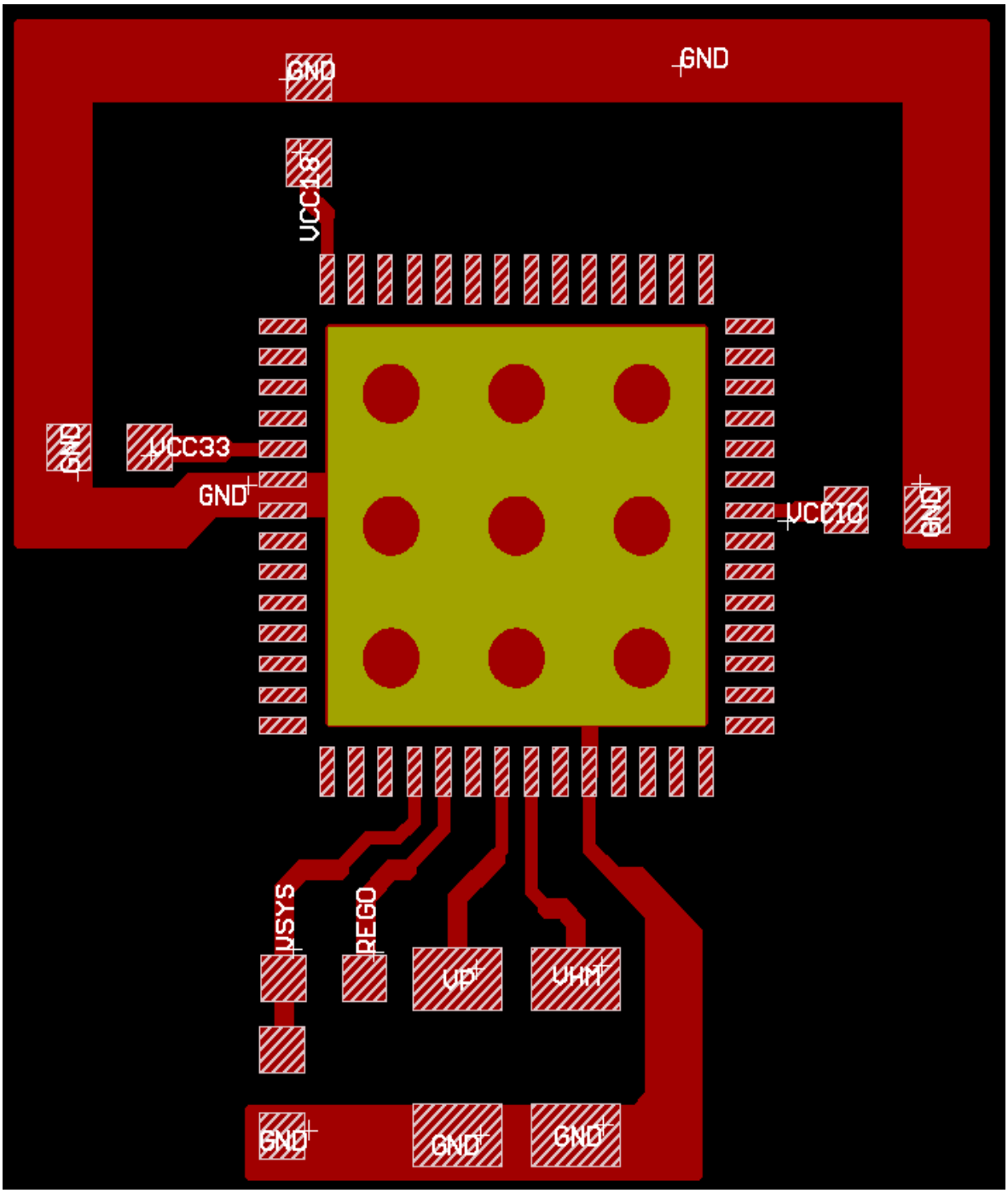
Table 9-5. I/O Ports Pin Description (Continued)

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
PD0/SWDIO	46	PD0	I/O	I/O port D0.
		SWDIO	I/O	Serial wire debug I/O.
PD1/SWDCL/EXTCLK	45	PD1	I/O	I/O port D1.
		SWDCL	I	Serial wire debug clock.
		EXTCLK	I	External clock.
PD2/PWMA3/PWMA4/PWMB0	44	PD2	I/O	I/O port D2.
		PWMA3	I/O	Timer A PWM/capture 3.
		PWMA4	I/O	Timer A PWM/capture 4.
		PWMB0	I/O	Timer B PWM/capture 0.
PD3/PWMA5/PWMA7/PWMB1	43	PD3	I/O	I/O port D3.
		PWMA5	I/O	Timer A PWM/capture 5.
		PWMA7	I/O	Timer A PWM/capture 7.
		PWMB1	I/O	Timer B PWM/capture 1.
PD4/PWMD1	42	PD4	I/O	I/O port D4.
		PWMD1	I/O	Timer D PWM/capture 1.
PD5/PWMA5/PWMC1	41	PD5	I/O	I/O port D5.
		PWMA5	I/O	Timer A PWM/capture 5.
		PWMC1	I/O	Timer C PWM/capture 1.
PD6/PWMA7/PWMB1	40	PD6	I/O	I/O port D6.
		PWMA7	I/O	Timer A PWM/capture 7.
		PWMB1	I/O	Timer B PWM/capture 1.
PD7/PWMA6/PWMD0	39	PD7	I/O	I/O port D7.
		PWMA6	I/O	Timer A PWM/capture 6.
		PWMD0	I/O	Timer D PWM/capture 0.
PE0/SPICLK	47	PE0	I/O	I/O port E0.
		SPICLK	I/O	SPI clock.
PE1/SPIMOSI/UARTTX	48	PE1	I/O	I/O port E1.
		SPIMOSI	I/O	SPI master out slave in (MOSI).
		UARTTX	O	UART transmit output.
PE2/SPIMISO/UARTRX	49	PE2	I/O	I/O port E2.
		SPIMISO	I/O	SPI master in slave out (MISO).
		UARTRX	I	UART receive input.

Table 9-6. I/O Ports Pin Description (Continued)

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
PE3/SPICS0/nRESET1	50	PE3	I/O	I/O port E3.
		SPICS0	O	SPI chip select 0.
		nRESET1	I	Reset input 1 (active low).
PE4/SPICS1/I2CSCL	51	PE4	I/O	I/O port E4.
		SPICS1	O	SPI chip select 1.
		I2CSCL	I/O	I2C clock.
PE5/SPICS2/I2CSDA	52	PE5	I/O	I/O port E5.
		SPICS2	O	SPI chip select 2.
		I2CSDA	I/O	I2C data.
PE6	53	PE6	I/O	I/O port E6.

Figure 9-1. Power Supply Bypass Capacitor Routing



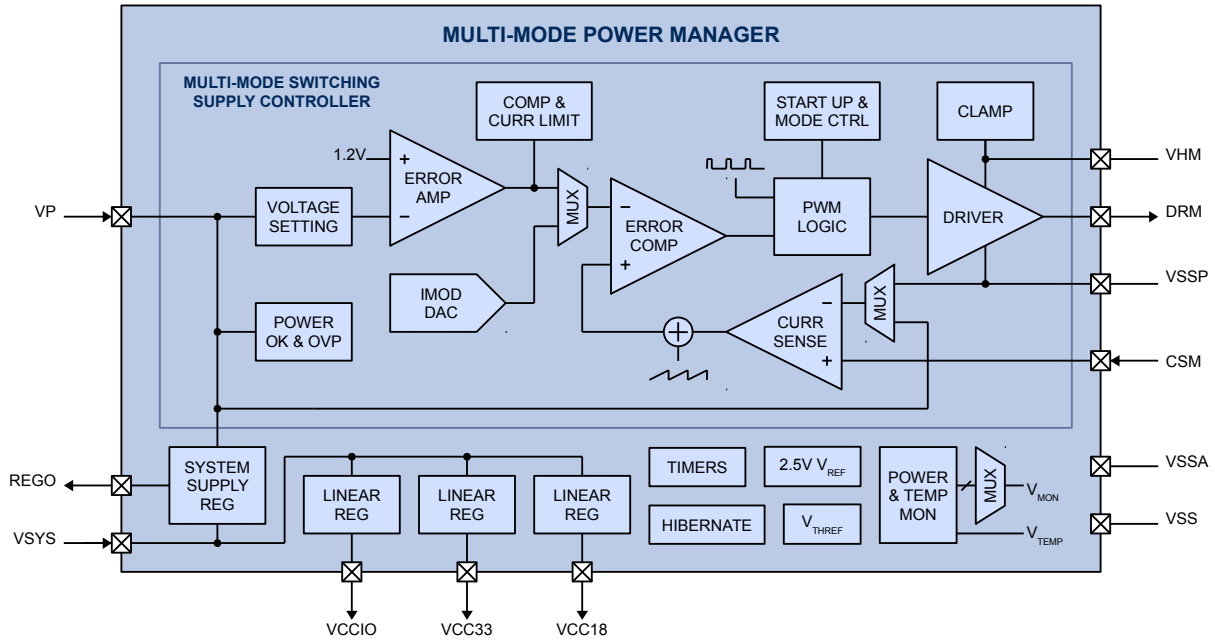
10. MULTI-MODE POWER MANAGER (MMPM)

10.1. Features

- Multi-mode switching supply controller configurable as high voltage or ultra-high-voltage buck, AC/DC flyback
- DC supply up to 52V or line AC input
- 4 linear regulators with power and hibernate management
- Power and temperature monitor, warning, and fault detection

10.2. Block Diagram

Figure 10-1. Multi-Mode Power Manager



10.3. Functional Description

The Multi-Mode Power Manager (Figure 10-1) is optimized to efficiently provide "all-in-one" power management required by the PAC and associated application circuitry from a wide range of input power sources. It incorporates a dedicated multi-mode switching supply (MMSS) controller operable as a buck, flyback, or boost converter to efficiently convert power from a DC or AC input source to generate a main supply output V_P. Four linear regulators provide V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CC18} supplies for 5V system, 5V or 3.3V I/O, 3.3V mixed signal, and 1.8V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

10.3.1. Multi-Mode Switching Supply (MMSS) Controller

The MMSS controller drives an external power transistor for pulse-width modulation switching of an inductor or transformer for power conversion. The DRM output drives the gate of the n-channel MOSFET or the base of the NPN between the V_{HM} on state and V_{SSP} off state at proper duty cycle and switching frequency to ensure that the main supply voltage V_P is regulated. The V_P regulation voltage is initially set to 9V during start up, and can be

reconfigured to be 5V, 12V, or 15V by the microcontroller after initialization. When V_P is lower than the target regulation voltage, the internal feedback control circuitry causes the inductor current to increase to raise V_P. Conversely, when V_P is higher than the regulation voltage, the feedback loop control causes the inductor current to decrease to lower V_P. The feedback loop is internally stabilized. The output current capability of the switching supply is determined by the external current sense resistor. In the high-side current sense buck mode, the inductor current signal is sensed differentially between the CSM pin and V_P, and has a peak current limit threshold of 0.26V. In the low-side current sense flyback or boost mode, the inductor current signal is sensed differentially between the CSM pin and V_{SSP}, and has a peak current limit threshold of 1V.

The MMSS controller is flexible and configurable as a buck, flyback, or boost converter. Input sources include battery supply for buck mode (Figure 10-2), and AC line supply voltage range for ultra-high-voltage buck mode (Figure 10-3), AC/DC flyback mode(Figure10-4). The MMSS controller operational mode is determined by external configuration and register setting from the microcontroller after power up. It can operate in either high-side or low-side current sense mode, and does not require external feedback loop compensation circuitry. For optional extended application range, the MMSS also incorporates additional digital control by the microcontroller to add accurate computations for outer feedback loop control such as power factor correction and accurate current control.

Figure 10-2. Buck Mode

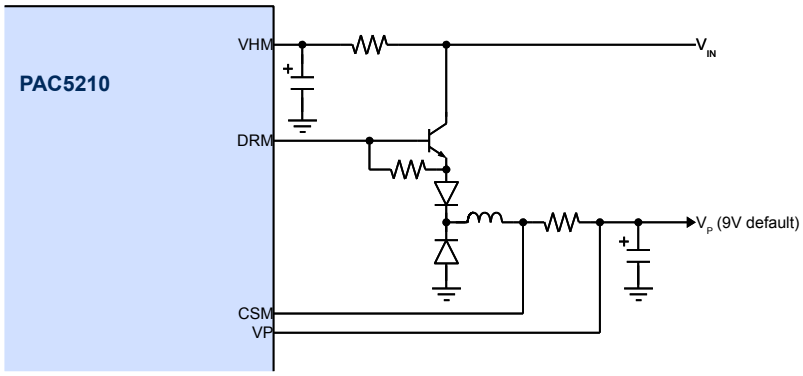


Figure 10-3. Ultra-High-Voltage Buck Mode

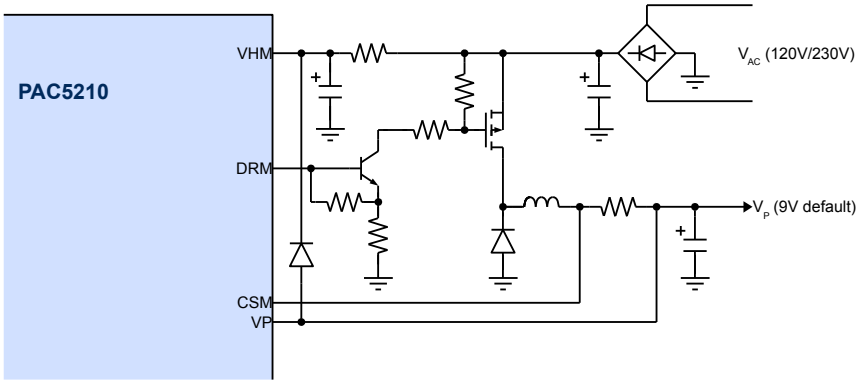
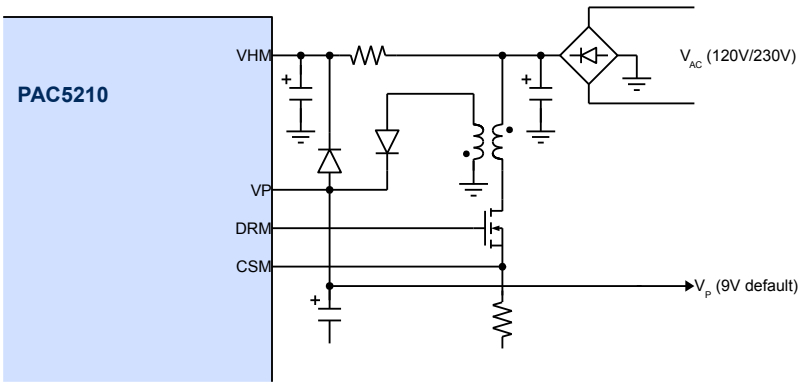


Figure 10-4. AC/DC Flyback Mode



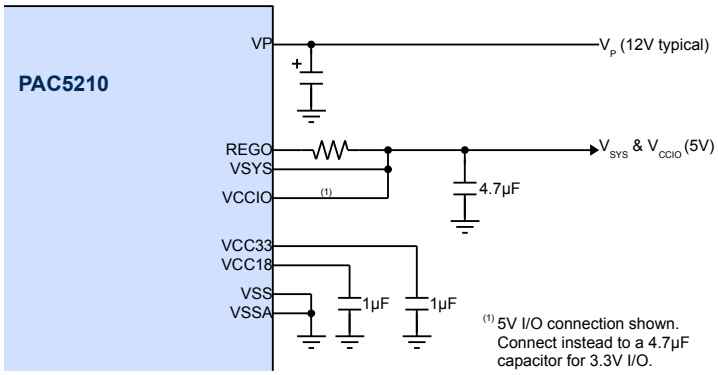
The MMSS detects and selects between high-side and low-side mode during start up based on the placement of the current sense resistor and the CSM pin voltage. It employs a safe start up mode with a 9.5kHz switching frequency until V_P exceeds 4.3V under-voltage-lockout threshold, then transitions to the 45kHz default switching frequency for at least 6ms to bring V_P close to the target voltage, before enabling the linear regulators. Any extra load should only be applied after the supplies are available and the microprocessor has initialized. The switching frequency can be reconfigured by the microprocessor to be 181kHz to 500kHz in the high switching frequency mode for battery-based applications, and to be 45kHz to 125kHz in the low switching frequency mode for AC applications. Upon initialization, the microcontroller must reconfigure the MMSS to the desired settings for V_P regulation voltage, switching mode, switching frequency, and V_{HM} clamp. Refer to the PAC application notes and user guide for MMSS controller design and programming.

If a stable external 4.5V to 18V power source is available, it can power the V_P main supply and all the linear regulators directly without requiring the MMSS controller to operate. In such applications, V_{HM} can be connected directly to V_P and the microcontroller should disable the MMSS upon initialization to reduce power loss.

10.3.2. Linear Regulators

The MMPM includes up to four linear regulators. The system supply regulator is a medium voltage regulator that takes the V_P supply and sources up to 200mA at REGO until V_{SYS}, externally coupled to REGO, reaches 5V. This allows a properly rated external resistor to be connected from REGO to V_{SYS} to close the current loop and offload power dissipation between V_P and V_{SYS}. Once V_{SYS} is above 4V, the three additional 40mA linear regulators for V_{CCIO}, V_{CC33}, and V_{CC18} supplies sequentially power up. Figure 10-5 shows typical circuit connections for the linear regulators. For 5V I/O systems, short the V_{CCIO} pin to V_{SYS} to bypass the V_{CCIO} regulator. For 3.3V I/O systems, the V_{CCIO} regulator generates 3.3V. The V_{CC33} and V_{CC18} regulators generate 3.3V and 1.8V, respectively. When V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CC18} are all above their respective power good thresholds, and the configurable power on reset duration has expired, the microcontroller is initialized.

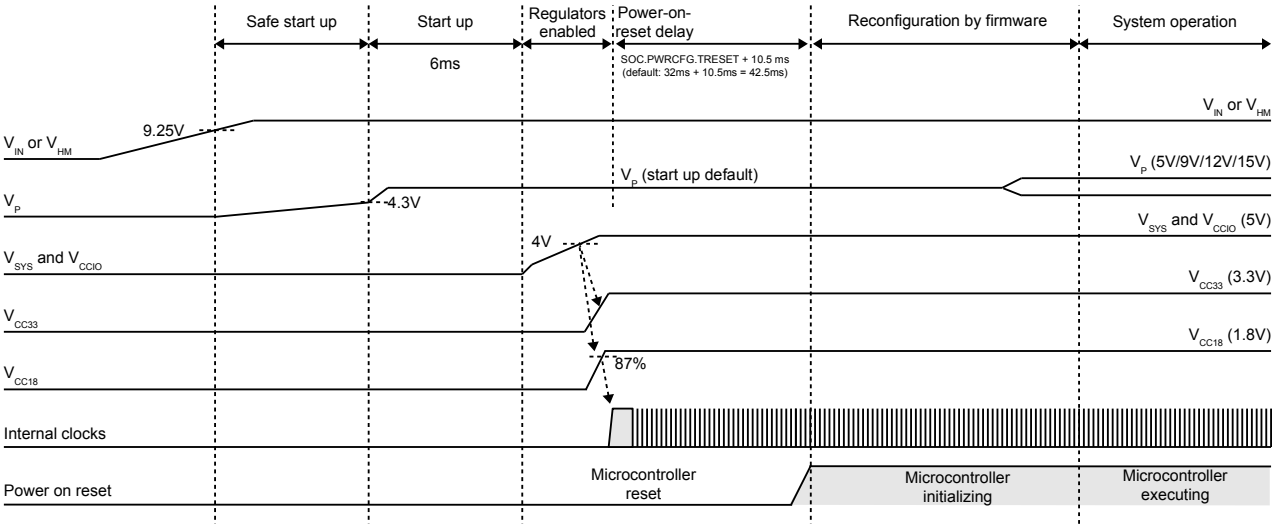
Figure 10-5. Linear Regulators



10.3.3. Power Up Sequence

The MMPM follows a typical power up sequence as in the Figure 10-6 below. A typical sequence begins with input power supply being applied, followed by the safe start up and start up durations to bring the switching supply output V_P to 9V, before the linear regulators are enabled. When all the supplies are ready, the internal clocks become available, and the microcontroller starts executing from the program memory. During initialization, the microcontroller can reconfigure the switching supply to a different V_P regulation voltage such as 15V and to an appropriate switching frequency and switching mode. The total loading on the switching supply must be kept below 25% of the maximum output current until after the reconfiguration of the switching supply is complete. For AC input supply applications, the start up sequence includes an additional charging time for V_{HM} depending on the start-up resistor and capacitor values.

Figure 10-6. Power Up Sequence



10.3.4. Hibernate Mode

The IC can go into an ultra-low power hibernate mode via the microcontroller firmware or via the optional push button (PBTN, see *Push Button* description in *Configurable Analog Front End*). In hibernate mode, only a minimal amount (typically 18µA) of current is used by V_{HM}, and the MMSS controller and all internal regulators

are shut down to eliminate power drain from the output supplies. The system exits hibernate mode after a wake-up timer duration (configurable from 125ms to 8s or infinite) has expired or, if push button enabled, after an additional push button event has been detected. When exiting the hibernate mode, the power manager goes through the start up cycle and the microcontroller is reinitialized. Only the persistent power manager status bits (resets and faults) are retained during hibernation.

10.3.5. Power and Temperature Monitor

Whenever any of the V_{SYS}, V_{CCIO}, V_{CC33}, or V_{CC18} power supplies falls below their respective power good threshold voltage, a fault event is detected and the microcontroller is reset. The microcontroller stays in the reset state until V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CC18} supply rails are all good again and the reset time has expired. A microcontroller reset can also be initiated by a maskable temperature fault event that occurs when the IC temperature reaches 170°C. The fault status bits are persistent during reset, and can be read by the microcontroller upon re-initialization to determine the cause of previous reset.

A power monitoring signal V_{MON} is provided onto the ADC pre-multiplexer for monitoring various internal power supplies. V_{MON} can be set to be V_{CC18}, 0.4•V_{CC33}, 0.4•V_{CCIO}, 0.4•V_{SYS}, 0.1•V_{REGO}, 0.1•V_P, 0.0333•V_{HM}, or the internal compensation voltage V_{COMP} for switching supply power monitoring.

For power and temperature warning, a V_P low event at 77% of the regulation voltage and an IC temperature warning event at 140°C are provided as maskable interrupts to the microcontroller. These warnings allow the microcontroller to safely power down the system.

In addition to the temperature warning interrupt and fault reset, a temperature monitor signal V_{TEMP} = 1.5 + 5.04e-3 • (T - 25°C) (V) is provided onto the ADC pre-multiplexer for IC temperature measurement.

10.3.6. Voltage Reference

The reference block includes a 2.5V high precision reference voltage that provides the 2.5V reference voltage for the ADC, the DACs, and the 4-level programmable threshold voltage V_{THREF} (0.1V, 0.2V, 0.5V, and 1.25V).