



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# PAC5220

## *Power Application Controller™*

Multi-Mode Power Manager™

Configurable Analog Front End™

Application Specific Power Drivers™

ARM® Cortex™-M0 Controller Core



## TABLE OF CONTENTS

1. Styles and Formatting Conventions.....	24
1.1. Overview.....	24
1.2. Number Representation.....	24
1.3. Formatting Styles.....	24
2. Memory and Register Map.....	25
2.1. Memory Map.....	25
2.2. Register Map.....	26
3. Information Block.....	38
3.1. Register.....	38
3.1.1. Register Map.....	38
3.1.2. ROOSC11.....	38
3.1.3. VREFV.....	38
3.1.4. ADCGAIN.....	39
3.1.5. ADCOFF.....	39
3.1.6. FTTEMP.....	39
3.1.7. TEMPS.....	39
3.1.8. CLKREF.....	39
3.1.9. DIEREV.....	39
3.1.10. PACIDR.....	39
3.2. Details of Operation.....	40
3.2.1. Overview.....	40
4. System Clock Control.....	41
4.1. Register.....	41
4.1.1. Register Map.....	41
4.1.2. CCSCTL.....	41
4.1.3. PLLCTL.....	42
4.1.4. OSCCTL.....	42
4.1.5. XTALCTL.....	42
4.2. Details of Operation.....	43
4.2.1. Block Diagram.....	43
4.2.2. Configuration.....	43
4.2.3. ROOSC.....	44
4.2.4. CLKREF.....	44
4.2.5. XTAL.....	44
4.2.6. EXTCLK.....	44
4.2.7. PLL.....	44
4.2.8. FRCLK.....	45
4.2.9. FCLK.....	45
4.2.10. HCLK.....	45
4.2.11. ACLK.....	45
4.2.12. Clock Gating.....	45
5. Watchdog Timer.....	46
5.1. Register.....	46
5.1.1. Register Map.....	46
5.1.2. WDTCTL.....	46
5.1.3. WDTCDV.....	47
5.1.4. WDTCTR.....	47
5.2. Details of Operation.....	48
5.2.1. Block Diagram.....	48
5.2.2. Configuration.....	48
5.2.3. Watchdog Timer.....	48

5.2.4. Access WDT Registers.....	48
5.2.5. WDT Clock Setting.....	48
5.2.6. General Purpose Timer Mode.....	48
5.2.7. Watchdog Timer Mode.....	49
6. General Purpose Timer.....	50
6.1. Register.....	50
6.1.1. Register Map.....	50
6.1.2. RTCCTL.....	50
6.1.3. RTCCDV.....	51
6.1.4. RTCCTR.....	51
6.2. Details of Operation.....	52
6.2.1. Block Diagram.....	52
6.2.2. Configuration.....	52
6.2.3. General Purpose Timer.....	52
6.2.4. Access GPT Registers.....	52
6.2.5. GPT Clock.....	52
6.2.6. General Purpose Timer Mode.....	52
7. GPIO Port A.....	53
7.1. Register.....	53
7.1.1. Register Map.....	53
7.1.2. GPIOAO.....	53
7.1.3. GPIOAOUTEN.....	54
7.1.4. GPIOADS.....	54
7.1.5. GPIOAPU.....	55
7.1.6. GPIOAPD.....	56
7.1.7. GPIOAIN.....	56
7.1.8. GPIOAPSEL.....	57
7.1.9. GPIOAINTP.....	58
7.1.10. GPIOAINTE.....	58
7.1.11. GPIOAINTF.....	59
7.1.12. GPIOAINTM.....	60
7.2. Details of Operation.....	61
7.2.1. Block Diagram.....	61
7.2.2. Configuration.....	61
7.2.3. GPIO A Block.....	61
7.2.4. Input.....	61
7.2.5. Output and Output Enable.....	61
7.2.6. Output Drive Strength.....	62
7.2.7. Weak Pull Up and Pull Down.....	62
7.2.8. Peripheral Select.....	62
7.2.9. Interrupt.....	62
8. GPIO Port B.....	63
8.1. Register.....	63
8.1.1. Register Map.....	63
8.1.2. GPIOBOUT.....	63
8.1.3. GPIOBOUTEN.....	63
8.1.4. GPIOBDS.....	64
8.1.5. GPIOBPU.....	64
8.1.6. GPIOBPD.....	65
8.1.7. GPIOBIN.....	65
8.1.8. GPIOBPSEL.....	65
8.1.9. GPIOBINTP.....	66
8.1.10. GPIOBINTE.....	67
8.1.11. GPIOBINTF.....	67

8.1.12. GPIOBINTM.....	68
8.2. Details of Operation.....	69
8.2.1. Block Diagram.....	69
8.2.2. Configuration.....	69
8.2.3. GPIO B Block.....	69
8.2.4. Input.....	69
8.2.5. Output and Output Enable.....	69
8.2.6. Output Drive Strength.....	69
8.2.7. Weak Pull Up and Pull Down.....	70
8.2.8. Peripheral Select.....	70
8.2.9. Interrupt.....	70
9. GPIO Port C.....	71
9.1. Register.....	71
9.1.1. Register Map.....	71
9.1.2. GPIOCOUT.....	71
9.1.3. GPIOCOUTEN.....	72
9.1.4. GPIOCIN.....	72
9.1.5. GPIOCINE.....	73
9.1.6. GPIOCINTP.....	74
9.1.7. GPIOCINTE.....	74
9.1.8. GPIOCINTF.....	75
9.1.9. GPIOCINTM.....	75
9.2. Details of Operation.....	77
9.2.1. Block Diagram.....	77
9.2.2. Configuration.....	77
9.2.3. GPIO C Block.....	77
9.2.4. Analog Input.....	77
9.2.5. Output and Output Enable.....	77
9.2.6. Interrupt.....	77
10. GPIO Port D.....	79
10.1. Register.....	79
10.1.1. Register Map.....	79
10.1.2. GPIODO.....	79
10.1.3. GPIODOOUTEN.....	80
10.1.4. GPIODDS.....	80
10.1.5. GPIODPU.....	81
10.1.6. GPIODPD.....	82
10.1.7. GPIODIN.....	82
10.1.8. GPIODPSEL.....	83
10.1.9. GPIODINTP.....	84
10.1.10. GPIODINTE.....	84
10.1.11. GPIODINTF.....	85
10.1.12. GPIODINTM.....	85
10.2. Details of Operation.....	87
10.2.1. Block Diagram.....	87
10.2.2. Configuration.....	87
10.2.3. GPIO D Block.....	87
10.2.4. Input.....	87
10.2.5. Output and Output Enable.....	87
10.2.6. Output Drive Strength.....	88
10.2.7. Weak Pull Up and Pull Down.....	88
10.2.8. Peripheral Select.....	88
10.2.9. Interrupt.....	88
11. GPIO Port E.....	89

11.1. Register.....	89
11.1.1. Register Map.....	89
11.1.2. GPIOEOUT.....	89
11.1.3. GPIOEOUTEN.....	90
11.1.4. GPIOEDS.....	90
11.1.5. GPIOEPU.....	91
11.1.6. GPIOEPD.....	92
11.1.7. GPIOEIN.....	92
11.1.8. GPIOEPSEL.....	93
11.1.9. GPIOEINTP.....	94
11.1.10. GPIOEINTE.....	94
11.1.11. GPIOEINTF.....	95
11.1.12. GPIOEINTM.....	95
11.2. Details of Operation.....	97
11.2.1. Block Diagram.....	97
11.2.2. Configuration.....	97
11.2.3. GPIO E Block.....	97
11.2.4. Input.....	97
11.2.5. Output and Output Enable.....	97
11.2.6. Output Drive Strength.....	97
11.2.7. Weak Pull Up and Pull Down.....	98
11.2.8. Peripheral Select.....	98
11.2.9. Interrupt.....	98
12. Timer A.....	99
12.1. Register.....	99
12.1.1. Register Map.....	99
12.1.2. TACTL.....	100
12.1.3. TAPRD.....	101
12.1.4. TACTR.....	101
12.1.5. TACC0CTRL.....	101
12.1.6. TACC0CTR.....	101
12.1.7. TACC1CTRL.....	102
12.1.8. TACC1CTR.....	102
12.1.9. TACC2CTRL.....	102
12.1.10. TACC2CTR.....	103
12.1.11. TACC3CTRL.....	103
12.1.12. TACC3CTR.....	103
12.1.13. TACC4CTRL.....	103
12.1.14. TACC4CTR.....	104
12.1.15. TACC5CTRL.....	104
12.1.16. TACC5CTR.....	104
12.1.17. TACC6CTRL.....	105
12.1.18. TACC6CTR.....	105
12.1.19. TACC7CTRL.....	105
12.1.20. TACC7CTR.....	106
12.1.21. DTGA0CTL.....	106
12.1.22. DTGA0LED.....	106
12.1.23. DTGA0TED.....	106
12.1.24. DTGA1CTL.....	107
12.1.25. DTGA1LED.....	107
12.1.26. DTGA1TED.....	107
12.1.27. DTGA2CTL.....	107
12.1.28. DTGA2LED.....	108
12.1.29. DTGA2TED.....	108

12.1.30. DTGA3CTL.....	108
12.1.31. DTGA3LED.....	109
12.1.32. DTGA3TED.....	109
12.2. Details of Operation.....	110
12.2.1. Block Diagram.....	110
12.2.2. Configuration.....	110
12.2.3. Timer A Block.....	110
12.2.4. Timer.....	110
12.2.5. Register update.....	111
12.2.6. Timer Modes.....	111
12.2.7. Single Shot Mode.....	111
12.2.8. Input Clock And Pre-Scaler.....	111
12.2.9. Timer Synchronization.....	111
12.2.10. PWM/Compare Units.....	112
12.2.11. Timer and PWM/Capture Interrupt.....	113
12.2.12. Dead-Time Generator.....	114
12.2.13. PWM Output and Capture Input Pin Selection.....	116
13. Timer B.....	117
13.1. Register.....	117
13.1.1. Register Map.....	117
13.1.2. TBCTL.....	117
13.1.3. TBPRD.....	118
13.1.4. TBCTR.....	118
13.1.5. TBCC0CTRL.....	118
13.1.6. TBCC0CTR.....	119
13.1.7. TBCC1CTRL.....	119
13.1.8. TBCC1CTR.....	119
13.1.9. TBCC2CTRL.....	120
13.1.10. TBCC2CTR.....	120
13.1.11. TBCC3CTRL.....	120
13.1.12. TBCC3CTR.....	121
13.1.13. DTGB0CTL.....	121
13.1.14. DTGB0LED.....	121
13.1.15. DTGB0TED.....	122
13.2. Details of Operation.....	123
13.2.1. Block Diagram.....	123
13.2.2. Configuration.....	123
13.2.3. Timer B Block.....	123
13.2.4. Timer.....	123
13.2.5. Register update.....	124
13.2.6. Timer Modes.....	124
13.2.7. Single Shot Mode.....	124
13.2.8. Input Clock And Pre-Scaler.....	124
13.2.9. Timer Synchronization.....	124
13.2.10. PWM/Compare Units.....	125
13.2.11. Timer and PWM/Capture Interrupt.....	126
13.2.12. Dead-Time Generator.....	127
13.2.13. PWM Output and Capture Input Pin Selection.....	129
14. Timer C.....	130
14.1. Register.....	130
14.1.1. Register Map.....	130
14.1.2. TCCTL.....	130
14.1.3. TCPRD.....	131
14.1.4. TCCTR.....	131

14.1.5. TCCC0CTRL.....	131
14.1.6. TCCC0CTR.....	132
14.1.7. TCCC1CTRL.....	132
14.1.8. TCCC1CTR.....	132
14.1.9. DTGC0CTL.....	133
14.1.10. DTGC0LED.....	133
14.1.11. DTGC0TED.....	133
14.2. Details of Operation.....	134
14.2.1. Block Diagram.....	134
14.2.2. Configuration.....	134
14.2.3. Timer C Block.....	134
14.2.4. Timer.....	134
14.2.5. Register update.....	135
14.2.6. Timer Modes.....	135
14.2.7. Single Shot Mode.....	135
14.2.8. Input clock and Pre-scaler.....	135
14.2.9. Timer synchronization.....	135
14.2.10. PWM/Compare Units.....	136
14.2.11. Timer and PWM/Capture Interrupt.....	137
14.2.12. Dead-Time Generator.....	138
14.2.13. PWM Output and Capture Input Pin Selection.....	140
15. Timer D.....	141
15.1. Register.....	141
15.1.1. Register Map.....	141
15.1.2. TDCTL.....	141
15.1.3. TDPRD.....	142
15.1.4. TDCTR.....	142
15.1.5. TDCC0CTL.....	142
15.1.6. TDCC0CTR.....	143
15.1.7. TDCC1CTRL.....	143
15.1.8. TDCC1CTR.....	143
15.1.9. DTGD0CTL.....	144
15.1.10. DTGD0LED.....	144
15.1.11. DTGD0TED.....	144
15.2. Details of Operation.....	145
15.2.1. Block Diagram.....	145
15.2.2. Configuration.....	145
15.2.3. Timer D Block.....	145
15.2.4. Timer.....	145
15.2.5. Register Update.....	146
15.2.6. Timer Modes.....	146
15.2.7. Single Shot Mode.....	146
15.2.8. Input Clock And Pre-Scaler.....	146
15.2.9. Timer Synchronization.....	146
15.2.10. PWM/Compare Units.....	147
15.2.11. Timer and PWM/Capture Interrupt.....	148
15.2.12. Dead-Time Generator.....	148
15.2.13. PWM Output and Capture Input Pin Selection.....	150
16. FLASH Memory Controller.....	151
16.1. Register.....	151
16.1.1. Register Map.....	151
16.1.2. FLASHLOCK.....	151
16.1.3. FLASHCTL.....	152
16.1.4. FLASHPAGE.....	152

16.1.5. FLASHPERASE.....	153
16.1.6. SWDACCESS.....	153
16.1.7. FLASHWSTATE.....	153
16.1.8. FLASHBWRITE.....	153
16.1.9. FLASHBWDATA.....	154
16.2. Details of Operation.....	155
16.2.1. Block Diagram.....	155
16.2.2. Configuration.....	155
16.2.3. FLASH Memory.....	155
16.2.4. Writing to FLASH Controller Registers.....	155
16.2.5. FLASH Wait State.....	155
16.2.6. FLASH Page Erase.....	156
16.2.7. Write to FLASH.....	156
16.2.8. Buffered Write to FLASH.....	156
16.2.9. SWD Debug Access Disable.....	157
17. ADC and AUTO SEQUENCER.....	158
17.1. Register.....	158
17.1.1. Register Map.....	158
17.1.2. EMUXCTL.....	159
17.1.3. EMUXDATA.....	160
17.1.4. ADCCTL.....	161
17.1.5. ADCCR.....	161
17.1.6. ADCINT.....	162
17.1.7. AS0CTL.....	163
17.1.8. AS0S0.....	164
17.1.9. AS0R0.....	164
17.1.10. AS0S1.....	164
17.1.11. AS0R1.....	165
17.1.12. AS0S2.....	165
17.1.13. AS0R2.....	165
17.1.14. AS0S3.....	166
17.1.15. AS0R3.....	166
17.1.16. AS0S4.....	166
17.1.17. AS0R4.....	167
17.1.18. AS0S5.....	167
17.1.19. AS0R5.....	167
17.1.20. AS0S6.....	168
17.1.21. AS0R6.....	168
17.1.22. AS0S7.....	168
17.1.23. AS0R7.....	169
17.1.24. AS1CTL.....	169
17.1.25. AS1S0.....	170
17.1.26. AS1R0.....	170
17.1.27. AS1S1.....	171
17.1.28. AS1R1.....	171
17.1.29. AS1S2.....	171
17.1.30. AS1R2.....	172
17.1.31. AS1S3.....	172
17.1.32. AS1R3.....	172
17.1.33. AS1S4.....	173
17.1.34. AS1R4.....	173
17.1.35. AS1S5.....	173
17.1.36. AS1R5.....	174
17.1.37. AS1S6.....	174

17.1.38. AS1R6.....	174
17.1.39. AS1S7.....	175
17.1.40. AS1R7.....	175
17.2. Details of Operation.....	175
17.2.1. Block Diagram.....	175
17.3. Details of Operation.....	175
17.3.1. Basic Configuration.....	175
17.3.2. ADC, Autosequencer and EMUX.....	176
17.3.3. Clock Setting.....	176
17.3.4. ADC.....	177
17.3.5. EMUX.....	177
17.3.6. Auto Sequencer ASC0, ASC1.....	177
18. I <sup>2</sup> C.....	182
18.1. Register.....	182
18.1.1. Register Map.....	182
18.1.2. I2CCFG.....	182
18.1.3. I2CSTATUS.....	182
18.1.4. I2CIE.....	184
18.1.5. I2CMCTRL.....	184
18.1.6. I2CMRXDATA.....	185
18.1.7. I2CMTXDATA.....	185
18.1.8. I2CBAUD.....	185
18.1.9. I2CSL RXDATA.....	185
18.1.10. I2CSL TXDATA.....	186
18.1.11. I2CADDR.....	186
18.2. Details of Operation.....	187
18.2.1. Block Diagram.....	187
18.2.2. Configuration.....	187
18.2.3. I2C.....	187
18.2.4. I2C Clock setting.....	187
18.2.5. I2C Addressing.....	188
18.2.6. I2C Master Read Transactions.....	188
19. UART.....	191
19.1. Register.....	191
19.1.1. Register Map.....	191
19.1.2. UARTRTX/UARTDL_L.....	191
19.1.3. UARTIER/UARTDL_H.....	192
19.1.4. UARTIIR.....	192
19.1.5. UARTLCR.....	193
19.1.6. UARTMCR.....	193
19.1.7. UARTLSR.....	193
19.1.8. UARTSP.....	194
19.1.9. UARTFCTL2.....	194
19.1.10. UARTIER2.....	195
19.1.11. UARTDL_L2.....	195
19.1.12. UARTDL_H2.....	195
19.1.13. UARTFD_F.....	195
19.1.14. UARTSTAT.....	195
19.2. Details of Operation.....	197
19.2.1. Block Diagram.....	197
19.2.2. Configuration.....	197
19.2.3. UART.....	197
19.2.4. UART Clock Rate Setting.....	197
19.2.5. Data settings.....	199

19.2.6. FIFO Settings.....	199
19.2.7. Error Checking on Received Data.....	199
20. SOC Bus bridge.....	200
20.1. Register.....	200
20.1.1. Register Map.....	200
20.1.2. SOCBCTL.....	200
20.1.3. SOCBCFG.....	200
20.1.4. SOCBCLKDIV.....	201
20.1.5. SOCBSTAT.....	201
20.1.6. SOCBCSSTR.....	202
20.1.7. SOCBD.....	203
20.1.8. SOCBINT_EN.....	203
20.2. Details of Operation.....	204
20.2.1. Block Diagram.....	204
20.2.2. Configuration.....	204
20.2.3. SOC Bridge.....	204
20.2.4. SOC Bridge Clock Rate Setting.....	204
20.2.5. Enable and Setup of SOC Bridge.....	205
20.2.6. SOC Interrupt.....	205
20.2.7. SOC Bridge Protocol.....	205
20.2.8. Reading from SOC Bridge.....	205
20.2.9. Writing to SOC Bridge.....	205
21. SPI.....	206
21.1. Register.....	206
21.1.1. Register Map.....	206
21.1.2. SPICTL.....	206
21.1.3. SPICFG.....	207
21.1.4. SPICLKDIV.....	208
21.1.5. SPISTAT.....	208
21.1.6. SPICSSTR.....	210
21.1.7. SPID.....	211
21.1.8. SPIINT_EN.....	211
21.2. Details of Operation.....	212
21.2.1. Block Diagram.....	212
21.2.2. Configuration.....	212
21.2.3. SPI.....	212
21.2.4. SPI Clock Rate Setting.....	212
21.2.5. Master Slave Mode.....	213
21.2.6. Clock Phase, Polarity.....	213
21.2.7. SPI Early Data Transmit.....	213
21.2.8. Data Format.....	214
21.2.9. Chip Select Settings.....	215
21.2.10. Auto Retransmit Data Word.....	215
21.2.11. Loop Back Mode.....	215
21.2.12. SPI Interrupt.....	216
21.2.13. SPI Enable.....	216
22. Multi-Mode Power Manager.....	217
22.1. Register.....	217
22.1.1. Register Map.....	217
22.1.2. SYSTAT.....	217
22.1.3. DEVID.....	218
22.1.4. VERID.....	218
22.1.5. PWRCTL.....	218
22.1.6. PWRSTAT.....	219

22.1.7. PSTATSET.....	219
22.1.8. IMOD.....	220
22.1.9. SCFG.....	220
22.1.10. SCFG2.....	220
23. Configurable Analog FRONT END.....	222
23.1. Register.....	222
23.1.1. Register Map.....	222
23.1.2. SOC.CFGAIO0.....	223
23.1.3. SOC.CFGAIO1.....	223
23.1.4. SOC.CFGAIO2.....	225
23.1.5. SOC.CFGAIO3.....	225
23.1.6. SOC.CFGAIO4.....	227
23.1.7. SOC.CFGAIO5.....	227
23.1.8. SOC.CFGAIO6.....	229
23.1.9. SOC.CFGAIO7.....	230
23.1.10. SOC.CFGAIO8.....	231
23.1.11. SOC.CFGAIO9.....	232
23.1.12. SOC.SIGSET.....	233
23.1.13. SOC.HPDAC.....	233
23.1.14. SOC.LPDAC0.....	233
23.1.15. SOC.LPDAC1.....	233
23.1.16. SOC.ADCSCAN.....	234
23.1.17. SOC.ADCIN1.....	234
23.1.18. SOC.PROTINTM.....	234
23.1.19. SOC.PROTSTAT.....	235
23.1.20. SOC.DOOUTSIG0.....	235
23.1.21. SOC.DOOUTSIG1.....	236
23.1.22. SOC.DINSIG0.....	236
23.1.23. SOC.DINSIG1.....	237
23.1.24. SOC.SIGINTM.....	237
23.1.25. SOC.SIGINTF.....	238
23.1.26. SOC.ENSIG.....	238
23.2. Details of Operation.....	239
23.2.1. Block Diagram.....	239
23.2.2. Configuration.....	239
23.2.3. Configurable Analog Front End.....	239
23.3. AIO1, AIO0.....	240
23.3.1. Block Diagram.....	240
23.3.2. AIO1, AIO0.....	240
23.3.3. AIO1, AIO0 digital I/O Mode.....	240
23.3.4. AIO1, AIO0 differential Amplifier Mode.....	241
23.3.5. AIO1, AIO0 Protection.....	241
23.4. AIO3, AIO2.....	243
23.4.1. Block Diagram.....	243
23.4.2. AIO3, AIO2.....	243
23.4.3. AIO3, AIO2 digital I/O Mode.....	243
23.4.4. AIO3, AIO2 differential Amplifier Mode DAO32.....	244
23.4.5. AIO3, AIO2 Protection.....	244
23.5. AIO5, AIO4.....	246
23.5.1. Block Diagram.....	246
23.5.2. AIO5, AIO4.....	246
23.5.3. AIO5, AIO4 digital I/O Mode.....	246
23.5.4. AIO5, AIO4 differential Amplifier Mode DAO54.....	247
23.5.5. AIO5, AIO4 Protection.....	247

23.6. AIO6.....	249
23.6.1. Block Diagram.....	249
23.6.2. AIO6.....	249
23.6.3. AIO6 digital I/O Mode.....	250
23.6.4. AIO6 Single Ended Amplifier Mode.....	250
23.6.5. AIO6 Comparator Mode.....	250
23.6.6. AIO6 Special Mode.....	251
23.6.7. AIO6 Push Button Mode.....	251
23.7. AIO7.....	253
23.7.1. Block Diagram.....	253
23.7.2. AIO7.....	253
23.7.3. AIO7 digital I/O Mode.....	253
23.7.4. AIO7 Single Ended Amplifier Mode.....	254
23.7.5. AIO7 Comparator Mode.....	254
23.7.6. AIO7 Special Mode.....	255
23.8. AIO8.....	257
23.8.1. Block Diagram.....	257
23.8.2. AIO8.....	257
23.8.3. AIO8 digital I/O Mode.....	258
23.8.4. AIO8 Single Ended Amplifier Mode.....	258
23.8.5. AIO8 Comparator Mode.....	258
23.8.6. AIO8 Special Mode.....	259
23.9. AIO9.....	261
23.9.1. Block Diagram.....	261
23.9.2. AIO9.....	261
23.9.3. AIO9 digital I/O Mode.....	262
23.9.4. AIO9 Single Ended Amplifier Mode.....	262
23.9.5. AIO9 Comparator Mode.....	262
23.9.6. AIO9 Special Mode.....	263
23.10. EMUX and ADMUX.....	265
23.10.1. Block Diagram.....	265
23.10.2. EMUX.....	265
23.10.3. ADMUX.....	266
24. Application Specific Power Driver.....	268
24.1. Register.....	268
24.1.1. Register Map.....	268
24.1.2. SOC.CFGDRV0.....	268
24.1.3. SOC.CFGDRV1.....	268
24.1.4. SOC.CFGDRQ6.....	269
24.1.5. SOC.CFGDRQ7.....	269
24.1.6. SOC.DOUTDRV.....	270
24.1.7. SOC.DINDRV.....	270
24.1.8. SOC.ENDRV.....	270
24.1.9. SOC.EMBBM.....	271
24.2. Details of Operation.....	272
24.2.1. Block Diagram.....	272
24.2.2. Configuration.....	272
24.2.3. Application Specific Power Driver.....	272
24.3. ENHS1, ENLS1 Protection.....	273
24.3.1. Block Diagram.....	273
24.3.2. ENHS1, ENLS1 Protection.....	273
24.4. DRL0 Low Side Driver.....	274
24.4.1. Block Diagram.....	274
24.4.2. DRL0.....	274

24.5. DRL1 Low Side Driver.....	275
24.5.1. Block Diagram.....	275
24.5.2. DRL1.....	275
24.6. DRL2 Low Side Driver.....	276
24.6.1. Block Diagram.....	276
24.6.2. DRL2.....	276
24.7. DRH3 High Side Driver.....	277
24.7.1. Block Diagram.....	277
24.7.2. DRH3.....	277
24.8. DRH4 High Side Driver.....	278
24.8.1. Block Diagram.....	278
24.8.2. DRH4.....	278
24.9. DRH5 High Side Driver.....	279
24.9.1. Block Diagram.....	279
24.9.2. DRH5.....	279
24.10. OHI6.....	280
24.10.1. Block Diagram.....	280
24.10.2. OHI6.....	280
24.11. OHI7.....	281
24.11.1. Block Diagram.....	281
24.11.2. OHI7.....	281
25. Arm Cortex-M0 Reference.....	282
25.1. Introduction.....	282
25.1.1. Overview.....	282
25.1.2. About the Cortex-M0 processor and core peripherals.....	282
25.2. The Cortex-M0 Processor.....	284
25.2.1. Programmers Model.....	284
25.2.2. Memory model.....	291
25.2.3. Exception model.....	296
25.2.4. Fault handling.....	302
25.2.5. Power management.....	303
25.3. The Cortex-M0 Instruction Set.....	305
25.3.1. Instruction set summary.....	305
25.3.2. Intrinsic Functions.....	307
25.3.3. About the Instruction Descriptions.....	308
25.3.4. Memory access instructions.....	313
25.3.5. General data processing instructions.....	320
25.3.6. Branch and control instructions.....	332
25.3.7. Miscellaneous instructions.....	334
25.4. Cortex-M0 Peripherals.....	344
25.4.1. About the Cortex-M0 peripherals.....	344
25.4.2. Nested Vectored Interrupt Controller.....	344
25.4.3. System Control Block.....	350
25.4.4. System timer, SysTick.....	357
26. Legal Information.....	361

## LIST OF TABLES

Table 2-1. Embedded FLASH Register Map.....	26
Table 2-2. ROM Register Map.....	27
Table 2-3. System Clock Control Register Map.....	27
Table 2-4. FLASH Memory Controller Register Map.....	27
Table 2-5. Watchdog Timer Register Map.....	28
Table 2-6. General Purpose Timer Register Map.....	28
Table 2-7. GPIO Port A Register Map.....	28
Table 2-8. GPIO Port B Register Map.....	29
Table 2-9. GPIO Port AB Register Map.....	30
Table 2-10. GPIO Port C Register Map.....	30
Table 2-11. GPIO Port D Register Map.....	30
Table 2-12. GPIO Port CD Register Map.....	31
Table 2-13. GPIO Port E Register Map.....	31
Table 2-14. Timer A Register Map.....	32
Table 2-15. Timer B Register Map.....	33
Table 2-16. Timer C Register Map.....	33
Table 2-17. Timer D Register Map.....	34
Table 2-18. EMUX Register Map.....	34
Table 2-19. ADC Register Map.....	34
Table 2-20. ADC Auto-Sampling Sequencer 0 Register Map.....	34
Table 2-21. ADC Auto-Sampling Sequencer 1 Register Map.....	35
Table 2-22. I2C Register Map.....	35
Table 2-23. UART Register Map.....	36
Table 2-24. SOC Bus Bridge Register Map.....	36
Table 2-25. SPI Register Map.....	37
Table 2-26. Multi-Mode Power Manager Register Map.....	37
Table 3-1. Information Block Register Map.....	38
Table 4-1. System Clock Control Register Map.....	41
Table 5-1. Watchdog Timer Register Map.....	46
Table 6-1. General Purpose Timer Register Map.....	50
Table 7-1. GPIO Port A Register Map.....	53
Table 8-1. GPIO Port B Register Map.....	63
Table 9-1. GPIO Port C Register Map.....	71
Table 10-1. GPIO Port D Register Map.....	79
Table 11-1. GPIO Port E Register Map.....	89
Table 12-1. Timer A Register Map.....	99
Table 12-2. Timer A Signal to Pin Mapping.....	116
Table 13-1. Timer B Register Map.....	117
Table 13-2. Timer B Signal to Pin Mapping.....	129
Table 14-1. Timer C Register Map.....	130
Table 14-2. Timer C Signal to Pin Mapping.....	140
Table 15-1. Timer D Register Map.....	141
Table 15-2. Timer D Signal to Pin Mapping.....	150
Table 16-1. FLASH Memory Controller Register Map.....	151
Table 17-1. Register Map – EMUX.....	158
Table 17-2. Register Map – ADC.....	158
Table 17-3. Register Map – ADC Auto Sequencer 0.....	158
Table 17-4. Register Map – ADC Auto Sequencer 1.....	159
Table 18-1. I2C Register Map.....	182
Table 19-1. UART Register Map.....	191
Table 20-1. SOC Bus Bridge Register Map.....	200

Table 21-1. SPI Register Map.....	206
Table 22-1. Multi-Mode Power Manager Register Map.....	217
Table 23-1. Configurable Analog Front End Register Map.....	222
Table 24-1. Application Specific Power Driver Register Map.....	268
Table 25-1. Summary of processor mode and stack use options.....	284
Table 25-2. Core register set summary.....	285
Table 25-3. Core register set summary.....	287
Table 25-4. APSR bit assignments.....	287
Table 25-5. IPSR bit assignments.....	287
Table 25-6. EPSR bit assignments.....	288
Table 25-7. PRIMASK register bit assignments.....	289
Table 25-8. CONTROL register bit assignments.....	290
Table 25-9. Memory Access Behavior.....	294
Table 25-10. Properties of the different exception types.....	297
Table 25-11. Execution return behavior.....	302
Table 25-12. Cortex-M0 instructions.....	306
Table 25-13. CMSIS intrinsic functions to generate some Cortex-M0 instructions.....	307
Table 25-14. CMSIS intrinsic functions to access special registers.....	308
Table 25-15. Condition code suffixes.....	313
Table 25-16. Memory access instructions.....	313
Table 25-17. Data processing instructions.....	320
Table 25-18. ADC, ADD, RSB, SBC, and SUB operand restrictions.....	322
Table 25-19. Branch and Control instructions.....	332
Table 25-20. Branch ranges.....	333
Table 25-21. Miscellaneous instructions.....	334
Table 25-22. Core peripheral register regions.....	344
Table 25-23. NVIC register summary.....	344
Table 25-24. CMSIS access NVIC functions.....	345
Table 25-25. ISER bit assignments.....	345
Table 25-26. ICER bit assignments.....	346
Table 25-27. ISPR bit assignments.....	347
Table 25-28. ICPR bit assignments.....	347
Table 25-29. IPR bit assignments.....	348
Table 25-30. CMSIS access NVIC functions.....	350
Table 25-31. Summary of the SCB register.....	350
Table 25-32. CPUID register bit assignments.....	351
Table 25-33. ICSR register bit assignments.....	352
Table 25-34. AIRCR register bit assignments.....	353
Table 25-35. SCR register bit assignments.....	354
Table 25-36. CCR register bit assignments.....	355
Table 25-37. System fault handler priority fields.....	356
Table 25-38. SHPR2 register bit assignments.....	356
Table 25-39. SHPR3 register bit assignments.....	356
Table 25-40. System timer register summary.....	357
Table 25-41. SYST_CSR register bit assignments.....	358
Table 25-42. SYST_RVR register bit assignments.....	358
Table 25-43. SYST_CVR register bit assignments.....	359
Table 25-44. SYST_CALIB register bit assignments.....	359

## LIST OF REGISTERS

Register 3-1. ROOSC11 (ROOSC11 Frequency Value, 0x0010 0010).....	38
Register 3-2. VREFV (VREF Reference Voltage Value, 0x0010 0020).....	38
Register 3-3. ADCGAIN (ADC Gain Value, 0x0010 0022).....	39
Register 3-4. ADCOFF (ADC Offset, 0x0010 0024).....	39
Register 3-5. FTTEMP (FT Temp value, 0x0010 0028).....	39
Register 3-6. TEMPS (Temperature Sensor reading, 0x0010 002A).....	39
Register 3-7. CLKREF (CLKREF Frequency Value, 0x0010 002C).....	39
Register 3-8. DIEREV (Device die revision, 0x0010 0040).....	39
Register 3-9. PACIDR (PAC part number and revision, 0x0010 0044).....	39
Register 4-1. CCSCTL (System Clock Control, 0x4000 0000).....	41
Register 4-2. PLLCTL (PLL Control, 0x4000 0004).....	42
Register 4-3. OSCCTL (Ring Oscillator Control, 0x4000 0008).....	42
Register 4-4. XTALCTL (Crystal Driver Control, 0x4000 000C).....	42
Table 4-5. PLL output frequency settings using 4MHz ROOSC as input.....	45
Register 5-1. WDTCTL (Watchdog Timer Control, 0x4003 0000).....	46
Register 5-2. WDTCDV (Watchdog Timer Count-Down Value, 0x4003 0004).....	47
Register 5-3. WDTCTR (Watchdog Timer Counter, 0x4003 0008).....	47
Register 6-1. RTCCTL (Real Time Clock Control, 0x4004 0000).....	50
Register 6-2. RTCCDV (Real Time Clock Count-Down Value, 0x4004 0004).....	51
Register 6-3. RTCCTR (Real Time Clock Counter, 0x4004 0008).....	51
Register 7-1. GPIOAOUT (GPIO Port A Output, 0x4007 0000).....	53
Register 7-2. GPIOAOUTEN (GPIO Port A Output Enable, 0x4007 0004).....	54
Register 7-3. GPIOADS (GPIO Port A Output Drive Strength, 0x4007 0008).....	54
Register 7-4. GPIOAPU (GPIO Port A Weak Pull Up, 0x4007 000C).....	55
Register 7-5. GPIOAPD (GPIO Port A Weak Pull Down, 0x4007 0010).....	56
Register 7-6. GPIOAIN (GPIO Port A Input, 0x4007 0014).....	56
Register 7-7. GPIOAPSEL (GPIO Port A Peripheral Select, 0x4007 001C).....	57
Register 7-8. GPIOAINTP (GPIO Port A Interrupt Polarity, 0x4007 0020).....	58
Register 7-9. GPIOAINTEN (GPIO Port A Interrupt Enable, 0x4007 0024).....	58
Register 7-10. GPIOAINTF (GPIO Port A Interrupt Flag, 0x4007 0028).....	59
Register 7-11. GPIOAINTM (GPIO Port A Interrupt Mask, 0x4007 002C).....	60
Register 8-1. GPIOBOUT (GPIO Port B Output, 0x4007 0040).....	63
Register 8-2. GPIOBOUTEN (GPIO Port B Output Enable, 0x4007 0044).....	63
Register 8-3. GPIOBDS (GPIO Port B Output Drive Strength, 0x4007 0048).....	64
Register 8-4. GPIOBPU (GPIO Port B Weak Pull Up, 0x4007 004C).....	64
Register 8-5. GPIOBPD (GPIO Port B Weak Pull Down, 0x4007 0050).....	65
Register 8-6. GPIOBIN (GPIO Port B Input, 0x4007 0054).....	65
Register 8-7. GPIOBPSEL (GPIO Port B Peripheral Select, 0x4007 005C).....	65
Register 8-8. GPGPIOBININTP (GPIO Port B Interrupt Polarity, 0x4007 0060).....	66
Register 8-9. GPIOBINTE (GPIO Port B Interrupt Enable, 0x4007 0064).....	67
Register 8-10. GPIOBINTF (GPIO Port B Interrupt Flag, 0x4007 0068).....	67
Register 8-11. GPIOBINTM (GPIO Port B Interrupt Mask, 0x4007 006C).....	68
Register 9-1. GPIOCOUT (GPIO Port C Output, 0x4008 0000).....	71
Register 9-2. GPIOCOUTEN (GPIO Port C Output Enable, 0x4008 0004).....	72
Register 9-3. GPIOCIN (GPIO Port C Input, 0x4008 0018).....	72
Register 9-4. GPIOCINE (GPIO Port C Input Enable, 0x4008 0014).....	73
Register 9-5. GPIOCINTP (GPIO Port C Interrupt Polarity, 0x4008 0020).....	74
Register 9-6. GPIOCINTE (GPIO Port C Interrupt Enable, 0x4008 0024).....	74
Register 9-7. GPIOCINTF (GPIO Port C Interrupt, 0x4008 0028).....	75
Register 9-8. GPIOCINTM (GPIO Port C Interrupt Mask, 0x4008 002C).....	75
Register 10-1. GPIODO (GPIO Port D Output, 0x4008 0040).....	79

Register 10-2. GPIODOUTEN (GPIO Port D Output Enable, 0x4008 0044).....	80
Register 10-3. GPIODDS (GPIO Port D Output Drive Strength, 0x4008 0048).....	80
Register 10-4. GPIODPU (GPIO Port D Weak Pull Up, 0x4008 004C).....	81
Register 10-5. GPIODPD (GPIO Port D Weak Pull Down, 0x4008 0050).....	82
Register 10-6. GPIODIN (GPIO Port D Input, 0x4008 0054).....	82
Register 10-7. GPIODPSEL (GPIO Port D Peripheral Select, 0x4008 005C).....	83
Register 10-8. GPIODINTP (GPIO Port D Interrupt Polarity, 0x4008 0060).....	84
Register 10-9. GPIODINTE (GPIO Port D Interrupt Enable, 0x4008 0064).....	84
Register 10-10. GPIODINTF (GPIO Port D Interrupt, 0x4008 0068).....	85
Register 10-11. GPIODINTM (GPIO Port D Interrupt Mask, 0x4008 006C).....	85
Register 11-1. GPIOEOUT (GPIO Port E Output, 0x4009 0000).....	89
Register 11-2. GPIOEOUTEN (GPIO Port E Output Enable, 0x4009 0004).....	90
Register 11-3. GPIOEDS (GPIO Port E Output Drive Strength, 0x4009 0008).....	90
Register 11-4. GPIOEPU (GPIO Port E Weak Pull Up, 0x4009 000C).....	91
Register 11-5. GPIOEPD (GPIO Port E Weak Pull Down, 0x4009 0010).....	92
Register 11-6. GPIOEIN (GPIO Port E Input, 0x4009 0014).....	92
Register 11-7. GPIOEPSEL (GPIO Port E Peripheral Select, 0x4009 001C).....	93
Register 11-8. GPIOEINTP (GPIO Port E Interrupt Polarity, 0x4009 0020).....	94
Register 11-9. GPIOEINTE (GPIO Port E Interrupt Enable, 0x4009 0024).....	94
Register 11-10. GPIOEINTF (GPIO Port E Interrupt Flag, 0x4009 0028).....	95
Register 11-11. GPIOEINTM (GPIO Port E Interrupt Mask, 0x4009 002C).....	95
Register 12-1. TACTL (Timer A Control, 0x400D 0000).....	100
Register 12-2. TAPRD (Timer A Period, 0x400D 0004).....	101
Register 12-3. TACTR (Timer A Counter, 0x400D 0008).....	101
Register 12-4. TACC0CTRL (Timer A PWMA0 Capture and Compare Control, 0x400D 0040).....	101
Register 12-5. TACC0CTR (Timer A PWMA0 Capture and Compare Counter, 0x400D 0044).....	101
Register 12-6. TACC1CTRL (Timer A PWMA1 Capture and Compare Control, 0x400D 0048).....	102
Register 12-7. TACC1CTR (Timer A PWMA1 Capture and Compare Counter, 0x400D 004C).....	102
Register 12-8. TACC2CTRL (Timer A PWMA2 Capture and Compare Control, 0x400D 0050).....	102
Register 12-9. TACC2CTR (Timer A PWMA2 Capture and Compare Counter, 0x400D 0054).....	103
Register 12-10. TACC3CTRL (Timer A PWMA3 Capture and Compare Control, 0x400D 0058).....	103
Register 12-11. TACC3CTR (Timer A PWMA3 Capture and Compare Counter, 0x400D 005C).....	103
Register 12-12. TACC4CTRL (Timer A PWMA4 Capture and Compare Control, 0x400D 0060).....	103
Register 12-13. TACC4CTR (Timer A PWMA4 Capture and Compare Counter, 0x400D 0064).....	104
Register 12-14. TACC5CTRL (Timer A PWMA5 Capture and Compare Control, 0x400D 0068).....	104
Register 12-15. TACC5CTR (Timer A PWMA5 Capture and Compare Counter, 0x400D 006C).....	104
Register 12-16. TACC6CTRL (Timer A PWMA6 Capture and Compare Control, 0x400D 0070).....	105
Register 12-17. TACC6CTR (Timer A PWMA6 Capture and Compare Counter, 0x400D 0074).....	105
Register 12-18. TACC7CTRL (Timer A PWMA7 Capture and Compare Control, 0x400D 0078).....	105
Register 12-19. TACC7CTR (Timer A PWMA7 Capture and Compare Counter, 0x400D 007C).....	106
Register 12-20. DTGA0CTL (Timer A Dead Time Generator 0 Control, 0x400D 00A0).....	106
Register 12-21. DTGA0LED (Timer A Dead Time Generator 0 Leading Edge Delay, 0x400D 00A4).....	106
Register 12-22. DTGA0TED (Timer A Dead Time Generator 0 Trailing Edge Delay, 0x400D 00A8).....	106
Register 12-23. DTGA1CTL (Timer A Dead Time Generator 1 Control, 0x400D 00B0).....	107
Register 12-24. DTGA1LED (Timer A Dead Time Generator 1 Leading Edge Delay, 0x400D 00B4).....	107
Register 12-25. DTGA1TED (Timer A Dead Time Generator 1 Trailing Edge Delay, 0x400D 00B8).....	107
Register 12-26. DTGA2CTL (Timer A Dead Time Generator 2 Control, 0x400D 00C0).....	107
Register 12-27. DTGA2LED (Timer A Dead Time Generator 2 Leading Edge Delay, 0x400D 00C4).....	108
Register 12-28. DTGA2TED (Timer A Dead Time Generator 2 Trailing Edge Delay, 0x400D 00C8).....	108
Register 12-29. DTGA3CTL (Timer A Dead Time Generator 3 Control, 0x400D 00D0).....	108
Register 12-30. DTGA3LED (Timer A Dead Time Generator 3 Leading Edge Delay, 0x400D 00D4).....	109
Register 12-31. DTGA3TED (Timer A Dead Time Generator 3 Trailing Edge Delay, 0x400D 00D8).....	109
Register 13-1. TBCTL (Timer B Control, 0x400E 0000).....	117
Register 13-2. TBPRD (Timer B Period, 0x400E 0004).....	118

Register 13-3. TBCTR (Timer B Counter, 0x400E 0008).....	118
Register 13-4. TBCC0CTRL (Timer B PWMB0 Capture and Compare Control, 0x400E 0040).....	118
Register 13-5. TBCC0CTR (Timer B PWMB0 Capture and Compare Counter, 0x400E 0044).....	119
Register 13-6. TBCC1CTRL (Timer B PWMB1 Capture and Compare Control, 0x400E 0048).....	119
Register 13-7. TBCC1CTR (Timer B PWMB1 Capture and Compare Counter, 0x400E 004C).....	119
Register 13-8. TBCC2CTRL (Timer B PWMB2 Capture and Compare Control, 0x400E 0050).....	120
Register 13-9. TBCC2CTR (Timer B PWMB2 Capture and Compare Counter, 0x400E 0054).....	120
Register 13-10. TBCC3CTRL (Timer B PWMB3 Capture and Compare Control, 0x400E 0058).....	120
Register 13-11. TBCC3CTR (Timer B PWMB3 Capture and Compare Counter, 0x400E 005C).....	121
Register 13-12. DTGB0CTL (Timer B Dead Time Generator 0 Control, 0x400E 00A0).....	121
Register 13-13. DTGB0LED (Timer B Dead Time Generator 0 Leading Edge Delay, 0x400E 00A4).....	121
Register 13-14. DTGB0TED (Timer B Dead Time Generator 0 Trailing Edge Delay, 0x400E 00A8).....	122
Register 14-1. TCCTL (Timer C Control, 0x400F 0000).....	130
Register 14-2. TCPRD (Timer C Period, 0x400F 0004).....	131
Register 14-3. TCCTR (Timer C Counter, 0x400F 0008).....	131
Register 14-4. TCCC0CTRL (Timer C PWMC0 Capture and Compare Control, 0x400F 0040).....	131
Register 14-5. TCCC0CTR (Timer C PWMC0 Capture and Compare Counter, 0x400F 0044).....	132
Register 14-6. TCCC1CTRL (Timer C PWMC1 Capture and Compare Control, 0x400F 0048).....	132
Register 14-7. TCCC1CTR (Timer C PWMC1 Capture and Compare Counter, 0x400F 004C).....	132
Register 14-8. DTGC0CTL (Timer C Dead Time Generator 0 Control, 0x400F 00A0).....	133
Register 14-9. DTGC0LED (Timer C Dead Time Generator 0 Leading Edge Delay, 0x400F 00A4).....	133
Register 14-10. DTGC0TED (Timer C Dead Time Generator 0 Trailing Edge Delay, 0x400F 00A8).....	133
Register 15-1. TDCTL (Timer D Control, 0x4010 0000).....	141
Register 15-2. TDPRD (Timer D Period, 0x4010 0004).....	142
Register 15-3. TDCTR (Timer D Counter, 0x4010 0008).....	142
Register 15-4. TDCC0CTRL (Timer D PWMD0 Capture and Compare Control, 0x4010 0040).....	142
Register 15-5. TDCC0CTR (Timer D PWMD0 Capture and Compare Counter, 0x4010 0044).....	143
Register 15-6. TDCC1CTRL (Timer D PWMD1 Capture and Compare Control, 0x4010 0048).....	143
Register 15-7. TDCC1CTR (Timer D PWMD1 Capture and Compare Counter, 0x4010 004C).....	143
Register 15-8. DTGD0CTL (Timer D Dead Time Generator 0 Control, 0x4010 00A0).....	144
Register 15-9. DTGD0LED (Timer D Dead Time Generator 0 Leading Edge Delay, 0x4010 00A4).....	144
Register 15-10. DTGD0TED (Timer D Dead Time Generator 0 Trailing Edge Delay, 0x4010 00A8).....	144
Register 16-1. FLASHLOCK (FLASH Lock, 0x4002 0000).....	151
Register 16-2. FLASHCTL (FLASH Control and Status, 0x4002 0004).....	152
Register 16-3. FLASHPAGE (FLASH Page Selector, 0x4002 0008).....	152
Register 16-4. FLASHPERASE (FLASH Page Erase, 0x4002 0014).....	153
Register 16-5. SWDACCESS (SDW Access Status, 0x4002 0024).....	153
Register 16-6. FLASHWSTATE (FLASH Access Wait State, 0x4002 0028).....	153
Register 16-7. FLASHBWRITE (Buffered FLASH Write, 0x4002 002C).....	153
Register 16-8. FLASHBWDATA (Buffered FLASH Write Data, 0x4002 0030).....	154
Register 17-1. EMUXCTL (ADC external MUX control register 0x4015 0000).....	159
Register 17-2. EMUXDATA (EMUX data register 0x4015 0004).....	160
Register 17-3. ADCCTL (ADC control register 0x4015 0008).....	161
Register 17-4. ADCCR (ADC conversion result register 0x4015 000C).....	161
Register 17-5. ADCINT (ADC Interrupt register 0x4015 0010).....	162
Register 17-6. AS0CTL (Auto Sequencer 0 control register 0x4015 0040).....	163
Register 17-7. AS0S0 (Auto sequencer 0-sample 0 control 0x4015 0044).....	164
Register 17-8. AS0R0 ( Auto sequencer 0-sample 0 result register 0x4015 0048).....	164
Register 17-9. AS0S1 (Auto sequencer 0-sample 1 control 0x4015 004C).....	164
Register 17-10. AS0R1 ( Auto sequencer 0-sample 1 result register 0x4015 0050).....	165
Register 17-11. AS0S2 (Auto sequencer 0-sample 2 control 0x4015 0054).....	165
Register 17-12. AS0R2 ( Auto sequencer 0-sample 2 result register 0x4015 0058).....	165
Register 17-13. AS0S3 (Auto sequencer 0-sample 3 control 0x4015 005C).....	166
Register 17-14. AS0R3 ( Auto sequencer 0-sample 3 result register 0x4015 0060).....	166

Register 17-15. AS0S4 (Auto sequencer 0-sample 4 control 0x4015 0064).....	166
Register 17-16. AS0R4 ( Auto sequencer 0-sample 4 result register 0x4015 0068).....	167
Register 17-17. AS0S5 (Auto sequencer 0-sample 5 control 0x4015 006C).....	167
Register 17-18. AS0R5 ( Auto sequencer 0-sample 5 result register 0x4015 0070).....	167
Register 17-19. AS0S6 (Auto sequencer 0-sample 6 control 0x4015 0074).....	168
Register 17-20. AS0R6 ( Auto sequencer 0-sample 6 result register 0x4015 0078).....	168
Register 17-21. AS0S7 (Auto sequencer 0-sample 7 control 0x4015 007C).....	168
Register 17-22. AS0R7 ( Auto sequencer 0-sample 7 result register 0x4015 0080).....	169
Register 17-23. AS1CTL (Auto Sequencer 1 control register 0x4015 0100).....	169
Register 17-24. AS1S0 (Auto sequencer 1-sample 0 control 0x4015 0104).....	170
Register 17-25. AS1R0 ( Auto sequencer 1-sample 0 result register 0x4015 0108).....	170
Register 17-26. AS1S1 (Auto sequencer 1-sample 1 control 0x4015 010C).....	171
Register 17-27. AS1R1 ( Auto sequencer 1-sample 1 result register 0x4015 0110).....	171
Register 17-28. AS1S2 (Auto sequencer 1-sample 2 control 0x4015 0114).....	171
Register 17-29. AS1R2 ( Auto sequencer 1-sample 2 result register 0x4015 0118).....	172
Register 17-30. AS1S3 (Auto sequencer 1-sample 3 control 0x4015 011C).....	172
Register 17-31. AS1R3 ( Auto sequencer 1-sample 3 result register 0x4015 0120).....	172
Register 17-32. AS1S4 (Auto sequencer 1-sample 4 control 0x4015 0124).....	173
Register 17-33. AS1R4 ( Auto sequencer 1-sample 4 result register 0x4015 0128).....	173
Register 17-34. AS1S5 (Auto sequencer 1-sample 5 control 0x4015 012C).....	173
Register 17-35. AS1R5 ( Auto sequencer 1-sample 5 result register 0x4015 0130).....	174
Register 17-36. AS1S6 (Auto sequencer 1-sample 6 control 0x4015 0134).....	174
Register 17-37. AS1R6 ( Auto sequencer 1-sample 6 result register 0x4015 0138).....	174
Register 17-38. AS1S7 (Auto sequencer 1-sample 7 control 0x4015 013C).....	175
Register 17-39. AS1R7 ( Auto sequencer 1-sample 7 result register 0x4015 0140).....	175
Register 18-1. I2CCFG (I2C Configuration, 0x401B 0000).....	182
Register 18-2. I2CSTATUS (I2C Interrupt Status, 0x401B 0004).....	182
Register 18-3. I2CIE (I2C Interrupt Enable, 0x401B 0008).....	184
Register 18-4. I2CMCTRL (I2C Master Access Control, 0x401B 0030).....	184
Register 18-5. I2CMRXDATA (I2C Master Receive Data, 0x401B 0034).....	185
Register 18-6. I2CMTXDATA (I2C Master Transmit Data, 0x401B 0038).....	185
Register 18-7. I2CBAUD (I2C Baud Rate, 0x401B 0040).....	185
Register 18-8. I2CSLRXDATA (I2C Slave Receive Data, 0x401B 0070).....	185
Register 18-9. I2CSLTXDATA (I2C Slave Transmit Data, 0x401B 0074).....	186
Register 18-10. I2CADDR (I2C Slave Address, 0x401B 0074).....	186
Table 18-11. I2CBAUD settings for different HCLK.....	187
Register 19-1. UARTRTX (UART Receive/Transmit FIFO, 0x401D 0000).....	191
Register 19-2. UARTIER (UART Interrupt Enable, 0x401D 0004).....	192
Register 19-3. UARTIIR (UART Interrupt Identification, 0x401D 0008).....	192
Register 19-4. UARTRCR (UART Line Control, 0x401D 000C).....	193
Register 19-5. UARTRMCR (UART Modem Control, 0x401D 0010).....	193
Register 19-6. UARTRLSR (UART Line Status, 0x401D 0014).....	193
Register 19-7. UARTRSP (UART Scratch Pad, 0x401D 001C).....	194
Register 19-8. UARTRFCTL2 (FIFO Control, 0x401D 0020).....	194
Register 19-9. UARTIER2 (UART Interrupt Enable, 0x401D 0024).....	195
Register 19-10. UARTRDL_L2 (UART Divisor Latch Low Byte, 0x401D 0028).....	195
Register 19-11. UARTRDL_H2 (UART Divisor Latch High Byte, 0x401D 002C).....	195
Register 19-12. UARTRFD_F (UART Fractional Divisor Value, 0x401D 0038).....	195
Register 19-13. UARTRSTAT (UART FIFO Status, 0x401D 0040).....	195
Register 19-14. UART Divisor Settings for 50 MHz HCLK.....	198
Register 20-1. SOCBCTL (SOC Bus Bridge Control, 0x4020 0000).....	200
Register 20-2. SOCBCFG (SOC Bus Bridge Configuration, 0x4020 0004).....	200
Register 20-3. SOCBCLK (SOC Bus Bridge Clock Divider, 0x4020 0008).....	201
Register 20-4. SOCBSTAT (SOC Bus Bridge Status, 0x4020 0014).....	201

Register 20-5. SOCBSTAT (SOC Bus Bridge Chip Select Steering, 0x4020 0018).....	202
Register 20-6. SOCBD (SOC Bus Bridge Data, 0x4020 001C).....	203
Register 20-7. SOCBINT_EN (SOC Bus Bridge Interrupt Enable, 0x4020 0020).....	203
Register 21-1. SPICTL (SPI Control, 0x4021 0000).....	206
Register 21-2. SPICFG (SPI Configuration, 0x4021 0004).....	207
Register 21-3. SPICLKDIV (SPI Clock Divider, 0x4021 0008).....	208
Register 21-4. SPISTAT (SPI Status, 0x4021 0014).....	208
Register 21-5. SPICSSSTR (SPI Chip Select Steering, 0x4021 0018).....	210
Register 21-6. SPID (SPI Data, 0x4021 001C).....	211
Register 21-7. SPIINT_EN (SPI Interrupt Enable, 0x4021 0020).....	211
Register 22-1. SYSSTAT (System Status, 0x00).....	217
Register 22-2. DEVID (Device Identification, 0x08).....	218
Register 22-3. VERID (Version Identification, 0x09).....	218
Register 22-4. PWRCTL (Power Manager Control, 0x10).....	218
Register 22-5. PWRSTAT (Power Manager Status, 0x11h, Persistent In Hibernate Mode).....	219
Register 22-6. PSTATSET (Power Manager Setting, 0x12).....	219
Register 22-7. IMOD (Current Modulation, 0x13).....	220
Register 22-8. SCFG (Switching Supply Configuration, 0x14).....	220
Register 22-9. SCFG2 (Switching Supply Configuration 2, 0x15).....	220
Register 23-1. SOC.SOC.CFGAIO0 (AIO0 Configuration, SOC 0x20).....	223
Register 23-2. SOC.CFGAIO1 (AIO1 Configuration, SOC 0x21).....	223
Register 23-3. SOC.SOC.CFGAIO2 (AIO2 Configuration, SOC 0x22).....	225
Register 23-4. SOC.CFGAIO3 (AIO3 Configuration, SOC 0x23).....	225
Register 23-5. SOC.SOC.CFGAIO4 (AIO4 Configuration, SOC 0x24).....	227
Register 23-6. SOC.CFGAIO5 (AIO5 Configuration, SOC 0x25).....	227
Register 23-7. SOC.CFGAIO6 (AIO6 Configuration, SOC 0x26).....	229
Register 23-8. SOC.CFGAIO7 (AIO7 Configuration, SOC 0x27).....	230
Register 23-9. SOC.CFGAIO8 (AIO8 Configuration, SOC 0x28).....	231
Register 23-10. SOC.CFGAIO9 (AIO9 Configuration, SOC 0x29).....	232
Register 23-11. SOC.SIGSET (Signal Manager Configuration, SOC 0x2A).....	233
Register 23-12. SOC.HPDAC (HPDAC Setting, SOC 0x2B).....	233
Register 23-13. SOC.LPDAC0 (LPDAC Setting [9:2], SOC 0x2C).....	233
Register 23-14. SOC.LPDAC1 (LPDAC Setting [1:0], SOC 0x2D).....	233
Register 23-15. SOC.ADCSCAN (ADCSCAN Configuration, SOC 0x2E).....	234
Register 23-16. SOC.ADCIN1 (AD Mux Selector, SOC 0x2F).....	234
Register 23-17. SOC.PROTINTM (Protection Interrupt Enable, SOC 0x30).....	234
Register 23-18. SOC.PROTSTAT (Protection Interrupt, SOC 0x31).....	235
Register 23-19. SOC.DOUTSIG0 (AIO Digital Output, SOC 0x32).....	235
Register 23-20. SOC.DOUTSIG1 (AIO Digital Output, SOC 0x33).....	236
Register 23-21. SOC.DINSIG0 (AIO Digital Input, SOC 0x34).....	236
Register 23-22. SOC.DINSIG1 (AIO Digital Input 1, SOC 0x35).....	237
Register 23-23. SOC.SIGINTM (AIO6,7,8,9 Interrupt Enable, SOC 0x36).....	237
Register 23-24. SOC.SIGINTF (AIO6,7,8,9 Interrupt, SOC 0x37).....	238
Register 23-25. SOC.ENSIG (Signal Manager Control SOC 0x38).....	238
Register 23-26. EMUX Packet Structure.....	265
Register 24-1. SOC.CFGDRV0 (Driver Configuration 0, SOC 0x60).....	268
Register 24-2. SOC.CFGDRV1 (Driver Configuration 1, SOC 0x61).....	268
Register 24-3. SOC.CFGDRQ6 (OHI6 Configuration, SOC 0x62).....	269
Register 24-4. SOC.CFGDRQ7 (OHI7 Configuration, SOC 0x63).....	269
Register 24-5. SOC.DOUTDRV (OHI6, OHI7 Output, SOC 0x64).....	270
Register 24-6. SOC.DINDRV (OHI6, OHI7 Input, SOC 0x65).....	270
Register 24-7. SOC.ENDRV (Application Specific Power Driver Control, SOC 0x66).....	270
Register 24-8. SOC.EMBBM (High-Side, Low-Side Break Before Make Control, SOC 0x67).....	271

## LIST OF FIGURES

Figure 2-1. Memory Map.....	25
Figure 4-1. System Clock Control.....	43
Figure 5-1. WDT.....	48
Figure 6-1. GPT.....	52
Figure 7-1. GPIO Port A.....	61
Figure 8-1. GPIO Port B.....	69
Figure 9-1. GPIO Port C.....	77
Figure 10-1. GPIO Port D.....	87
Figure 11-1. GPIO Port E.....	97
Figure 12-1. Timer A.....	110
Figure 12-2. PWMA[x] and PWMA[x+4] Example Using Timer A Up Mode and Up/Down Mode.....	113
Figure 12-3. CA[x] and CA[x+4] Capture Example.....	113
Figure 12-4. DTGAX Bypass Example.....	114
Figure 12-5. DTGAX Bypass and Inverting LS Example.....	115
Figure 12-6. DTGAX LED and TED Example.....	115
Figure 12-7. DTGAX LED and TED with On Time Preservation Example.....	116
Figure 13-1. Timer B.....	123
Figure 13-2. PWMB0 and PWMB1 Example Using Timer B Up Mode and Up/Down Mode.....	126
Figure 13-3. CB0 and CB1 Capture Example.....	126
Figure 13-4. DTGB0 Bypass Example.....	127
Figure 13-5. DTGB0 Bypass and Inverting LS Example.....	128
Figure 13-6. DTGB0 LED and TED Example.....	128
Figure 13-7. DTGB0 LED and TED with On Time Preservation Example.....	129
Figure 14-1. Timer C.....	134
Figure 14-2. PWMC0 and PWMC1 Example Using Timer C Up Mode and Up/Down Mode.....	137
Figure 14-3. CC0 and CC1 Capture Example.....	137
Figure 14-4. DTGC0 Bypass Example.....	138
Figure 14-5. DTGC0 Bypass and Inverting LS Example.....	139
Figure 14-6. DTGC0 LED and TED Example.....	139
Figure 14-7. DTGC0 LED and TED with On Time Preservation Example.....	140
Figure 15-1. Timer D.....	145
Figure 15-2. PWMD0 and PWMD1 Example Using Timer D Up Mode and Up/Down Mode.....	147
Figure 15-3. CD0 and CD1 Capture Example.....	148
Figure 15-4. DTGD0 Bypass Example.....	149
Figure 15-5. DTGD0 Bypass and Inverting LS Example.....	149
Figure 15-6. DTGD0 LED and TED Example.....	150
Figure 15-7. DTGD0 LED and TED with On Time Preservation Example.....	150
Figure 16-1. FLASH Memory Controller.....	155
Figure 17-1. ADC, EMUX, ASC0, ASC1.....	176
Figure 17-2. ADC Conversion (Single Shot).....	177
Figure 17-3. ADC Conversion (Repeat Mode).....	177
Figure 17-4. ASCx, ADCCTL.ADCMODE = 001b, 010b, 100b, 101b.....	178
Figure 17-5. ASCx, ADCCTL.ADCMODE = 011b, 110b.....	178
Figure 17-6. ASCx, ADCCTL.ADCMODE = 111b.....	179
Figure 17-7. ASxSy Sample with ASxSy.EMUXS = 00b and ASxSy.DELAY = 11b.....	179
Figure 17-8. ASxSy Sample with ASxSy.EMUXS = 01b and ASxSy.DELAY = 11b.....	180
Figure 17-9. ASxSy Sample with ASxSy.EMUXS = 10b and ASxSy.DELAY = 11b.....	180
Figure 17-10. ASCx, 8 samples, No Collision.....	180
Figure 17-11. ASCx 8 samples, Collision.....	181
Figure 17-12. ASC0 8 samples, ASC1 4 samples, Collision.....	181
Figure 18-1. I2C.....	187

Figure 18-2. I2C Master Read Transaction.....	188
Figure 18-3. I2C Master Read Waveforms.....	189
Figure 19-1. UART.....	197
Figure 20-1. SOC Bridge.....	204
Figure 20-2. Single Read from SOC Bridge.....	205
Figure 20-3. Single Write to SOC Bridge.....	205
Figure 21-1. SPI.....	212
Figure 21-2. SPI clock polarity and phase.....	213
Figure 21-3. SPIMOSI early transmit in master mode.....	214
Figure 21-4. SPIMISO early transmit in slave mode.....	214
Figure 21-5. SPICSt.....	215
Figure 23-1. Configurable Analog Front End.....	239
Figure 23-2. AIO1, AIO0.....	240
Figure 23-3. AIO3, AIO2.....	243
Figure 23-4. AIO5, AIO4.....	246
Figure 23-5. AIO6.....	249
Figure 23-6. AIO7.....	253
Figure 23-7. AIO8.....	257
Figure 23-8. AIO9.....	261
Figure 23-9. EMUX.....	265
Figure 23-10. EMUX Timing.....	266
Figure 24-1. Application Specific Power Driver.....	272
Figure 24-2. ENHS1, ENLS1 Protection.....	273
Figure 24-3. DRL0.....	274
Figure 24-4. DRL1.....	275
Figure 24-5. DRL2.....	276
Figure 24-6. DRH3.....	277
Figure 24-7. DRH4.....	278
Figure 24-8. DRH5.....	279
Figure 24-9. OHI6.....	280
Figure 24-10. OHI7.....	281
Figure 25-1. Cortex-M0 implementation.....	282
Figure 25-2. Core Registers.....	285
Figure 25-3. PSR.....	286
Figure 25-4. PRIMASK.....	289
Figure 1-6. CONTROL.....	289
Figure 25-5. CONTROL.....	289
Figure 25-6. Memory Map.....	292
Figure 25-7. Memory Ordering Restrictions.....	293
Figure 25-8. Little Endian Format.....	296
Figure 25-9. Vector Table.....	299
Figure 25-10. Exception Entry Stack Contents.....	301
Figure 25-11. ASR #3.....	309
Figure 25-12. LSR #3.....	310
Figure 25-13. LSL #3.....	311
Figure 25-14. ROR #3.....	311
Figure 25-15. ISER.....	345
Figure 25-16. ICER.....	346
Figure 25-17. ISPR.....	346
Figure 25-18. ICPR.....	347
Figure 25-19. IPR.....	348
Figure 25-20. CPUID.....	351
Figure 25-21. ICSR.....	352
Figure 25-22. AIRCR.....	353

---

Figure 25-23. SCR.....	354
Figure 25-24. CCR.....	355
Figure 25-25. SHPR2.....	356
Figure 25-26. SHPR3.....	356
Figure 25-27. SYST_CSR.....	358
Figure 25-28. SYST_RVR.....	358
Figure 25-29. SYST_CVR.....	359
Figure 25-30. SYST_CALIB.....	359

## 1. STYLES AND FORMATTING CONVENTIONS

### 1.1. Overview

This chapter describes formatting and styles used through the document.

### 1.2. Number Representation

Numbers in a base other than decimal have a prefix or postfix as indicator. All numbers use little endian formatting, most significant bit/digit is to the left. Digits for binary and hexadecimal representation are grouped with a single space every four digits to improve readability. Binary numbers use “b” as postfix, hexadecimal numbers use “0x” as prefix.

For example 1011b binary = 0xB hexadecimal = 11 decimal.

### 1.3. Formatting Styles

TYPE	EXAMPLE	DESCRIPTION
Register Name	<b>RTCCTL</b>	Register names use capital letter and bold formatting.
Register Bit(s)	<b>RTCCTL.RTCCLKDIV</b>	Register bits are always represented with the register name separated with a period
Function selected by Register bit(s)	<b>[RTCCTL.RTCCLKDIV]</b>	Within text blocks, functions selected with a register bit setting are set in brackets. For example <b>[RTCCTL.RTCCLKDIV]</b> means divider settings /2 to /65536.
Pin Function	XIN	Pin functions use capital letters
Formulas	CLK = FCLK / DIV	Formulas use Teletype font.
Links	<a href="#">Number Representation</a>	Clickable Links are underlined and blue
CPU Mnemonic	MRS	CPU Mnemonic use Teletype font.
Operands	{ <i>Rd</i> , } <i>Rn</i> , <i>Rm</i>	Operands use Italic
Code examples	B loopA	Code examples use Teletype font.

## 2. MEMORY AND REGISTER MAP

### 2.1. Memory Map

Figure 2-1. Memory Map

