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PAC5232 Data Sheet

Power Application Controller®

Multi-Mode Power Manager™

Configurable Analog Front End™

Application Specific Power Drivers™

ARM© Cortex®-M0 Controller Core

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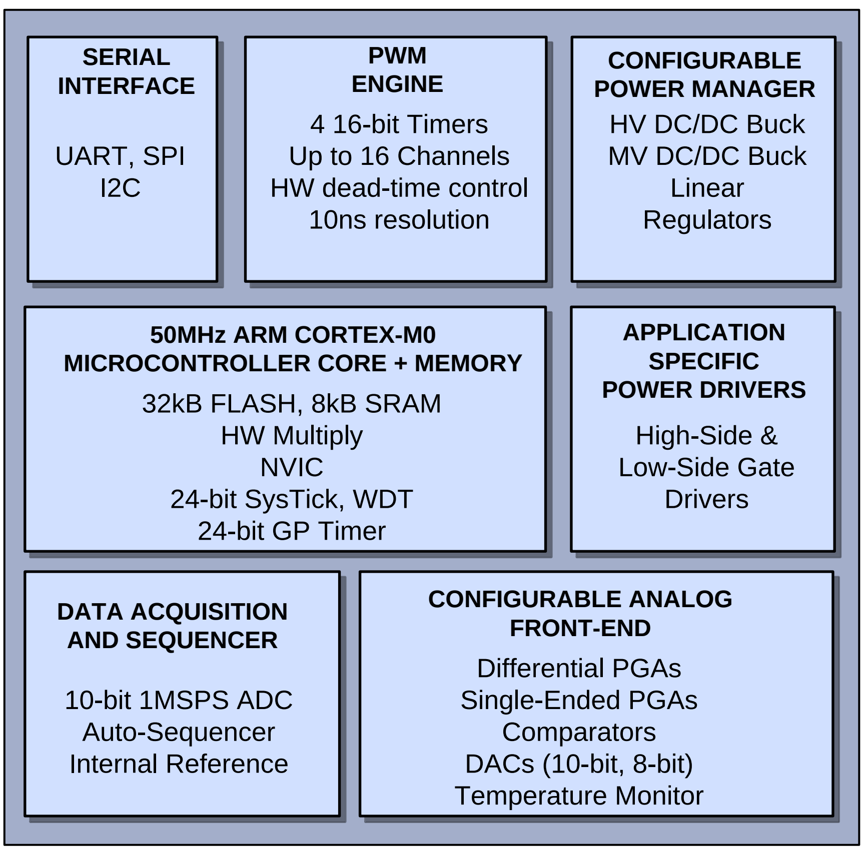
1 GENERAL DESCRIPTION

The PAC5232 is a Power Application Controller® (PAC) product that is optimized for high-speed motor control and driving. The PAC5232 integrates a 50MHz ARM Cortex®-M0 32-bit microcontroller core with a highly-configurable Power manager, Active-Semi's proprietary and patent-pending Configurable Analog Front-End™ and Application Specific Power Drivers™ to form the most compact microcontroller-based power and motor control solution available.

The PAC5232 microcontroller features 32kB of embedded FLASH and 8kB of SRAM memory, a 1MSPS analog-to-digital converter (ADC) with programmable auto-sequencer, 3.3V/5V IO, flexible clock control system, PWM and general-purpose timers and several serial communications interfaces.

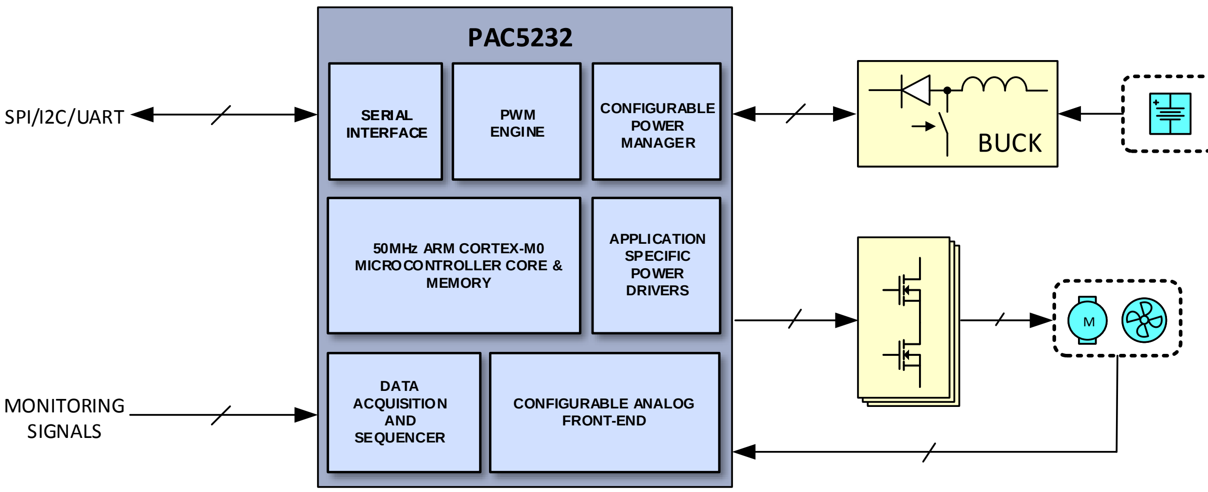
The Configurable Power Manager (CPM) provides "all-in-one" efficient power management solution for multiple types of power sources. It features a configurable high-voltage switching supply controller capable of operating a buck converter, a configurable medium-voltage switching regulator, and four linear regulated voltage supplies. The Application Specific Power Drivers (ASPD) are 180V power drivers designed for half bridge, H-bridge, 3-phase, and general purpose driving. The Configurable Analog Front End (CAFE) comprises differential programmable gain amplifiers, single-ended programmable gain amplifiers, comparators, digital-to-analog converters, and I/Os for programmable and inter-connectible signal sampling, feedback amplification, and sensor monitoring of multiple analog input signals.



The PAC5232 is available in a 51-pin, 8x8mm TQFN package.

2 PAC® FAMILY APPLICATIONS

- Garden Tools
- Telecom Fans
- Light Electric Vehicle
- Battery Powered Motor Controllers and Drivers from 48VC – 120VDC



3 PRODUCT SELECTION SUMMARY

PART NUMBER	PIN PKG	POWER MANAGER		CONFIGURABLE ANALOG FRONT END					APPLICATION SPECIFIC POWER DRIVERS			MCU					APPLICATION
		INPUT VOLTAGE	DC/DC	DIFF-PGA	PGA	COMPARATOR	DAC	ADC CHANNEL	VBST/VSRC	POWER DRIVER	PWM CHANNEL	SPEED (MHz)	FLASH (kB)	SRAM (kB)	GPIO	SERIAL COMM	
PAC5232	51L 8x8 QFN	25V-160V	Y	3	4	10	2	9	180V	3 LS (2A) 3 HS (2A)	6@VP 6@VCCIO	50	32	8	29	UART SPI I2C SWD	3 half-bridge 3 phase control BEMF Trapezoidal or FOC

Notes: DIFF-PGA = differential programmable gain amplifier; HS = high-side, LS = low-side, PGA = programmable gain amplifier, VSRC = Bootstrap Voltage Source

4 ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING
PAC5232QX	-40°C to 105°C	51L 8x8 QFN	51 + Exposed Pad	Tray

5 FEATURES

5.1 Feature Overview

- **Configurable Power Manager**
  - High-voltage buck switching supply controller
    - Input Voltage: 25V – 160V
    - Configurable Output Voltage: 12V or 15V
  - 5V medium-voltage switching supply regulator
  - 3 Linear regulators with power and hibernate management
  - Power and temperature monitor, warning, fault detection
- **Proprietary Configurable Analog Front-End**
  - 10 Analog Front-End IO pins
  - 3 Differential Programmable Gain Amplifiers
  - 4 Single-ended Programmable Gain Amplifiers
  - Programmable Over-Current Protection
  - 10 Comparators
  - 2 10-bit DACs
- **Proprietary Application Specific Power Drivers**
  - 3 180V high-side gate drivers with 2A gate driving capability
  - 3 low-side gate drivers with 2A gate driving capability
  - Configurable propagation delay and fault protection
- **3.3V I/Os**
  - 2 general-purpose I/Os with tri-state and dedicated analog input to ADC
- **True 5V I/Os**
  - 11 general-purpose I/Os with tri-state, pull-up, pull-down and dedicated I/O supply
  - Configurable as true 5V or 3.3V I/Os
- **50MHz ARM© Cortex®-M0 32-bit Microcontroller Core**
  - Single-cycle 32-bit x 32-bit hardware multiplier
  - Integrated sleep and deep sleep modes
  - Nested Vectored Interrupt Controller (NVIC) with 20 Interrupts with 3 levels of priority
  - 24-Bit SysTick Timer
  - Wake-up Interrupt Controller (WIC) allowing power-saving sleep modes
  - Clock-gating allowing low-power operation
- **Memory**
  - 32kB FLASH
  - 8kB SRAM
- **Analog to Digital Converter (ADC)**
  - 10-bit resolution
  - 1MSPS
  - Dual Programmable ADC Auto-Sequencers
- **Flexible clock and PLL from internal 1.25% oscillator, ring oscillator, external clock or crystal**
- **9 Timing Generators**
  - Four 16-bit timers with up to 16 PWM/CC blocks and 7 independent dead-time controllers
  - 24-bit watchdog timer
  - 4s or 8s watchdog timer
  - 24-bit real time clock
  - 24-bit SysTick timer
  - Wake-up timer for sleep modes from 0.125s to 8s
- **SPI, I2C, and UART serial communication interfaces**
- **SWD debug interface with interface disable function**

6 ABSOLUTE MAXIMUM RATINGS

The table below shows the absolute maximum ratings for this device.

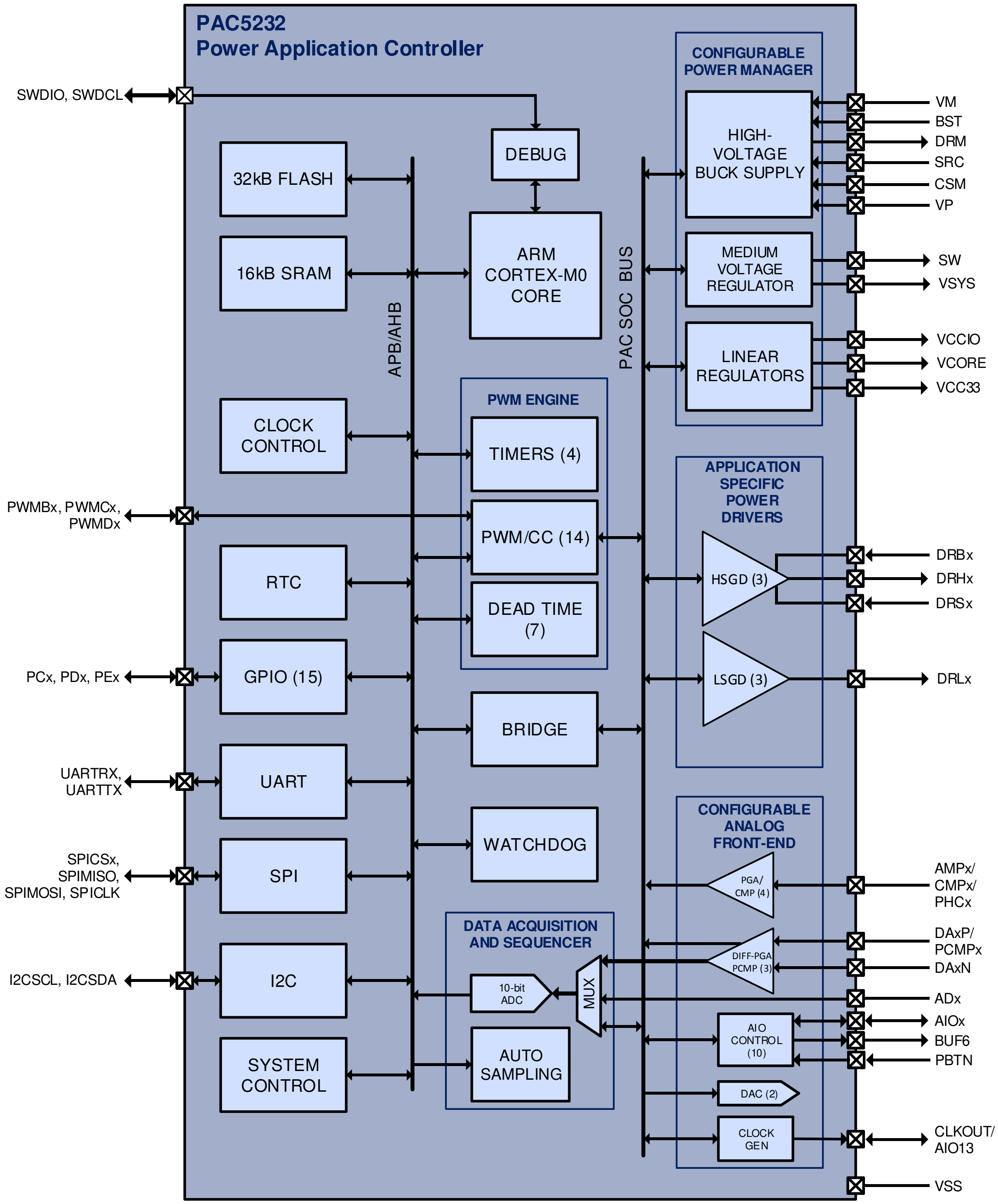
To prevent damage to the device, do not exceed these limits. Exposure to the absolute maximum rating conditions for long periods of time may affect device reliability.

The device is not guaranteed to function properly outside of the operating conditions.

PARAMETER		VALUE	UNIT
VM to VSS		-0.3 to 160	V
BST to VSS		-0.3 to 180	V
BST to SRC		-0.3 to 20	V
SRC to VSS		-10 to VM + 15	V
DRM to SRC		-0.3 to BST + 0.3	V
VP to VSS		-0.3 to 20	V
SW to VSS		-0.3 to V_P + 0.3	V
CSM to VP		-0.3 to 0.3	V
VSYS to VSS		-0.3 to 6	V
AIO<9:7>, AIO<5:0>, VCCIO, AIO6 to VSS		-0.3 to V_{SYS} + 0.3	V
PD<x>, PE<x> to VSS		-0.3 to V_{CCIO} + 0.3	V
PC<x> to VSS		-0.3 to V_{CC33} + 0.3	V
VCC33 to VSS		-0.3 to 4.1	V
VCORE to VSS		-0.3 to 2.5	V
DRL0, DRL1, DRL2 to VSS		-0.3 to V_P + 0.3	V
DRB3, DRB4, DRB5 to VSS		-0.3 to 180	V
DRS3, DRS4, DRS5 to VSS		-10 to VM + 15	V
DRB3 to DRS3, DRB4 to DRS4, DRB5 to DRS5		-0.3 to 20	V
DRH3 to DRS3, DRH4 to DRS4, DRH5 to DRS5		-0.3 to V_{DRBx} + 0.3	V
VSS RMS Current[1]		0.2	A_{RMS}
Operating temperature range		-40 to 105	°C
Electrostatic Discharge (ESD)	Human body model (JEDEC)	2	kV
	Charge device model (JEDEC)	1	kV

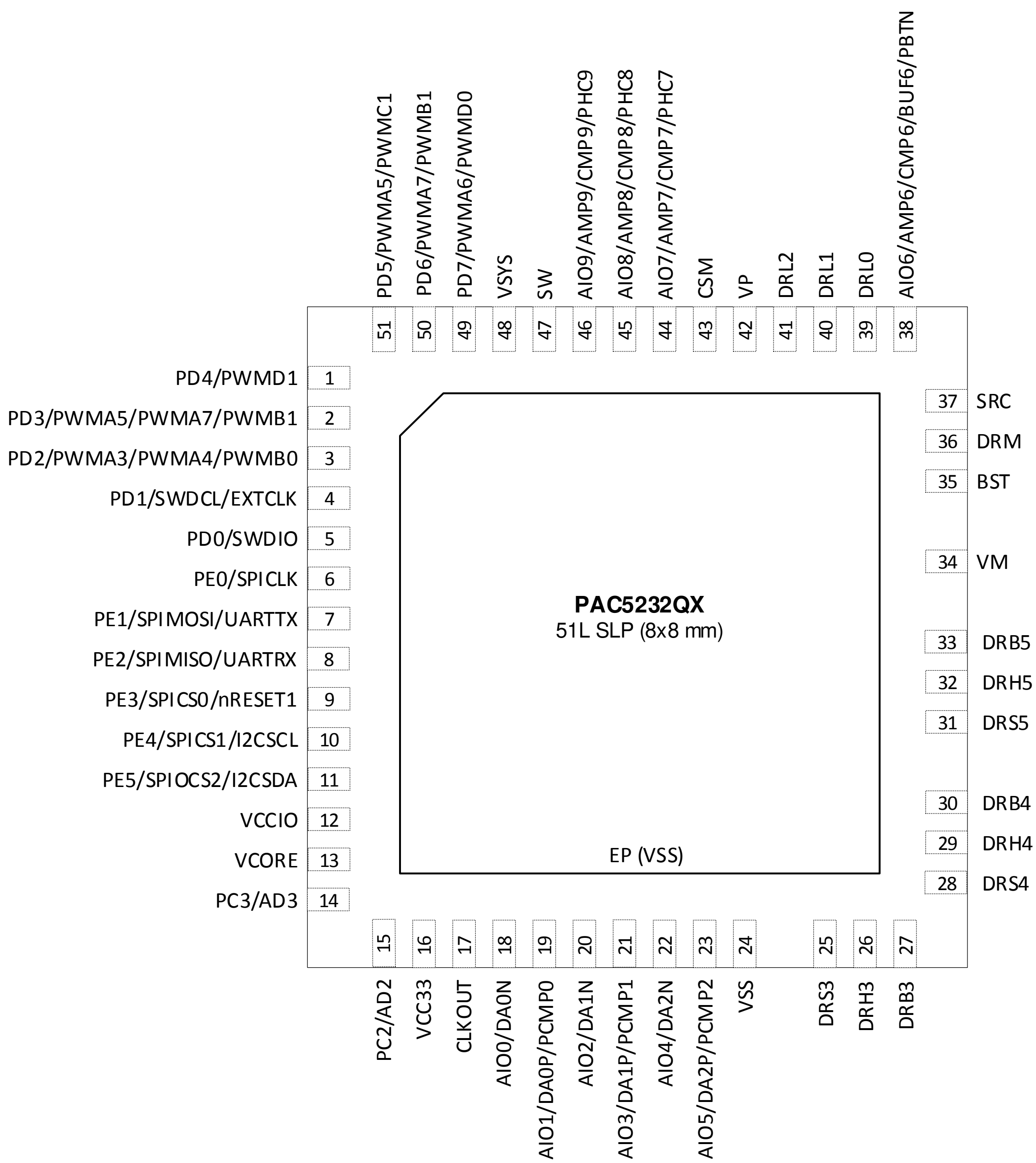
[1] Peak current may be 10 times higher than the RMS value for pulses shorter than 10µs.

7 ARCHITECTURAL BLOCK DIAGRAM



8 PIN CONFIGURATION

8.1 PAC5232QX Pin Configuration (51L SLP 8x8 mm Package)



9 PIN DESCRIPTION

9.1 Power and Ground Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
VCCIO	12	Power	Internally generated digital I/O 3.3V power supply. Connect a 2.2µF or higher value ceramic capacitor from V_{CCIO} to V_{SSA}.
VCORE	13	Power	Internally generated digital I/O 1.8V power supply. Connect a 2.2µF or higher value ceramic capacitor from V_{CC18} to V_{SSA}.
VCC33	16	Power	Internally generated 3.3V power supply. Connect to a 2.2µF or higher value ceramic capacitor from V_{CC33} to V_{SSA}.
VSS	24	Power	Ground.
VM	34	Power	High-Voltage Buck Regulator supply controller input. Connect a high value electrolytic capacitor in parallel with a 0.1µF ceramic capacitor from VM to VSS. This pin requires good capacitive bypass to V_{SS}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin.
BST	35	Power	High-Voltage Buck Regulator bootstrap input. Connect a 2.2µF or higher value ceramic capacitor from BST to SRC with a shorter than 10mm trace from the pin.
DRM	36	Power	High-Voltage Buck Regulator Switching supply driver output. Connect to the gate of the external power N-channel MOSFET.
SRC	37	Power	High-Voltage Buck Regulator Source. Connect to the source of the high-side power MOSFET of the high-voltage buck regulator.
VP	42	Power	Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 10µF ceramic capacitor in parallel with a 100µF aluminum capacitor from V_P to V_{SS} for voltage loop stabilization. If the switching frequency of the HV-BUCK is >= 200kHz, then the 100µF aluminum capacitor can be replaced with 47µF, but the efficiency will be worse. This pin requires good capacitive bypassing to V_{SS}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin.
CSM	43	Power	High-Voltage Buck Regulator Switching supply current sense input. Connect to the positive side of the current sense resistor.
SW	47	Power	Switch node for the medium-voltage buck regulator.
VSYS	48	Power	5V System power supply. Connect to a 22µF/6.3V (20%) or higher ceramic capacitor from V_{SYS} to V_{SS}.
EP (VSS)	EP	Power	Exposed pad. Must be connected to V_{SS} in a star ground configuration. Connect to a large PCB copper area for power dissipation heat sinking.

9.2 Signal Manager Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
CLKOUT	17	CLKOUT	I/O	Low-frequency clock reference output (250Hz – 2kHz), or GPIO.
AIO0	18	AIO0	I/O	Analog front end I/O 0.
		DA0N	Analog	Differential PGA 0 negative input.
AIO1	19	AIO1	I/O	Analog front end I/O 1.
		DA0P	Analog	Differential PGA 0 positive input.
AIO2	20	AIO2	I/O	Analog front end I/O 2.
		DA1N	Analog	Differential PGA 1 negative input.
AIO3	21	AIO3	I/O	Analog front end I/O 3.

		DA1P	Analog	Differential PGA 1 positive input.
AIO4	22	AIO4	I/O	Analog front end I/O 4.
		DA2N	Analog	Differential PGA 2 negative input.
AIO5	23	AIO5	I/O	Analog front end I/O 5.
		DA2P	Analog	Differential PGA 2 positive input.
AIO6	38	AIO6	I/O	Analog front end I/O 6.
		AMP6	Analog	PGA input 6.
		CMP6	Analog	Comparator input 6.
		BUF6	Analog	Buffer output 6.
		PBTN	Analog	Push button input.
AIO7	44	AIO7	I/O	Analog front end I/O 7.
		AMP7	Analog	PGA input 7.
		CMP7	Analog	Comparator input 7.
		PHC7	Analog	Phase comparator input 7.
AIO8	45	AIO8	I/O	Analog front end I/O 8.
		AMP8	Analog	PGA input 8.
		CMP8	Analog	Comparator input 8.
		PHC8	Analog	Phase comparator input 8.
AIO9	46	AIO9	I/O	Analog front end I/O 9.
		AMP9	Analog	PGA input 9.
		CMP9	Analog	Comparator input 9.
		PHC9	Analog	Phase comparator input 9.

9.3 Driver Manager Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
DRS3	25	Analog	High-side gate driver source 3.
DRH3	26	Analog	High-side gate driver 3.
DRB3	27	Analog	High-side gate driver bootstrap 3. Connect a 1µF or higher value ceramic capacitor from DRB3 to DRS3 with a 10mm or shorter trace from the pin.
DRS4	28	Analog	High-side gate driver source 4.
DRH4	29	Analog	High-side gate driver 4.
DRB4	30	Analog	High-side gate driver bootstrap 4. Connect a 1µF or higher value ceramic capacitor from DRB4 to DRS4 with a 10mm or shorter trace from the pin.
DRS5	31	Analog	High-side gate driver source 5.
DRH5	32	Analog	High-side gate driver 5.
DRB5	33	Analog	High-side gate driver bootstrap 5. Connect a 1µF or higher value ceramic capacitor from DRB5 to DRS5 with a 10mm or shorter trace from the pin.
DRL0	39	Analog	Low-side gate driver 0.
DRL1	40	Analog	Low-side gate driver 1.
DRL2	41	Analog	Low-side gate driver 2.

9.4 I/O Ports Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION[2]
PD4	1	PD4	I/O	I/O port D4.
		PWMD1	I/O	Timer D PWM/capture 1.
PD3	2	PD3	I/O	I/O port D3.
		PWMA5	I/O	Timer A PWM/capture 5.
		PWMA7	I/O	Timer A PWM/capture 7.
		PWMB1	I/O	Timer B PWM/capture 1.
PD2	3	PD2	I/O	I/O port D2.
		PWMA3	I/O	Timer A PWM/capture 3.
		PWMA4	I/O	Timer A PWM/capture 4.
		PWMB0	I/O	Timer B PWM/capture 0.
PD1	4	PD1	I/O	I/O port D1.
		SWDCL	I	Serial wire debug clock.
		EXTCLK	I	External clock input.
PD0	5	PD0	I/O	I/O port D0.
		SWDIO	I/O	Serial wire debug I/O.
PE0	6	PE0	I/O	I/O port E0.
		SPICLK	I/O	SPI clock.
PE1	7	PE1	I/O	I/O port E1.
		SPIMOSI	I/O	SPI master out, slave in (MOSI)
		UARTTX	O	UART transmit output.
PE2	8	PE2	I/O	I/O port E2.
		SPI MISO	I/O	SPI master in, slave out (MISO)
		UARTRX	I	UART receive input.
PE3	9	PE3	I/O	I/O port E3.
		SPICS0	O	SPI chip select 0.
		nRESET1	I	Reset input 1.
PE4	10	PE4	I/O	I/O port E4.
		SPICS1	O	SPI chip select 1.
		I2CSCL	I/O	I2C clock
PE5	11	PE5	I/O	I/O port E5.
		SPICS2	O	SPI chip select 2.
		I2CSDA	I/O	I2C data.
PC3	14	PC3	I/O	I/O port C3.
		AD3	Analog	ADC input 3.
PC2	15	PC2	I/O	I/O port C2.
		AD2	Analog	ADC input 2.

[2] For a full description of all of the pin configurations for each digital I/O, see the PAC5232 User Guide for the Peripheral MUX.

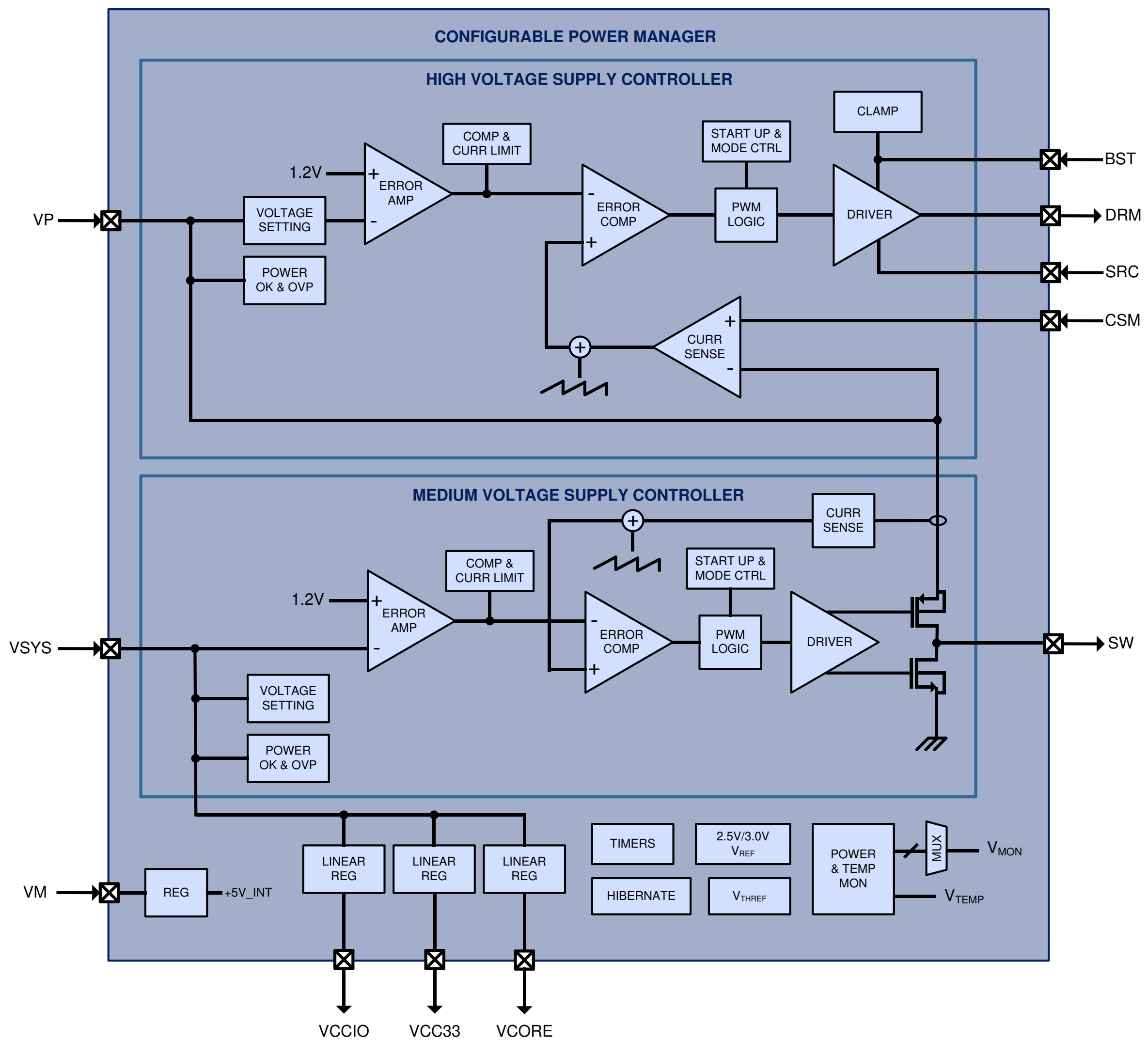
PD7	49	PD7	I/O	I/O port D7.
		PWMA6	I/O	Timer A PWM/capture 6.
		PWMD0	I/O	Timer D PWM/capture 0.
PD6	50	PD6	I/O	I/O port D6.
		PWMA7	I/O	Timer A PWM/capture 7.
		PWMB1	I/O	Timer B PWM/capture 1.
PD5	51	PD5	I/O	I/O port D5.
		PWMA5	I/O	Timer A PWM/capture 5.
		PWMC1	I/O	Timer C PWM/capture 1.

10 CONFIGURABLE POWER MANAGER (CPM)

10.1 Features

- 160V Buck DC/DC Controller (HV Buck)
  - 25V – 160V input
- 5V Switching Regulator (MV Buck)
- 3 linear regulators with power and hibernate management, including V_{REF} for ADC
- Power and temperature monitor, warning, and fault detection

Figure 10-1 CPM Block Diagram



Rev 1.1
6-Jan-2018

10.2 Functional Description

The Configurable Power Manager (Figure 10-1) is optimized to efficiently provide “all-in-one” power management required by the PAC® and associated application circuitry. It incorporates a high-voltage power supply controller that is used to convert power from a DC input source to generate a main supply output V_P. There is also an integrated medium-voltage buck DC/DC regulator to generate V_{SYS}.

Three other linear regulators provide V_{CCIO}, V_{CC33}, and V_{CORE} supplies for 3.3V I/O, 3.3V mixed signal, and 1.9V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

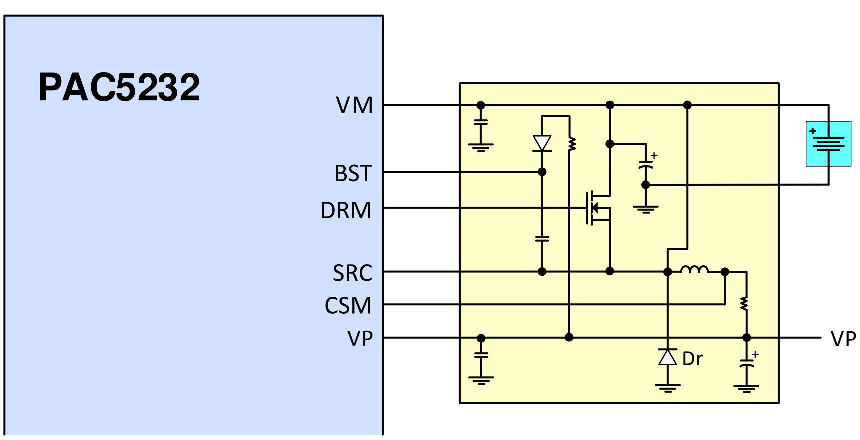
10.3 High-Voltage Supply Controller (HV-BUCK)

The PAC5232 contains a High-Voltage Supply Controller for a Buck DC/DC. This power supply is used to supply the various regulators in the PAC5232, as generating the V_P gate drive voltage for the Application Specific Driver Manager (ASPD).

The HV-BUCK controller drives an external power MOSFET for pulse-width modulation switching of an inductor or transformer for power conversion. The VM is the HV-BUCK supply controller input. The DRM output drives the gate of the N-CH MOSFET between the V_M on state and V_{SS} off state at proper duty cycle and switching frequency to ensure that the main supply voltage V_P is regulated. The gate of the high-side power MOSFET is connected to the DRM pin and the source of the high-side power MOSFET is connected to SRC.

The V_P regulation voltage is initially set to 12V during start up, and can be reconfigured to be 15V by the microcontroller after initialization. When V_P is lower than the target regulation voltage, the internal feedback control circuitry causes the inductor current to increase to raise V_P. Conversely, when V_P is higher than the regulation voltage, the feedback loop control causes the inductor current to decrease to lower V_P. The feedback loop is internally stabilized. The output current capability of the switching supply is determined by the external current sense resistor. The inductor current signal is sensed differentially between the CSM pin and V_P, and has a peak current limit threshold of 0.2V.

Figure 10-2 HV-BUCK Example



The switching frequency and output voltage of the HV-BUCK can be reconfigured by the MCU. The switching frequency can be configured to be between 50kHz and 400kHz and the gate drive output voltage can be configured to either 12V or 15V to work for a range of MOSFET or IGBT based inverters.

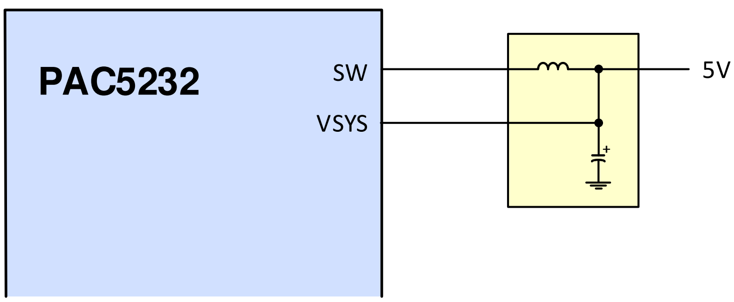
The Rectifier Diode (Dr) must be a low QRR diode.

10.4 Medium-Voltage Buck Regulator (MV-BUCK)

The PAC5232 contains a Medium-Voltage Buck Switching Regulator that generates a 5V, 200mA supply for the device, as well as PCB functions.

The SW pin is the switch node of the Buck regulator. The Power MOSFET is integrated, so connect this pin to VSYS through an external inductor. The VSYS pin is the 5V regulator output, which should be bypassed to ground.

Figure 10-3 MV-BUCK Switching Regulator Example

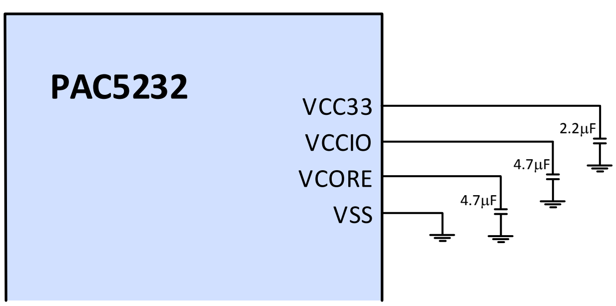


The output of VSYS is fixed at 5V and the switching frequency is 1.33MHz. This regulator supplies at least 200mA. This buck regulator offers better thermal and efficiency performance.

10.5 Linear Regulators

The CPM includes three additional linear regulators. VSYS supplies these three regulators. Once VSYS is above 4.5V, these three additional 40mA linear regulators for VCCIO, VCC33, and VCORE supplies sequentially power up.

Figure 10-4 Linear Regulators Example



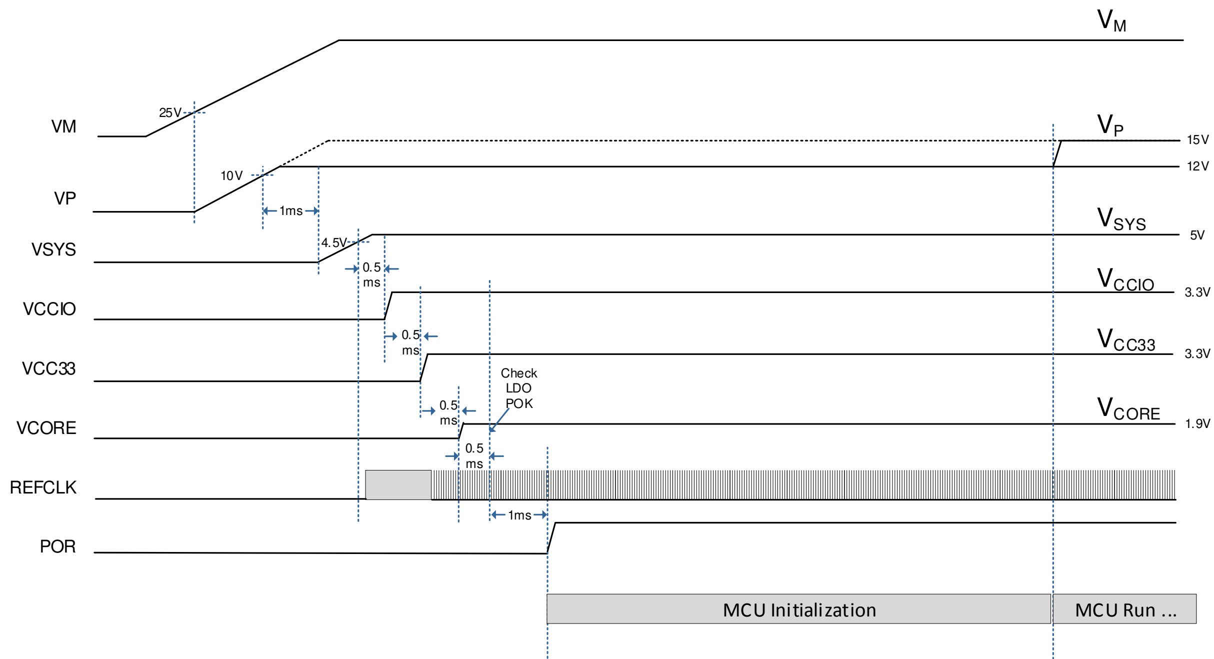
The figure above shows typical circuit connections for the linear regulators. The VCCIO regulator generates a dedicated 3.3V supply for IO. The VCC33 and VCORE regulators generate 3.3V and 1.9V, respectively. When VSYS, VCCIO, VCC33, and VCORE are all above their respective power good thresholds, and the configurable power on reset duration has expired, the microcontroller is initialized.[3]

[3] Note that the VCORE LDO may not have any addition load on it from the PCB. The only components connected to VCORE should be a bypass capacitor to ground.

10.6 Power-up Sequence

The CPM follows a typical power up sequence as in the Figure 10-5 below.

Figure 10-5 Power-Up Sequence



A typical sequence begins with motor power supply (VM) being applied and rising to 25V. When VM rises to 25V, the HV-BUCK controller is started and VP starts to rise. When VP rises over the UVLO rising threshold, then there is a 1ms delay and then the MV-BUCK is enabled. When VSYS rises to 4.5V, then there is a 0.5ms delay and the VCCIO LDO is enabled. Then there is a 0.5ms delay and the VCC33 LDO is enabled. Then there is a 0.5ms delay and the VCORE LDO is enabled.

There is then a 0.5ms delay and the power good threshold of all LDOs is checked. If all are OK, then there is an additional 1ms delay, then the POR signal is asserted to the MCU and it begins executing firmware.

During the firmware initialization process, the MCU may change the VP output voltage setting from the 12V default to 15V.

10.7 Hibernate Mode

The IC can go into an ultra-low power hibernate mode via the microcontroller firmware or via the optional push button (PBTN, see *Push Button* description in *Configurable Analog Front End*). In hibernate mode, only a minimal amount (typically 19µA at 56V) of current is used by V_M, and the CPM controller and all internal regulators are shut down to eliminate power drain from the output supplies. The system exits hibernate mode after a wake-up timer duration (configurable from 125ms to 8s or infinite) has expired or, if push button enabled, after an additional push button event has been detected. When exiting the hibernate mode, the power manager goes through the start up cycle and the microcontroller is reinitialized. Only the persistent power manager status bits (resets and faults) are retained during hibernation.

10.8 Power and Temperature Monitor

Whenever any of the V_{SYS}, V_{CCIO}, V_{CC33}, or V_{CORE} power supplies falls below their respective power good threshold voltage, a fault event is detected and the microcontroller is reset. The microcontroller stays in the reset state until V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CC18} supply rails are all good again and the reset time has expired. A microcontroller reset can also be initiated by a maskable temperature fault event that occurs when the IC temperature reaches 165°C. The fault status bits are persistent during reset, and can be read by the microcontroller upon re-initialization to determine the cause of previous reset.

A power monitoring signal V_{MON} is provided onto the ADC pre-multiplexer for monitoring various internal power supplies. V_{MON} can be set to be V_{CORE}, 0.4•V_{CORE}, 0.4•V_{CC33}, 0.4•V_{CCIO}, 0.4•V_{SYS}, 0.1•V_P, or the internal compensation voltage V_{COMP} for switching supply power monitoring.

For power and temperature warning, an IC temperature warning event at 140°C are provided as a maskable interrupt to the microcontroller. This warning allows the microcontroller to safely power down the system.

In addition to the temperature warning interrupt and fault reset, a temperature monitor signal is provided onto the ADC pre-multiplexer for IC temperature measurement.

This value has a compensation coefficient available in INFO FLASH that can be used to obatin an accurate temperature. The parameter VT300K will be stored in INFO FLASH and will indicate the compensation factor.

The temperature can then be obatined by the following formula:

$V_{TEMP\_KELVIN} = 300 * (VM + 0.075) / (VT300K + 0.075)$

For information on on the location of this temperature coefficient, see the PAC5232 User Guide.

10.9 Voltage Reference

The reference block includes a 1.2V high-precision reference voltage used internally and for all the LDOs. There is also a high-accuracy 2.5V reference for the ADC V_{REF} on the MCU. There is also a 4-level programmable threshold voltage V_{THREF} (0.1V, 0.2V, 0.5V, and 1.25V).

10.10 Electrical Characteristics

Table 10-1 High-Voltage Buck Controller Electrical Characteristics

(V_M = 30V, V_P = 12V and T_J = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{HIB;VM}$	V_M hibernate mode supply current	Hibernate mode, VM = 56V		19	26	µA
		Hibernate mode, VM = 80V		22.5		µA
$V_{UVLOR;VM}$	V_M UVLO rising		23	25	27	V
$V_{UVLOF;VM}$	V_M UVLO hysteresis			2		V
$V_{REF;VP}$	V_P output regulation voltage	Set to 12V	-5%	12	-5%	V
$k_{POKR;VP}$	V_P power OK threshold	V_P rising		91		%
$k_{POKF;VP}$		V_P falling		87		%
$k_{OVPR;VP}$	V_P OV protection threshold	V_P rising, blanking = 10µs		130		%
$t_{ONMIN;DRM}$	DRM minimum on time		90	200	300	ns
$t_{OFFMIN;DRM}$	DRM minimum off time		390	600	1150	ns
$V_{UVLOR;VP}$	V_P UVLO rising			10		V
$V_{UVLOF;VP}$	V_P UVLO falling			8		V
$V_{CSM;ILIM}$	CSM current limit threshold		-12%	0.2	12%	V
$F_{S;DRM}$	Switching frequency	Frequency setting: 50kHz, 100kHz (default), 200kHz, 400kHz	-5		5	%
$I_{SOURCE;DRM}$	DRM output high source current			100		mA
$I_{SINK;DRM}$	DRM output low sink current			200		mA
	HV-BUCK inductor value			100		µH
I_{DSG}	Discharge current			10		mA
V_{VM}	Motor voltage range		0		160	V
$V_{SRC;VSS}$	SRC to ground range		-10		VM + 10	V
$V_{SRC;VM}$	SRC to VM range				10	V
$V_{BST;VSS}$	BST to ground range				175	V

Table 10-2 Medium-Voltage Buck Controller Electrical Characteristics

(V_M = 30V, V_P = 12V and T_J = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{VSYS}	V_{SYS} output voltage accuracy		-3%	5	3%	V
F_{SW}	Switching frequency		-5%	1.33	5%	MHz
$I_{VSYS;LIM}$	V_{SYS} current limit		420		550	mA
I_{VSYS}	V_{SYS} output current	V_{SYS} > 3V	200			mA
		V_{SYS} < 2.5V	100			mA
$V_{POK;VSYS}$	V_{SYS} power OK threshold	Rising	4.25	4.5	4.75	V
		Falling		4.2		V
	V_{SYS} power OK blanking delay			10		µs
	MV-BUCK inductor value	Current rating of at least 750mA	6.8 – 20%		10 + 20%	µH
$V_{UVLO;VSYS}$	V_{SYS} UVLO	Rising		4.5		V
		Falling		4.2		V
$V_{OVP;VSYS}$	V_{SYS} OVP	Rising		5.5		V
		Falling		5.2		V