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PAC5523 Data Sheet

Power Application Controller®

Multi-Mode Power Manager™
Configurable Analog Front End™
Application Specific Power Drivers™
ARM© Cortex®-M4F Controller Core

www.active-semi.com

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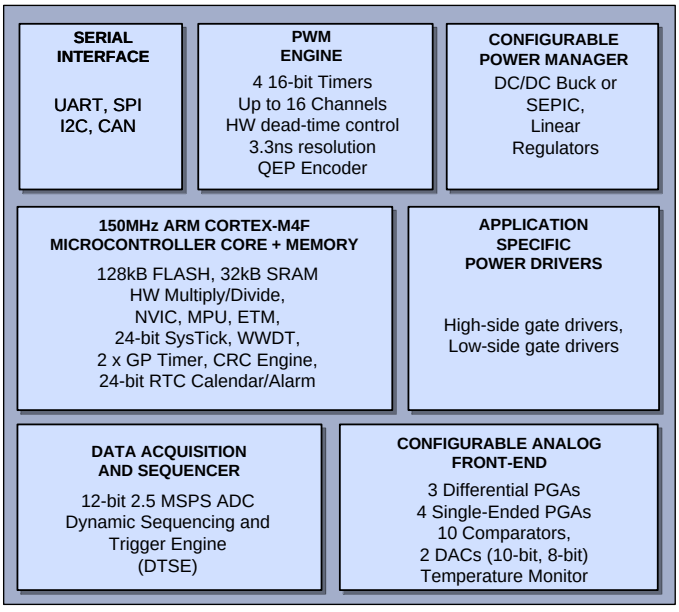
GENERAL DESCRIPTION

The PAC5523 is a custom Power Application Controller© (PAC) product that is optimized for high-speed BLDC motor control. The PAC5523 integrates a 150MHz ARM Cortex-M4F 32-bit microcontroller core with Active-Semi's proprietary and patent-pending Multi-Mode Power Manager™, Configurable Analog Front-End™ and Application Specific Power Drivers™ to form the most compact microcontroller-based power and motor control solution available.

The PAC5523 microcontroller features 128kB of embedded FLASH and 32kB of SRAM memory, a 2.5MSPS analog-to-digital converter (ADC) with programmable auto-sampling of up to 24 conversion sequences, 3.3V IO, flexible clock control system, PWM and general-purpose timers and several serial communications interfaces.

The Multi-Mode Power Manager (MMPM) provides "all-in-one" efficient power management solution for multiple types of power sources. It features a configurable multi-mode switching supply controller capable of operating a buck or SEPIC converter and up to four linear regulated voltage supplies. The Application Specific Power Drivers (ASPD) are power drivers designed for half bridge, H-bridge, 3-phase, intelligent power module (IPM), and general purpose driving. The Configurable Analog Front End (CAFE) comprises differential programmable gain amplifiers, single-ended programmable gain amplifiers, comparators, digital-to-analog converters, and I/Os for programmable and inter-connectible signal sampling, feedback amplification, and sensor monitoring of multiple analog input signals.

Figure 1-1. PAC5523 Power Application Controller

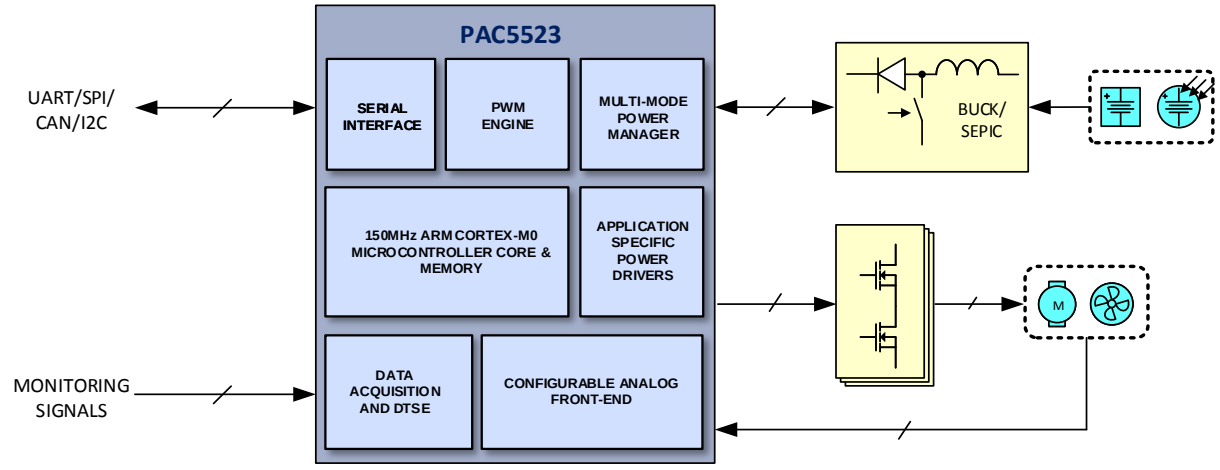


The PAC5523 is available in a 48-pin, 6x6mm TQFN package.

1 PAC FAMILY APPLICATIONS

- General-purpose high-voltage system controllers
- Home appliances
- Ceiling Fans
- Standing Fans
- Compressors
- Power Tools
- Garden Tools
- Motor Controllers
- Industrial Applications
- Drone/RC

Figure 1-1 Simplified Application Diagram



2 PRODUCT SELECTION SUMMARY

Table 2-1 Product Selection Summary

PART NUMBER	PIN PKG	POWER MANAGER		CONFIGURABLE ANALOG FRONT END					APPLICATION SPECIFIC POWER DRIVERS			MICROCONTROLLER						PRIMARY APPLICATION
		INPUT VOLTAGE	MULTI-MODE SW	DIFF-PGA	PGA	COMPARATOR	DAC	ADC CHANNEL	VSRC	POWER DRIVER	PWM CHANNEL	SPEED (MHz)	FLASH (kB)	SRAM (kB)	GPIO	COMM	XTAL	
PAC5523	48-pin 6x6 TQFN	5.2 – 70V	Y	3	4	10	2	15	70V	3 LS (1.5A/1.5A) 3 HS (1.5A/1.5A)	6@VP 15@VCCIO	150	128	32	10@VSYS 3 @ VP 15@VCCIO	UART SPI I2C CAN SWD JTAG ETM	N	3 half-bridge 3 phase control BEMF Trapezoidal or FOC

Notes: DIFF-PGA = differential programmable gain amplifier; HS = high-side, LS = low-side, PGA = programmable gain amplifier, VSRC = Bootstrap Voltage Source

3 ORDERING INFORMATION

Table 3-1 Ordering Information

PART NUMBER[1]	TEMPERATURE RANGE	PACKAGE	PINS	PACKING
PAC5523QM	-40°C to 125°C	TQFN66-48	48 + Exposed Pad	Tray

[1] See *Product Selection Summary* for product features for each part number

4 FEATURES

4.1 Feature Overview

- **Proprietary Multi-Mode Power Manager**
  - Multi-mode switching supply controller configurable for DC/DC Buck or SEPIC topologies
  - Direct battery supply from 5V – 20V
  - 4 Linear regulators with power and hibernate management
  - Power and temperature monitor, warning, fault detection
- **Proprietary Configurable Analog Front-End**
  - 10 Analog Front-End IO pins
  - 3 Differential Programmable Gain Amplifiers
  - 4 Single-ended Programmable Gain Amplifiers
  - Programmable Over-Current Protection
  - 10 Comparators
  - 2 DACs (10-bit and 8-bit)
  - Integrated BEMF comparator mode with virtual center-tap
- **Proprietary Application Specific Power Drivers**
  - 3 Low-side and 3 High-Side gate drivers with 1.5A gate driving capacity
  - Configurable propagation delay and fault protection
- **150MHz ARM Cortex-M4F 32-bit Microcontroller Core**
  - Single-cycle 32-bit x 32-bit hardware multiplier
  - 32-bit hardware divider
  - DSP Instructions and Saturation Arithmetic Support
  - Integrated sleep and deep sleep modes
  - Single-precision Floating Point Unit (FPU)
  - 8-region Memory Protection Unit (MPU)
  - Nested Vectored Interrupt Controller (NVIC) with 32 Interrupts with 8 levels of priority
  - 24-Bit SysTick Timer
  - Wake-up Interrupt Controller (WIC) allowing power-saving sleep modes
  - Clock-gating allowing low-power operation
  - Embedded Trace Macrocell (ETM) for in-system debugging at real-time without breakpoints
- **Memory**
  - 128kB FLASH
  - 32kB SRAM with ECC
  - 2 x 1kB INFO FLASH area for manufacturing information
  - 1 x 1kB INFO FLASH area for user parameter storage and application configuration or code
  - Code Protection

- **Analog to Digital Converter (ADC)**
  - 12-bit resolution
  - 2.5MSPS
  - Programmable Dynamic Triggering and Sampling Engine (DTSE)
- **I/O**
  - 3.3V Digital Input/Output or Analog Input for ADC
  - Configurable weak pull-up and pull-down
  - Configurable drive strength (6mA to 25mA minimum)
  - Dedicated Integrated IO power supply (3.3V)
  - Flexible peripheral MUX allowing each IO pin to be configured with one of up to 8 peripheral functions
  - Flexible Interrupt Controller
- **Flexible Clock Control System (CCS)**
  - 300MHz PLL from internal 2% oscillator
  - 20MHz Ring Oscillator
  - 20MHz External Clock Input
- **Timing Generators**
  - Four 16-bit timers with up to 32 PWM/CC blocks
    - 16 Programmable Hardware Dead-time generators
    - Up to 300MHz input clock for high-resolution PWM
  - 16-bit Windowed Watchdog Timer (WWDT)
  - 24-bit Real-time Clock (RTC) with Calendar and Alarm Functions
  - 24-bit SysTick Timer
  - 2 x 24-bit General-purpose count-down timers with interrupt
  - Wake-up timer for sleep modes from 0.125s to 8s
- **Communication Peripherals**
  - 3 x USART
    - SPI or UART modes
    - SPI Master/Slave, up to 25MHz
    - UART, up to 1Mbps
  - I2C Master/Slave
  - CAN 2.0A/B Controller
  - Single Wire Debugger (SWD)/JTAG
  - Embedded Trace Macrocell (ETM)
- **4-Level User-Configurable Code Protection**
- **96-bit Unique ID**
- **CRC Engine**
  - Offloads software for communications and safety protocol through hardware acceleration
  - Configurable Polynomial (CRC-16 or CRC-8)
  - Configurable Input Data Width, Input and Output Reflection
  - Programmable Seed Value

5 ABSOLUTE MAXIMUM RATINGS

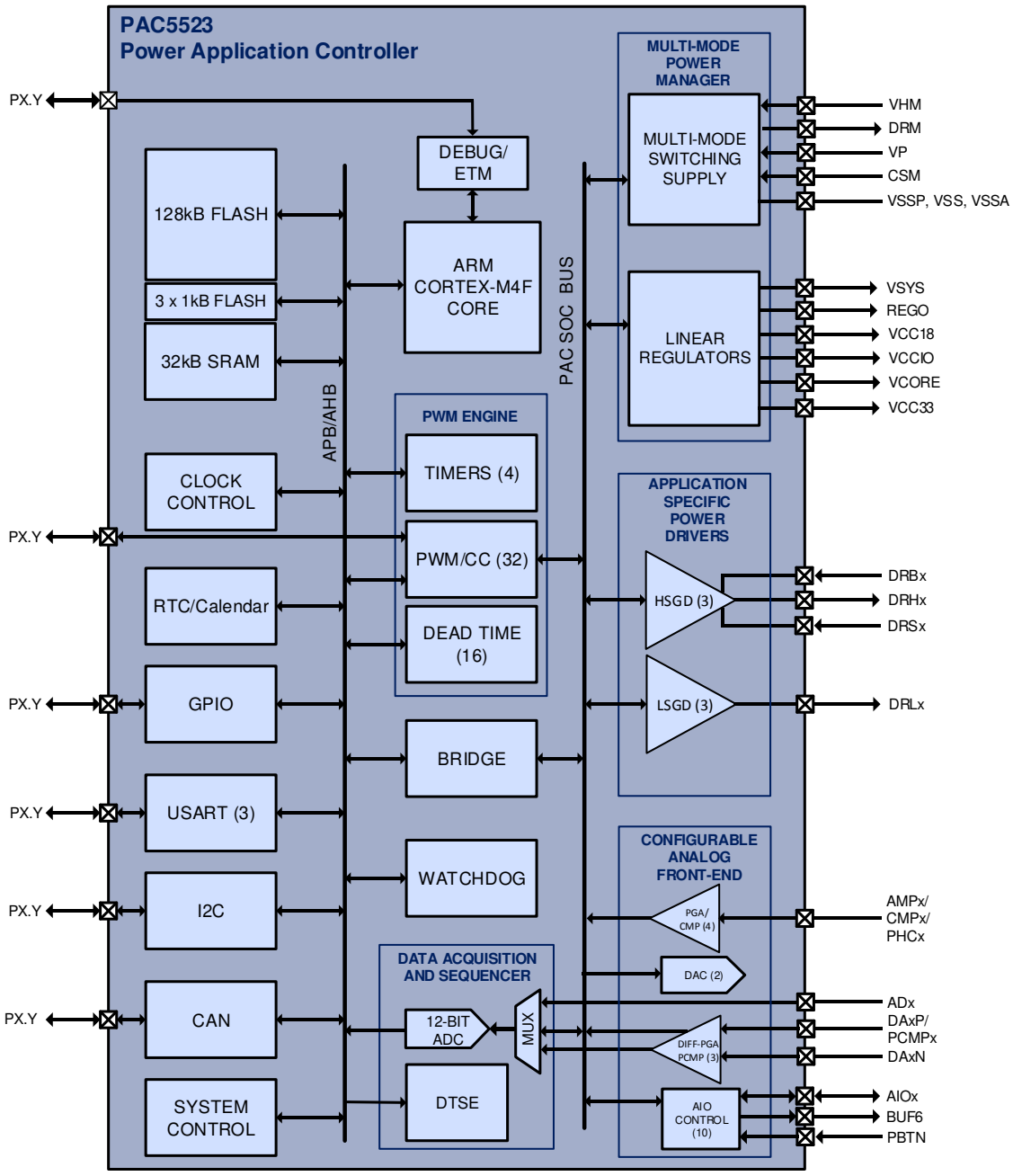
Table 5-1 Absolute Maximum Ratings[2]

PARAMETER		VALUE	UNIT
VHM, DRM to VSSP		-0.3 to 72	V
VP to VSS		-0.3 to 20	V
CSM, REGO to VSS		-0.3 to V_P + 0.3	V
VSYS, VCCIO, AIO6 to VSS		-0.3 to 6	V
VCC33 to VSS		-0.3 to 4.1	V
VCORE to VSS		-0.3 to 1.44	V
VCC18 to VSS		-0.3 to 2.5	V
AIO[0..5, 7..9] to VSS		-0.3 to V_{SYS} + 0.3	V
PD[0..7], PE[0..7]		-0.3 to 4.6	V
DRLx to VSSP		-0.3 to VP + 0.3	V
DRBx to VSSP		-0.3 to 84	V
DRSx to VSSP		-6 to 72	V
DRSx allowable offset slew rate (dVDRSx/dt)		5	V/ns
DRBx, DRHx to respective DRSx		-0.3 to 20	V
VSSP, VSSA to VSS		-0.3 to 0.3	V
VSS, VSYS, DRLx, DRHx, VSYSSW RMS current[3]		0.2	A_{RMS}
VSSP RMS current[3]		0.4	A_{RMS}
VP RMS current[3]		0.6	A_{RMS}
Operating temperature range		-40 to 125	°C
Electrostatic Discharge (ESD)	Human body model (JEDEC)	2	kV
	Charge device model (JEDEC)	1	kV

[2] Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.
[3] Peak current can be 10 times higher than RMS value for pulses shorter than 10μs

6 ARCHITECTURAL BLOCK DIAGRAM

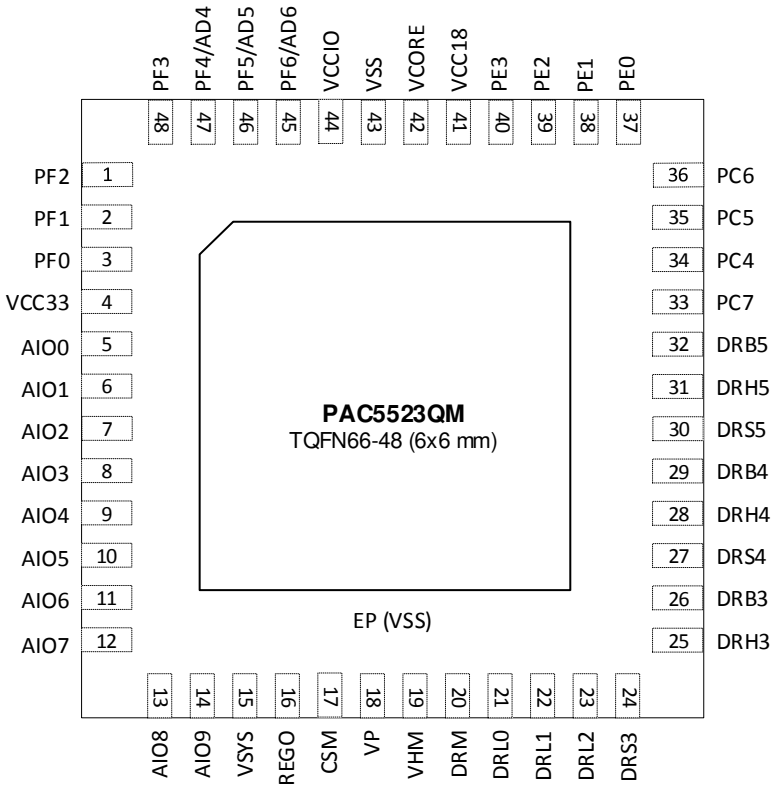
Figure 6-1 Architectural Block Diagram



7 PIN CONFIGURATION

7.1 PAC5523QM

Figure 7-1 PAC5523QM Pin Configuration (TQFN66-48 Package)



8 PIN DESCRIPTION

Table 8-1 Multi-Mode Power Manager (MMPM) and System Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
VCC33	4	Power	Internally generated 3.3V power supply. Connect to a 2.2µF or higher value ceramic capacitor from V_{CC33} to V_{SSA}.
VSYS	15	Power	5V System power supply. Connect to a 6.8µF (20%) or higher ceramic capacitor from V_{SYS} to V_{SS}.
REGO	16	Power	System regulator output. Connect to V_{SYS} directly or through an external power-dissipating resistor.
CSM	17	Power	Switching supply current sense input. Connect to the positive side of the current sense resistor.
VP	18	Power	Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 0.1µF ceramic capacitor from V_P to V_{SS} for voltage loop stabilization. This pin requires good capacitive bypassing to V_{SS}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin.
VHM	19	Power	Switching supply controller supply input. Connect a 1µF or higher value ceramic capacitor, or a 0.1µF ceramic capacitor in parallel with a 10µF or higher electrolytic capacitor from V_{HM} to V_{SSP}. This pin requires good capacitive bypassing to V_{SSP}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin.
DRM	20	Power	Switching supply driver output. Connect to the base or gate of the external power NPN or n-channel MOSFET. See User Guide and application notes.
VCC18	41	Power	Internally generated 1.8V power supply. Connect a 2.2µF or higher value ceramic capacitor from V_{CC18} to V_{SSA}.
VCORE	42	Power	Internally generated 1.2V core power supply. Connect a 2.2µF or higher value ceramic capacitor from V_{CORE} to V_{SSA}.
VSS	43	Power	Ground.
VCCIO	44	Power	Internally generated digital I/O 3.3V power supply. Connect a 4.7µF or higher value ceramic capacitor from V_{CCIO} to V_{SSA}.
EP (VSS)	EP	Power	Exposed pad. Must be connected to V_{SS} in a star ground configuration. Connect to a large PCB copper area for power dissipation heat sinking.

Table 8-2 Configurable Analog Front End (CAFE) Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
AIO0	5	AIO0	I/O	Analog front end I/O 0.
		DA0N	Analog	Differential PGA 0 negative input.
AIO1	6	AIO1	I/O	Analog front end I/O 1.
		DA0P	Analog	Differential PGA 0 positive input.
AIO2	7	AIO2	I/O	Analog front end I/O 2.
		DA1N	Analog	Differential PGA 1 negative input.
AIO3	8	AIO3	I/O	Analog front end I/O 3.
		DA1P	Analog	Differential PGA 1 positive input.
AIO4	9	AIO4	I/O	Analog front end I/O 4.
		DA2N	Analog	Differential PGA 2 negative input.
AIO5	10	AIO5	I/O	Analog front end I/O 5.
		DA2P	Analog	Differential PGA 2 positive input.
AIO6	11	AIO6	I/O	Analog front end I/O 6.
		AMP6	Analog	PGA input 6.
		CMP6	Analog	Comparator input 6.
		BUF6	Analog	Buffer output 6.
		PBTN	Analog	Push button input.
AIO7	12	AIO7	I/O	Analog front end I/O 7.
		AMP7	Analog	PGA input 7.
		CMP7	Analog	Comparator input 7.
		PHC7	Analog	Phase comparator input 7.
AIO8	13	AIO8	I/O	Analog front end I/O 8.
		AMP8	Analog	PGA input 8.
		CMP8	Analog	Comparator input 8.
		PHC8	Analog	Phase comparator input 8.
AIO9	14	AIO9	I/O	Analog front end I/O 9.
		AMP9	Analog	PGA input 9.
		CMP9	Analog	Comparator input 9.
		PHC9	Analog	Phase comparator input 9.

Table 8-3 Application Specific Power Drivers (ASPD) Pin Description

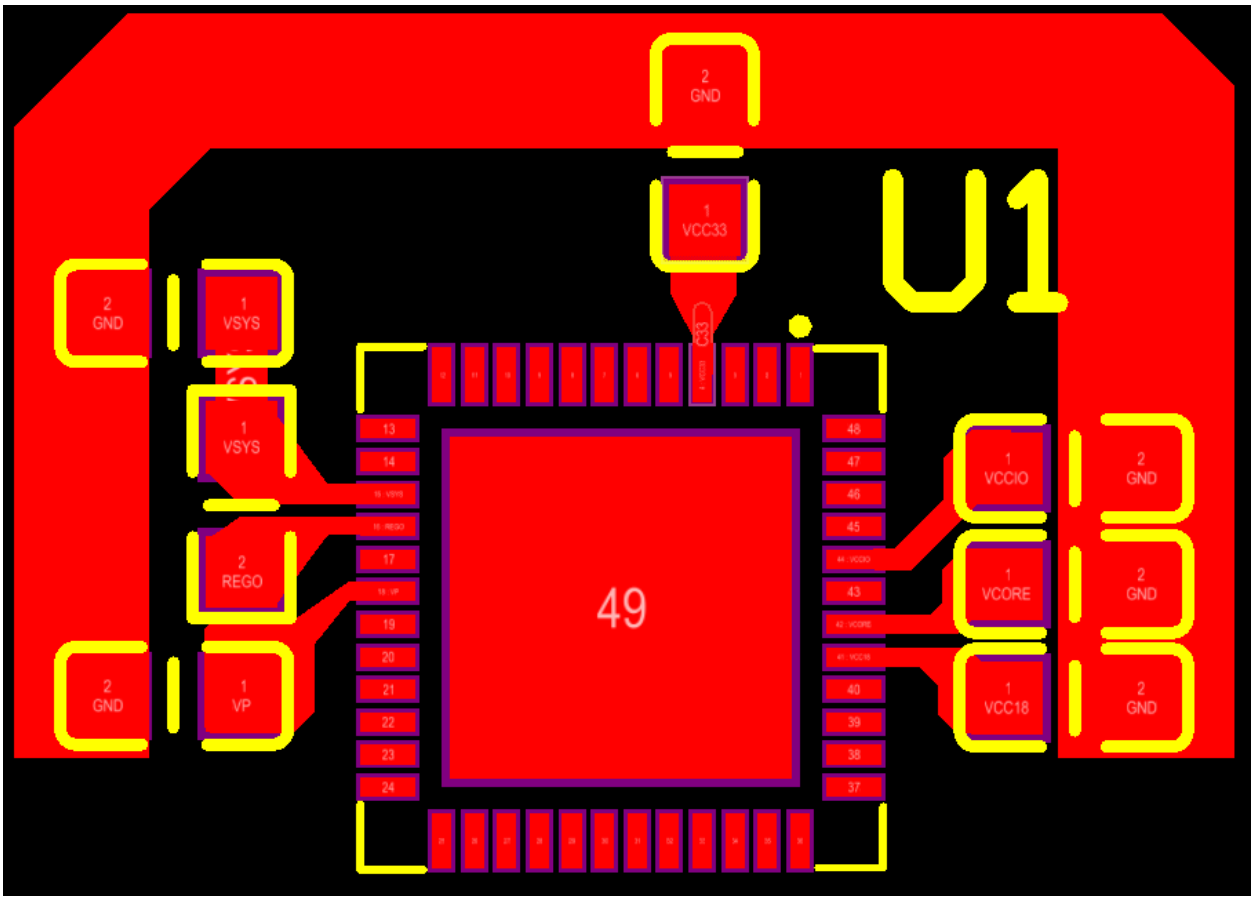
PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
DRL0	21	Analog	Low-side gate driver 0.
DRL1	22	Analog	Low-side gate driver 1.
DRL2	23	Analog	Low-side gate driver 2.
DRS3	24	Analog	High-side gate driver source 3.
DRH3	25	Analog	High-side gate driver 3.
DRB3	26	Analog	High-side gate driver bootstrap 3.
DRS4	27	Analog	High-side gate driver source 4.
DRH4	28	Analog	High-side gate driver 4.
DRB4	29	Analog	High-side gate driver bootstrap 4.
DRS5	30	Analog	High-side gate driver source 5.
DRH5	31	Analog	High-side gate driver 5.
DRB5	32	Analog	High-side gate driver bootstrap 5.

Table 8-4 I/O Ports Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION[4]
PF2	1	PF2	I/O	I/O port PF2.
PF1	2	PF1	I/O	I/O port PF1.
PF0	3	PF0	I/O	I/O port PF0.
PC7	33	PC7	I/O	I/O port PC7.
PC4	34	PC4	I/O	I/O port PC4.
PC5	35	PC5	I/O	IO port PC5.
PC6	36	PC6	I/O	I/O port PC6.
PE0	37	PE0	I/O	I/O port PE0.
PE1	38	PE1	I/O	I/O port PE1.
PE2	39	PE2	I/O	I/O port PE2.
PE3	40	PE3	I/O	I/O port PE3.
PF6	45	PF6	I/O	I/O port PF6.
		AD6	Analog Input	ADC channel ADC6.
PF5	46	PF5	I/O	I/O port PF5.
		AD5	Analog Input	ADC channel ADC5.
PF4	47	PF4	I/O	I/O port PF4.
		AD4	Analog Input	ADC channel ADC4.
PF3	48	PF3	I/O	I/O port PF3.

[4] For a full description of all of the pin configurations for each digital I/O, see the PAC55XX Family User Guide for the Peripheral MUX.

Figure 8-1 Power Supply Bypass Capacitor Routing

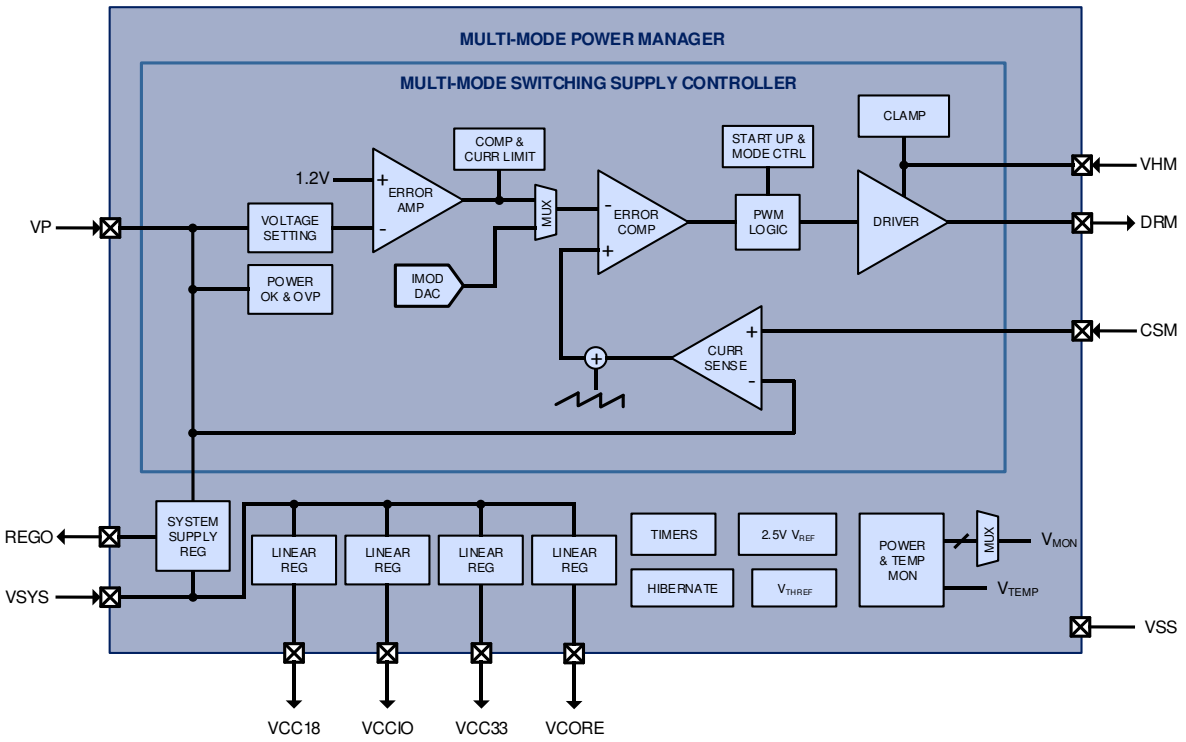


9 MULTI-MODE POWER MANAGER (MMPM)

9.1 Features

- Multi-mode switching supply controller configurable as buck or SEPIC
- DC supply up to 70V input
- Direct DC input of up to 20V with no DC/DC
- 5 linear regulators with power and hibernate management, including V_{REF} for ADC
- Power and temperature monitor, warning, and fault detection

Figure 9-1 MMPM Block Diagram



9.2 Functional Description

The Multi-Mode Power Manager (Figure 9-1) is optimized to efficiently provide “all-in-one” power management required by the PAC and associated application circuitry. It incorporates a dedicated multi-mode switching supply (MMSS) controller operable as a Buck or SEPIC converter to efficiently convert power from a DC input source to generate a main supply output V_P. Five linear regulators provide V_{CC18}, V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CORE} supplies for MCU FLASH, 5V system, 3.3V I/O, 3.3V mixed signal, and 1.2V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

9.3 Multi-Mode Switching Supply (MMSS) Controller

The MMSS controller drives an external power transistor for pulse-width modulation switching of an inductor or transformer for power conversion. The DRM output drives the gate of the N-CH MOSFET or the base of the NPN between the V_{HM} on state and V_{SSP} off state at proper duty cycle and switching frequency to ensure that the main supply voltage V_P is regulated. The V_P regulation voltage is initially set to 15V during start up, and can be reconfigured to be 9V or 12V by the microcontroller after initialization. When V_P is lower than the target regulation voltage, the internal feedback control circuitry causes the inductor current to increase to raise V_P. Conversely, when V_P is higher than the regulation voltage, the feedback loop control causes the inductor current to decrease to lower V_P. The feedback loop is internally stabilized. The output current capability of the switching supply is determined by the external current sense resistor. In the high-side current sense buck or SEPIC mode, the inductor current signal is sensed differentially between the CSM pin and V_P, and has a peak current limit threshold of 0.26V.

The MMSS controller is flexible and configurable as a buck or SEPIC converter. Input sources include battery supply for buck mode (Figure 9-2) or SEPIC mode (Figure 9-3). The MMSS controller operational mode is determined by external configuration and register settings from the microcontroller after power up. It can operate in either high-side or low-side current sense mode, and does not require external feedback loop compensation circuitry.

Figure 9-2 Buck Mode

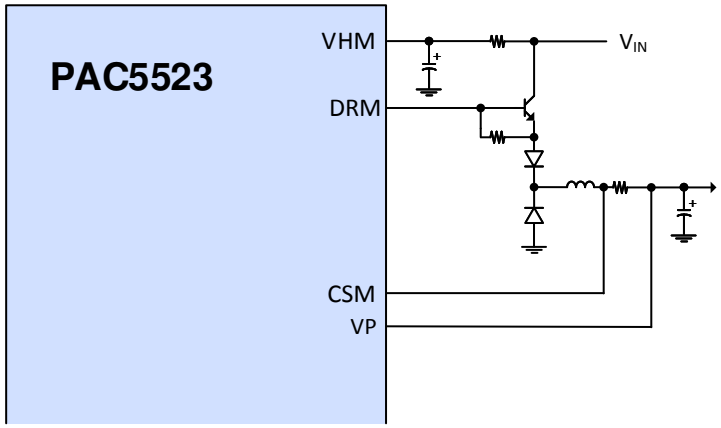
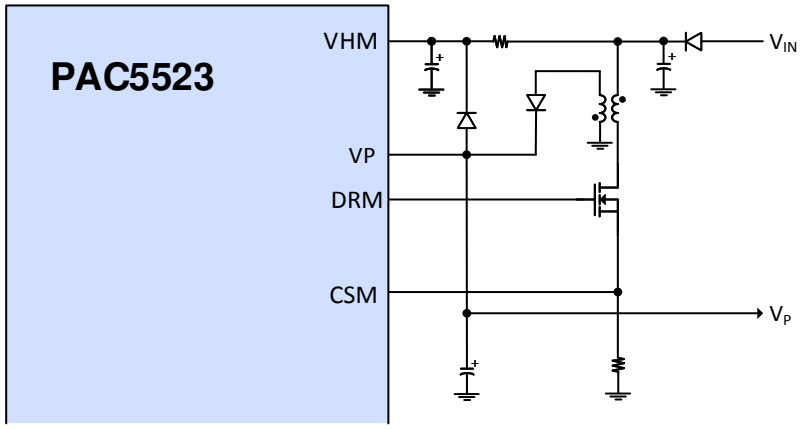


Figure 9-3 SEPIC Mode



The MMSS detects and selects between high-side and low-side mode during start up based on the placement of the current sense resistor and the CSM pin voltage. It employs a safe start up mode with a 9.5kHz switching frequency until V_P exceeds 4.3V under-voltage-lockout threshold, then transitions to the 45kHz default switching frequency for at least 6ms to bring V_P close to the target voltage, before enabling the linear regulators. Any extra load should only be applied after the supplies are available and the microprocessor has initialized. The switching frequency can be reconfigured by the microprocessor to be 181kHz to 500kHz in the high switching frequency mode for battery-based applications, and to be 45kHz to 125kHz in the low switching frequency mode. Upon initialization, the microcontroller must reconfigure the MMSS to the desired settings for V_P regulation voltage, switching mode, switching frequency, and V_{HM} clamp. Refer to the PAC application notes and user guide for MMSS controller design and programming.

If a stable external 5V to 20V power source is available, it can power the V_P main supply and all the linear regulators directly without requiring the MMSS controller to operate. In such applications, V_{HM} can be connected directly to V_P and the microcontroller should disable the MMSS upon initialization to reduce power loss.

Figure 9-4 Direct Battery Supply