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# PACSZ1284

# IEEE 1284 Parallel Port ESD/EMI/Termination Network

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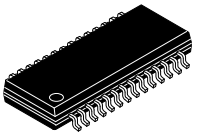


QSOP−28
QR SUFFIX
CASE 492AA

### Product Description

The PACSZ1284 combines EMI filtering, ESD protection, and signal termination in a single QSOP package for parallel port interfaces complying to the IEEE 1284 standard.

The PACSZ1284 provides a complete parallel port termination solution. It integrates the equivalent of 60 discrete components, making it ideal for space critical applications. The pins of the device which connect to the parallel port are protected to ±30 kV contact discharge, well beyond Level 4 of the IEC 61000−4−2 specification. All other pins are ESD−protected for contact discharges up to ±8 kV per IEC 61000−4−2.

There are two values available for pull−up resistor R1. For the PACSZ1284−02, R1 = 2.2 kΩ; for the PACSZ1284−04, R1 = 4.7 kΩ.

The PACSZ1284 is housed in a 28−pin QSOP package and is available with RoHS compliant lead−free finishing.

### Features

- 17 EMI Filters
- 17 ESD Protectors Yielding Protection to 30 kV Contact Discharge, per IEC 61000−4−2 Specification
- 17 Terminators with Choice of Resistor Values
- 28−Pin QSOP Package
- These Devices are Pb−Free and are RoHS Compliant

### Applications

- Parallel Ports of PCs, Printers, Peripherals, and Set−Top Boxes

### MARKING DIAGRAM

PACSZ1284 02QR

PACSZ1284 02QR = Specific Device Code

PACSZ128404QR

PACSZ128404QR = Specific Device Code

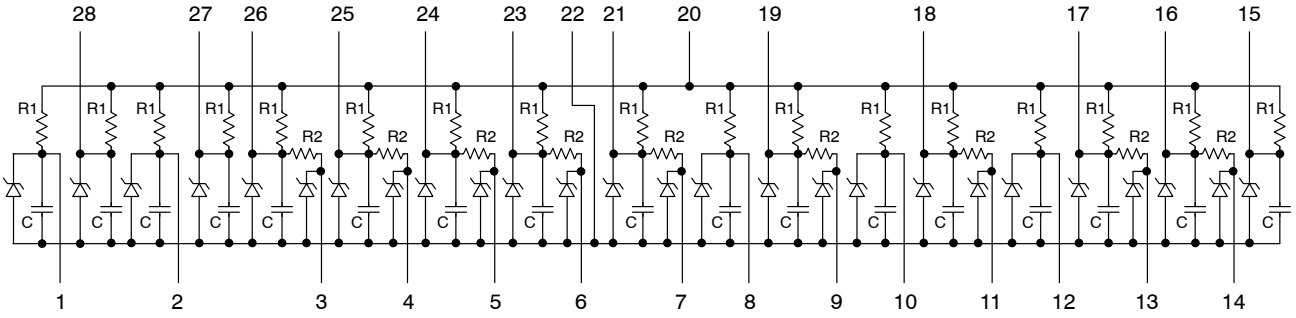
### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| PACSZ1284−02QR | QSOP−28 (Pb−Free) | 2500/Tape & Reel |
| PACSZ1284−04QR | QSOP−28 (Pb−Free) | 2500/Tape & Reel |

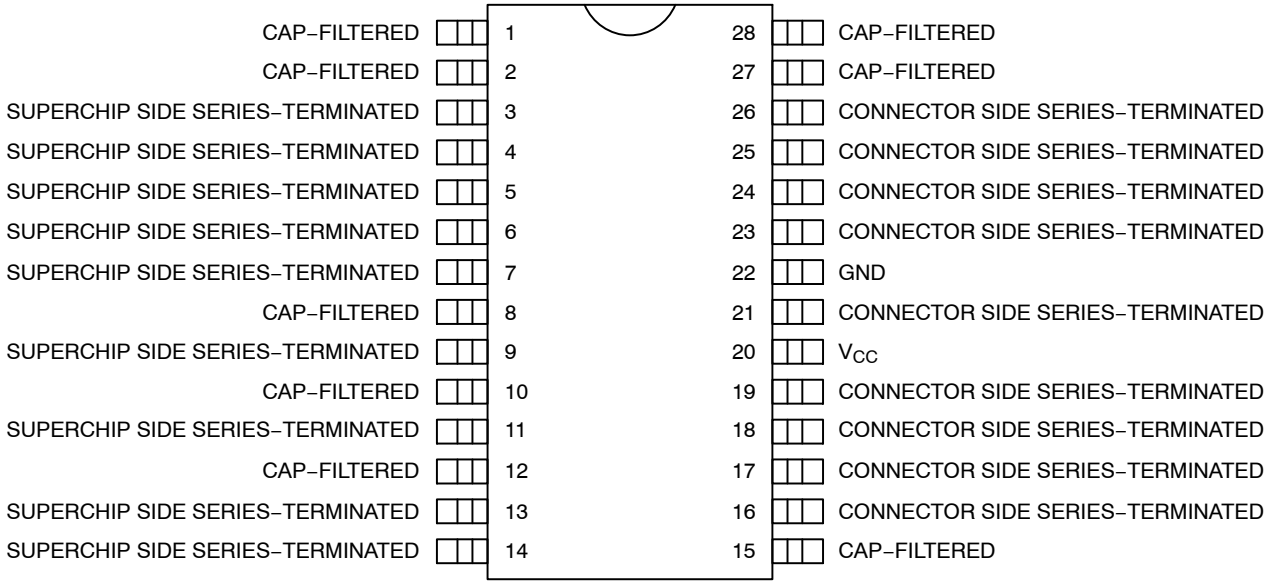
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## ELECTRICAL SCHEMATIC

| PACSZ1284−02 | PACSZ1284−04 |
|---|---|
| R1 = 2.2 kΩ<br>R2 = 33 Ω<br>C = 150 pF | R1 = 4.7 kΩ<br>R2 = 33 Ω<br>C = 150 pF |




## PACKAGE / PINOUT DIAGRAMS




28−Pin QSOP

**Table 1. PIN DESCRIPTIONS**

| Leads | Name | Description |
|---|---|---|
| 1, 2, 8, 10, 12, 15, 27, 28 | Capacitor−Filtered | IEEE 1284 Signals which Require No Series Termination |
| 3−7, 9, 11, 13, 14 | Super I/O Chip Side Series−Terminated | IEEE 1284 Signals on the Super I/O Chip Side which Require Series Termination |
| 16−19, 21, 23−26 | Parallel Port<br>Connector Side Series−Terminated | IEEE 1284 Signals on the Parallel Port Connector Side which Require Series Termination |
| 20 | $V_{CC}$ | Supply Rail for the Device |
| 22 | GND | Ground Reference for the Device |

## SPECIFICATIONS

**Table 2. ABSOLUTE MAXIMUM RATINGS**

| Parameter | Rating | Units |
|---|---|---|
| $V_{CC}$ Voltage | 5.5 | V |
| Input Voltage Range, No Clamping | −0.4 to 5.5 | V |
| Storage Temperature Range | −40 to +150 | °C |
| Power Dissipation per Resistor | 0.1 | W |
| Package Power Dissipation | 1.0 | W |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 3. STANDARD OPERATING CONDITIONS**

| Parameter | Rating | Units |
|---|---|---|
| $V_{CC}$ Voltage | 5.0 | V |
| Operating Temperature | −40 to +85 | °C |

**Table 4. ELECTRICAL OPERATING CHARACTERISTICS**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $TOL_R$ | Absolute Resistance Tolerance | Measured at $T_A$ = 25°C | | | ±20 | % |
| $TOL_C$ | Absolute Capacitance Tolerance | Measured at 1 MHz, 2.5 VDC, $T_A$ = 25°C | | | ±20 | % |
| $I_{LEAK}$ | Leakage Current to GND | Measured at 5.0 VDC, $T_A$ = 25°C | | 1 | 10 | μA |
| $V_{ESDi}$ | ESD Protection, Input Pins | Pins 3, 4, 5, 6, 7, 9, 11, 13, & 14, per IEC 61000−4−2 Specification (Notes 1 and 2) | ±8 | | | kV |
| $V_{ESD}$ | ESD Protection, Connector Pins | Pins 1, 2, 8, 10, 12, 15, 16, 17, 18, 19, 21, 23, 24, 25, 26, 27, & 28, per IEC 61000−4−2 Specification (Notes 1 and 3) | ±30 | | | kV |
| $V_{CLAMP}$ | Clamping Voltage under ESD Discharge | ESD Applied to Connector Pin, Measured at Corresponding Input Pin; +8 kV Discharge, Human Body Model (Note 1) | | 8.3 | | V |
| | | ESD Applied to Connector Pin, Measured at Corresponding Input Pin; −8 kV Discharge, Human Body Model (Note 1) | | −2.7 | | V |

1. ESD voltage applied between Input/Connector pins and ground, one pin at a time.
2. Pins 3−7, 9, 11, 13, and 14 typically connect to the I/O pins of a Super I/O chip.
3. Pins 1, 2, 8, 10, 12, 15−19, 21, and 23−28 typically connect to the Parallel Port connector.

## PERFORMANCE INFORMATION

### Filter Capacitors

The IEEE 1284 specification requires both termination and EMI filtering on a total of 17 lines. Basic filtering is provided through the presence of a capacitor on all signal lines. The filter capacitor is the junction capacitance of an ESD diode. The typical capacitance at a reverse voltage of 2.5 V is 150 pF. This diode capacitance is somewhat voltage dependent. See Figure 1.

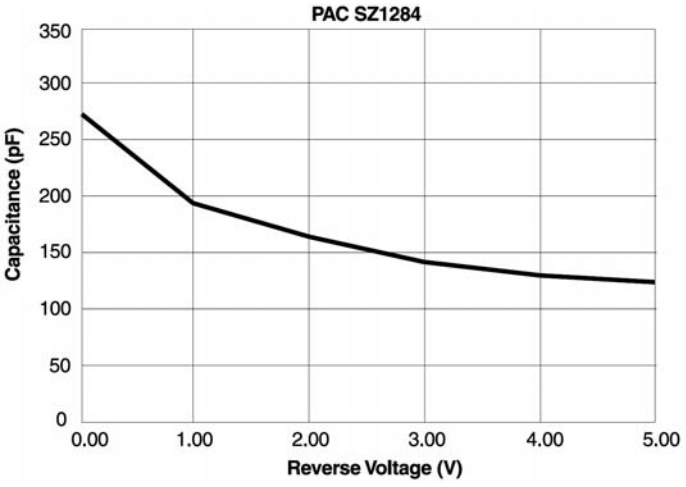



**Figure 1. Diode Capacitance vs. Reverse Voltage**

The higher speed Data and Strobe lines (9 in total) require an additional series resistor termination for proper operation, while the eight (8) Status lines do not. See Table 5.

### Filter Insertion Loss

Figure 2 shows the typical Insertion Loss graphs of the PACSZ1284 for Data and Strobe signals. The curves are dependent on the physical location of the filter elements with respect to the ground terminal of this device. These graphs are measured in a 50 Ω environment on a Hewlett Packard HP 8753C Analyzer. The signal source is introduced at the resistor input and the output is measured at the corresponding protection diode. The actual pins measured are labeled in the Figure 2 graph.

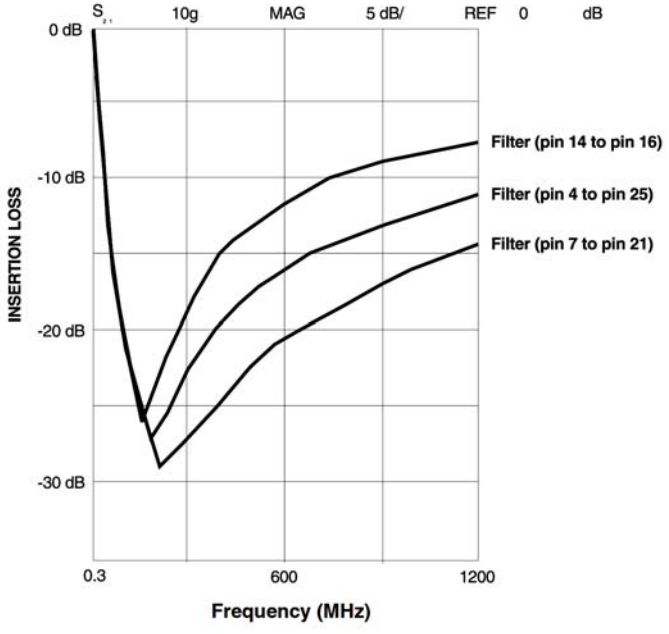



**Figure 2. Typical Filter Insertion Loss**

## APPLICATION INFORMATION

### Termination Considerations

The IEEE 1284 specification requires both termination and EMI filtering on a total of 17 signal lines. Control and Status lines (8 in total) only require a pull−up resistor and a filter capacitor. The Data lines and Strobe also require a series termination resistor in addition to the pull−up resistors and filter capacitors. See Table 5, in conjunction with the schematic diagram on page 2.

**Table 5. IEEE 1284 TERMINATION REQUIREMENTS**

| Signal Termination Requirements | |
|---|---|
| **Signal Name** | **Series Termination** |
| Data1 − Data8 | Yes |
| Strobe | Yes |
| Init | Not Required |
| AutoFeedXT | Not Required |
| Selectin | Not Required |
| ACK | Not Required |
| Busy | Not Required |
| Paper Empty | Not Required |
| Select | Not Required |
| Fault | Not Required |

### Interfacing to IEEE 1284 Connectors

IEEE 1284 defines three interface connectors:

- 1284 A is a 25−pin DB series connector which is the de facto PC standard for the host connection
- 1284 B is a 36−pin, 0.085 inch centerline connector used on the peripheral device
- 1284 C is a new 36−pin, 0.050 inch centerline connector which can be used for both host and peripheral

Figure 3A shows a possible hook−up between the 1284−A connector on a PC motherboard and the PACSZ1284, illustrating how the pin configuration of the PACSZ1284 allows for easy interconnect between the two. The dotted I/O signals of the PACSZ1284 will typically be connected to a Super I/O chip on the motherboard.

Figure 3B shows a possible hook−up between the 1284−B connector on a peripheral and the PACSZ1284

Figure 3C shows a possible hook−up between the 1284−C connector and the PACSZ1284.

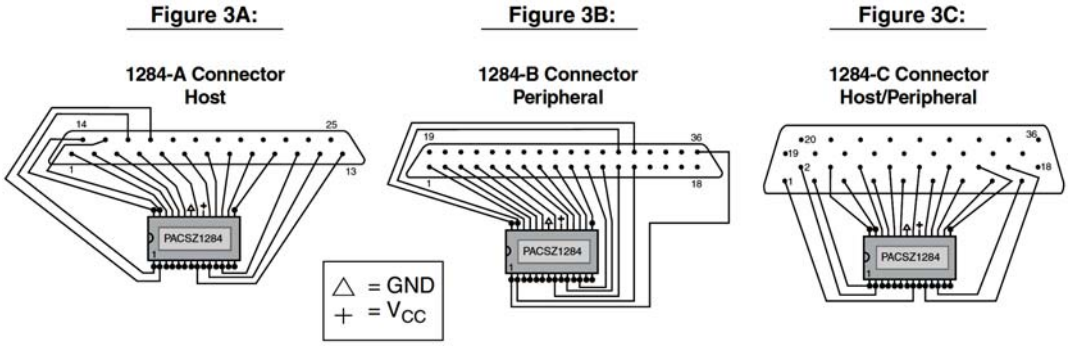



**Figure 3. Example Connections of IEEE 1284 Connectors with PACSZ1284**

Table 6 provides the IEEE 1284 signal assignments for the three connectors, and example PACSZ1284 pin connections.

When connecting a 1284−A host to a 1284−B peripheral, the “Peripheral Logic High” signal is not used. Similarly, when a 1284−A host is connected to a 1284−C peripheral, the “Peripheral Logic High” and “Host Logic High” are not used. These two signals are optionally used to detect a “Power Off” or “Cable Disconnect” state for host and peripheral, respectively.

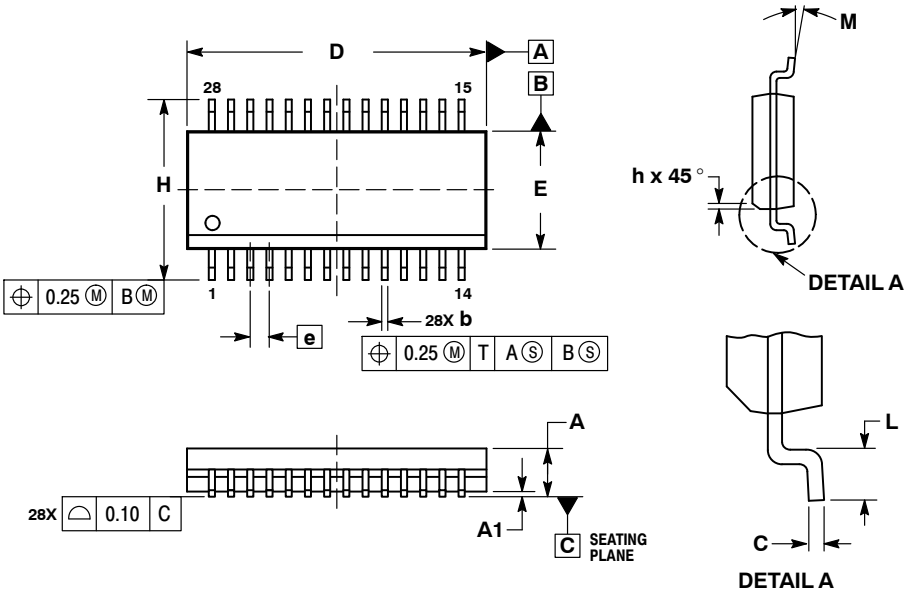
## APPLICATION INFORMATION (Cont'd)

**Table 6. IEEE 1284 CONNECTOR PINOUTS AND PACSZ1284 CONNECTION GUIDELINES**

| PACSZ1284 Pin Type | 1284−A 25−Pin DSUB | | 1284−B 36−Pin Champ | | 1284−C 36−Pin High Density | |
|---|---|---|---|---|---|---|
| | Signal | Pin | Signal | Pin | Signal | Pin |
| P−Port Conn. Side, Series−Terminated (16−19, 21, or 23−26) | STROBE | 1 | STROBE | 1 | STROBE | 15 |
| P−Port Conn. Side, Series−Terminated (16−19, 21, or 23−26) | Data 1 | 2 | Data 1 | 2 | Data 1 | 6 |
| P−Port Conn. Side, Series−Terminated (16−19, 21, or 23−26) | Data 2 | 3 | Data 2 | 3 | Data 2 | 7 |
| P−Port Conn. Side, Series−Terminated (16−19, 21, or 23−26) | Data 3 | 4 | Data 3 | 4 | Data 3 | 8 |
| P−Port Conn. Side, Series−Terminated (16−19, 21, or 23−26) | Data 4 | 5 | Data 4 | 5 | Data 4 | 9 |
| P−Port Conn. Side, Series−Terminated (16−19, 21, or 23−26) | Data 5 | 6 | Data 5 | 6 | Data 5 | 10 |
| P−Port Conn. Side, Series−Terminated (16−19, 21, or 23−26) | Data 6 | 7 | Data 6 | 7 | Data 6 | 11 |
| P−Port Conn. Side, Series−Terminated (16−19, 21, or 23−26) | Data 7 | 8 | Data 7 | 8 | Data 7 | 12 |
| P−Port Conn. Side, Series−Terminated (16−19, 21, or 23−26) | Data 8 | 9 | Data 8 | 9 | Data 8 | 13 |
| Capacitor−Filtered (1, 2, 8, 10, 12, 15, 27, or 28) | ACK | 10 | ACK | 10 | ACK | 3 |
| Capacitor−Filtered (1, 2, 8, 10, 12, 15, 27, or 28) | BUSY | 11 | BUSY | 11 | BUSY | 1 |
| Capacitor−Filtered (1, 2, 8, 10, 12, 15, 27, or 28) | PError | 12 | PError | 12 | PError | 5 |
| Capacitor−Filtered (1, 2, 8, 10, 12, 15, 27, or 28) | Select | 13 | Select | 13 | Select | 2 |
| Capacitor−Filtered (1, 2, 8, 10, 12, 15, 27, or 28) | AUTOFD | 14 | AUTOFD | 14 | AUTOFD | 17 |
| Capacitor−Filtered (1, 2, 8, 10, 12, 15, 27, or 28) | FAULT | 15 | FAULT | 32 | FAULT | 4 |
| Capacitor−Filtered (1, 2, 8, 10, 12, 15, 27, or 28) | INIT | 16 | INIT | 31 | INIT | 14 |
| Capacitor−Filtered (1, 2, 8, 10, 12, 15, 27, or 28) | Selectin | 17 | Selectin | 36 | Selectin | 16 |
| | Ground | 18 | Ground | 19 | Ground | 19 |
| | Ground | 19 | Ground | 20 | Ground | 20 |
| | Ground | 20 | Ground | 21 | Ground | 21 |
| | Ground | 21 | Ground | 22 | Ground | 22 |
| | Ground | 22 | Ground | 23 | Ground | 23 |
| | Ground | 23 | Ground | 24 | Ground | 24 |
| | Ground | 24 | Ground | 25 | Ground | 25 |
| | Ground | 25 | Ground | 26 | Ground | 26 |
| | | | Ground | 27 | Ground | 27 |
| | | | Ground | 28 | Ground | 28 |
| | | | Ground | 29 | Ground | 29 |
| | | | Ground | 30 | Ground | 30 |
| | | | Not Defined | 33 | Ground | 31 |
| | | | Not Defined | 34 | Ground | 32 |
| | | | Not Defined | 35 | Ground | 33 |
| | | | Not Defined | 15 | Ground | 34 |
| | | | Logic Ground | 16 | Ground | 35 |
| | | | Chassis GND | 17 | Not Required | 36 |
| | | | Peripheral Logic | 18 | Host Logic High | 18 |

## PACKAGE DIMENSIONS

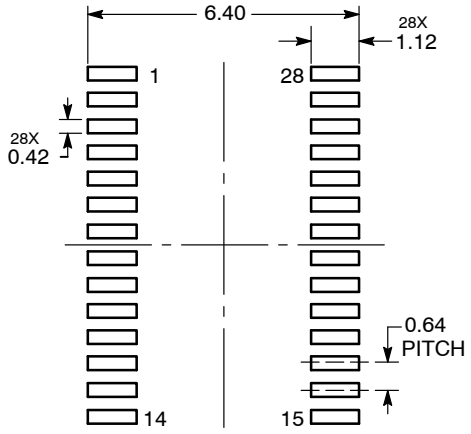
**QSOP28 NB**
CASE 492AA−01
ISSUE O




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS OR FLASH. END FLASH SHALL NOT EXCEED 0.25 PER SIDE.

| | MILLIMETERS | |
|---|---|---|
| DIM | MAX | MIN |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| b | 0.20 | 0.30 |
| C | 0.19 | 0.25 |
| D | 9.80 | 10.00 |
| E | 3.80 | 4.00 |
| e | 0.635 BSC | |
| H | 5.79 | 6.20 |
| h | 0.22 | 0.50 |
| L | 0.40 | 1.27 |
| M | 0 ° | 8 ° |

### SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS



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