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**ANTI-SATURATION FILTERLESS 2W CLASS-D STEREO AMPLIFIER
WITH DC VOLUME CONTROL AND MAX OUTPUT POWER SETTING**

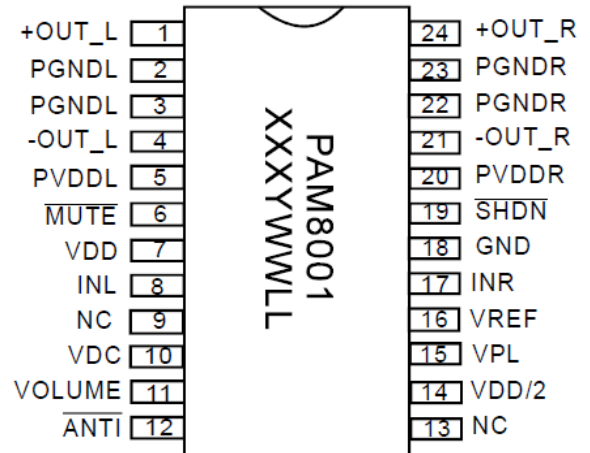
Description

The PAM8001 is a 2W, class-D audio amplifier. Advanced 64-step DC volume control minimizes external components and allows speaker volume control. PAM unique anti-saturation technology which detects output signal clip due to the over level input signal suppress the output signal clip automatically. Also control the gain for set max power. It can protect low wattage speaker from overdrive damage even same platform with high wattage model. It offers low THD+N, to produce high-quality sound reproduction. The new filterless architecture allows the device to drive the speaker directly, without low-pass output filters which will save system cost and PCB area.

With the same numbers of external components, the efficiency of the PAM8001 is much better than class-AB cousins. It can extend the battery life thus be ideal for portable applications.

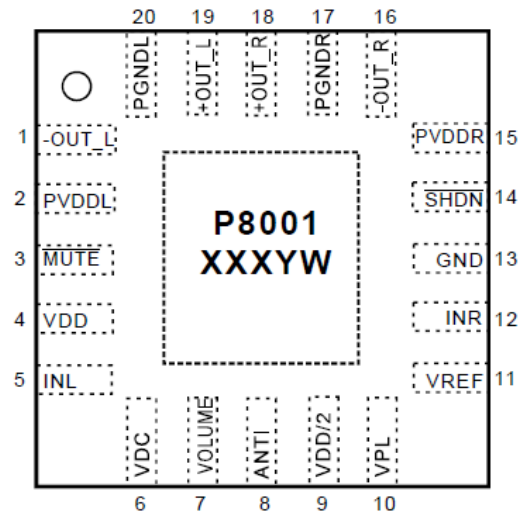
The PAM8001 is available in SSOP-24L and QFN3*3-20L package.

Pin Assignments



Features

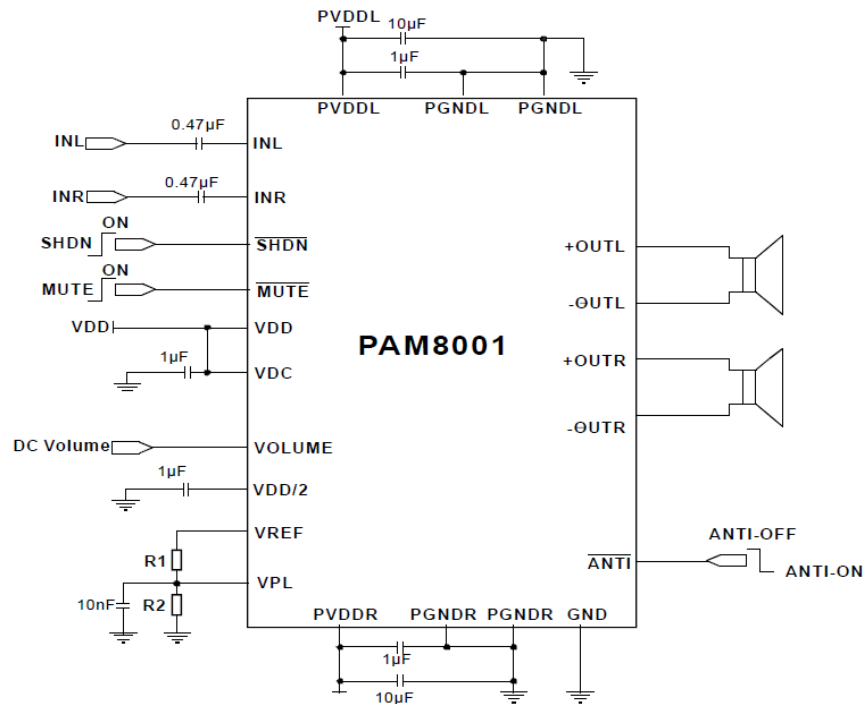
- 2W Output at 1% THD with a 4Ω Load at 5V Power Supply
- Filterless, Low Quiescent Current and Low EMI
- Low THD+N
- 64-Step DC Volume Control
- Unique Anti-Saturation Function
- Adjustable Max Output Power with No Clipping
- Superior Low Noise
- Low Pop Noise
- Efficiency up to 90%
- Short Circuit Protection
- Thermal Shutdown
- Few External Components to Save the Space and Cost
- Pb-Free Package



Applications

- LCD Monitors / TV Projectors
- Notebook Computers
- Portable Speakers
- Portable DVD Players, Game Machines
- VoIP/Speaker Phones
- All In One Computer /TV

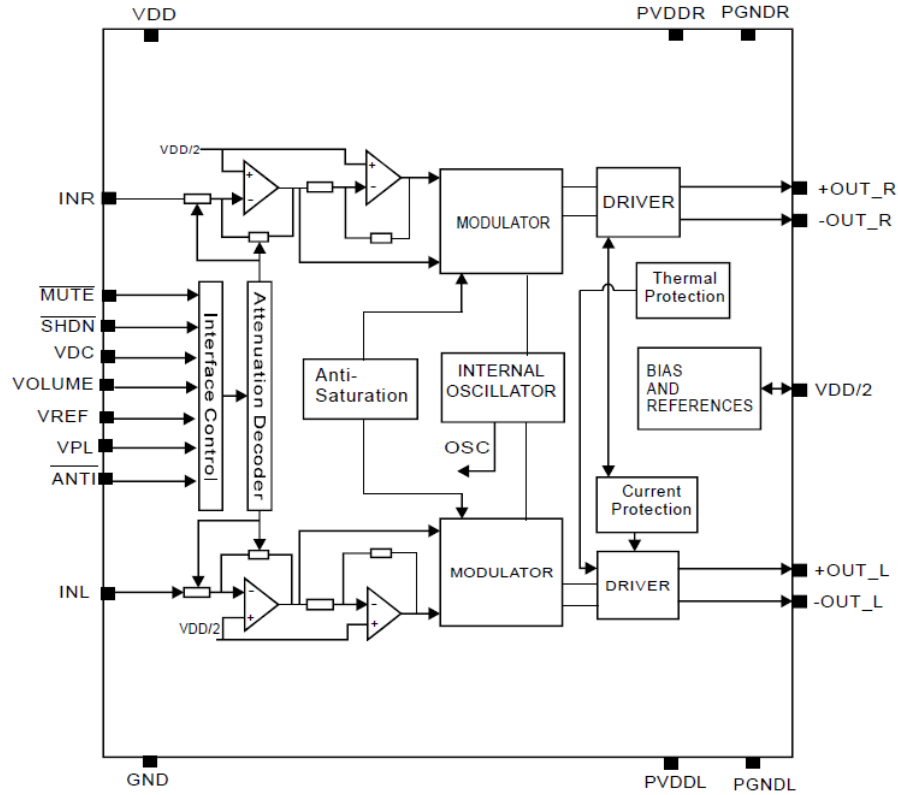
Typical Applications Circuit



Pin Descriptions

| Pin Number | | Pin Name | Function |
|------------|-------|--------------------------|---|
| QFN3x3 | SSOP | | |
| 1 | 4 | -OUT_L | Left Channel Negative Output |
| 2 | 5 | PVDDL | Left Channel Power Supply |
| 3 | 6 | $\overline{\text{MUTE}}$ | Mute Control Input (active low) |
| 4 | 7 | VDD | Analog VDD |
| 5 | 8 | INL | Left Channel Input |
| 6 | 10 | VDC | Analog Reference for Gain Control Selection |
| 7 | 11 | VOLUME | DC Volume Control to Set the Gain of Class-D |
| 8 | 12 | ANTI | Anti-Saturation On/Off Control |
| 9 | 14 | VDD/2 | Internal Common Mode Voltage, Connect a Bypass Capacitor from This Pin to GND |
| 10 | 15 | VPL | Maximum Output Power Setting Voltage |
| 11 | 16 | VREF | Reference Voltage Out for VPL |
| 12 | 17 | INR | Right Channel Input |
| 13 | 18 | GND | Analog Ground |
| 14 | 19 | $\overline{\text{SHDN}}$ | Shutdown Control Input (active low) |
| 15 | 20 | PVDDR | Right Channel Power Supply |
| 16 | 21 | -OUT_R | Right Channel Negative Output |
| 17 | 22/23 | PGNDR | Right Channel Power GND |
| 18 | 24 | +OUT_R | Right Channel Positive Output |
| 19 | 1 | +OUT_L | Left Channel Positive Output |
| 20 | 2/3 | PGNDL | Left Channel Power GND |
| | 9/13 | NC | No Connection |

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

| Parameter | Rating | Unit |
|--------------------------------|------------------------------|------|
| Supply Voltage | 6.0 | V |
| Input Voltage | -0.3 to V _{DD} +0.3 | |
| Operation Junction Temperature | -40 to +125 | °C |
| Storage Temperature | -65 to +150 | |
| Soldering Temperature | 300, 5sec | |

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

| Parameter | Rating | Unit |
|-------------------------------------|-------------|------|
| Supply Voltage Range | 2.5 to 5.5 | V |
| Junction Temperature Range | -40 to +125 | °C |
| Ambient Operation Temperature Range | -20 to +85 | |

Thermal Information

| Parameter | Symbol | Package | Maximum | Unit |
|--|---------------|------------|---------|------|
| Thermal Resistance (Junction to Ambient) | θ_{JA} | SSOP-24L | 96 | °C/W |
| Thermal Resistance (Junction to Ambient) | θ_{JA} | QFN3*3-20L | 31 | °C/W |

Electrical Characteristics (V_{DD} = 5V, Gain = Maximum, R_L = 8Ω, @T_A = +25°C, unless otherwise specified.)

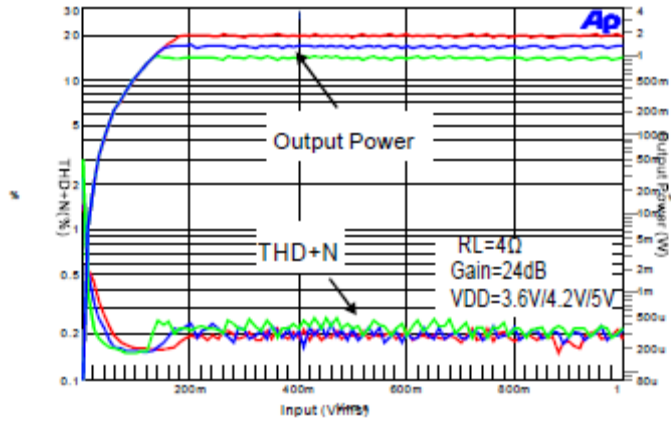
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|--------------------------------------|--|---------------------|-------|--------|------|
| V _{DD} | Supply Voltage Range | | 2.5 | | 5.5 | V |
| I _Q | Quiescent Current | No Load | | 11.5 | 15 | mA |
| V _{OS} | Output Offset Voltage | V _{IN} = 0V | | 20 | | mV |
| R _{DS(ON)} | Drain-Source On-State Resistance | I _{DS} = 0.5A | P MOSFET | 0.21 | | Ω |
| | | | N MOSFET | 0.165 | | |
| P _O | Output Power with Anti-Saturation | THD+N <1% f = 1kHz, V _{PL} = 1V | R _L = 8Ω | 1 | | W |
| | | | R _L = 4Ω | 1.9 | | |
| P _O | Output Power without Anti-Saturation | THD+N <10% f = 1kHz, V _{PL} = 1.5V | R _L = 8Ω | 1.35 | 1.5 | W |
| | | | R _L = 4Ω | 2.65 | 2.8 | |
| THD+N | Total Harmonic Distortion Plus Noise | R _L = 8Ω, P _O = 0.85W, f = 1kHz | | 0.08 | | % |
| | | R _L = 4Ω, P _O = 1.75W, f = 1kHz | | 0.08 | | |
| PSRR | Power Supply Ripple Rejection | Input AC-GND, f = 1KHz, V _{PP} = 200mV, Gain = 6dB | | 70 | | dB |
| CS | Channel Separation | P _O = 1W, f = 1KHz | | -85 | | dB |
| f _{OSC} | Oscillator Frequency | | 200 | 250 | 300 | kHz |
| η | Efficiency | P _O = 1.7W, f = 1KHz, R _L = 8Ω | 85 | 89 | | % |
| | | P _O = 3.0W, f = 1KHz, R _L = 4Ω | 80 | 83 | | % |
| V _n | Noise | Input AC-GND Gain = 6dB | A-Weighting | 50 | | μV |
| | | | No A-Weighting | 70 | | |
| SNR | Signal Noise Ratio | f = 20-20kHz, Gain = 6dB | | 85 | | dB |
| UVLO | Under Voltage Lock-Out | | | 2.0 | | V |
| I _{MUTE} | Mute Current | V _{MUTE} = 0.3V | | 4.2 | | mA |
| I _{SHDN} | Shutdown Current | V _{SHDN} = 0V | | | 1 | μA |
| V _{SH} | $\overline{\text{SHDN}}$ Input High | | 1.3 | | | V |
| V _{SL} | $\overline{\text{SHDN}}$ Input Low | | | | 0.65 | V |
| V _{MH} | $\overline{\text{MUTE}}$ Input High | | 1.3 | | | V |
| V _{ML} | $\overline{\text{MUTE}}$ Input Low | | | | 0.66 | V |
| V _{PL} | V _{PL} Threshold Voltage | Power Limit Off | | 1.5 | Note 1 | V |
| V _{REF} | V _{REF} Voltage | V _{DD} = 2.5V to 5.5V | | 1.2 | | V |
| I _D | V _{REF} Drive Current | V _{DD} = 2.5V to 5.5V | | | 150 | μA |
| OTP | Over Temperature Protection | | | 150 | | °C |
| OTH | Over Temperature Hysteresis | | | 30 | | °C |

Note: 1. Maximum Output Power vs. V_{PL} Voltage
V_{DD} = 5V, R_L = 4Ω, T_A = +25°C

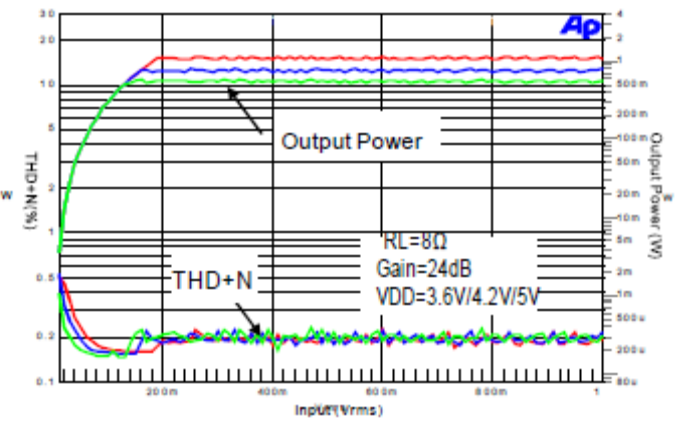
| | | | | | | | | | | | | | | |
|---------------------|---|------|------|------|------|------|------|------|------|------|------|------|------|------|
| V _{PL} (V) | 0 | 0.1 | 0.2 | 0.3 | 0.4 | 0.5 | 0.6 | 0.7 | 0.8 | 0.9 | 1.0 | 1.1 | 1.2 | >1.5 |
| P _O (W) | 0 | 0.04 | 0.11 | 0.21 | 0.34 | 0.50 | 0.68 | 0.94 | 1.28 | 1.52 | 1.90 | 2.15 | 2.40 | 2.8 |

Typical Operating Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

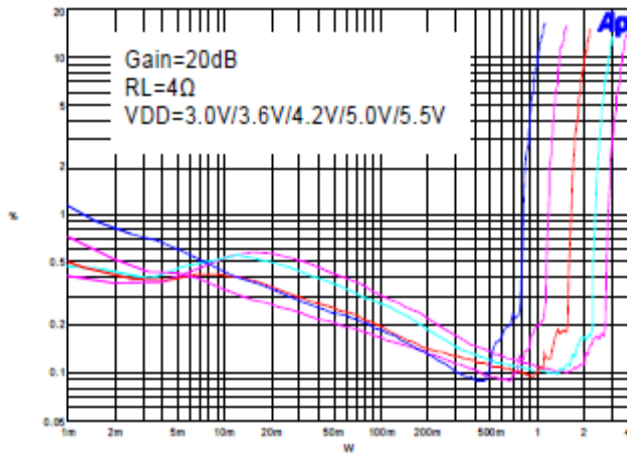
1. THD+N vs Output Power vs Input



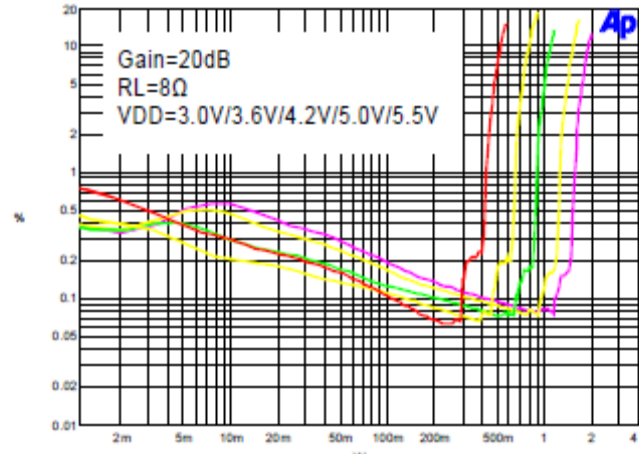
2. THD+N vs Output Power vs Input



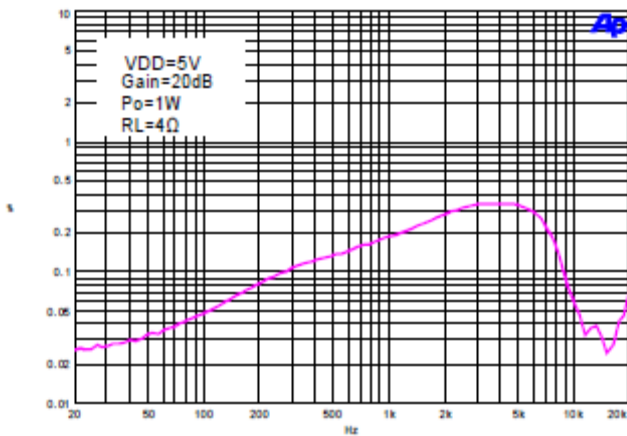
3. THD+N vs Output Power



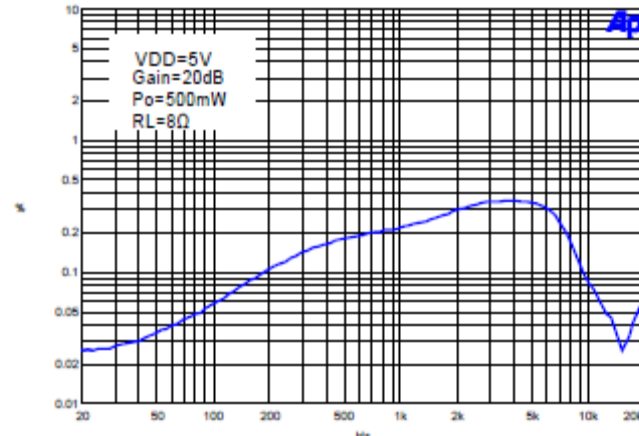
4. THD+N vs Output Power



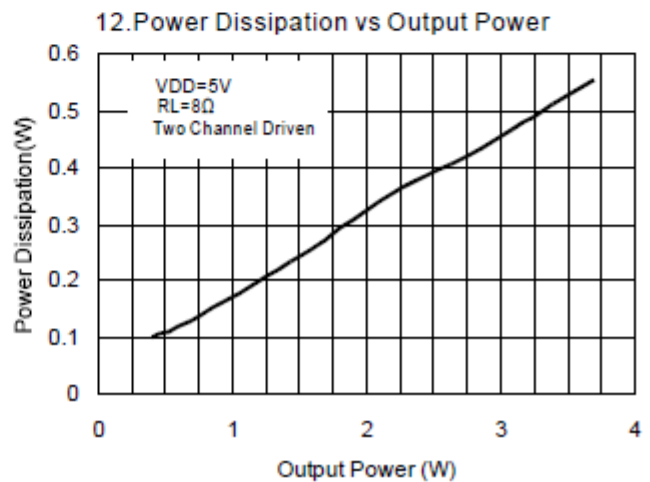
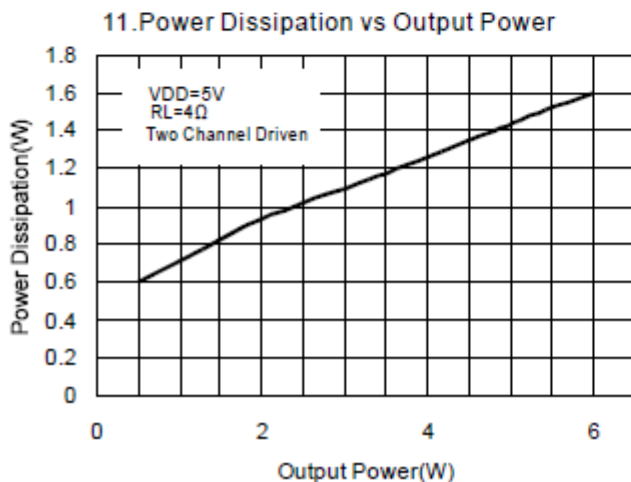
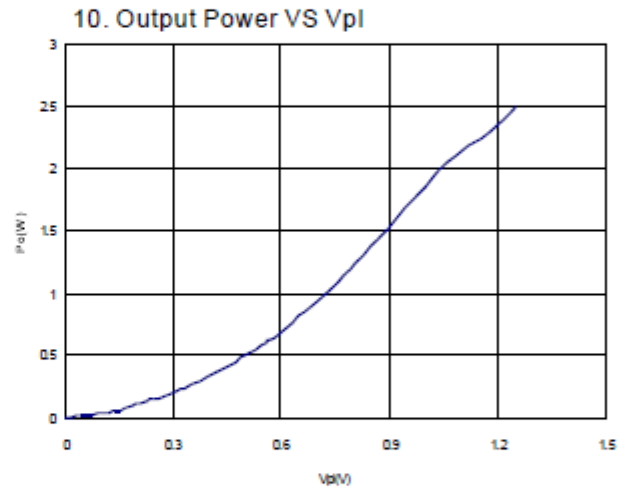
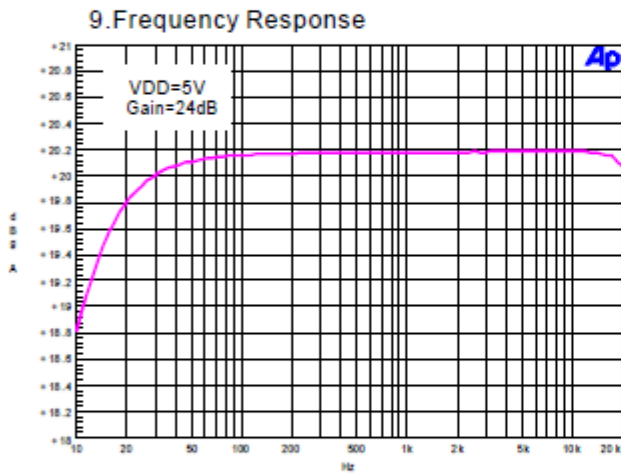
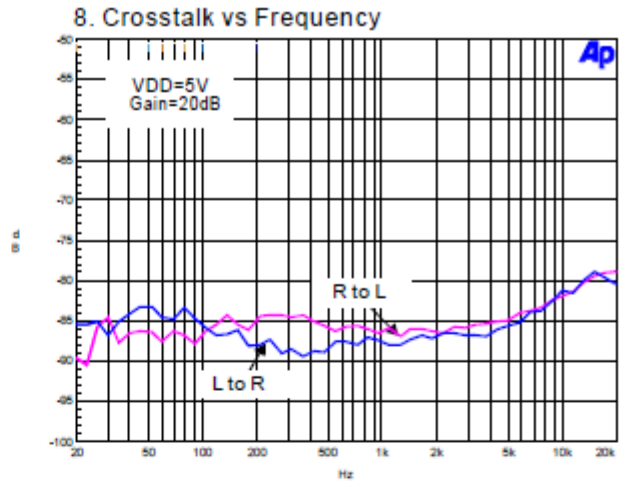
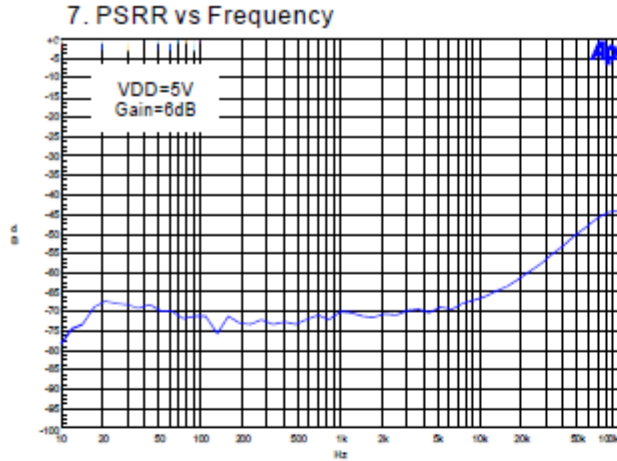
5. THD+N vs Frequency



6. THD+N vs Frequency

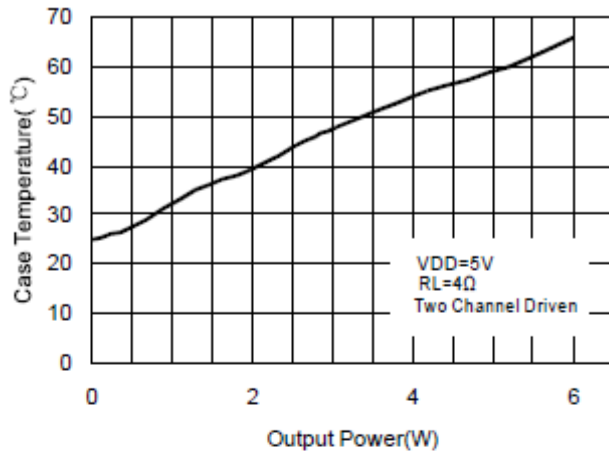


Typical Operating Characteristics (cont.) (@T_A = +25°C, unless otherwise specified.)

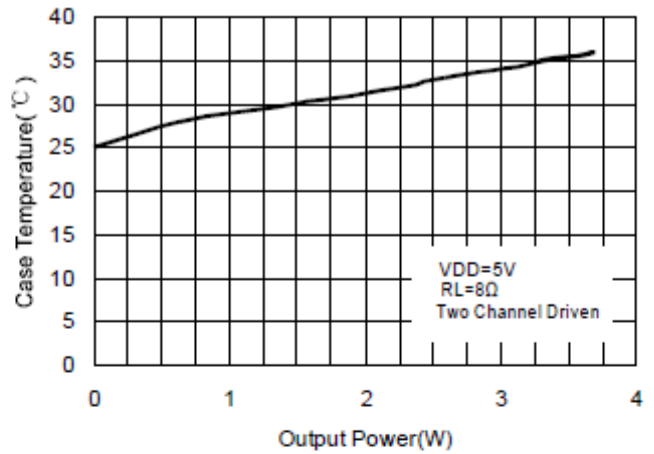


Typical Operating Characteristics (cont.) (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

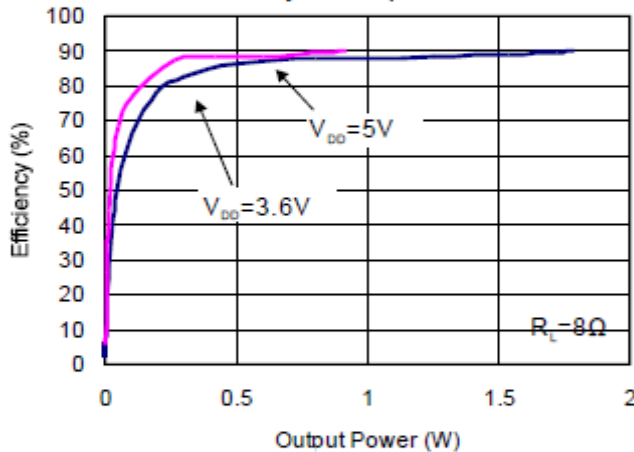
13. Case Temperature vs Output Power



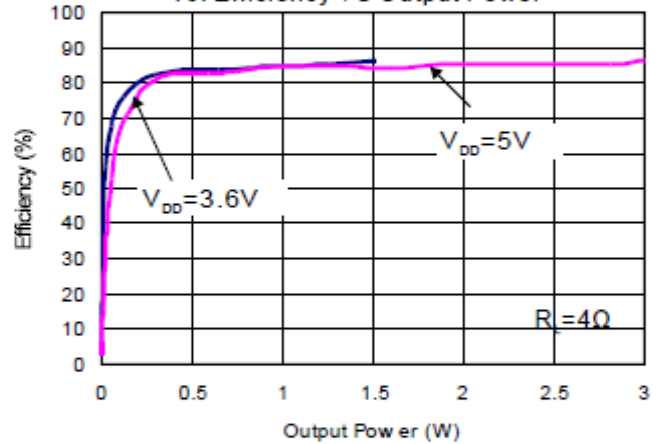
14. Case Temperature vs Output Power



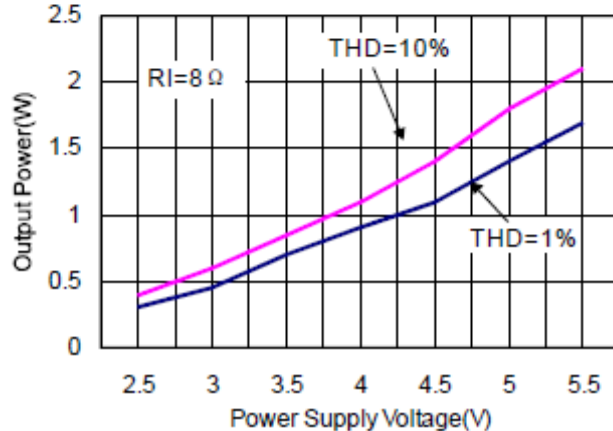
15. Efficiency VS Output Power



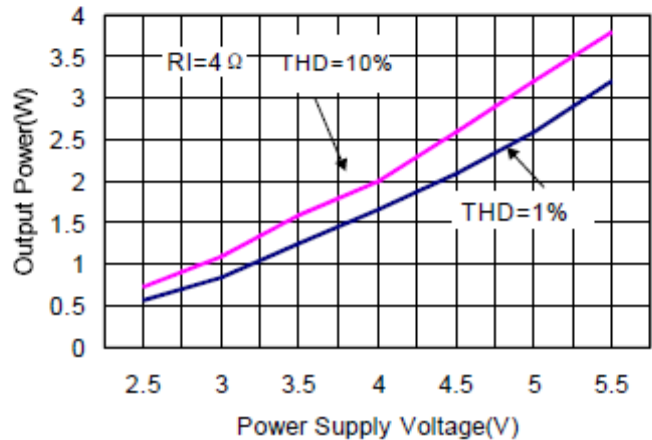
16. Efficiency VS Output Power



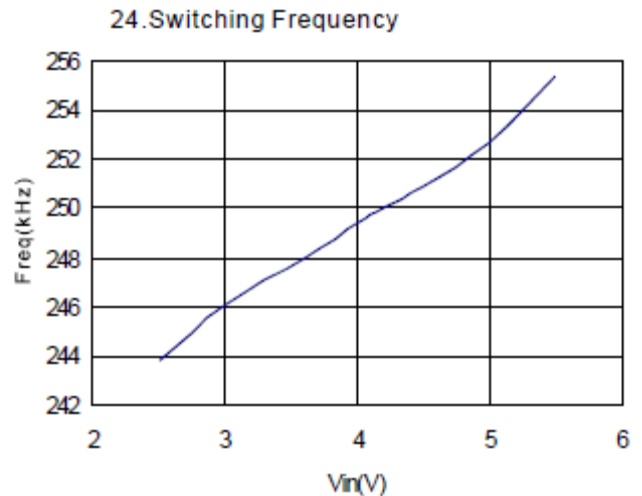
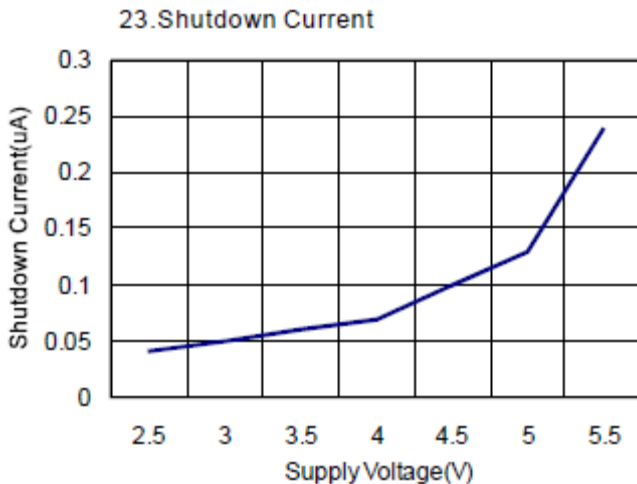
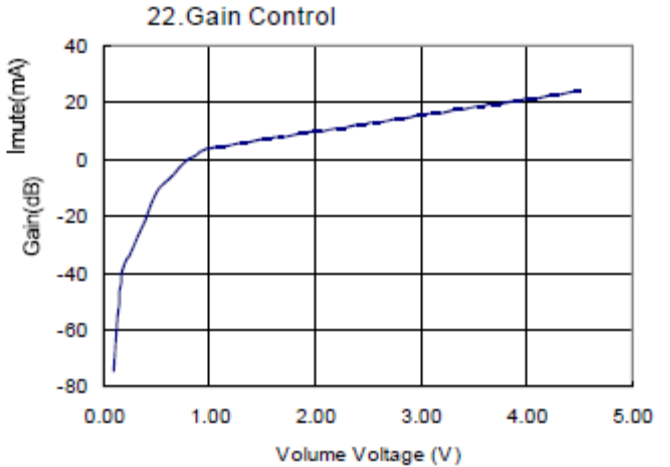
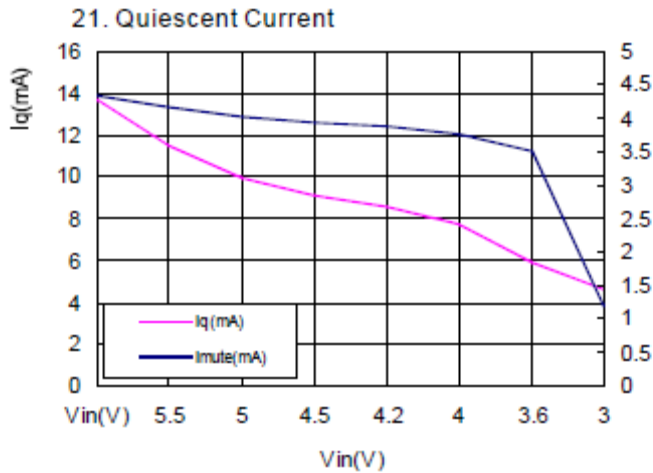
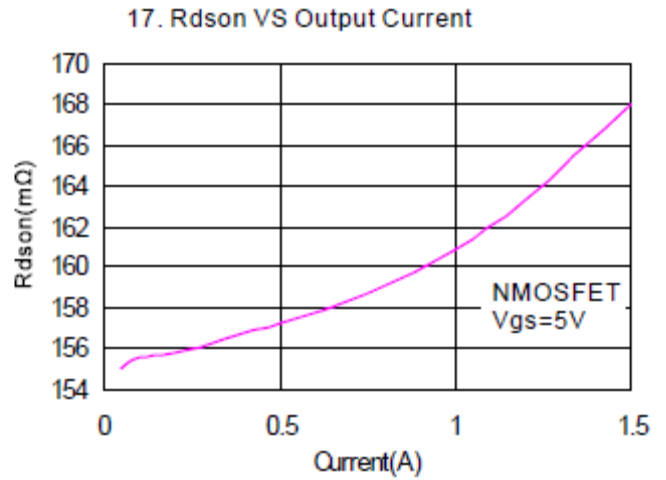
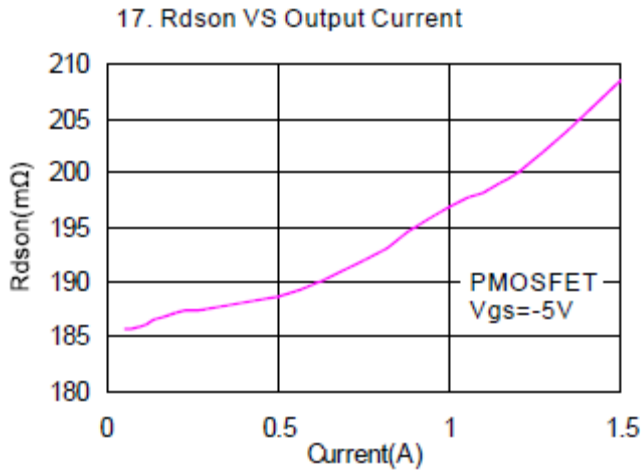
17. Output Power VS Supply Voltage



18. Output Power VS Supply Voltage



Typical Operating Characteristics (cont.) (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)



Typical Operating Characteristics (cont.) (@T_A = +25°C, unless otherwise specified.)

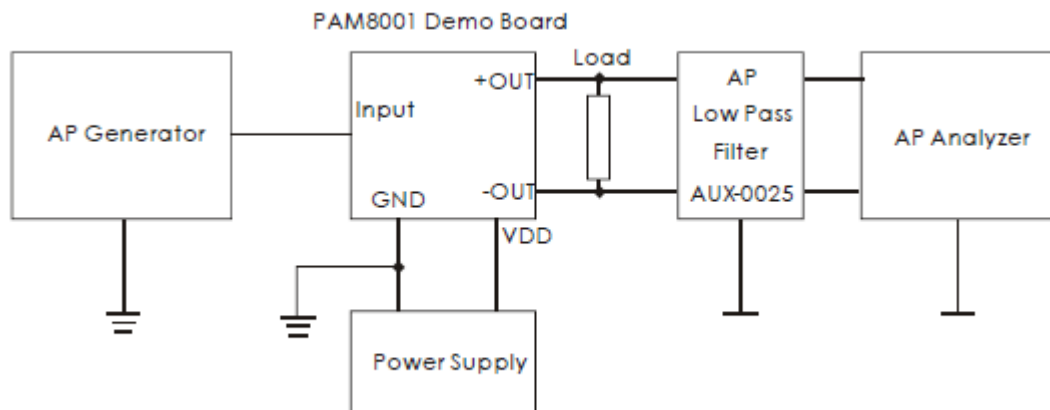
Table 1 DC Volume Control

| STEP | Gain (dB) | STEP | Gain (dB) |
|------|-----------|------|-----------|
| 0 | -75 | 32 | 11.6 |
| 1 | -40 | 33 | 12.0 |
| 2 | -34 | 34 | 12.4 |
| 3 | -28 | 35 | 12.8 |
| 4 | -22 | 36 | 13.2 |
| 5 | -16 | 37 | 13.6 |
| 6 | -10 | 38 | 14.0 |
| 7 | -7.5 | 39 | 14.4 |
| 8 | -5.0 | 40 | 14.8 |
| 9 | -2.5 | 41 | 15.2 |
| 10 | 0 | 42 | 15.6 |
| 11 | 1.5 | 43 | 16.0 |
| 12 | 3.0 | 44 | 16.4 |
| 13 | 4.0 | 45 | 16.8 |
| 14 | 4.4 | 46 | 17.2 |
| 15 | 4.8 | 47 | 17.6 |
| 16 | 5.2 | 48 | 18.0 |
| 17 | 5.6 | 49 | 18.4 |
| 18 | 6.0 | 50 | 18.8 |
| 19 | 6.4 | 51 | 19.2 |
| 20 | 6.8 | 52 | 19.6 |
| 21 | 7.2 | 53 | 20.0 |
| 22 | 7.6 | 54 | 20.4 |
| 23 | 8.0 | 55 | 20.8 |
| 24 | 8.4 | 56 | 21.2 |
| 25 | 8.8 | 57 | 21.6 |
| 26 | 9.2 | 58 | 22.0 |
| 27 | 9.6 | 59 | 22.4 |
| 28 | 10.0 | 60 | 22.8 |
| 29 | 10.4 | 61 | 23.2 |
| 30 | 10.8 | 62 | 23.6 |
| 31 | 11.2 | 63 | 24.0 |

Application Information

1. When the PAM8001 works with LC filters, it should be connected with the speaker before it's powered on, otherwise it will be damaged easily.
2. When the PAM8001 works without LC filters, it's better to add a ferrite chip bead at the outgoing line of speaker for suppressing the possible electro magnetic interference.
3. The absolute maximum rating of the PAM8001 operation voltage is 6.0V. When the PAM8001 is powered with 4 battery cells, it should be noted that the voltage of 4 new dry or alkaline batteries is over 6V, higher than its maximum operation voltage, which probably make the device damaged. Therefore, it's recommended to use either 4 Ni-MH (Nickel Metal Hydride) rechargeable batteries or 3 dry or alkaline batteries.
4. The input signal should not be too high, if too high, it will cause the clipping of output signal when increasing the volume. Because the DC volume control of the PAM8001 has big gain, it will make the device damaged.
5. When testing the PAM8001 without LC filters by using resistor instead of speaker as the output load, the test results, e.g. THD or efficiency, will be worse than those using speaker as load.

Test Setup for Performance Testing



- Notes:
1. The AP AUX-0025 low pass filter is necessary for class-D amplifier measurement with AP analyzer.
 2. Two 22 μ H inductors are used in series with load resistor to emulate the small speaker for efficiency measurement.

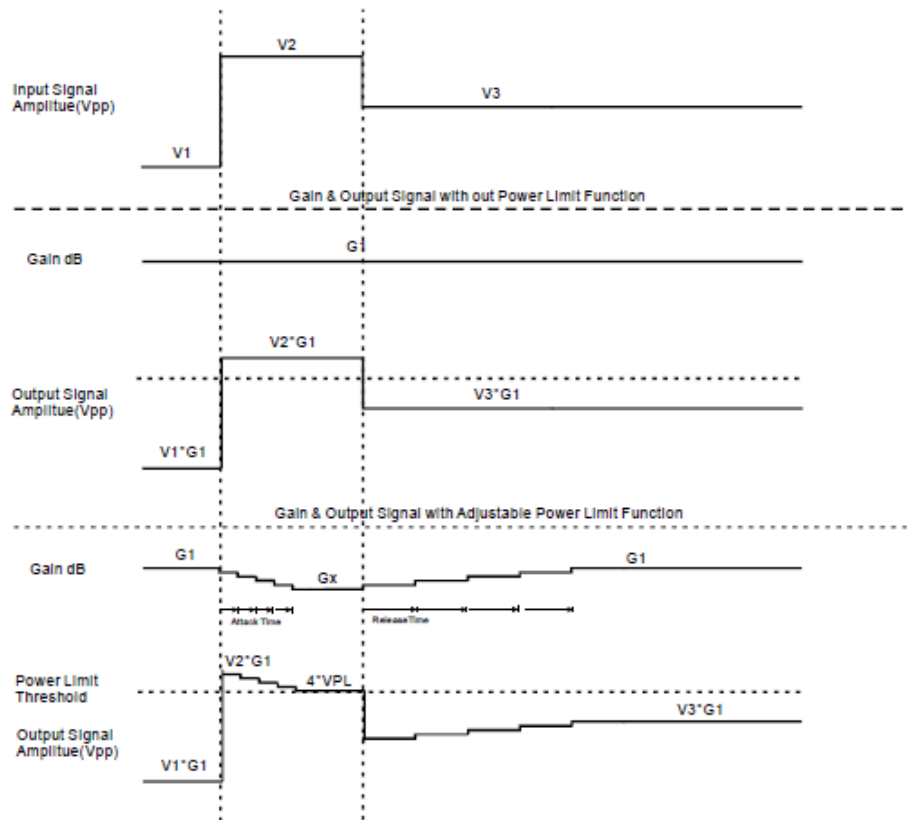
Description of Adjustable Power Limit with Anti-Saturation

Adjustable power limit provides AGC to the amplifier and limit the Maximum Output Power.

The behavior of power limit function showing as below.

The power limit control detect output signal amplitude continuously, when the peak output is excised limit threshold (setting by external resistor).Control system will decrease the one step gain(typical -0.5dB). Then attack time is reset for next gain decrease. The control system will decrease the gain step by step until the peak output signal equal to the threshold level. After these, when the input signal's amplitude decreased or DC volume control reduced the amplifier's gain or happened together, the control system will calculate the ideal output level. When that level lower then limit threshold , the will start to recovery to the original gain (which is setting by DC volume control).The first release step is no delay, reset with release time per step.

Application Information (cont.)



| Variable | Description | Typical Value | Unit |
|-------------------------|--|---------------|---------|
| VPL | Voltage for power limit voltage, Setting by external resistor divider | 0.4 to 1.2 | V |
| Gain Range | Adjustable gain range of power limit and anti-saturation function | 75 | dB |
| Gain Step Size | Gain step size for adjustable power limit and anti-saturation function | Note 2 | dB |
| Attack Time (per step) | The minimum time between two gain decrements. (per step) | 32 | μ S |
| Release Time (per step) | The minimum time between two gain increments. (per step) | 250 | mS |

Note: 2. Please contact Diodes for detail information.

Anti-Saturation Function

If the preset gain is higher than power set, anti-saturation is active by detecting the duty cycle of the PWM output. When the mode has been detected, the gain is automatically adjusted to the value that the output is not clip step by step. The attach is immediate and the release time is 250mS per step.

MUTE Operation

The **MUTE** pin is an input for controlling the output state of the PAM8001. A logic low on this pin disables the outputs, and a logic high on this pin enables the outputs. This pin may be used as a quick disable or enable of the outputs without a volume fade. Quiescent current is listed in the electrical characteristic table. The **MUTE** pin can be left floating due to the internal pull-up

Shutdown Operation

In order to reduce power consumption while not in use, the PAM8001 contains shutdown circuitry to turn off amplifier's bias circuitry. The amplifier is turned off when logic low is placed on the **SHDN** pin. By switching the **SHDN** pin connected to GND, the PAM8001 supply current draw will be minimized in idle mode. The **SHDN** pin can be left floating due to the internal pull-up.

Application Information (cont.)

For the best power on/off pop performance, the amplifier should be placed in the Mute mode prior to turning on/off the power supply.

Power Supply Decoupling

The PAM8001 is a high performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output THD and PSRR are as low as possible. Power supply decoupling affects low frequency on the power supply leads. For higher frequency response, optimum decoupling is achieved by using two capacitors of different types that target different types of noise frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1.0 μ F, placed as close as possible to the device V_{DD} terminal works best. For filtering lower-frequency noise signals, a large capacitor of 10 μ F (ceramic) or greater placed near the audio power amplifier is recommended.

Input Capacitor (C_i)

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance. In this case, input capacitor (C_i) and input resistance (R_i) of the amplifier form a high-pass filter with the corner frequency determined equation below,

$$f_c = \frac{1}{2\pi R_i C_i}$$

In addition to system cost and size, click and pop performance is affected by the size of the input coupling capacitor, C_i . A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally $\frac{1}{2} V_{DD}$). This charge comes from the internal circuit via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Analog Reference Bypass Capacitor (C_{BYP})

The Analog Reference Bypass Capacitor (C_{BYP}) at $V_{DD}/2$ pin, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. The noise is from the internal analog reference to the amplifier, which appears as degraded PSRR and THD+N.

A ceramic bypass capacitor (C_{BYP}) of 0.47 μ F to 1.0 μ F is recommended for the best THD and noise performance. Increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering leaving shutdown.

Under Voltage Lock-Out (UVLO)

The PAM8001 incorporates circuitry designed to detect when supply voltage is low. When the supply voltage drops to 1.8V or below, the PAM8001 outputs are disabled and the device comes out of this state and states to normal functional once $V_{DD} \geq 2.0V$.

Short Circuit Protection (SCP)

The PAM8001 has short circuit protection circuitry on the outputs that prevents the device from damage when output-to-output and output-to-GND short. When a short circuit is detected on the outputs, the outputs are disabled immediately. If the short was removed, the device activates again.

Over Temperature Protection

Thermal protection on the PAM8001 prevents the device from damage when the internal die temperature exceeds 150°C. There is a 15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 30°C. This large hysteresis will prevent motor boating sound well. The device begins normal operation at this point without external system interaction.

Application Information (cont.)

How to Reduce EMI (Electro Magnetic Interference)

A simple solution is to put an additional capacitor 1000uF at power supply terminal for power line coupling if the traces from amplifier to speakers are short (<20CM).

Most applications require a ferrite bead filter as shown at Figure 1. The ferrite filter reduces EMI around 1 MHz and higher. When selecting a ferrite bead, choose one with high impedance at high frequencies, and low impedance at low frequencies (MH2012HM221-T).

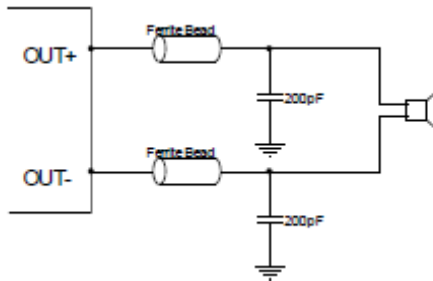


Figure 1 Ferrite Bead Filter to Reduce EMI

PCB Layout Guidelines Grounding

At this stage it is paramount to notice the necessity of separate grounds. Noise currents in the output power stage need to be returned to output noise ground and nowhere else. Were these currents to circulate elsewhere, they may get into the power supply, the signal ground, etc, worse yet, they may form a loop and radiate noise. Any of these cases results in degraded amplifier performance. The logical returns for the output noise currents associated with Class-D switching are the respective PGND pins for each channel. The switch state diagram illustrates that PGND is instrumental in nearly every switch state. This is the perfect point to which the output noise ground trace should return. Also note that output noise ground is channel specific. A two channel amplifier has two separate channels and consequently must have two separate output noise ground traces. The layout of the PAM8001 offers separate PGND connections for each channel and in some cases each side of the bridge. Output noise grounds must be tied to system ground at the power in exclusively. Signal currents for the inputs, reference, etc need to be returned to quite ground. This ground is only tied to the signal components and the GND pin, and GND then tied to system ground.

PCB Layout Example

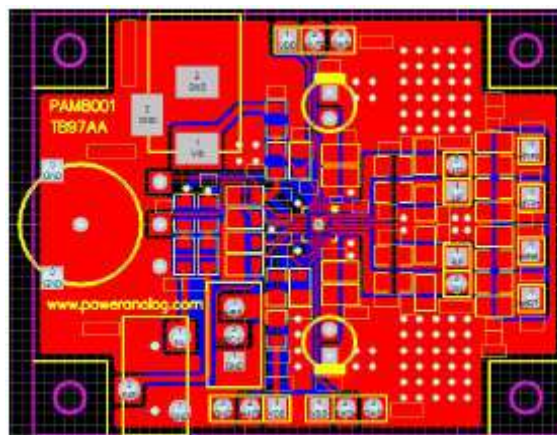
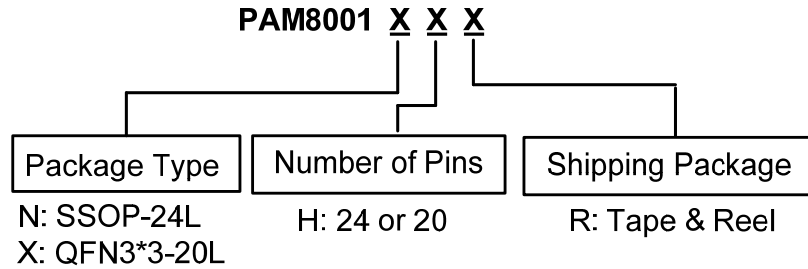


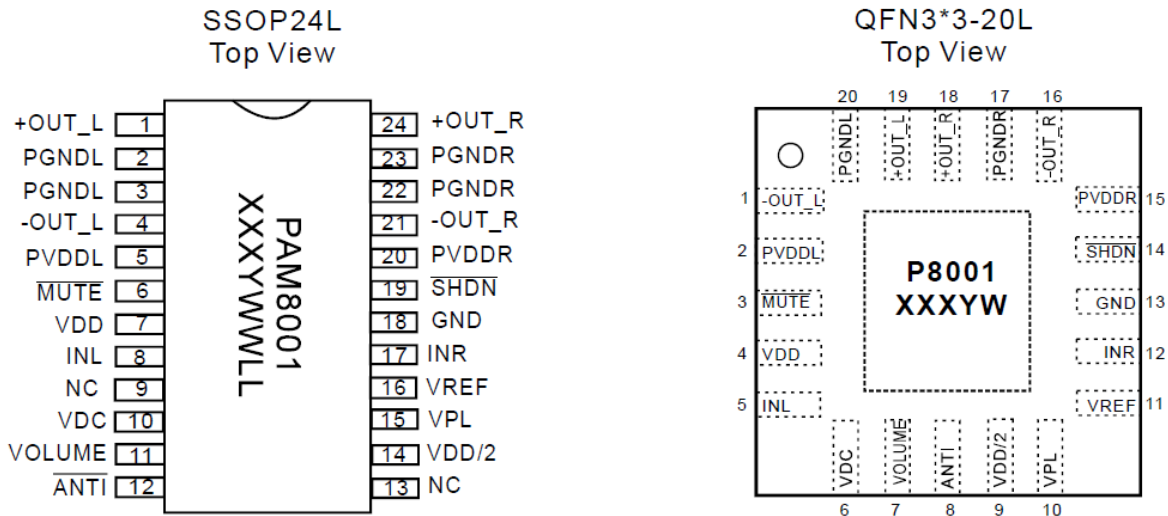
Figure 2 Top Layer

Ordering Information



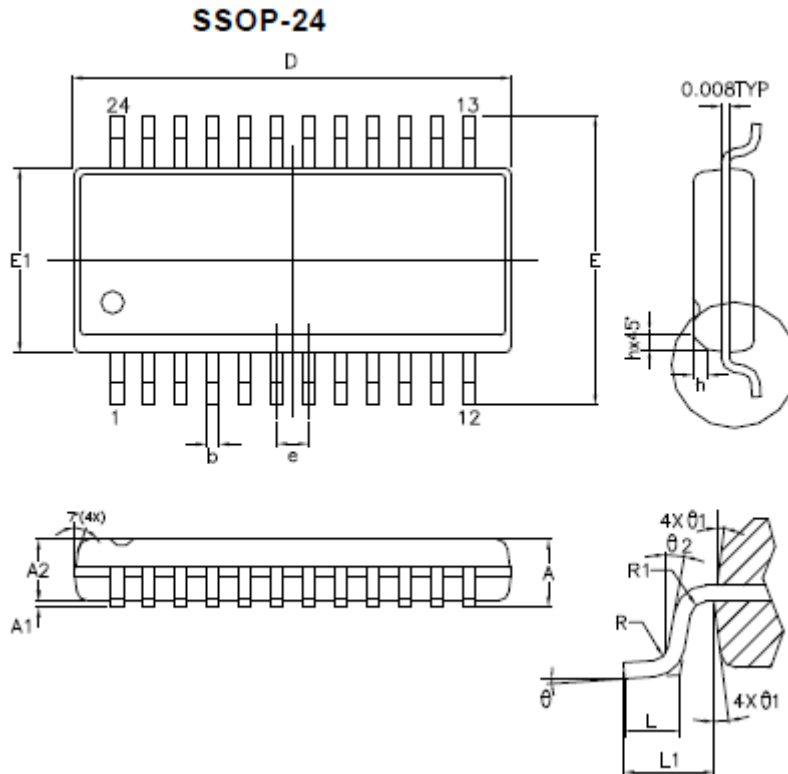
| Part Number | Package Type | Standard Package |
|-------------|--------------|------------------------|
| PAM8001NHR | SSOP-24L | 2500 Units/Tape & Reel |
| PAM8001XHR | QFN3*3-20L | 2500 Units/Tape & Reel |

Marking Information



X: Internal Code
Y: Year
W: Week
L: Internal Code

Package Outline Dimensions (All dimensions in mm.)

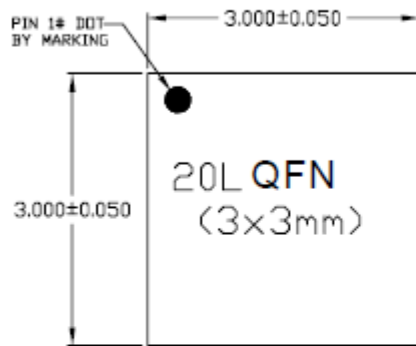


| SYMBOLS | MIN. | NOM. | MAX. |
|------------|-----------|-------|-------|
| A | 0.053 | 0.061 | 0.069 |
| A1 | 0.004 | — | 0.010 |
| A2 | 0.049 | 0.057 | 0.065 |
| b | 0.008 | 0.010 | 0.012 |
| D | 0.335 | 0.341 | 0.347 |
| E | 0.228 | 0.236 | 0.244 |
| E1 | 0.150 | 0.154 | 0.158 |
| e | — | 0.025 | — |
| L | 0.016 | 0.033 | 0.050 |
| L1 | 0.041 REF | | |
| R | 0.003 | — | — |
| R1 | 0.003 | — | — |
| h | 0.010 | 0.015 | 0.020 |
| θ | 0° | 4° | 8° |
| $\theta 1$ | 5° | 10° | 15° |
| $\theta 2$ | 0° | — | — |

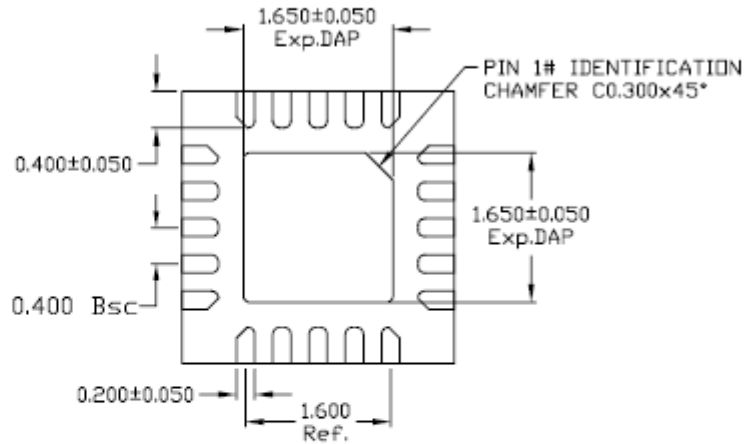
UNIT : INCH

Package Outline Dimensions (cont.) (All dimensions in mm.)

QFN3*3-20L



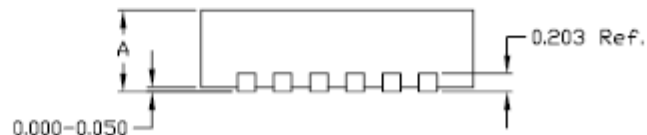
TOP VIEW



BOTTOM VIEW

NOTE
D TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE
BUT WITH DIFFERENT THICKNESS:

| A | QFN | |
|------|-------|-------|
| | MAX. | 0.800 |
| | NOM. | 0.750 |
| MIN. | 0.700 | |



SIDE VIEW

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